BLA9H0912L-1200P; BLA9H0912LS-1200P(G)

LDMOS avionics power transistor

AMPLEON

Rev. 2 — 10 January 2023

Product data sheet

1. Product profile

1.1 General description

1200 W LDMOS power transistor for avionics applications in the frequency range of 960 MHz to 1215 MHz.

Table 1. Typical performance

Typical RF performance at T_{case} = 25 °C; t_p = 50 μs; δ = 2 %; I_{Dq} = 75 mA; in a class-AB demo circuit.

Test signal	f	V_{DS}	P_L	G_p	η_D
	(MHz)	(V)	(W)	(dB)	(%)
pulsed RF	1030	50	1200	19	60
pulsed RF at 1 dB compression	960 to 1215	50	>1050	19	57

1.2 Features and benefits

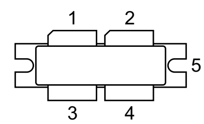
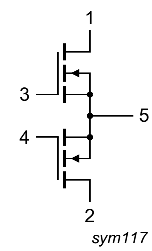
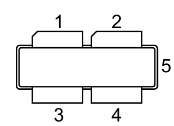
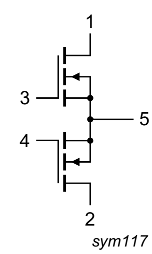
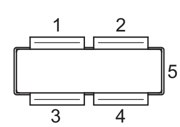
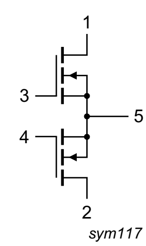
- High efficiency
- Excellent ruggedness
- Designed for avionics band operation
- Excellent thermal stability
- Easy power control
- Integrated dual sided ESD protection enables excellent off-state isolation
- High flexibility with respect to pulse formats
- Internally matched for ease of use
- For RoHS compliance see the product details on the Ampleon website

1.3 Applications

- Avionics applications in the frequency range of 960 MHz to 1215 MHz

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
BLA9H0912L-1200P (SOT539A)			
1	drain1		
2	drain2		
3	gate1		
4	gate2		
5	source [1]		
BLA9H0912LS-1200P (SOT539B)			
1	drain1		
2	drain2		
3	gate1		
4	gate2		
5	source [1]		
BLA9H0912LS-1200PG (SOT1248C)			
1	drain1		
2	drain2		
3	gate1		
4	gate2		
5	source [1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLA9H0912L-1200P	-	flanged balanced ceramic package; 2 mounting holes; 4 leads	SOT539A
BLA9H0912LS-1200P	-	earless flanged balanced ceramic package; 4 leads	SOT539B
BLA9H0912LS-1200PG	-	earless flanged LDMOST ceramic package; 4 leads	SOT1248C

4. Limiting values

Table 4. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Min	Max	Unit
V_{DS}	drain-source voltage	-	106	V
V_{GS}	gate-source voltage	–6	+11	V
T_{stg}	storage temperature	–65	+150	°C
T_j	junction temperature [1]	-	225	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$Z_{th(j-mb)}$	transient thermal impedance from junction to mounting base	T_{case} = 85 °C; P_L = 1200 W		
		t_p = 32 μs; δ = 2 %	0.027	K/W
		t_p = 10 μs; δ = 10 %	0.036	K/W
		t_p = 64 μs; δ = 1 %	0.032	K/W
		t_p = 2.4 ms; δ = 6.4 %	0.126	K/W

6. Characteristics

Table 6. DC characteristics
T_j = 25 °C, per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 4 mA	106	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 400 mA	1.5	2.0	2.5	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 50 V	-	-	2.8	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	-	60	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	280	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 400 mA	-	3.7	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 14 A	-	0.060	-	Ω

Table 7. RF characteristics
Test signal: pulsed RF; f = 1030 MHz; t_p = 50 μs; δ = 2 %; RF performance at V_{DS} = 50 V; I_{Dq} = 75 mA; T_{case} = 25 °C; unless otherwise specified, in a class-AB production circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	P_L = 1200 W	17.8	19	-	dB
η_D	drain efficiency	P_L = 1200 W	57	60	-	%
RL_{in}	input return loss	P_L = 1200 W	-	–15	-	dB
$P_{droop(pulse)}$	pulse droop power	P_L = 1200 W	-	0.2	0.5	dB

Table 7. RF characteristics *...continued*

Test signal: pulsed RF; f = 1030 MHz; t_p = 50 μs; δ = 2 %; RF performance at V_{DS} = 50 V; I_{Dq} = 75 mA; T_{case} = 25 °C; unless otherwise specified, in a class-AB production circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_r	rise time	P_L = 1200 W	-	6	50	ns
t_f	fall time	P_L = 1200 W	-	6	50	ns
$P_{L(2dB)}$	output power at 2 dB gain compression		-	1400	-	W

7. Test information

7.1 Ruggedness in class-AB operation

The BLA9H0912L-1200P, BLA9H0912LS-1200P and BLA9H0912LS-1200PG are capable of withstanding a load mismatch corresponding to VSWR = 20 : 1 through all phases under the following conditions: V_{DS} = 50 V; I_{Dq} = 75 mA; P_L = 1200 W; t_p = 50 μs; δ = 2 %.

7.2 Impedance information

Table 8. Typical impedance (per section)

f	Z_S [1]	Z_L [1]
(MHz)	(Ω)	(Ω)
BLA9H0912L-1200P; BLA9H0912LS-1200P		
950	0.717 – j1.793	0.965 – j1.305
1000	0.953 – j1.886	1.049 – j1.561
1050	1.091 – j1.910	1.032 – j1.780
1100	1.353 – j0.443	1.291 – j1.952
1150	1.962 – j1.061	1.474 – j2.081
1200	0.837 – j0.936	1.514 – j2.413
BLA9H0912LS-1200PG		
950	0.864 – j4.192	1.114 – j3.604
1000	1.168 – j4.414	1.249 – j4.020
1050	1.354 – j4.560	1.267 – j4.411
1100	1.481 – j2.963	1.625 – j4.718
1150	2.274 – j3.655	1.901 – j4.980
1200	1.097 – j3.801	2.087 – j5.532

[1] Z_S and Z_L defined in Figure 1.

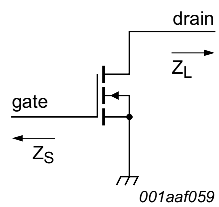
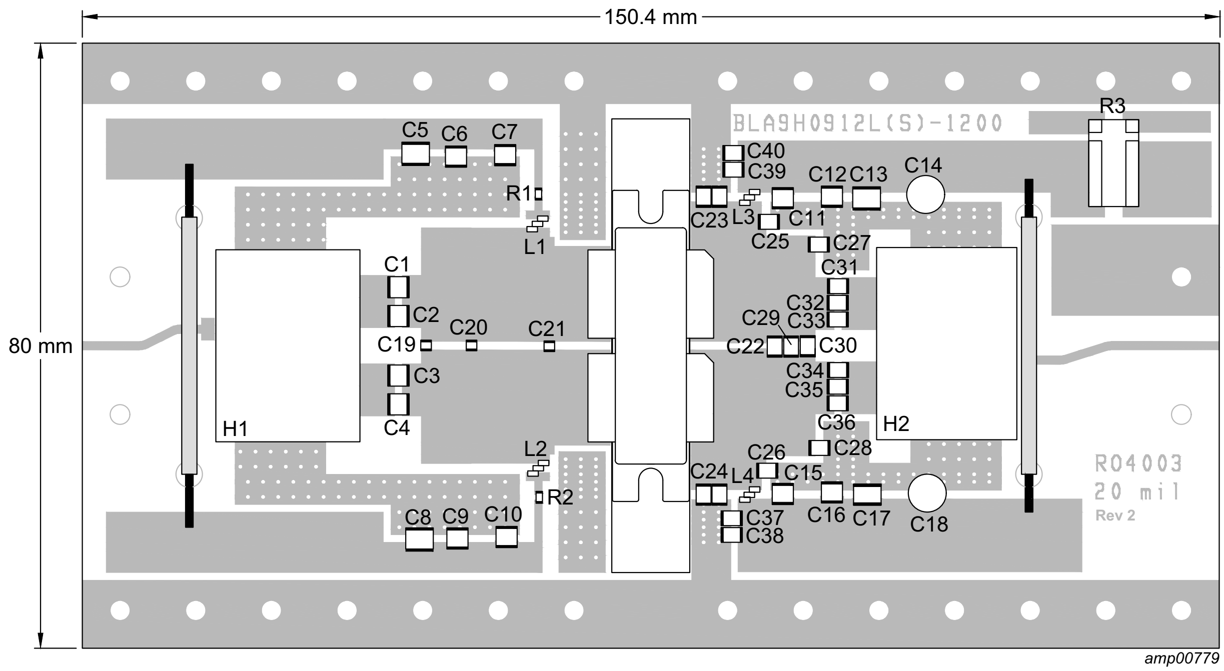


Fig 1. Definition of transistor impedance

7.3 Test circuit



Printed-Circuit Board (PCB): RO4003; ε_r = 3.55; thickness = 0.508 mm; thickness copper plating = 35 μm.

See Table 9 for a list of components.

Fig 2. Component layout for application circuit

Table 9. List of components

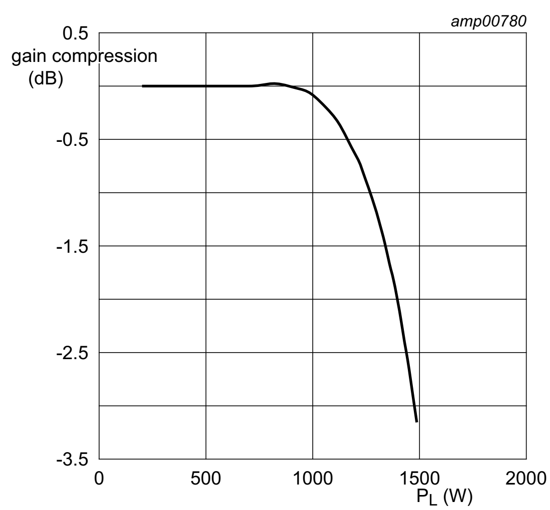
See Figure 2 for component layout.

Component	Description	Value	Remarks
C1, C2, C3, C4	multilayer ceramic chip capacitor	39 pF	ATC 100B
C5, C8, C13, C17	multilayer ceramic chip capacitor	10 μF	Murata: GRM55DR61H106KA88L
C6, C9, C12, C16	multilayer ceramic chip capacitor	1 nF	ATC 100B
C7, C10, C11, C15	multilayer ceramic chip capacitor	51 pF	ATC 100B
C14, C18	electrolytic capacitor	100 μF, 63 V	
C19, C20	multilayer ceramic chip capacitor	0.5 pF	ATC 100A
C21	multilayer ceramic chip capacitor	5.6 pF	ATC 100A
C22	multilayer ceramic chip capacitor	3.0 pF	ATC 100B

Table 9. List of components *…continued*
See Figure 2 for component layout.

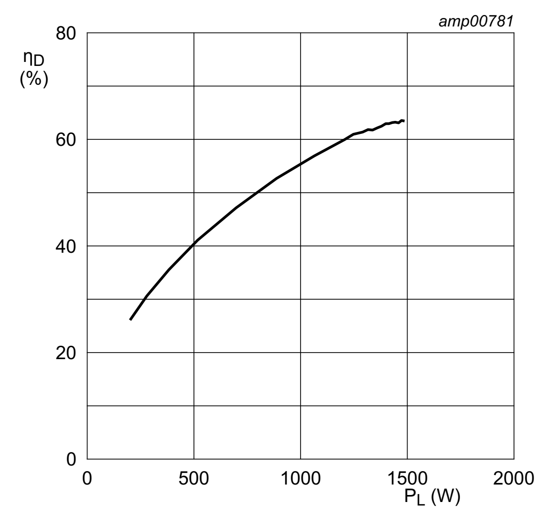
Component	Description	Value	Remarks
C23a, C23b, C24a, C24b	multilayer ceramic chip capacitor	5.1 pF	ATC 800B
C25, C26, C27, C28	multilayer ceramic chip capacitor	2.4 pF	ATC 100B
C29	multilayer ceramic chip capacitor	0.8 pF	ATC 100B
C30	multilayer ceramic chip capacitor	1.6 pF	ATC 100B
C31, C32, C33, C34, C35, C36	multilayer ceramic chip capacitor	43 pF	ATC 100B
C37, C39	multilayer ceramic chip capacitor	20 nF	ATC 200B
C38, C40	multilayer ceramic chip capacitor	1 nF	ATC 200B
H1, H2	balun transformer		Anaren: 3A412S
L1, L2	inductor	27 nH	Coilcraft: 1111SQ-27NJEB
L3, L4	inductor	1/2 turns, D = 1.5 mm, 8.9 nH	8 mm copper wire
R1, R2	resistor	5 Ω	SMD 0603
R3	resistor	5 mΩ	FC4L110R005FER

7.4 Graphical data



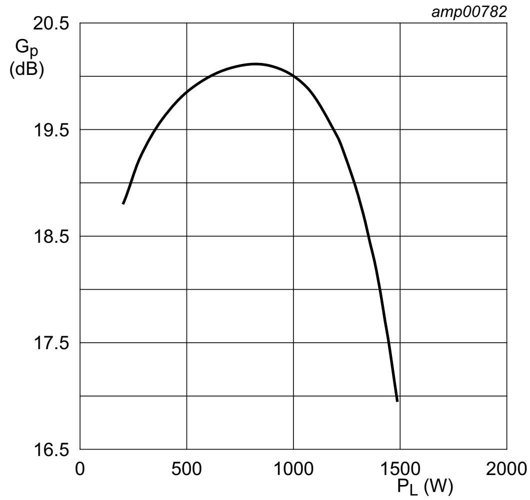
V_{DS} = 50 V; I_{Dq} = 75 mA; t_p = 50 μs; δ = 2 %.

Fig 3. Gain compression as a function of output power; typical values



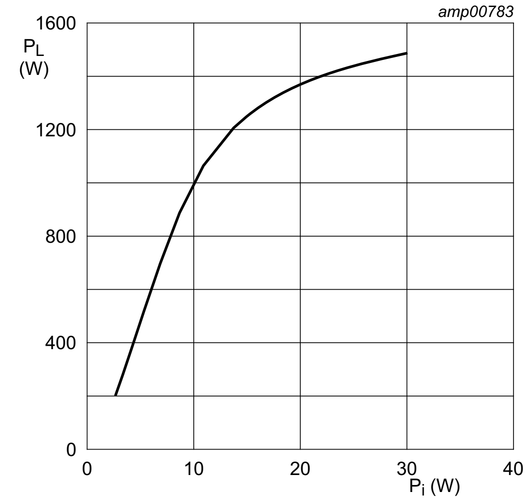
V_{DS} = 50 V; I_{Dq} = 75 mA; t_p = 50 μs; δ = 2 %.

Fig 4. Drain efficiency as a function of output power; typical values



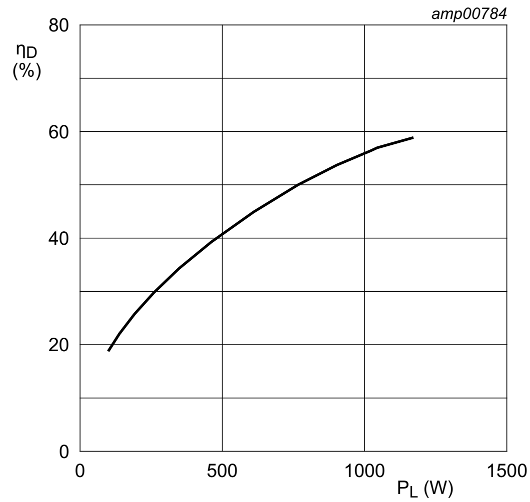
V_{DS} = 50 V; I_{Dq} = 75 mA; t_p = 50 μs; δ = 2 %.

Fig 5. Power gain as a function of output power; typical values



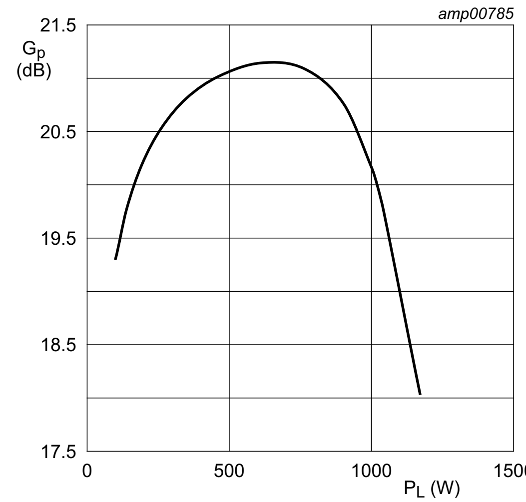
V_{DS} = 50 V; I_{Dq} = 75 mA; t_p = 50 μs; δ = 2 %.

Fig 6. Output power as a function of input power; typical values



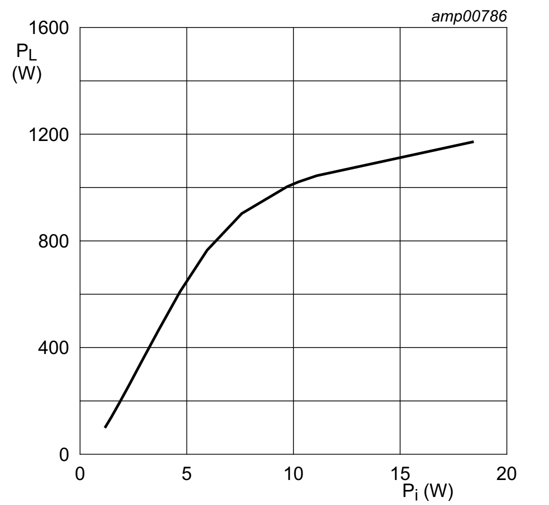
V_{DS} = 50 V; I_{Dq} = 200 mA; t_p = 2.4 ms; δ = 6.4 %.

Fig 7. Drain efficiency as a function of output power; typical values



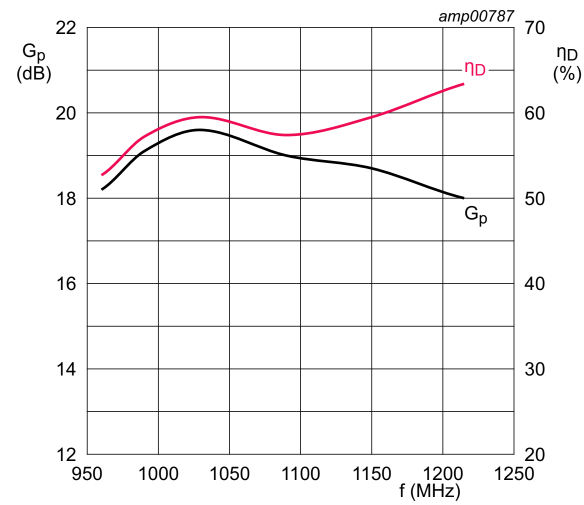
V_{DS} = 50 V; I_{Dq} = 200 mA; t_p = 2.4 ms; δ = 6.4 %.

Fig 8. Power gain as a function of output power; typical values



V_{DS} = 50 V; I_{Dq} = 200 mA; t_p = 2.4 ms; δ = 6.4 %.

Fig 9. Output power as a function of input power; typical values

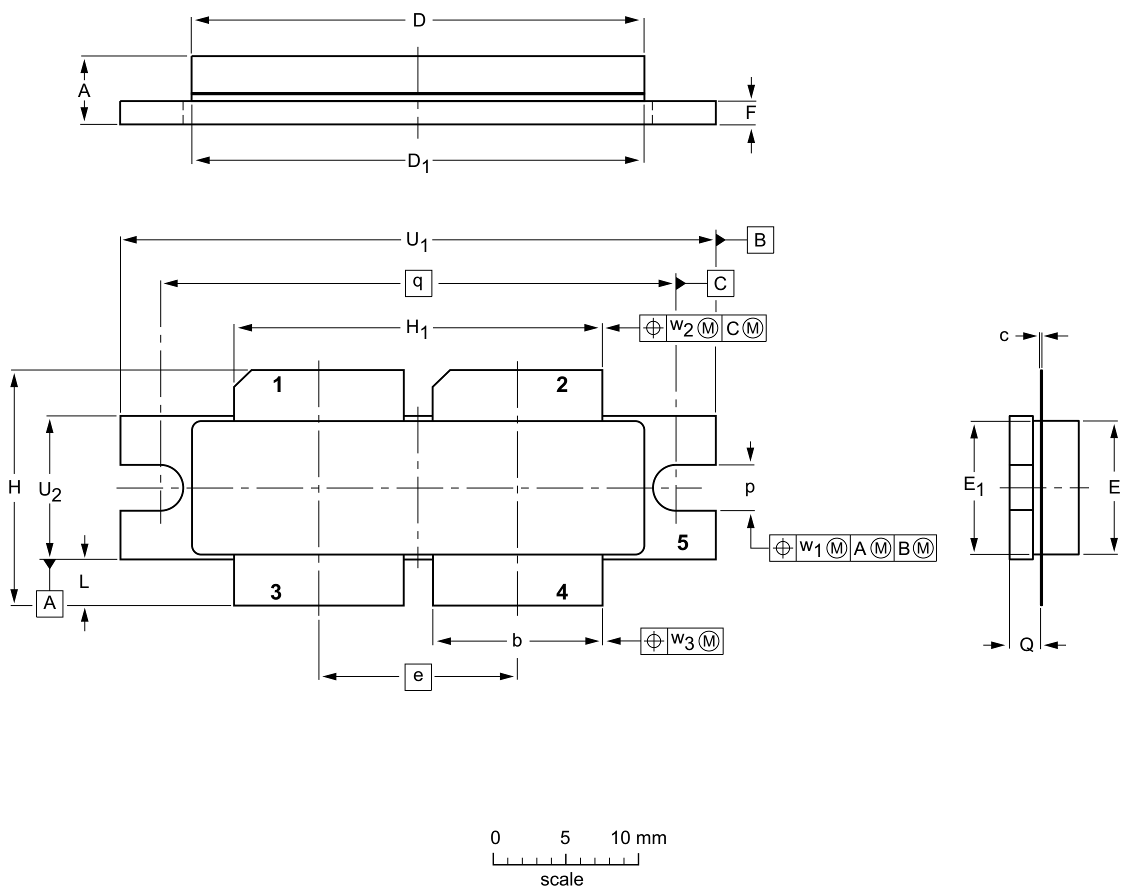


V_{DS} = 51.6 V; I_{Dq} = 100 mA; P_L = $P_{L(1dB)}$ (>1050 W); t_p = 50 μs; δ = 5 %.
Performance measured in a dedicated broadband fixture.

Fig 10. Power gain and drain efficiency as function of frequency; typical values

8. Package outline

Flanged balanced ceramic package; 2 mounting holes; 4 leads **SOT539A**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

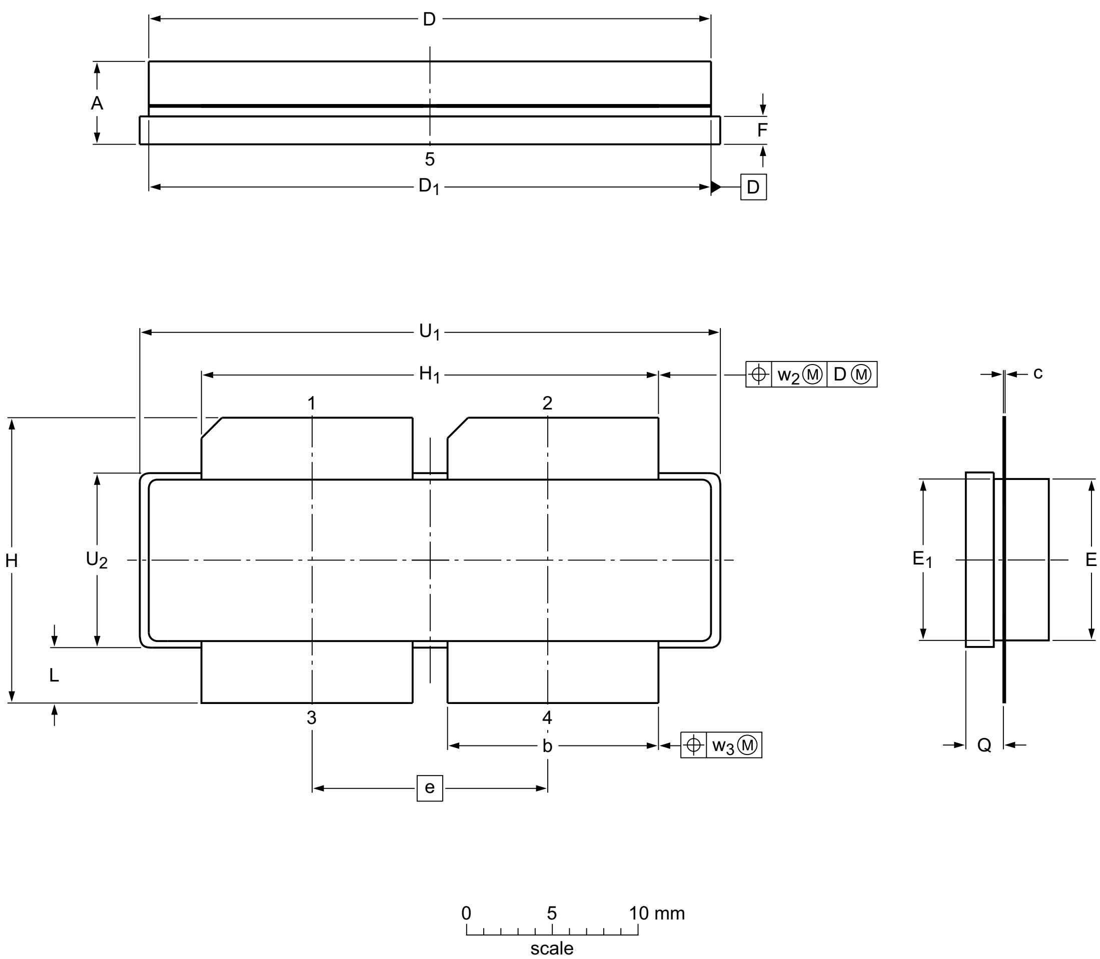
UNIT	A	b	c	D	D_1	e	E	E_1	F	H	H_1	L	p	Q	q	U_1	U_2	w_1	w_2	w_3
mm	4.7 4.2	11.81 11.56	0.18 0.10	31.55 30.94	31.52 30.96	13.72	9.50 9.30	9.53 9.27	1.75 1.50	17.12 16.10	25.53 25.27	3.48 2.97	3.30 3.05	2.26 2.01	35.56	41.28 41.02	10.29 10.03	0.25	0.51	0.25
inches	0.185 0.165	0.465 0.455	0.007 0.004	1.242 1.218	1.241 1.219	0.540	0.374 0.366	0.375 0.365	0.069 0.059	0.674 0.634	1.005 0.995	0.137 0.117	0.130 0.120	0.089 0.079	1.400	1.625 1.615	0.405 0.395	0.010	0.020	0.010

Note
1. millimeter dimensions are derived from the original inch dimensions.
2. recommended screw pitch dimension of 1.52 inch (38.6 mm) based on M3 screw.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT539A						~~10-02-02~~ 12-05-02

Fig 11. Package outline SOT539A

Earless flanged balanced ceramic package; 4 leads **SOT539B**



Dimensions

Unit(1)		A	b	c	D	D_1	E	E_1	e	F	H	H_1	L	Q	U_1	U_2	w_2	w_3
mm	max	4.7	11.81	0.18	31.55	31.52	9.5	9.53		1.75	17.12	25.53	3.48	2.26	32.39	10.29		
	nom								13.72								0.25	0.25
	min	4.2	11.56	0.10	30.94	30.96	9.3	9.27		1.50	16.10	25.27	2.97	2.01	32.13	10.03		
inches	max	0.185	0.465	0.007	1.242	1.241	0.374	0.375		0.069	0.674	1.005	0.137	0.089	1.275	0.405		
	nom								0.54								0.01	0.01
	min	0.165	0.455	0.004	1.218	1.219	0.366	0.365		0.059	0.634	0.995	0.117	0.079	1.265	0.395		

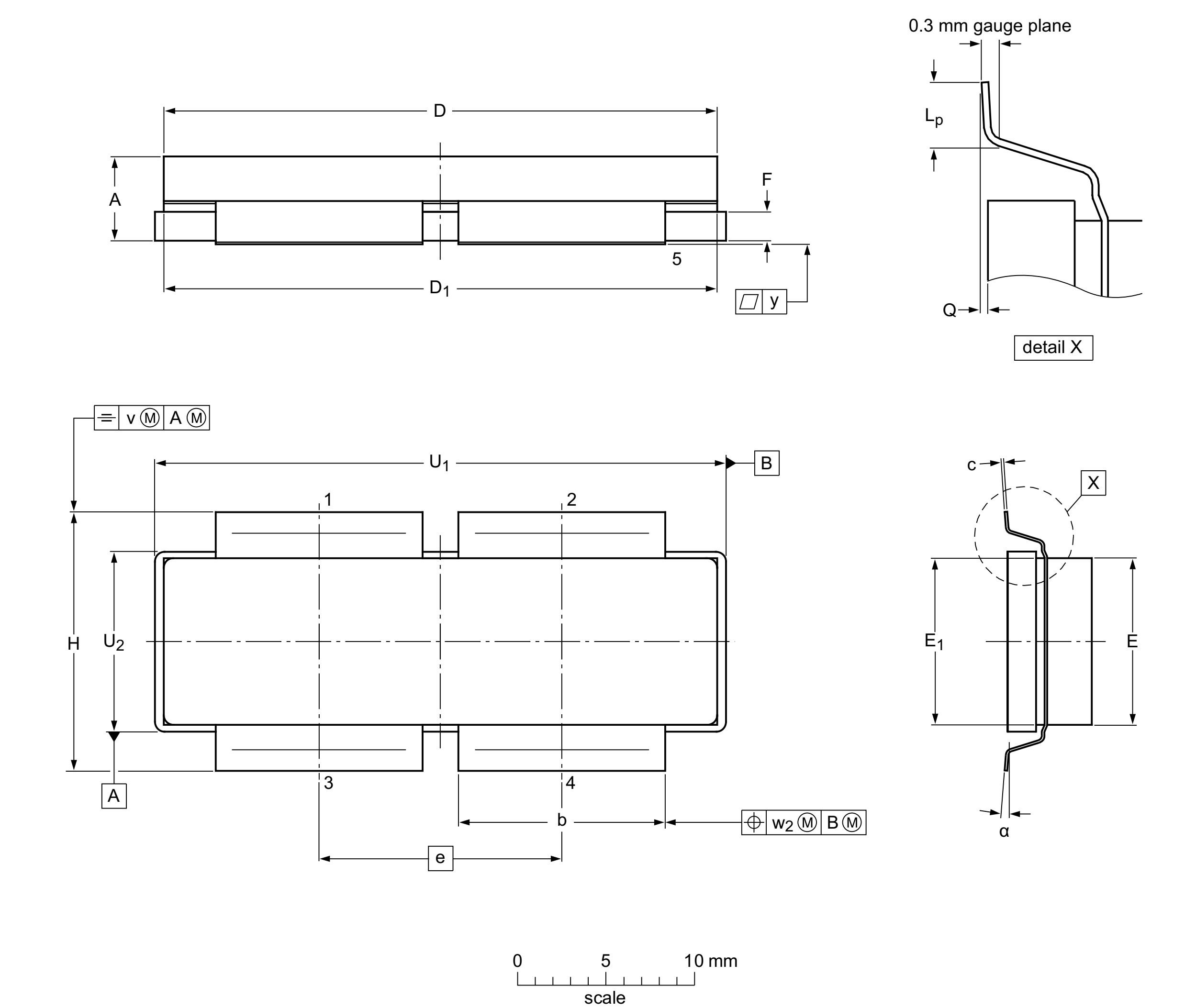
Note
1. millimeter dimensions are derived from the original inch dimensions.

sot539b_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT539B						~~12-05-02~~ 13-05-24

Fig 12. Package outline SOT539B

Earless flanged LDMOST ceramic package; 4 leads **SOT1248C**



Dimensions

Unit(1)		A	b	c	D	D_1	e	E	E_1	F	H	L_p	Q	U_1	U_2	v	w_2	y	α
	max	5.5	11.81	0.18	31.55	31.52		9.50	9.53	1.75	14.70	1.38	0.195	32.39	10.29	0.25	0.25	0.15	7°
mm	nom						13.72												
	min	4.2	11.56	0.10	30.94	30.96		9.30	9.27	1.50	14.50	0.98	0.045	32.13	10.03				0°
	max	0.217	0.465	0.007	1.242	1.241		0.374	0.375	0.069	0.579	0.055	0.008	1.275	0.405	0.01	0.01	0.006	7°
inches	nom						0.540												
	min	0.165	0.455	0.004	1.218	1.219		0.366	0.365	0.059	0.571	0.039	0.002	1.265	0.395				0°

Note

1. Millimeter dimensions are derived from the original inch dimensions.

sot1248c_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1248C						~~13-04-16~~ 13-08-15

Fig 13. Package outline SOT1248C

9. Handling information

CAUTION	
	This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices. Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

Table 10. ESD sensitivity

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C2A [1]
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	2 [2]

[1] CDM classification C2A is granted to any part that passes after exposure to an ESD pulse of 500 V.

[2] HBM classification 2 is granted to any part that passes after exposure to an ESD pulse of 2000 V.

10. Abbreviations

Table 11. Abbreviations

Acronym	Description
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
LDMOST	Laterally Diffused Metal-Oxide Semiconductor Transistor
MTF	Median Time to Failure
RoHS	Restriction of Hazardous Substances
SMD	Surface Mounted Device
VSWR	Voltage Standing Wave Ratio

11. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLA9H0912L-1200P_LS-1200P_LS-1200PG v.2	20230110	Product data sheet	-	BLA9H0912L-1200P_LS-1200P v.1
Modifications:	• Table 2 on page 2: added BLA9H0912LS-1200PG • Table 3 on page 2: added BLA9H0912LS-1200PG • Table 5 on page 3: changed P_L value from 600 W to 1200 W • Section 7.1 on page 4: added BLA9H0912LS-1200PG • Table 8 on page 4: updated table • Figure 13 on page 11: added figure of package outline SOT1248C • Section 12.2 on page 13: updated section • Section 12.3 on page 13: updated section			
BLA9H0912L-1200P_LS-1200P v.1	20181101	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.ampleon.com.

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13. Contact information

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14. Contents

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section ‘Legal information’.

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