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Renesas Electronics website: <http://www.renesas.com>

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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EOL announced Product

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2SK1403A

Silicon N Channel MOS FET

REJ03G0943-0300

Rev.3.00

May 15, 2006

Application

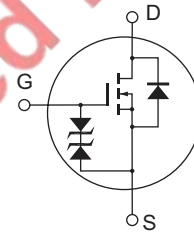
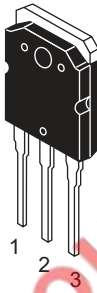
High speed power switching

Features

- Low on-resistance
- High speed switching
- Low drive current
- No secondary breakdown
- Suitable for switching regulator and DC-DC converter

Outline

RENESAS Package code: PRSS0004ZE-A
(Package name: TO-3P)



1. Gate
2. Drain
(Flange)
3. Source

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	650	V
Gate to source voltage	V_{GSS}	±30	V
Drain current	I_D	8	A
Drain peak current	$I_{D(pulse)}^{*1}$	32	A
Body to drain diode reverse drain current	I_{DR}	8	A
Channel dissipation	P_{ch}^{*2}	100	W
Channel temperature	T_{ch}	150	°C
Storage temperature	T_{stg}	-55 to +150	°C

Notes: 1. $PW \leq 10 \mu s$, duty cycle $\leq 1\%$
 2. Value at $T_C = 25^\circ C$

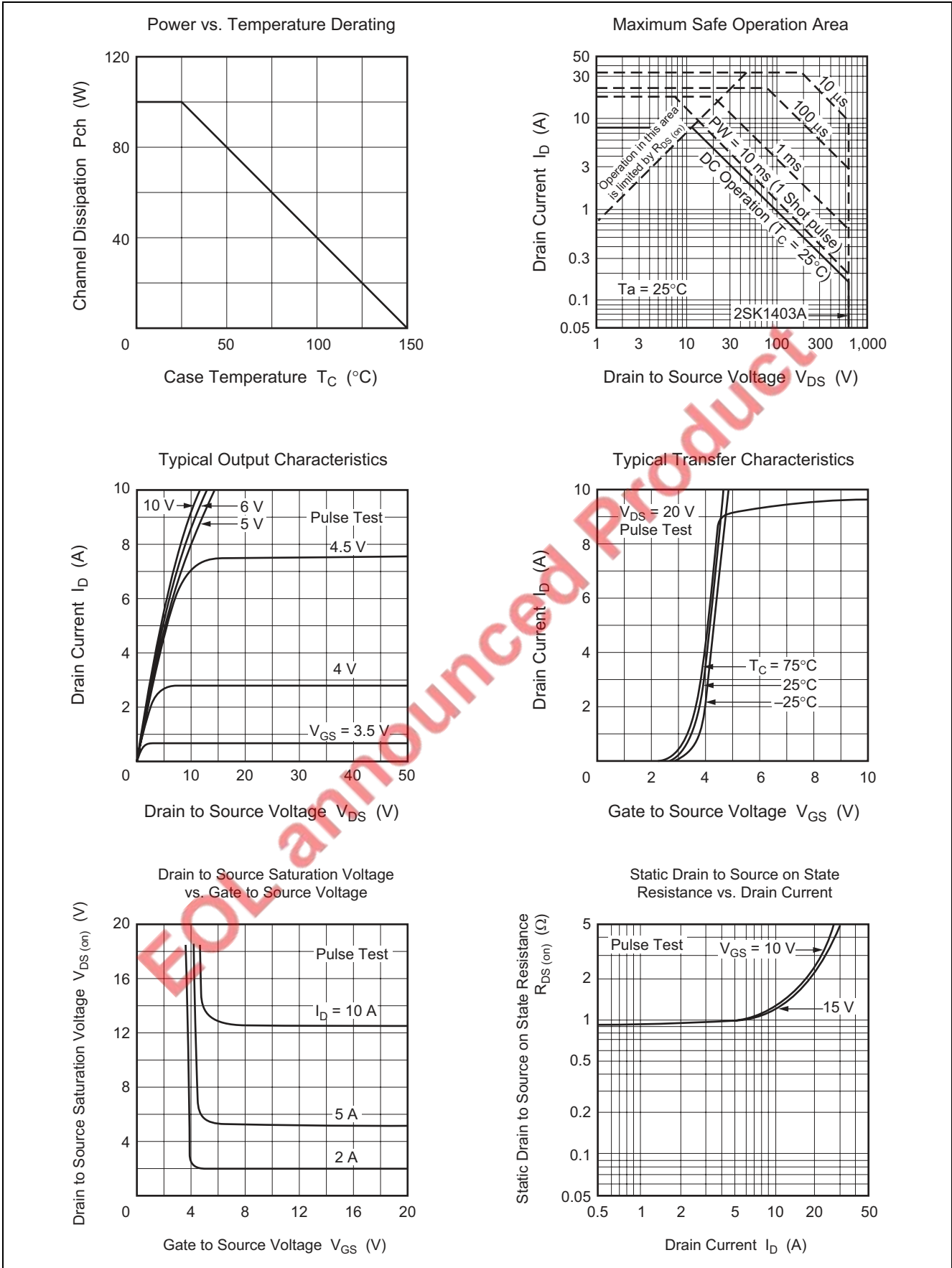
Electrical Characteristics

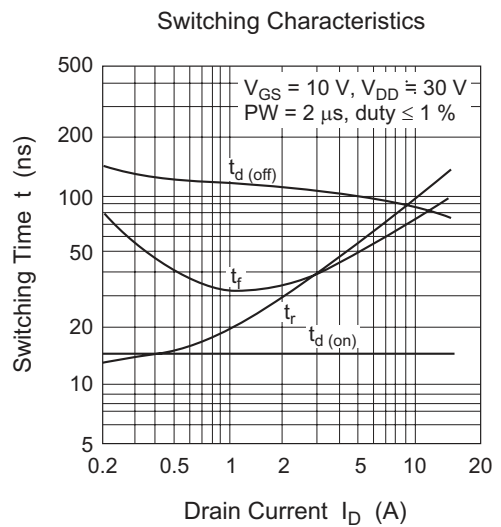
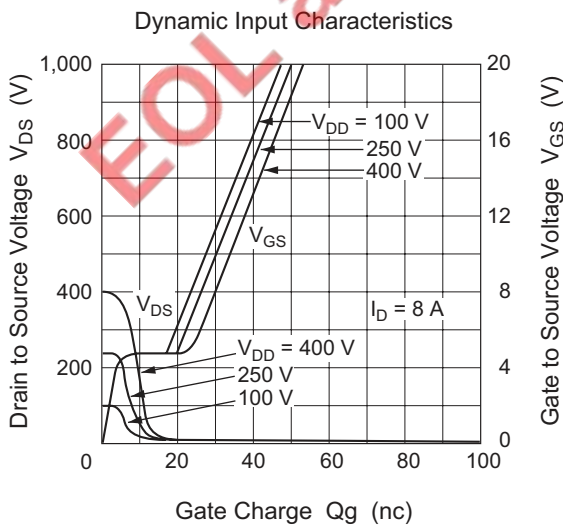
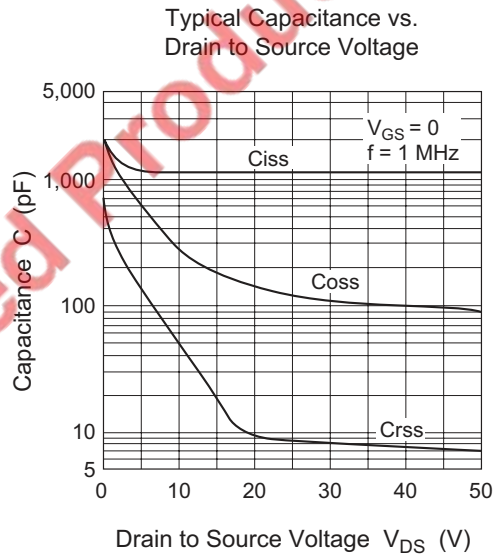
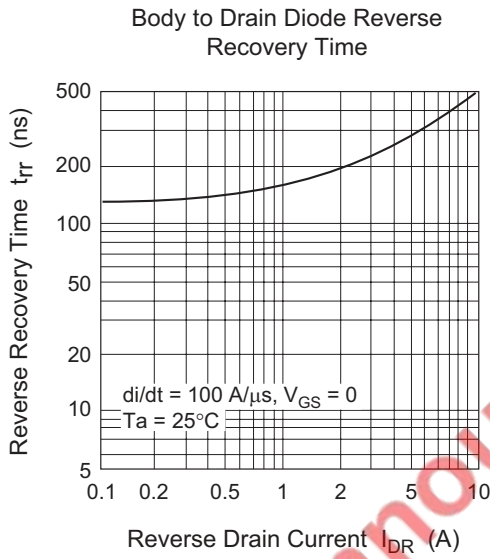
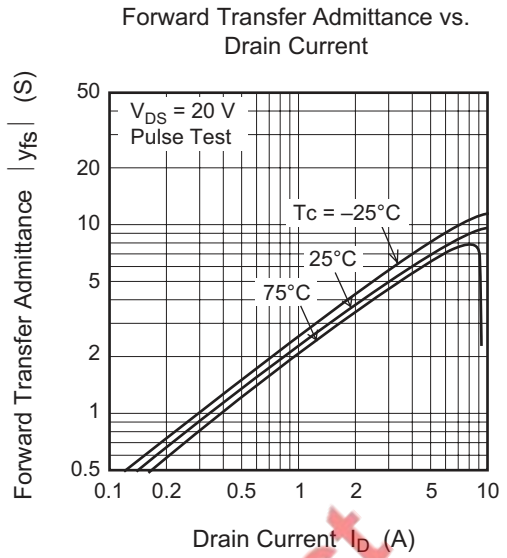
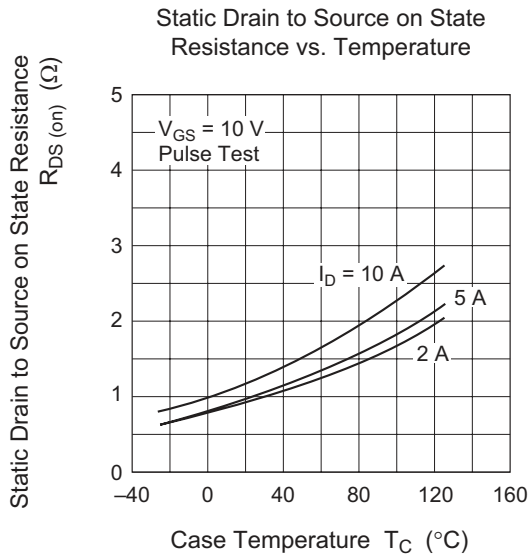
(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	650	—	—	V	$I_D = 10 \text{ mA}$, $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	±30	—	—	V	$I_G = \pm 100 \mu A$, $V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	±10	μA	$V_{GS} = \pm 25 \text{ V}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	250	μA	$V_{DS} = 550 \text{ V}$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	2.0	—	3.0	V	$I_D = 1 \text{ mA}$, $V_{DS} = 10 \text{ V}$
Static drain to source on state resistance	$R_{DS(on)}$	—	1.0	1.4	Ω	$I_D = 4 \text{ A}$, $V_{GS} = 10 \text{ V}^{*3}$
Forward transfer admittance	$ y_{fs} $	4.0	6.5	—	S	$I_D = 4 \text{ A}$, $V_{DS} = 10 \text{ V}^{*3}$
Input capacitance	C_{iss}	—	1180	—	pF	$V_{DS} = 10 \text{ V}$, $V_{GS} = 0$, $f = 1 \text{ MHz}$
Output capacitance	C_{oss}	—	265	—	pF	
Reverse transfer capacitance	C_{rss}	—	50	—	pF	
Turn-on delay time	$t_{d(on)}$	—	15	—	ns	$I_D = 4 \text{ A}$, $V_{GS} = 10 \text{ V}$, $R_L = 7.5 \Omega$
Rise time	t_r	—	50	—	ns	
Turn-off delay time	$t_{d(off)}$	—	105	—	ns	
Fall time	t_f	—	45	—	ns	
Body to drain diode forward voltage	V_{DF}	—	0.95	—	V	$I_F = 8 \text{ A}$, $V_{GS} = 0$
Body to drain diode reverse recovery time	t_{rr}	—	420	—	ns	$I_F = 8 \text{ A}$, $V_{GS} = 0$, $di_F/dt = 100 \text{ A}/\mu s$

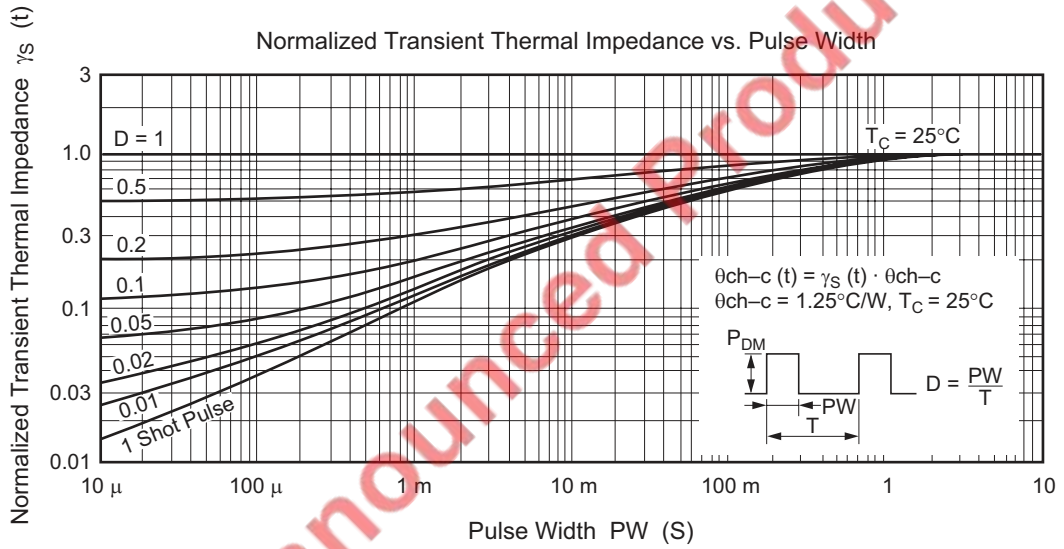
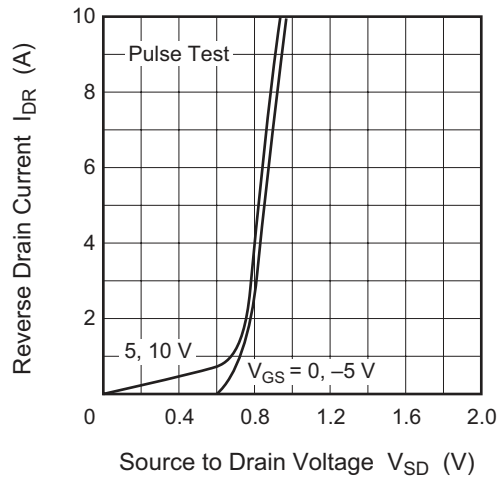
Note: 3. Pulse test

Main Characteristics

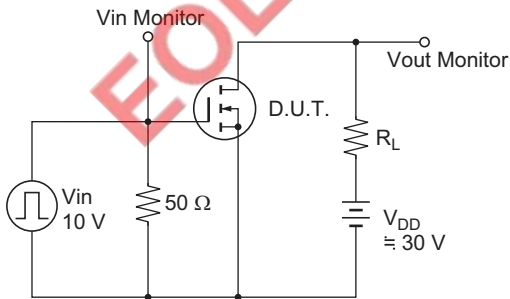




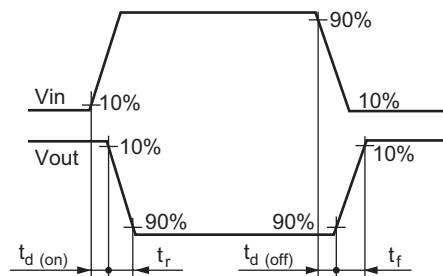
Reverse Drain Current vs. Source to Drain Voltage



Switching Time Test Circuit



Waveforms



Keep safety first in your circuit designs!

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