



# P3M06060K3 SiC MOS N-Channel Enhancement Mode

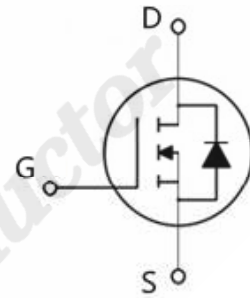
$V_{RRM}$	=	650	V
$I_D$	=	40	A
$I_D(100^\circ\text{C})$	=	28	A
$R_{DS(on)}$	=	60	m $\Omega$

## SiC MOS P3M06060K3 N-Channel Enhancement Mode



### Features

- Qualified to AEC-Q101
- High Blocking Voltage with Low On-Resistance
- High-Frequency Operation
- Ultra-Small  $Q_{gd}$
- 100% UIS tested



### Benefits

- Improve System Efficiency
- Increase Power Density
- Reduce Heat Sink Requirements
- Reduction of System Cost

TO-247-3

Gate	1
Drain	2
Source	3

### Applications

- Solar Inverters
- EV Battery Chargers
- High Voltage DC/DC Converters
- Switch Mode Power Supplies



### Order Information

Part Number	Package	Marking
P3M06060K3	TO-247-3	P3M06060K3



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## 1. Maximum Ratings

At  $T_J = 25^\circ\text{C}$ , unless specified otherwise

Parameter	Symbol	Value	Unit	Test Conditions
Drain - Source Voltage	$V_{DSmax}$	650	V	$V_{GS} = 0V$ $I_D = 100\mu A$
Gate - Source Voltage (dynamic)	$V_{GSmax}$	-8 / +20	V	AC ( $f > 1\text{ Hz}$ )
Gate - Source Voltage(static) turn-on gate voltage turn-off gate voltage	$V_{GS,on}$ $V_{GS,off}$	+15 / +18 -3	V	Static
Continuous Drain Current	$I_D$	40	A	$V_{GS} = 15V$ $T_C = 25^\circ\text{C}$
		28		$V_{GS} = 15V$ $T_C = 100^\circ\text{C}$
Pulsed Drain Current	$I_{D(pulse)}$	89	A	
Power Dissipation	$P_D$	188	W	
Operating Junction	$T_J$	-55 To +175	$^\circ\text{C}$	
Storage Temperature	$T_{stg}$	-55 To +175	$^\circ\text{C}$	
Solder Temperature	$T_L$	260	$^\circ\text{C}$	
Mounting Torque	$M_d$	1 8.8	Nm lbf-in	M3 or 6-32 screw



## 2. Electrical Characteristics

At  $T_J = 25^\circ\text{C}$ , unless specified otherwise

Parameter	Symbol	Value			Unit	Test Conditions
		Min.	Typ.	Max.		
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	650	/	/	V	$V_{GS} = 0V$ $I_D = 100\mu A$
Gate Threshold Voltage	$V_{GS(th)}$	1.8	2.4	/	V	(tested after 30ms pulse at $V_{GS} = 15V$ ) $V_{DS} = V_{GS}$ $I_D = 5mA$ $T_J = 25^\circ\text{C}$
		/	1.6	/	V	$V_{DS} = V_{GS}$ $I_D = 5mA$ $T_J = 175^\circ\text{C}$
Reverse Bias Drain Current	$I_{DSS}$	/	1	100	$\mu A$	$V_{GS} = 0V$ $V_{DS} = 650V$
Gate-Source Leakage Current	$I_{GSS}$	/	20	250	nA	$V_{GS} = 15V$ $V_{DS} = 0V$
Drain-Source On-State Resistance	$R_{DS(on)}$	/	60	78	m $\Omega$	$V_{GS} = 15V$ $I_D = 20A$ $T_J = 25^\circ\text{C}$
		/	52	/		$V_{GS} = 18V$ $I_D = 20A$ $T_J = 25^\circ\text{C}$
Trans conductance	$g_{fs}$	/	12	/	S	$V_{DS} = 20V$ $I_{DS} = 20A$ $T_J = 25^\circ\text{C}$
		/	11	/		$V_{DS} = 20V$ $I_{DS} = 20A$ $T_J = 175^\circ\text{C}$



# P3M06060K3 SiC MOS N-Channel Enhancement Mode

Parameter	Symbol	Value			Unit	Test Conditions
		Min.	Typ.	Max.		
Input Capacitance	$C_{iss}$	/	1853	/	pF	$V_{GS} = 0V$ $V_{DS} = 400V$ $f = 1MHz$ $V_{AC} = 25mV$
Output Capacitance	$C_{oss}$	/	139	/		
Reverse Transfer Capacitance	$C_{rss}$	/	8.3	/		
Coss Stored Energy	$E_{oss}$	/	13.6	/	$\mu J$	$V_{DS} = 400V$ $V_{GS} = -3/15V$ $I_D = 20A$ $R_G = 1\Omega$
Turn-on Energy	$E_{on}$	/	161.2	/	$\mu J$	
Turn-off Energy	$E_{off}$	/	31.7	/	$\mu J$	
Turn-On Delay Time	$T_{d(on)}$	/	15.2	/	ns	
Rise Time	$T_r$	/	24.3	/		
Turn-Off Delay Time	$T_{d(off)}$	/	22.8	/		
Fall Time	$T_f$	/	16.3	/		
Internal Gate Resistance	$R_{G(int)}$	/	1.2	/	$\Omega$	$f = 1MHz$ $V_{AC} = 25mV$
Gate to Source Charge	$Q_{gs}$	/	17.5	/	nC	$V_{DS} = 400V$ $I_{DS} = 20A$ $V_{GS} = -3 \text{ to } 15V$ $I_G = 50mA$
Gate to Drain Charge	$Q_{gd}$	/	15.3	/		
Total Gate Charge	$Q_g$	/	53.1	/		

### 3. Reverse Diode Characteristics

At  $T_J = 25^\circ\text{C}$ , unless specified otherwise

Parameter	Symbol	Value		Unit	Test Conditions
		Typ.	Max.		
Diode Forward Voltage	$V_{SD}$	5.7	/	V	$V_{GS} = -3\text{V}$ $I_{SD} = 10\text{A}$ $T_J = 25^\circ\text{C}$
		5.1	/	V	$V_{GS} = -3\text{V}$ $I_{SD} = 10\text{A}$ $T_J = 175^\circ\text{C}$
Continuous Diode Forward Current	$I_S$	27	/	A	$V_{GS} = -3\text{V}$
Reverse Recover Time	$t_{rr}$	28.9	/	ns	$V_{GS} = -3/15\text{V}$
Reverse Recovery Charge	$Q_{rr}$	328.3	/	nC	$I_{SD} = 20\text{A}$ $V_R = 400\text{V}$ $d_{if}/d_t = 3300\text{A}/\mu\text{s}$
Peak Reverse Recovery Current	$I_{rrm}$	21.6	/	A	$T_J = 25^\circ\text{C}$

### 4. Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal Resistance from Junction to Case	$R_{\theta JC}$	0.8	$^\circ\text{C}/\text{W}$

## 5. Typical Performance

At  $T_J = 25^\circ\text{C}$ , unless specified otherwise

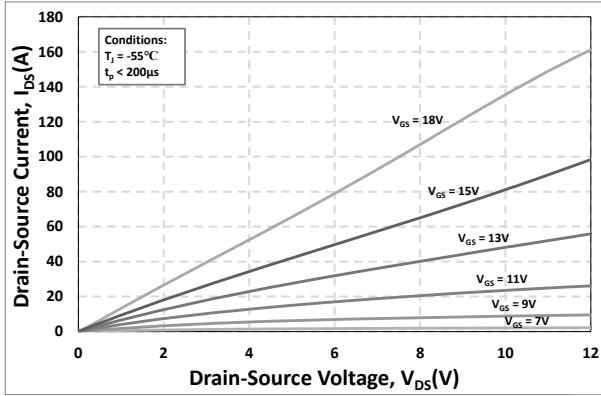


Figure 1. Output Characteristics  $T_J = -55^\circ\text{C}$

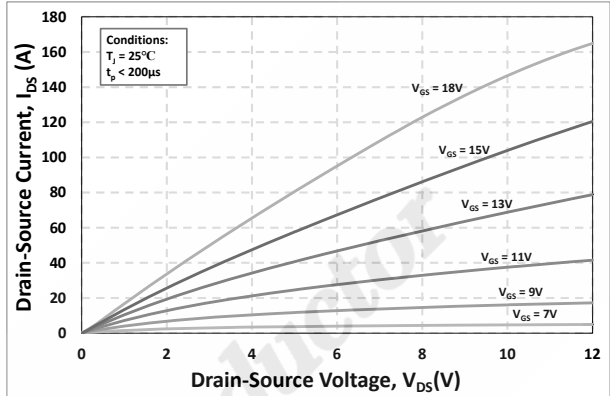


Figure 2. Output Characteristics  $T_J = 25^\circ\text{C}$

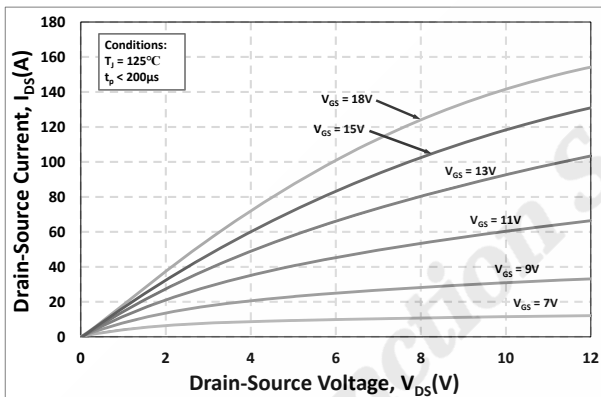


Figure 3. Output Characteristics  $T_J = 125^\circ\text{C}$

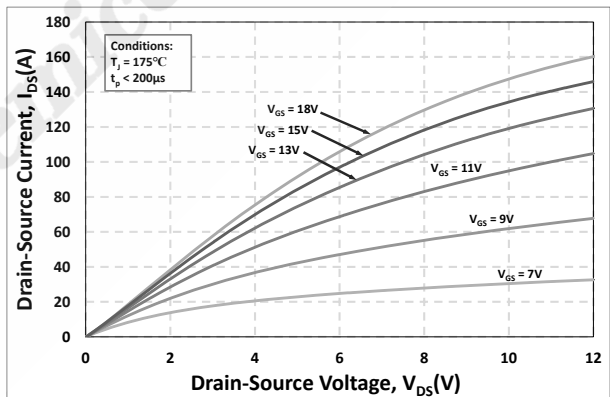


Figure 4. Output Characteristics  $T_J = 175^\circ\text{C}$

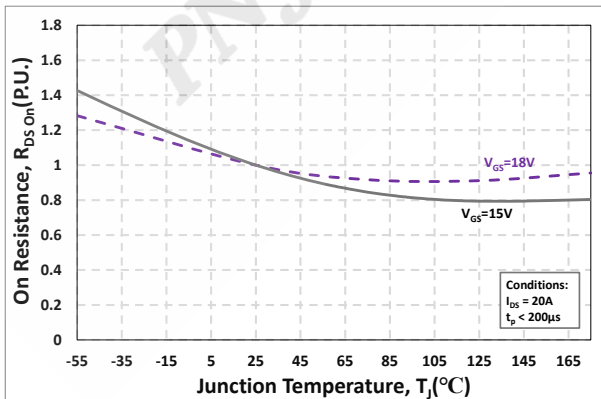


Figure 5. Normalized On-Resistance vs. Temperature

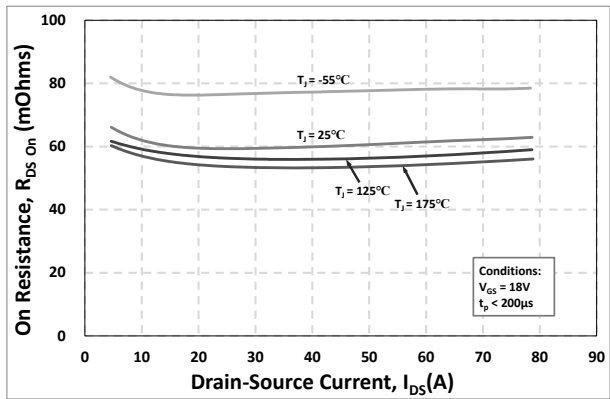


Figure 6. On-Resistance vs. Drain Current Various Temperatures



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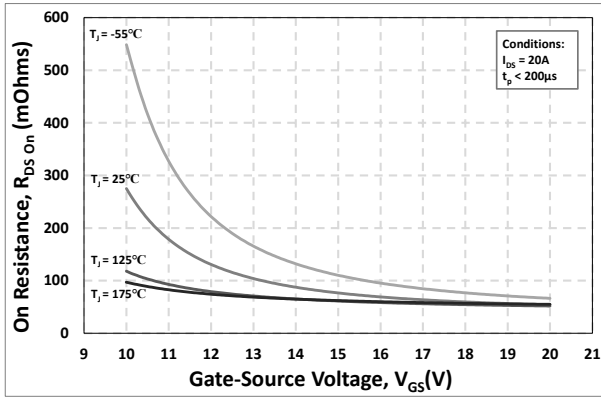


Figure 7. On-Resistance vs. Gate-Source Voltage

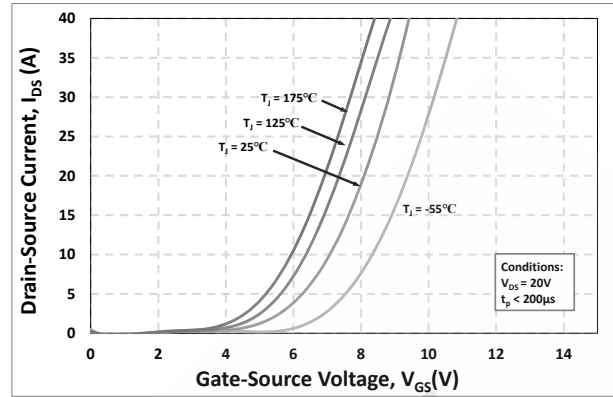


Figure 8. Transfer Characteristic for Various Junction Temperatures

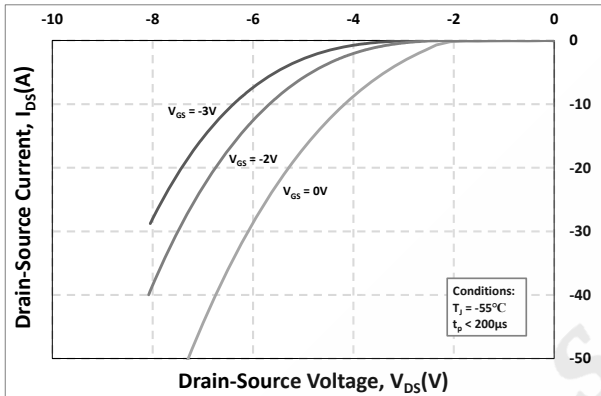


Figure 9. Body Diode Characteristic at -55°C

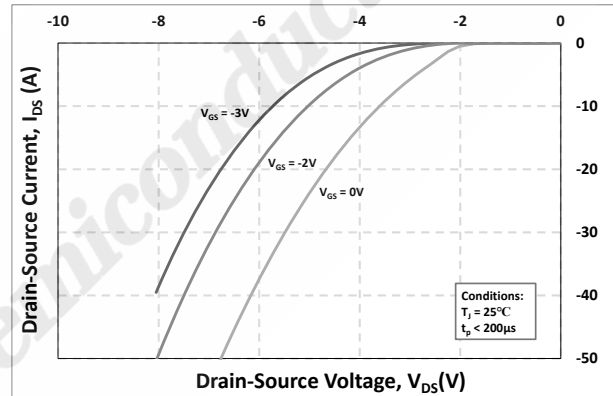


Figure 10. Body Diode Characteristic at 25°C

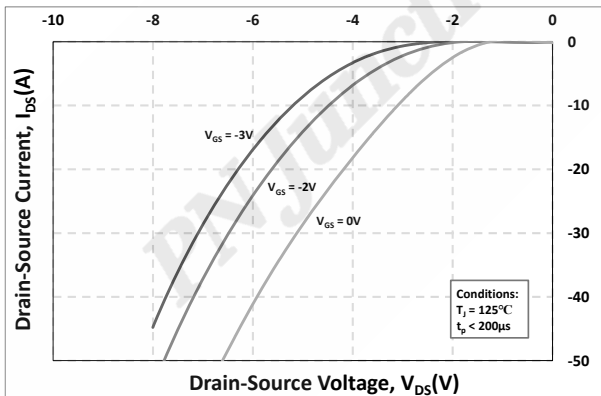


Figure 11. Body Diode Characteristic at 125°C

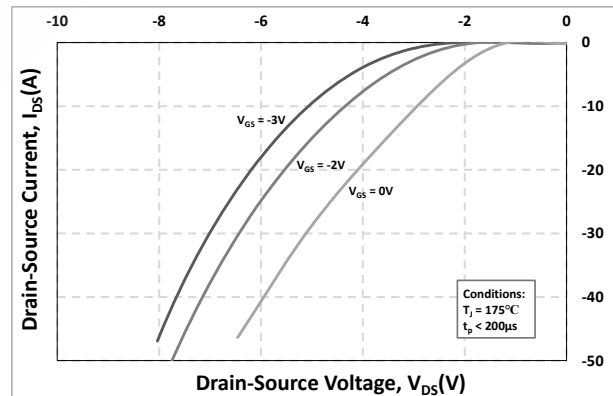


Figure 12. Body Diode Characteristic at 175°C





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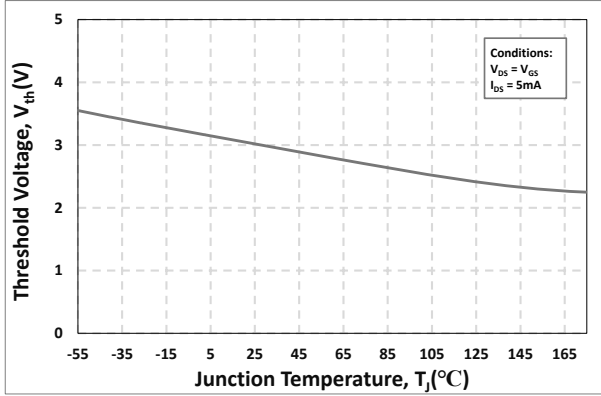


Figure 13. Threshold Voltage vs. Temperature

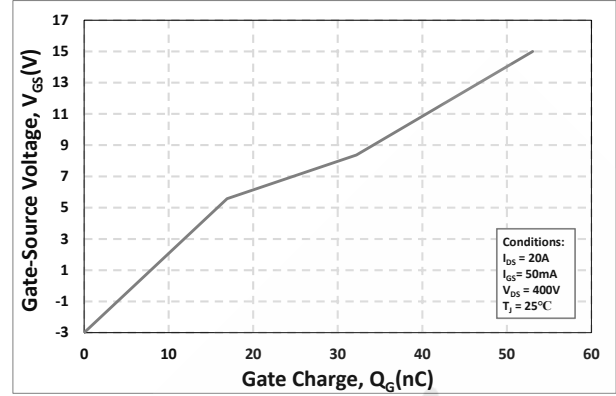


Figure 14. Gate Charge Characteristics

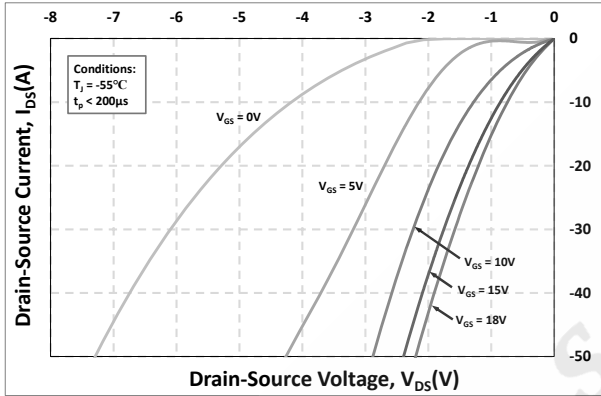


Figure 15. 3rd Quadrant Characteristic at -55°C

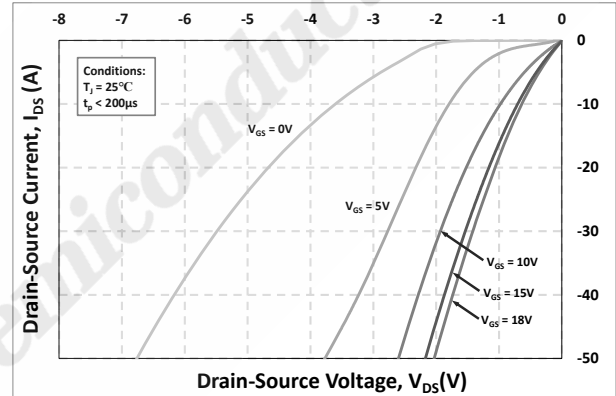


Figure 16. 3rd Quadrant Characteristic at 25°C

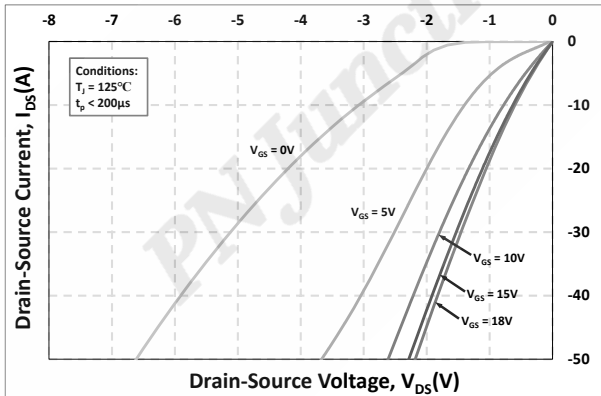


Figure 17. 3rd Quadrant Characteristic at 125°C

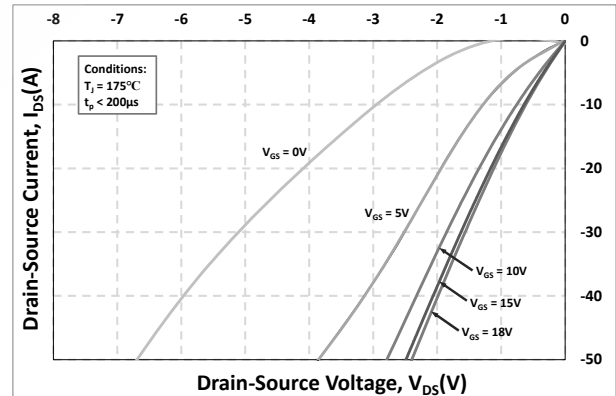


Figure 18. 3rd Quadrant Characteristic at 175°C

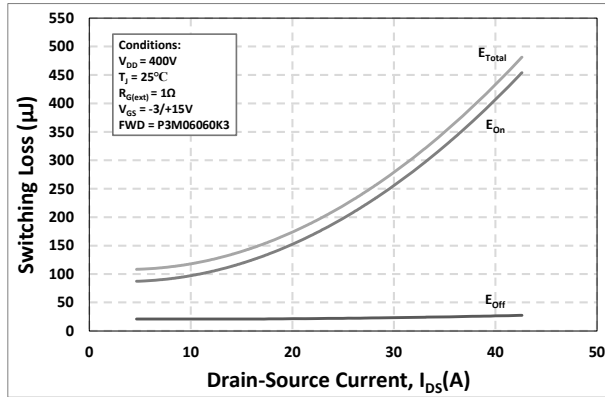


Figure 19. Clamped Inductive Switching Energy vs. Drain Current ( $V_{DD} = 400V$ )

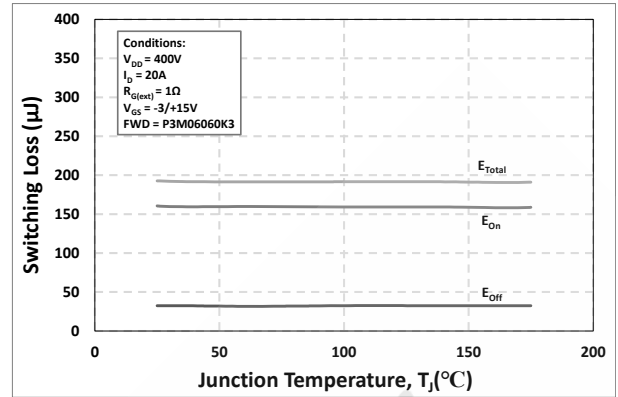


Figure 20. Clamped Inductive Switching Energy vs.  $R_{G(ext)}$

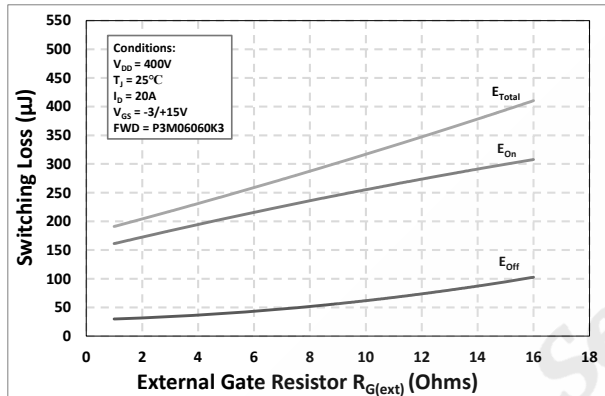


Figure 21. Clamped Inductive Switching Energy vs. Temperature

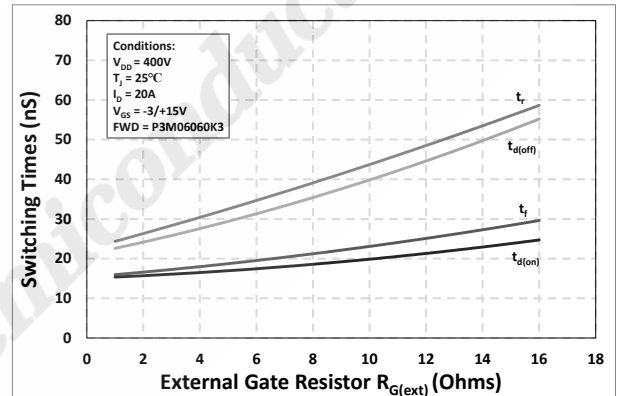


Figure 22. Switching Times vs.  $R_{G(ext)}$

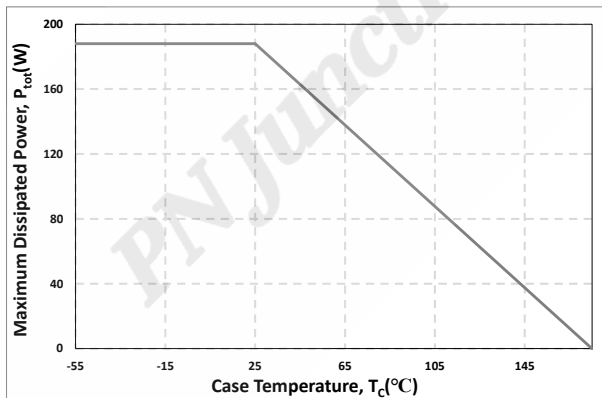


Figure 23. Maximum Power Dissipation Derating vs. Case Temperature

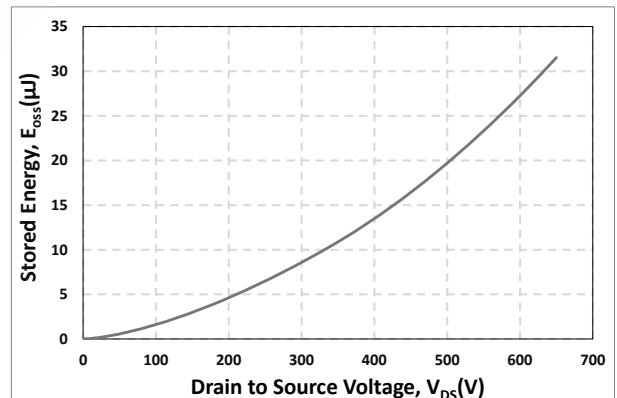


Figure 24. Output Capacitor Stored Energy

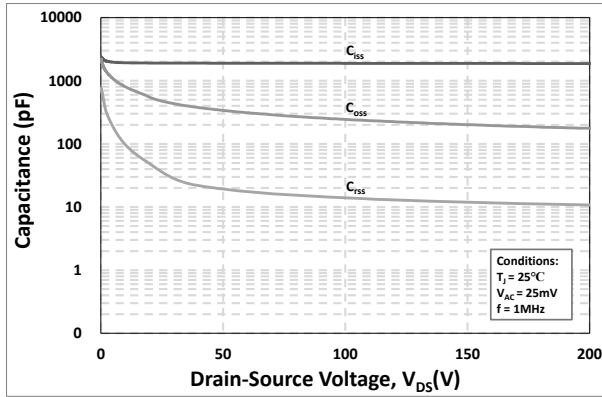


Figure 25. Capacitances vs. Drain-Source Voltage (0 - 200V)

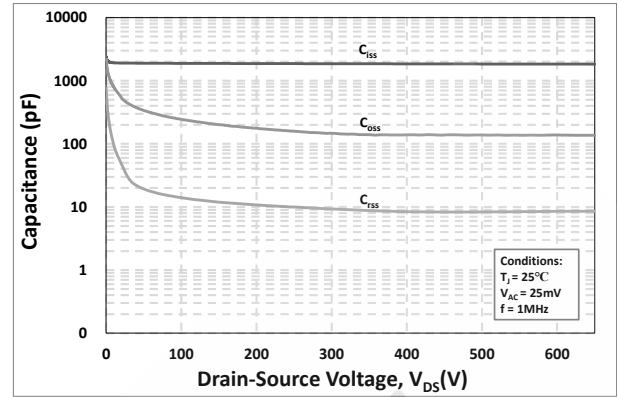


Figure 26. Capacitances vs. Drain-Source Voltage (0 - 650V)

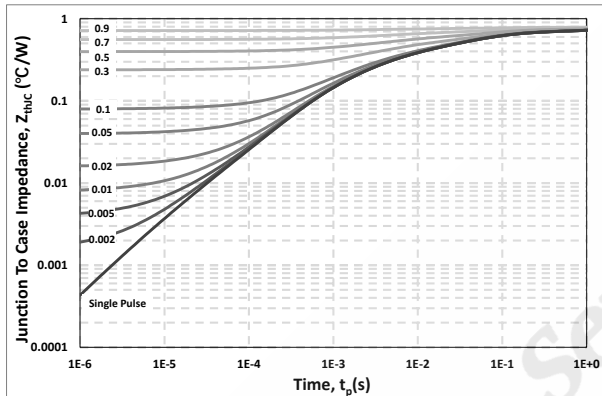


Figure 27. Transient Thermal Impedance (Junction - Case)

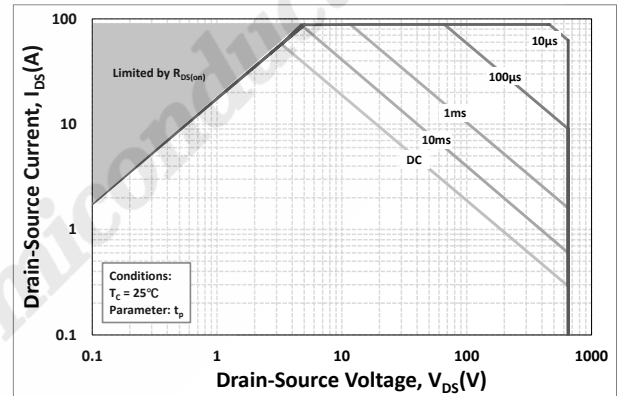


Figure 28. Safe Operating Area

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## 6. Definitions

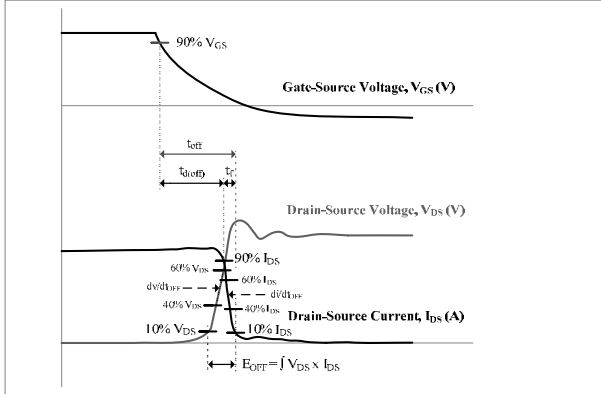


Figure 29. Turn-off Transient Definitions

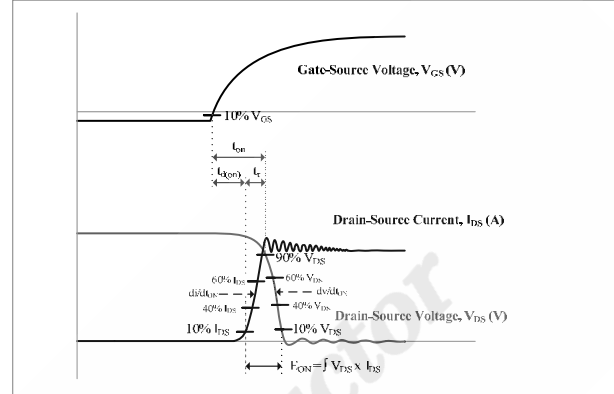


Figure 30. Turn-on Transient Definitions

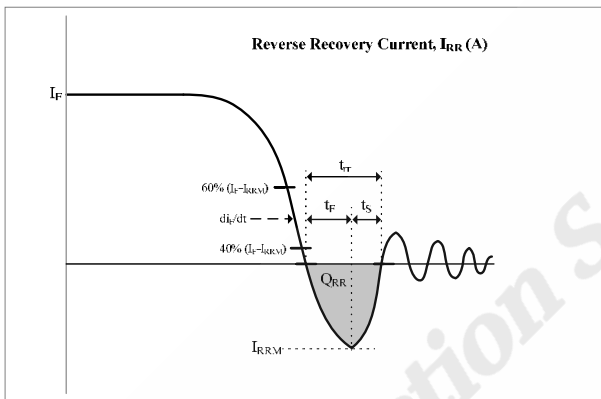


Figure 31. Reverse Recovery Definitions

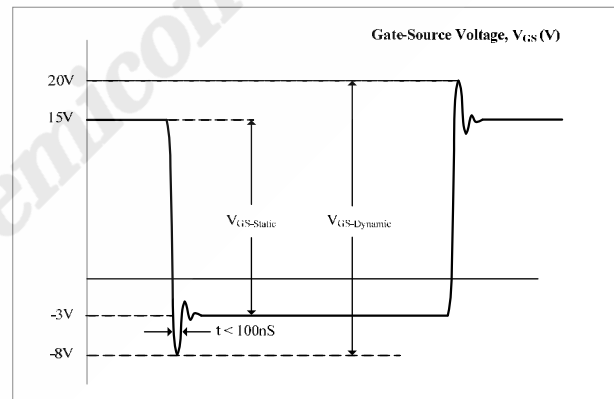
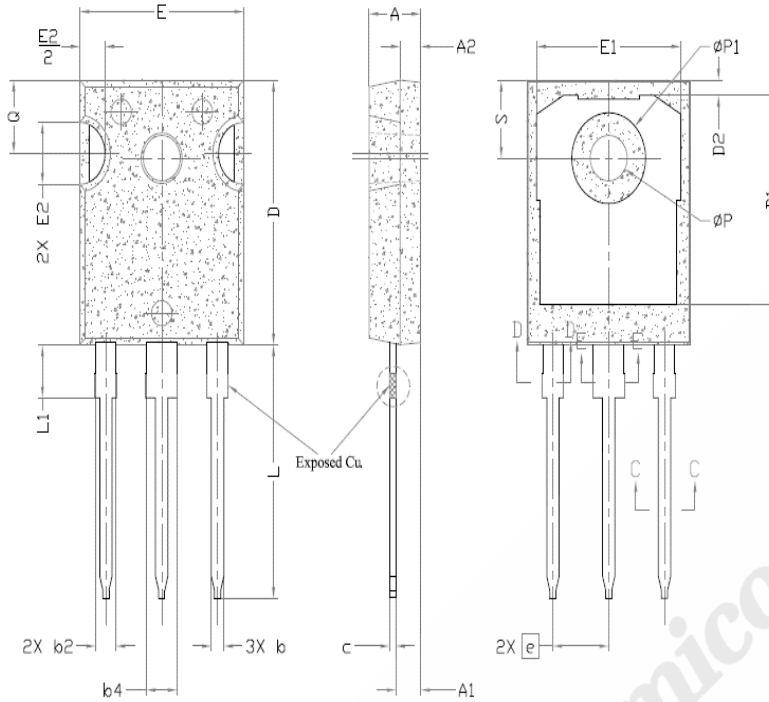


Figure 32. V<sub>GS</sub> Transient Definitions

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## 7. Package Outlines



SYMBOL	DIMENSIONS			NOTES
	MIN.	NOM.	MAX.	
A	4.83	5.02	5.21	
A1	2.29	2.41	2.55	
A2	1.50	2.00	2.49	
b	1.12	1.20	1.33	
b1	1.12	1.20	1.28	
b2	1.91	2.00	2.39	6
b3	1.91	2.00	2.34	
b4	2.87	3.00	3.22	6, 8
b5	2.87	3.00	3.18	
c	0.55	0.60	0.69	6
c1	0.55	0.60	0.65	
D	20.80	20.95	21.10	4
D1	16.25	16.55	17.65	5
D2	0.51	1.19	1.35	
E	15.75	15.94	16.13	4
E1	13.46	14.02	14.16	5
E2	4.32	4.91	5.49	3
e	5.44BSC			
L	19.81	20.07	20.32	
L1	4.10	4.19	4.40	6
$\phi P$	3.56	3.61	3.65	7
$\phi P1$	7.19REF.			
Q	5.39	5.79	6.20	
S	6.04	6.17	6.30	

Drawing and Dimensions

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## Important Notice

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For further information on the product, technology, delivery terms and conditions and prices please contact your nearest PN Junction office ([www.pnjsemi.com](http://www.pnjsemi.com)).

## Warnings

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