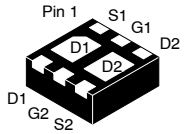
MOSFET – Dual, N-Channel, POWERTRENCH®

20 V, 3.7 A, 68 mΩ

FDMA1028NZ

V_{DS} MAX	$R_{DS(on)}$ MAX	I_D MAX
20 V	68 mΩ @ 4.5 V	3.7 A
	86 mΩ @ 2.5 V	



WDFN6 2x2, 0.65P
(MicroFET 2x2)
CASE 511DA

General Description

This device is designed specifically as a single package solution for dual switching requirements in cellular handset and other ultra−portable applications. It features two independent N−Channel MOSFETs with low on−state resistance for minimum conduction losses. The MicroFET™ 2x2 offers exceptional thermal performance for its physical size and is well suited to linear mode applications.

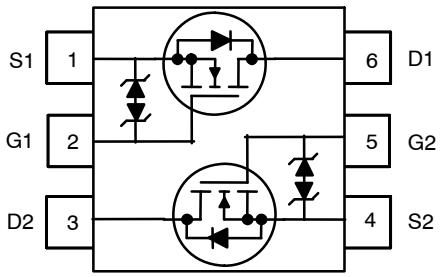
Features

- 3.7 A, 20 V
  $R_{DS(on)}$ = 68 mΩ at V_{GS} = 4.5 V
  $R_{DS(on)}$ = 86 mΩ at V_{GS} = 2.5 V
- Low Profile − 0.8 mm Maximum − In the New Package MicroFET 2x2 mm
- HBM ESD Protection Level > 2 kV (Note 3)
- Free from Halogenated Compounds and Antimony Oxides
- This Device is Pb−Free, Halide Free and is RoHS Compliant

MARKING DIAGRAM

&Z = Assembly Plant Code
&2 = 2−Digit Date Code
&K = 2−Digits Lot Run Traceability Code
028 = Device Code

PIN CONNECTIONS



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{DS}	Drain−Source Voltage	20	V
V_{GS}	Gate−Source Voltage	±12	V
I_D	Drain Current −Continuous (Note 1a) −Pulsed	 3.7 6	A
P_D	Power Dissipation for Single Operation (Note 1a) (Note 1b)	 1.4 0.7	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range	−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	86 (Single Operation)	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1b)	173 (Single Operation)	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1c)	69 (Dual Operation)	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1d)	151 (Dual Operation)	

ORDERING INFORMATION

Device	Package	Shipping†
FDMA1028NZ	WDFN6 (Pb−Free, Halide Free)	3000 / Tape & Reel

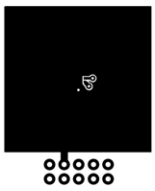
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain−Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	20	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25°C	–	15	–	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 16 V, V_{GS} = 0 V	–	–	1	μA
I_{GSS}	Gate−Body Leakage	V_{GS} = ±12 V, V_{DS} = 0 V	–	–	±10	μA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	I_D = 250 μA, V_{DS} = V_{GS}	0.6	1.0	1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25°C	–	−4	–	mV/°C
$R_{DS(on)}$	Static Drain−Source On−Resistance	V_{GS} = 4.5 V, I_D = 3.7 A	–	37	68	mΩ
		V_{GS} = 2.5 V, I_D = 3.3 A	–	50	86	
		V_{GS} = 4.5 V, I_D = 3.7 A, T_J = 125°C	–	53	90	
g_{FS}	Forward Transconductance	I_D = 3.7 A, V_{DS} = 10 V	–	16	–	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 10 V, V_{GS} = 0 V, f = 1.0 MHz	–	340	–	pF
C_{oss}	Output Capacitance		–	80	–	pF
C_{rss}	Reverse Transfer Capacitance		–	60	–	pF
Rg	Gate Resistance		–	–	25	Ω
SWITCHING CHARACTERISTICS (Note 2)						
$t_{d(on)}$	Turn−On Delay Time	V_{DD} = 10 V, I_D = 1 A, V_{GS} = 4.5 V, R_{GEN} = 6 Ω	–	8	16	ns
t_r	Turn−On Rise Time		–	8	16	ns
$t_{d(off)}$	Turn−Off Delay Time		–	14	26	ns
t_f	Turn−Off Fall Time		–	3	6	ns
Q_g	Total Gate Charge	V_{DS} = 10 V, I_D = 3.7 A, V_{GS} = 4.5 V	–	4	6	nC
Q_{gs}	Gate−Source Charge		–	0.7	–	nC
Q_{gd}	Gate−Drain Charge		–	1.1	–	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 oz. copper pad on a 1.5 x 1.5 in. board of FR−4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.
   a. $R_{\theta JA}$ = 86°C/W when mounted on a 1 in^2 pad of 2 oz copper, 1.5" x 1.5" x 0.062" thick PCB. For single operation.
   b. $R_{\theta JA}$ = 173°C/W when mounted on a minimum pad of 2 oz copper. For single operation.
   c. $R_{\theta JA}$ = 69°C/W when mounted on a 1 in^2 pad of 2 oz copper, 1.5" x 1.5" x 0.062" thick PCB. For dual operation.
   d. $R_{\theta JA}$ = 151°C/W when mounted on a minimum pad of 2 oz copper. For dual operation.



a. 86°C/W when mounted on a 1 in^2 pad of 2 oz copper.

b. 173°C/W when mounted on a minimum pad of 2 oz copper.

c. 69°C/W when mounted on a 1 in^2 pad of 2 oz copper.

d. 151°C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 μs, Duty Cycle < 2.0%
3. The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

TYPICAL CHARACTERISTICS

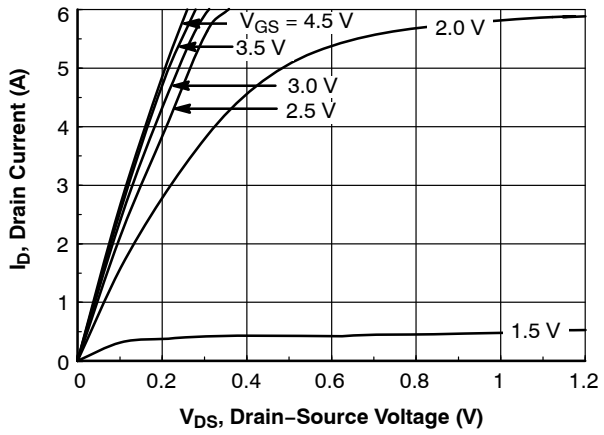


Figure 1. On−Region Characteristics

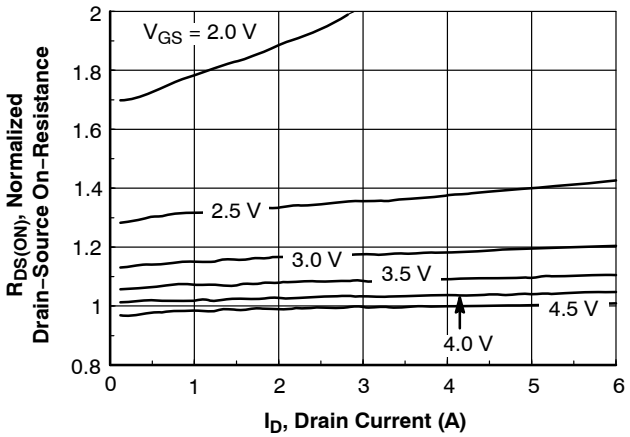


Figure 2. On−Resistance Variation with Drain Current and Gate Voltage

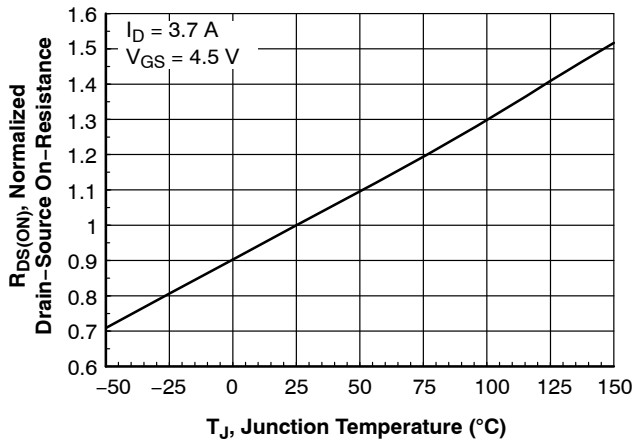


Figure 3. On−Resistance Variation with Temperature

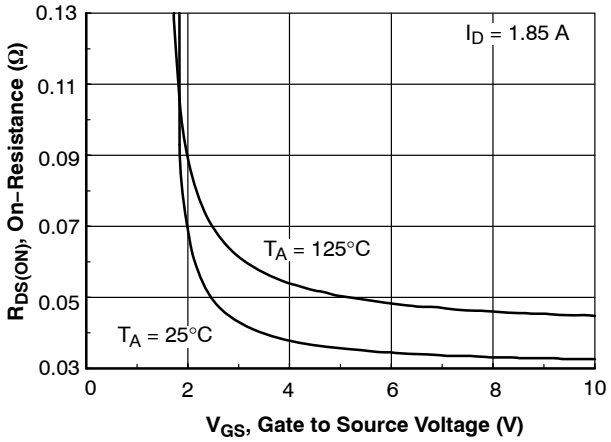


Figure 4. On−Resistance Variation with Gate−to−Source Voltage

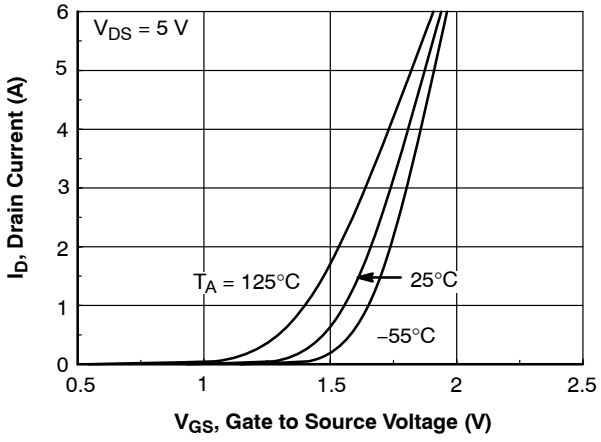


Figure 5. Transfer Characteristics

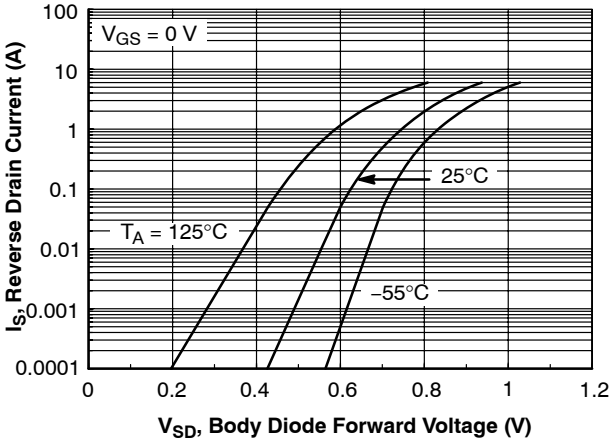


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

TYPICAL CHARACTERISTICS (continued)

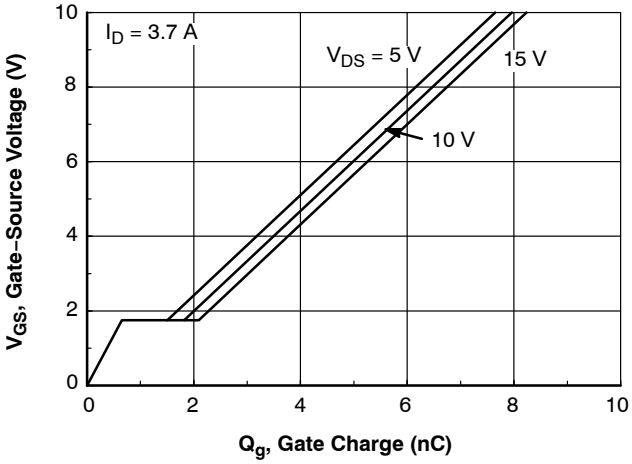


Figure 7. Gate Charge Characteristics

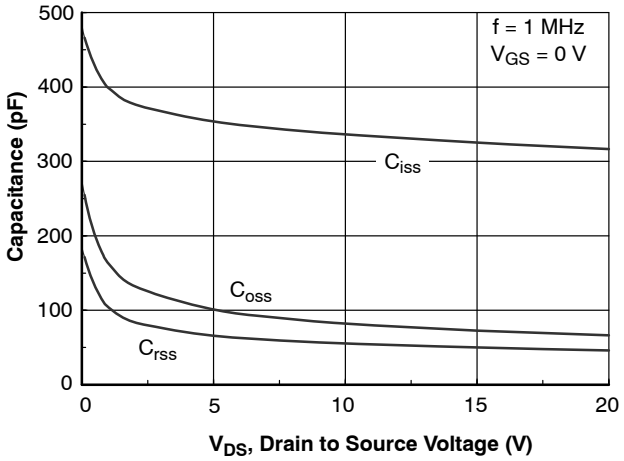


Figure 8. Capacitance Characteristics

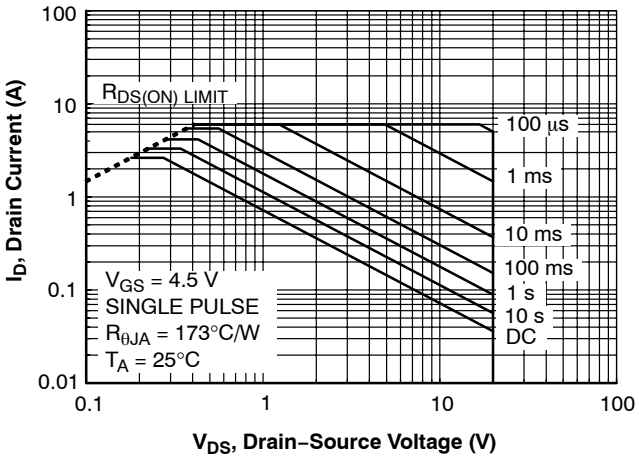


Figure 9. Maximum Safe Operating Area

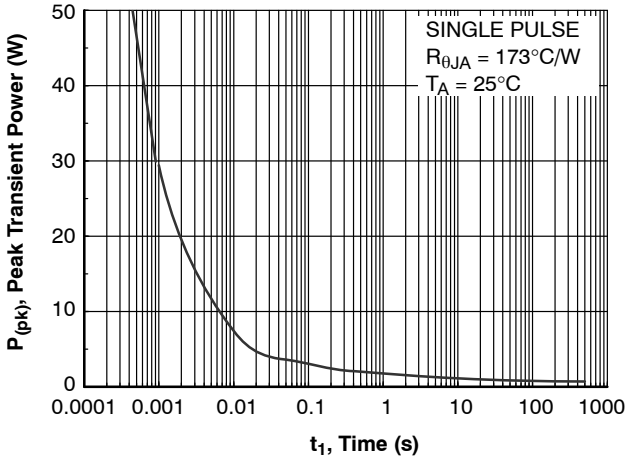


Figure 10. Single Pulse Maximum Power Dissipation

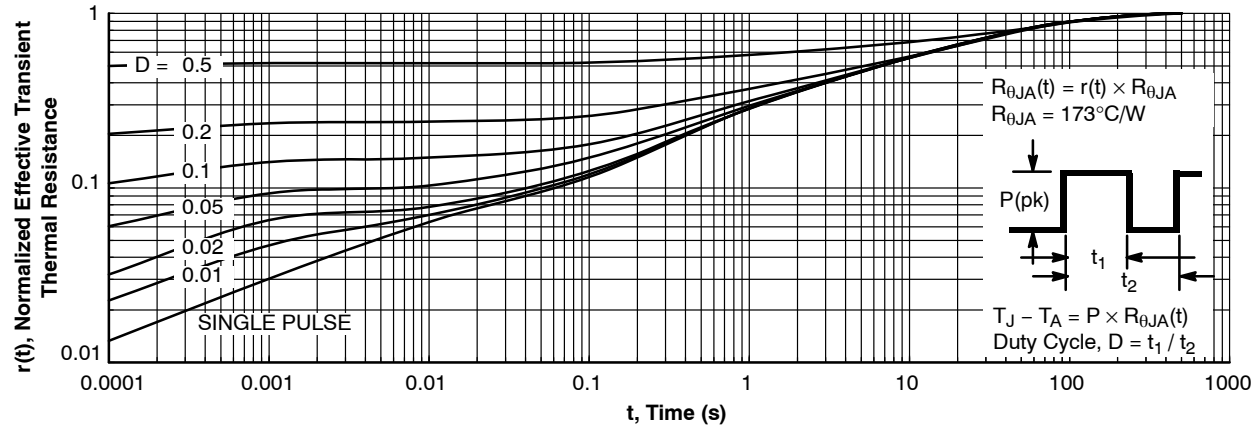


Figure 11. Transient Thermal Response Curve

Thermal characterization performed using the conditions described in Note 1b.
Transient thermal response will change depending on the circuit board design.

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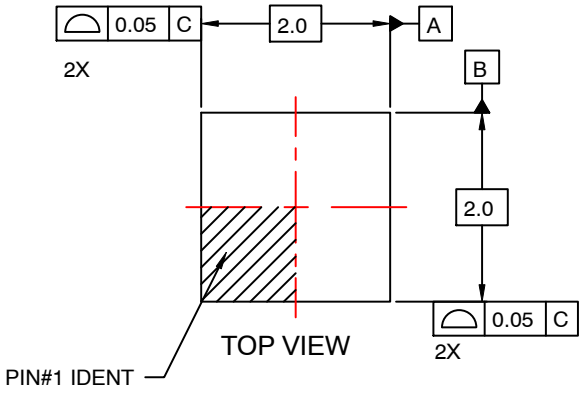
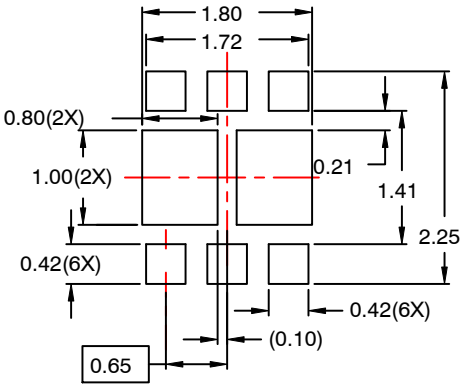
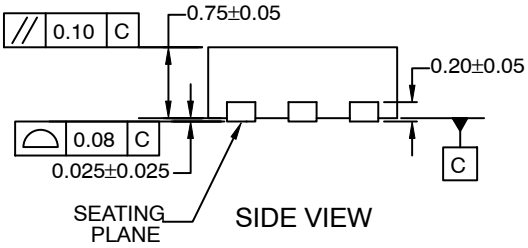
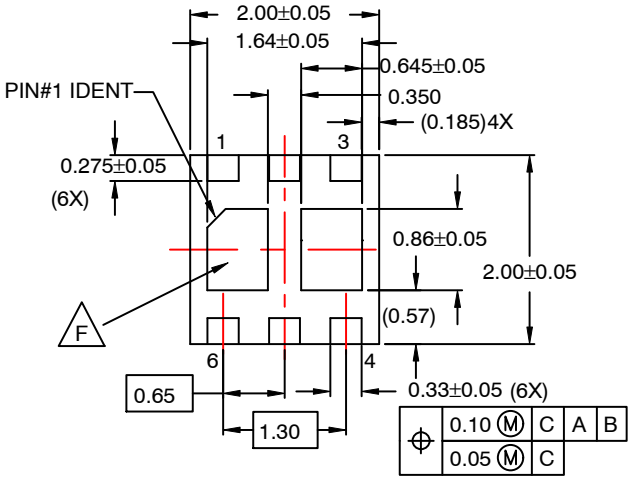




RECOMMENDED
LAND PATTERN





BOTTOM VIEW

NOTES:

A. CONFORM TO JADEC REGISTRATIONS MO−229, VARIATION VCCC, EXCEPT WHERE NOTED.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.

D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.

F. NON−JEDEC DUAL DAP

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