

ISOW784x to ISOW774x Adaptor Evaluation Module



ABSTRACT

This user's guide describes the ISOW784x to ISOW774x adaptor evaluation module (EVM). This EVM lets designers evaluate device performance for fast development and analysis of isolated systems. The EVM supports evaluation of the quad-channel digital isolator with integrated DC-DC converter ISOW774x of 20-pin WB SOIC package (DFM-20) on any PCB with ISOW784x 16-pin WB SOIC (DW-16) footprint as a replacement for ISOW784x device.

CAUTION

This evaluation module is made available for isolator parameter performance evaluation only and is not intended for isolation voltage testing. To prevent damage to the EVM, any voltage applied to device supply or data input pins must be maintained within 0 V to 5.5 V range as specified in datasheet section "Recommended Operating Conditions".

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1 Introduction

This user's guide describes EVM operation with respect to the ISOW774x quad-channel digital isolator with integrated DC-DC converter in 20-pin WB SOIC package (DFM-20). This user guide also includes the EVM BoM, EVM schematic, EVM PCB layout, and typical laboratory setup.

2 Overview

The ISOW774x, where 'x' can be any number from 0 to 4 based on the number of channels in reverse, is a galvanically-isolated quad-channel digital isolator with an integrated high-efficiency, low emissions power converter. The integrated DC-DC converter provides up to 550 mW of isolated power, eliminating the need for a separate isolated power supply in space-constrained isolated designs. The high-efficiency of the power converter allows for operation at a wide operating ambient temperature range of -40°C to $+125^{\circ}\text{C}$. This device provides improved emissions performance, allowing for simplified board design and has provisions for ferrite beads to further attenuate emissions. The ISOW774x has been designed with enhanced protection features in mind, including soft-start to limit inrush current, over-voltage and under-voltage lock out, fault detection on the EN/FLT pin, overload and short-circuit protection, and thermal shutdown.

The ISOW774x device provides high electromagnetic immunity while isolating CMOS or LVCMOS digital I/Os. The signal-isolation channel has a logic input and output buffer separated by a double capacitive silicon dioxide (SiO_2) insulation barrier, whereas, power isolation uses on-chip transformers separated by thin film polymer as insulating material. The ISOW774x can operate from a single supply voltage of 3 V to 5.5 V by connecting V_{IO} and V_{DD} together on PCB. If lower logic levels are required, these devices support 1.71 V to 5.5 V logic supply (V_{IO}) that can be independent from the power converter supply (V_{DD}) of 3 V to 5.5 V. V_{ISOIN} and V_{ISOOUT} needs to be connected on board with either a ferrite bead or fed through a LDO.

ISOW784x is a first-generation family of quad-channel digital isoaltors with integrated DC-DC converter and ISOW774x is the second-generation family of quad-channel digital isoaltors with integrated DC-DC converter. One of the major improvements done in ISOW774x family compared to ISOW784x is the radiated emissions performance. Other improvements include, lower output ripple voltage, separate logic and DC-DC converter supply, wider supply voltage option for data channels and many other smaller additional features. Unfortunately, ISOW774x isn't pin-compatible to ISOW784x and hence, ISOW774x cannot be directly evaluated on an existing customer PCB that is built with ISOW784x.

The ISOW-ADAPTOR-EVM is and adaptor PCB that enables customers to mount ISOW774x device on their existing PCBs with ISOW784x footprint. By facilitating mounting of ISOW774x on ISOW784x customer PCB, the adaptor PCB enables evaluation of existing ISOW784x customer PCB with ISOW774x to verify the overall improvements that can be achieved with the upgrade to ISOW774x. This is especially useful for verifying the improvement that can be achieved in radiated emissions performance by using ISOW774x in their existing PCB without needing any PCB redesign and saving significant development time.

3 Pin Configurations of the ISOW7841 and ISOW7741

Figure 3-1, Figure 3-2 and Figure 3-3 show the pin configurations of ISOW7841, ISOW7741 and ISOW-ADAPTOR-EVM, respectively.

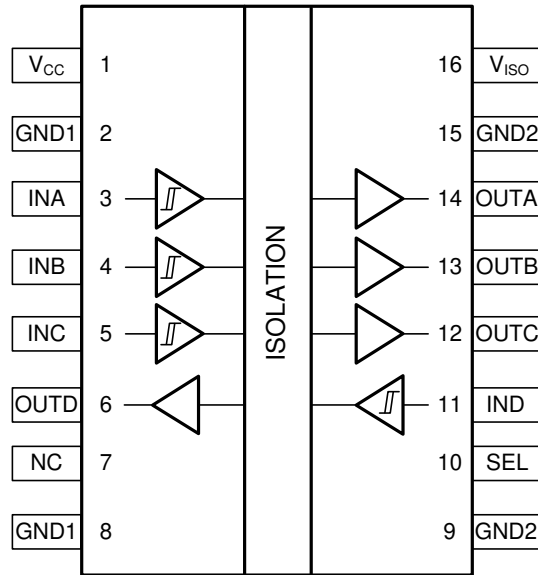


Figure 3-1. ISOW7841 Quad-Channel Digital Isolator with Integrated DC-DC Converter Pin Configuration

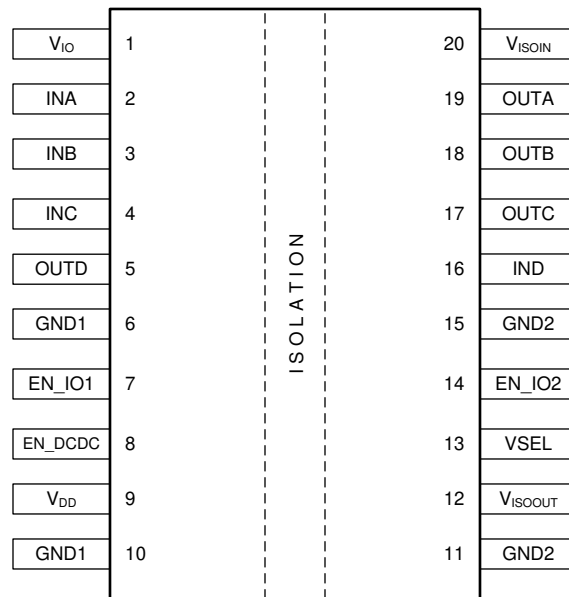


Figure 3-2. ISOW7741 Quad-Channel Digital Isolator with Integrated DC-DC Converter Pin Configuration

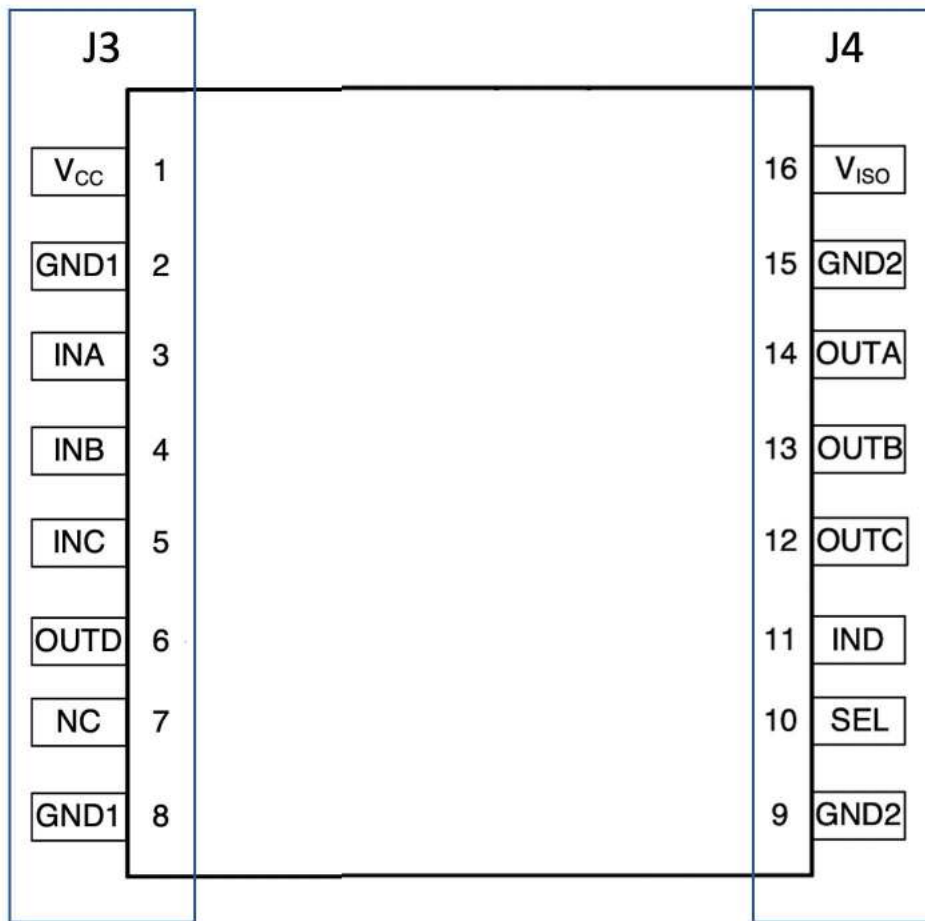


Figure 3-3. ISOW-ADAPTOR-EVM Pin Configuration

4 EVM Setup and Operation

This section describes the typical test setup and operation of the EVM for device evaluation. [Figure 4-1](#) shows how the ISOW-ADAPTOR-EVM can be mounted onto a PCB with ISOW784x footprint. The headers J3 and J4 are located under the PCB, hence, it might not be convenient to solder the whole PCB onto ISOW784x footprint as-is. Therefore, it is suggested that headers J3 and J4 are unplugged from J1 and J2 first, then J3 and J4 be soldered onto ISOW784x footprint after estimating their approximate positions and then headers J1 and J2 be plugged onto J3 and J4, respectively. If needed, headers J3 and J4 can also be slightly bent to adjust the positions making it convenient to mount J1 and J2 as needed. [Figure 4-2](#) shows a photograph of actual PCB side view highlighting J3 and J4 leads.

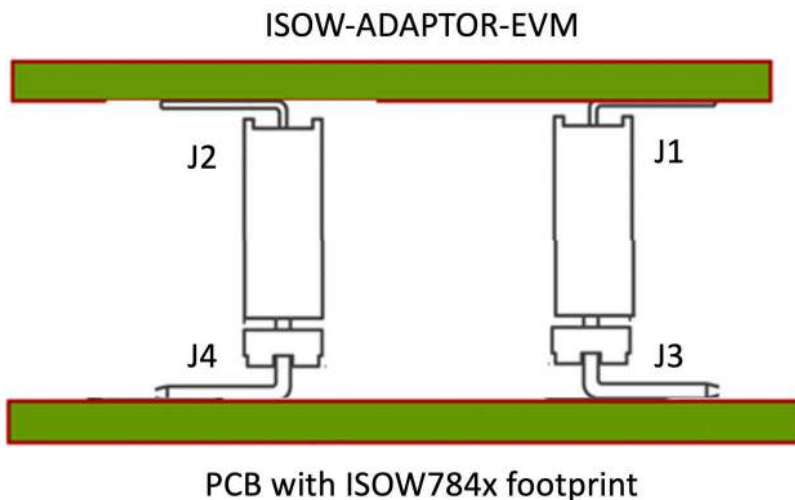


Figure 4-1. ISOW-ADAPTOR-EVM Connection Diagram



Figure 4-2. ISOW-ADAPTOR-EVM Side View

5 EVM Schematic

Figure 5-1 shows the ISOW-ADAPTOR-EVM schematic. Please note that headers J3 and J4 are not shown in the schematic as they are externally plugged onto J1 and J2.

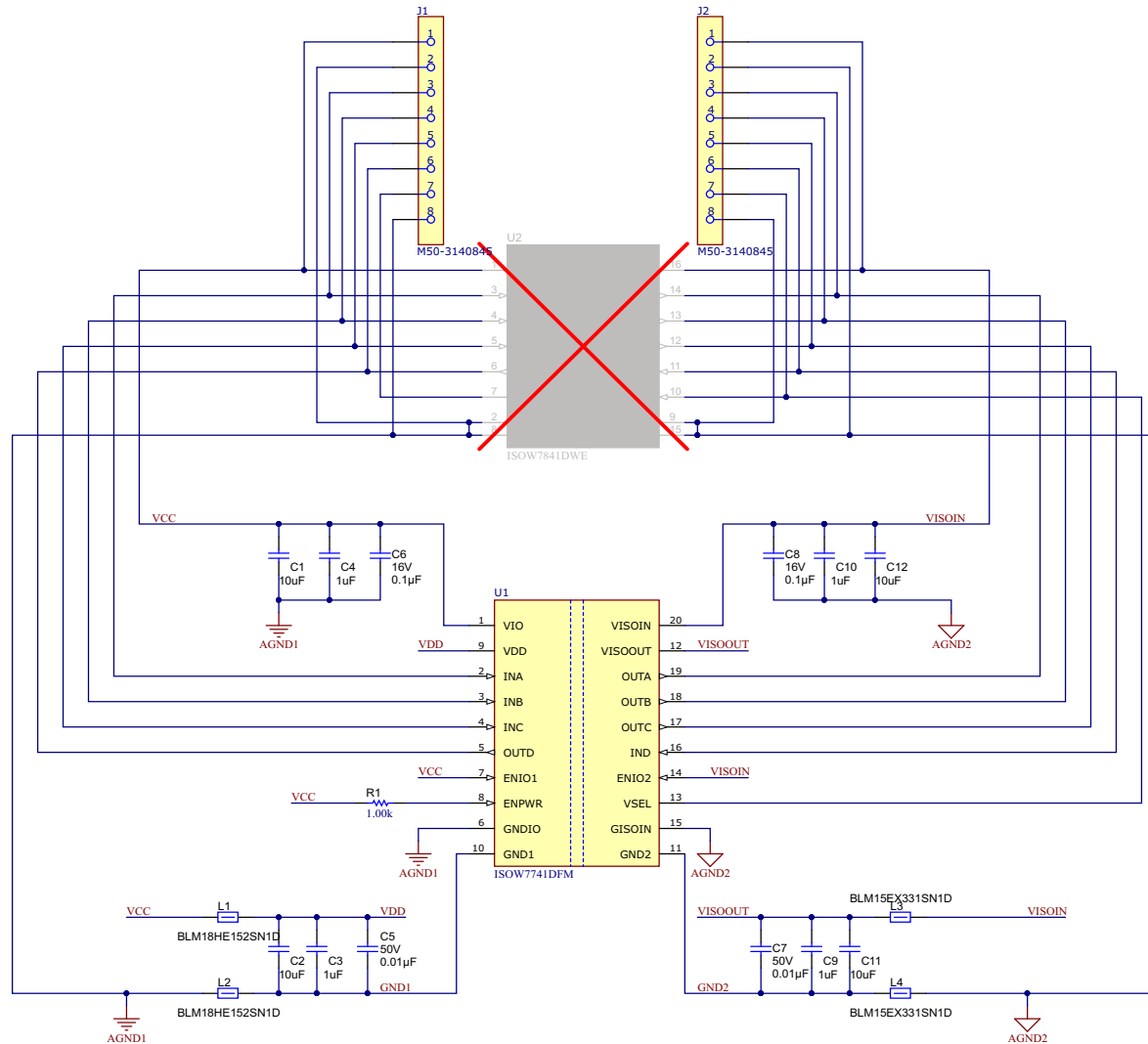


Figure 5-1. ISOW-ADAPTOR-EVM Schematic

6 PCB Layout and 3D Diagram

Figure 6-1 and Figure 6-2 show the printed-circuit board (PCB) layout top and bottom layers of the EVM, respectively, and Figure 6-3 shows a 3D diagram of the PCB visualizing how a finished board will look.

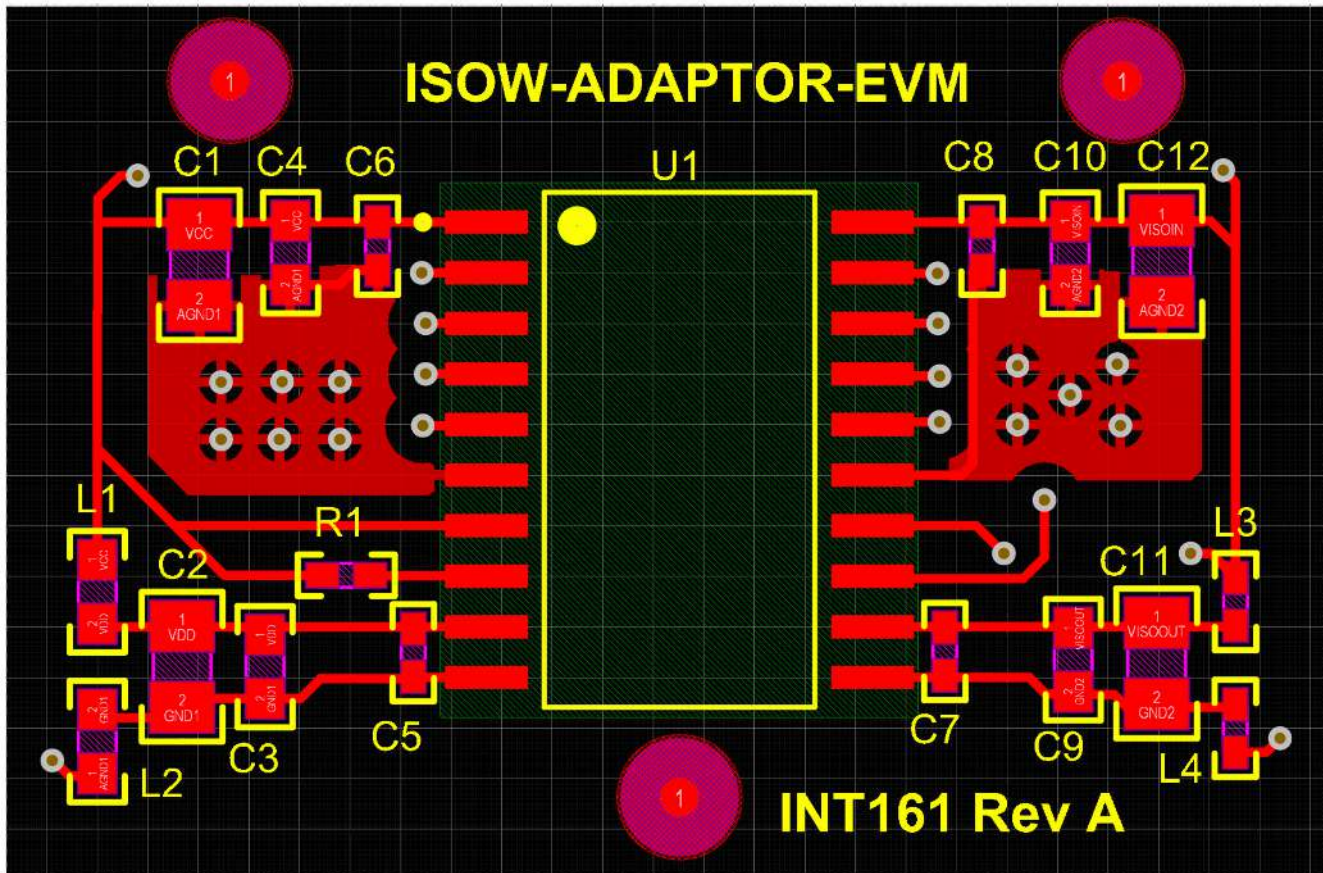


Figure 6-1. ISOW-ADAPTOR-EVM PCB Layout - Top Layer

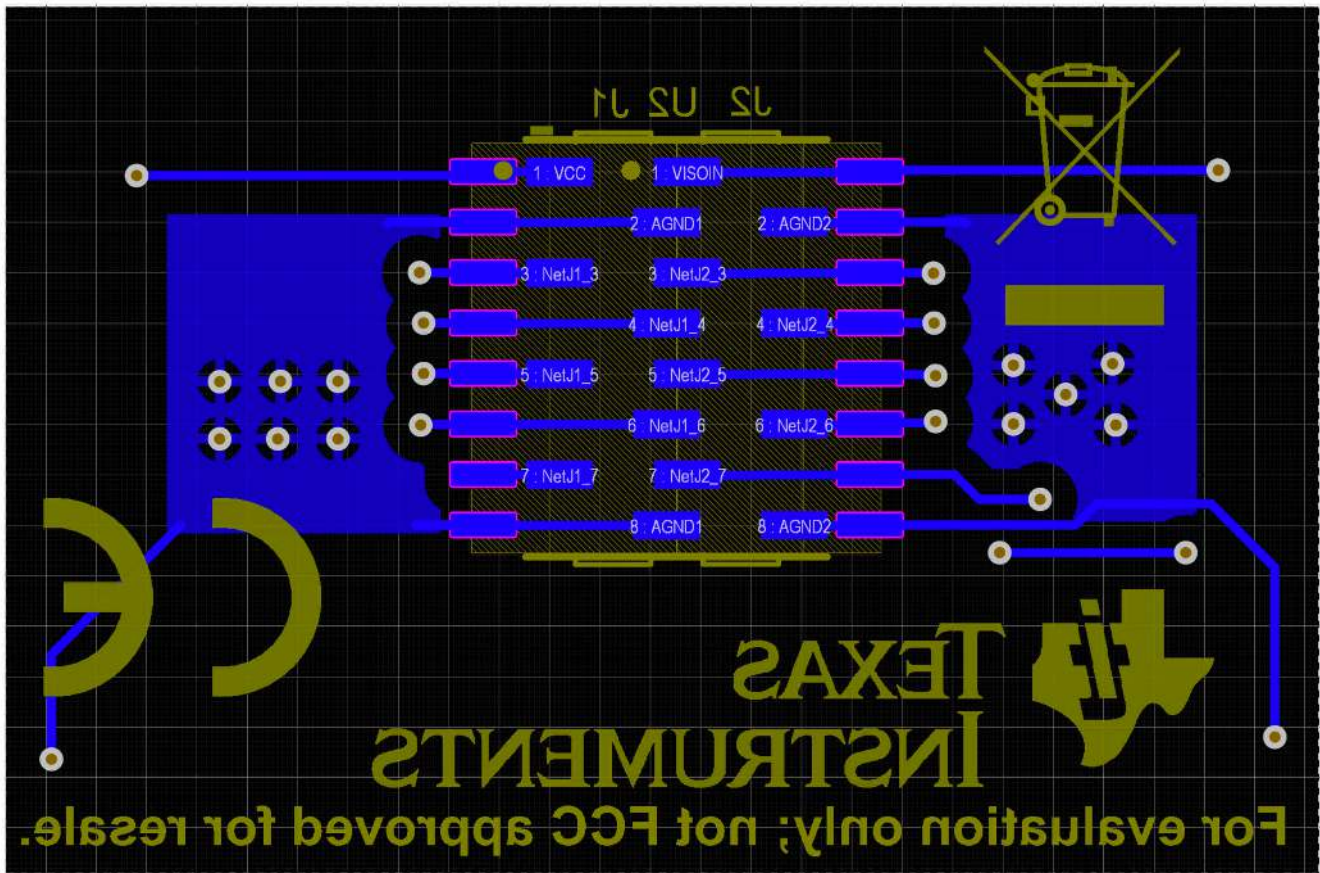


Figure 6-2. ISOW-ADAPTOR-EVM PCB Layout - Bottom Layer

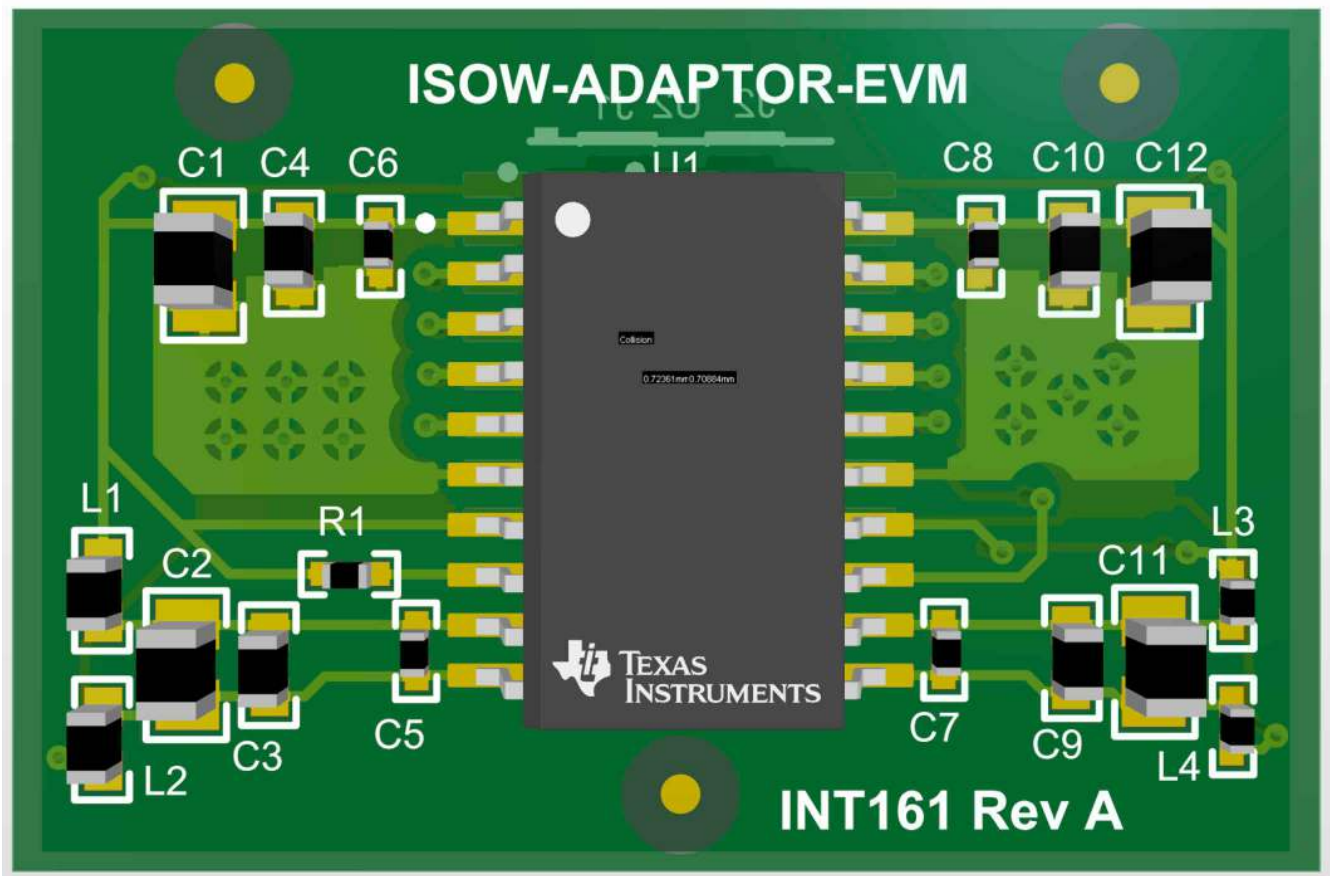


Figure 6-3. ISOW-ADAPTOR-EVM PCB 3D Diagram

7 Bill of Materials

Table 7-1 shows the bill of materials (BOM) for the EVM.

Table 7-1. Bill of Materials

Item	Designator	Description	Manufacturer	PartNumber	Quantity
1	C1, C2, C11, C12	CAP, CERM, 10 uF, 35 V, +/- 10%, X5R, 0805	MuRata	GRM21BR6YA106KE43L	4
2	C3, C4, C9, C10	CAP, CERM, 1 uF, 50 V, +/- 10%, X5R, 0603	Samsung Electro-Mechanics	CL10A105KA8NNNC	4
3	C5, C7	CAP, CERM, 0.01 uF, 50 V, +/- 10%, X7R, 0402	Walsin	0402B103K500CT	2
4	C6, C8	CAP, CERM, 0.1 uF, 16 V, +/- 10%, X7R, 0402	Walsin	CL05B104KO5NNNC	2
5	J1, J2	Female Header, 1.27mm, 8x1	Harwin	M50-3140845	2
6	J3, J4	Male Header, 1.27mm, 8x1	Sullins	GRPB081VWCN-RC	2
7	L1, L2	Ferrite Bead, 1500 ohm @ 100 MHz, 0.5 A, 0603	MuRata	BLM18HE152SN1D	2
8	L3, L4	Ferrite Bead, 330 ohm @ 100 MHz, 1.1 A, 0402	MuRata	BLM15EX331SN1D	2
9	R1	RES, 1.00 k, 1%, 0.0625 W, 0402	Yageo America	RC0402FR-071KL	1
10	U1	ISOW7741DFM	Texas Instruments	ISOW7741DFM	1
11	U2	ISOW7841DWE	Texas Instruments	ISOW7841DWE	0

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