



DGD21844M

600V HALF-BRIDGE GATE DRIVER IN SO-14

Description

The DGD21844M is a high-voltage and high-speed gate driver capable of driving N-Channel MOSFETs and IGBTs in a half-bridge configuration. High-voltage processing techniques enable the DGD21844M's high-side to switch to 600V in a bootstrap operation.

The DGD21844M logic inputs are compatible with standard TTL and CMOS levels (down to 3.3V) for easy interfacing with controlling devices. The driver outputs feature high-pulse current buffers designed for minimum driver cross conduction. Programmable deadtime by an external resistor provides more system level flexibility.

The DGD21844M is offered in the SO-14 (Type TH) package and the device's operating temperature extends from -40° C to $+125^{\circ}$ C.

Applications

- DC-DC converters
- DC-AC inverters
- AC-DC power supplies
- Motor controls
- Class-D power amplifiers

Up to 600V + Ī но Vcc VH Vcc o TO LOAD IN Vs SD* 0 SD⁴ DGD21844M DT COM Vss LO

Typical Configuration

Features

- Floating High-Side Driver in Bootstrap Operation to 600V
- Drives Two N-Channel MOSFETs or IGBTs in Half Bridge
 Configuration
- 1.9A Source / 2.3A Sink Output Current Capability
- Outputs Tolerant to Negative Transients
- Programmable Deadtime to Protect MOSFETs
- Wide Low-Side Gate Driver and Logic Supply: 10V to 20V
- Wide Logic Supply Voltage Offset Voltage: -5V to 5V
- Logic Input (IN and SD*) 3.3V Capability
- Schmitt Triggered Logic Inputs with Internal Pull Down
- Undervoltage Lockout for High- and Low-Side Drivers
- Extended Temperature Range: -40°C to +125°C
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony free. "Green" Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please <u>contact us</u> or your local Diodes representative. <u>https://www.diodes.com/quality/product-definitions/</u>

Mechanical Data

- Package: SO-14 (Type TH)
- Package Material: Molded Plastic. "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 3 per J-STD-020
- Terminals: Finish Matte Tin Plated Leads, Solderable per MIL-STD-202, Method 208 ⁽³⁾
- Weight: 0.142 grams (Approximate)



Top View

Ordering Information (Note 4)

Orderable Part Number	Paokago	Marking Reel Size (inches)		Tape Width (mm)	Packing		
Orderable Part Number Package	Fackage	warking	neel Size (Inches)	rape width (mm)	Qty.	Carrier	
DGD21844MS14-13	SO-14 (Type TH)	DGD21844M	13	16	2,500	Reel	

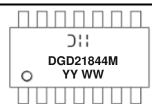
Notes: 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.

2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.

3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

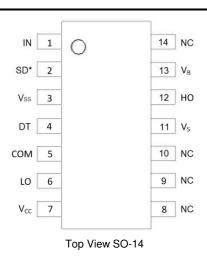
Marking Information



)'! = Manufacturer's Marking DGD21844M = Product Type Marking Code YY = Year (ex: 23 = 2023) WW = Week (01 to 53)



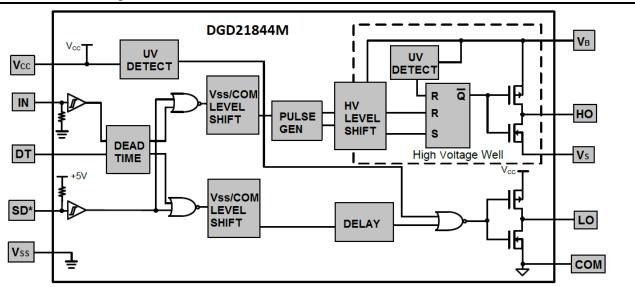
Pin Diagrams



Pin Descriptions

Pin Number	Pin Name	Function
1	IN	Logic input for high-side and low-side gate driver outputs (HO and LO), in phase with HO (referenced to V_{SS})
2	SD*	Logic input for shutdown (referenced to V _{SS}), enabled low
3	V _{SS}	Logic ground
4	DT	Programmable Deadtime lead, referenced to V _{SS}
5	COM	Low-side return
6	LO	Low-side gate drive output
7	V _{CC}	Low-side and logic fixed supply
8, 9, 10, 14	NC	No connection (no internal connection)
11	Vs	High-side floating supply return
12	HO	High-side gate drive output
13	VB	High-side floating supply

Functional Block Diagram





Absolute Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
High-Side Floating Supply Voltage	V _B	-0.3 to +624	V
High-Side Floating Supply Offset Voltage	Vs	V _B -24 to V _B +0.3	V
High-Side Floating Output Voltage	V _{HO}	V _S -0.3 to V _B +0.3	V
Offset Supply Voltage Transient	dV _S / dt	50	V/ns
Programmable Dead Time Pin Voltage	V _{DT}	V _{SS} -0.3 to V _{CC} +0.3	V
Logic and Low-Side Fixed Supply Voltage	V _{CC}	-0.3 to +24	V
Low-Side Output Voltage	V _{LO}	-0.3 to V _{CC} +0.3	V
Logic Supply Offset Voltage	V _{SS}	V _{CC} -24 to V _{CC} +0.3	V
Logic Input Voltage (IN and SD*)	V _{IN}	V _{SS} -0.3 to V _{CC} +0.3	V

Thermal Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Power Dissipation Linear Derating Factor (Note 5)	PD	1.0	W
Thermal Resistance, Junction to Ambient (Note 5)	R _{0JA}	120	°C/W
Operating Temperature	TJ	+150	
Lead Temperature (Soldering, 10s)	TL	+300	°C
Storage Temperature Range	T _{STG}	-55 to +150	

Note: 5. When mounted on a standard JEDEC 2-layer FR-4 board.

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
High Side Floating Supply Absolute Voltage	VB	V _S + 10	V _S + 20	V
High Side Floating Supply Offset Voltage	Vs	(Note 6)	600	V
High Side Floating Output Voltage	V _{HO}	Vs	VB	V
Logic and Low Side Fixed Supply Voltage	Vcc	10	20	V
Low Side Output Voltage	V _{LO}	0	V _{CC}	V
Logic Input Voltage (IN and SD*)	V _{IN}	V _{SS}	5	V
Programmable Dead Time Pin Voltage	V _{DT}	Vss	Vcc	V
Logic Ground	V _{SS}	-5	5	V
Ambient Temperature	T _A	-40	+125	°C

Note: 6. Logic operation for $V_S = -5V$ to +600V.



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Parameter	Symbol	Min	Тур	Max	Unit	Conditions
Logic "1" Input Voltage for HO & Logic "0" for LO	VIH	2.5		_	V	$V_{CC} = 10V$ to 20V
Logic "0" Input Voltage for HO & Logic "1" for LO	VIL	_		0.8	V	$V_{CC} = 10V$ to 20V
SD* Input Positive Going Threshold	V _{SDTH+}	2.5	—	_	V	$V_{CC} = 10V$ to 20V
SD* Input Negative Going Threshold	V _{SDTH-}	_	—	0.8	V	$V_{CC} = 10V$ to 20V
High Level Output Voltage, V _{BIAS} - V _O	V _{OH}	—	—	1.4	V	$I_{O} = 0mA$
Low Level Output Voltage, V _O	V _{OL}	—	—	0.2	V	I _O = 20mA
Offset Supply Leakage Current	I _{LK}	—	—	50	μA	$V_{B} = V_{S} = 600V$
Quiescent V _{BS} Supply Current	I _{BSQ}	20	60	150	μA	$V_{IN} = 0V \text{ or } 5V$
Quiescent V _{CC} Supply Current	Iccq	0.4	1.0	1.8	mA	$V_{IN} = 0V \text{ or } 5V$
Logic "1" Input Bias Current	I _{IN+}	—	25	60	μA	IN = 5V, SD* = 0V
Logic "0" Input Bias Current	I _{IN-}	—	—	1.0	μA	IN = 0V, SD* = 5V
V _{BS} Supply Undervoltage Positive Going Threshold	V _{BSUV+}	8.0	8.9	9.8	V	_
V _{BS} Supply Undervoltage Negative Going Threshold	V _{BSUV-}	7.4	8.2	9.0	V	_
V _{CC} Supply Undervoltage Positive Going Threshold	V _{CCUV+}	8.0	8.9	9.8	V	
V _{CC} Supply Undervoltage Negative Going Threshold	V _{CCUV-}	7.4	8.2	9.0	V	_
Output-High Short-Circuit Pulsed Current	I _{O+}	1.4	1.9	_	А	V _O = 0V, PW ≤ 10µs
Output-Low Short-Circuit Pulsed Current	I _{O-}	1.7	2.3	_	А	V _O = 15V, PW ≤ 10µs

DC Electrical Characteristics (V_{BIAS} (V_{CC}, V_{BS}) = 15V, V_{SS} = COM, @T_A = +25°C, unless otherwise specified.) (Note 7)

Note: 7. The V_{IN} and I_{IN} parameters are referenced to V_{SS} and are applicable to the two logic input pins: IN and SD*. The V_O and I_O parameters are referenced to COM and are applicable to the respective output pins: HO and LO.

AC Electrical Characteristics (V_{BIAS} (V_{CC}, V_{BS}) = 15V, V_{SS} = COM, C_L = 1000pF, @T_A = +25°C, unless otherwise specified.)

Parameter	Symbol	Min	Тур	Max	Unit	Conditions
Turn-On Propagation Delay	ton	_	585	900	ns	$V_{\rm S} = 0V$
Turn-Off Propagation Delay	toff	_	170	400	ns	$V_{\rm S} = 0V \text{ or } 600V$
Shut-Down Propagation Delay	tsp	_	180	270	ns	_
Delay Matching, HO & LO Turn-On	t DMON	_	_	90	ns	_
Delay Matching, HO & LO Turn-Off	t DMOFF	_	_	40	ns	_
Turn-On Rise Time	t _R	_	40	60	ns	$V_{\rm S} = 0V$
Turn-Off Fall Time	t⊨	_	20	35	ns	$V_{\rm S} = 0V$
		280	400	520	ns	$R_{DT} = 0\Omega$
Deadtime: t _{DT LO-HO} & t _{DT HO-LO}	tот	4	5	6	μs	R _{DT} = 200kΩ
	tмdt	_	0	50	ns	$R_{DT} = 0\Omega$
Deadtime Matching = tpт Lo-нo - tpт нo-Lo		_	0	600	ns	R _{DT} = 200kΩ



Timing Waveforms

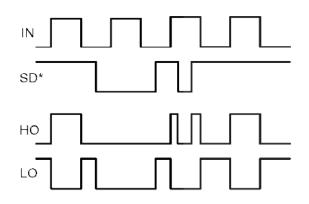


Figure 1. Input / Output Timing Diagram

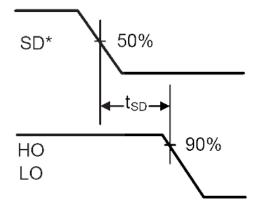
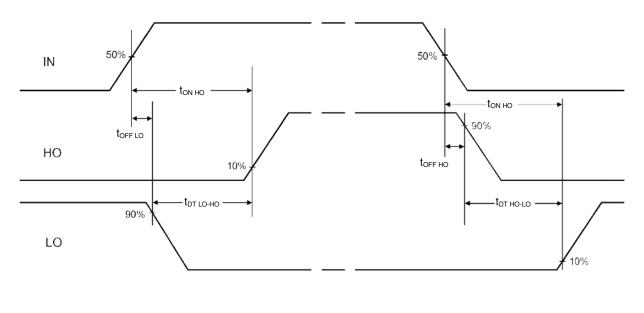
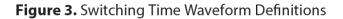


Figure 2. Shutdown Waveform Definitions



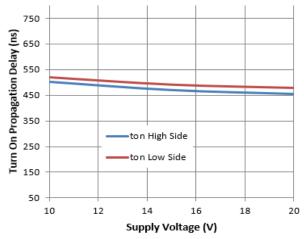
 $\begin{array}{l} \textbf{Deadtime } t_{\text{DT }L\text{O-HO}} = t_{\text{ON }H\text{O}} - t_{\text{OFF }L\text{O}} \\ t_{\text{DT }H\text{O-LO}} = t_{\text{ON }L\text{O}} - t_{\text{OFF }H\text{O}} \\ \textbf{Deadtime matching} \\ t_{\text{MDT}} = t_{\text{DT }L\text{O-HO}} - t_{\text{DT }H\text{O-LO}} \end{array}$

Delay matching $t_{DM OFF} = t_{OFF LO} - t_{OFFT HO}$





Typical Performance Characteristics ($V_{CC} = 15V$, $@T_A = +25^{\circ}C$, unless otherwise specified.)



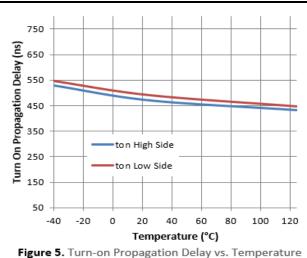


Figure 4. Turn-on Propagation Delay vs. Supply Voltage

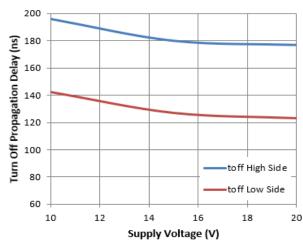
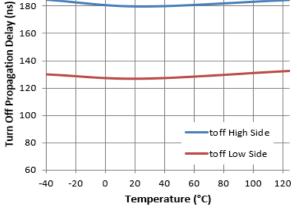


Figure 6. Turn-off Propagation Delay vs. Supply Voltage



200

180

Figure 7. Turn-off Propagation Delay vs. Temperature

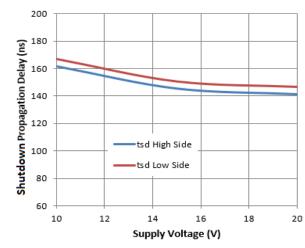
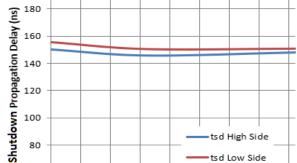


Figure 9. SD Propagation Delay vs. Supply Voltage



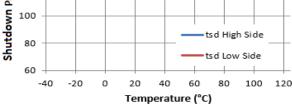
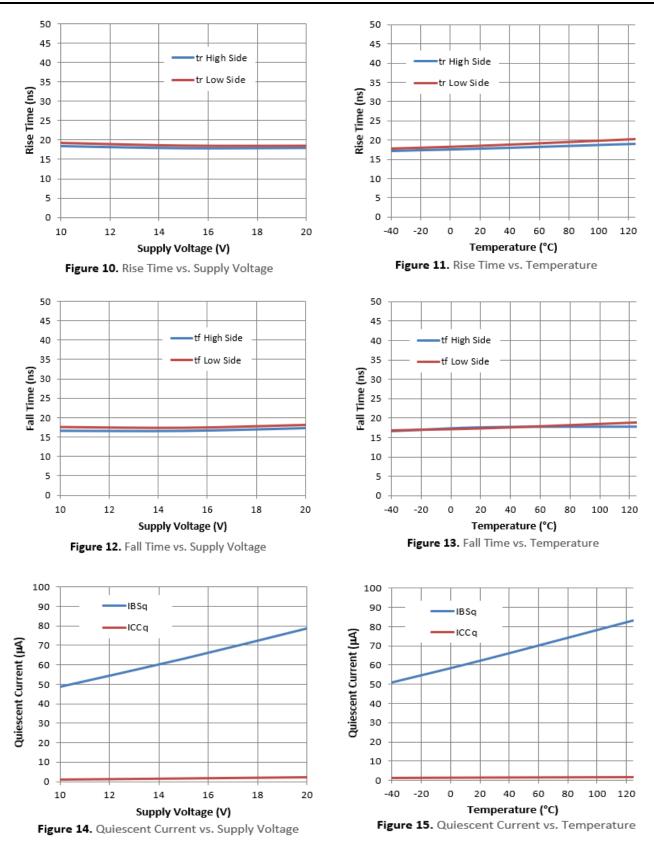


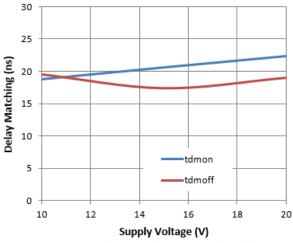
Figure 8. SD Propagation Delay vs. Temperature

200

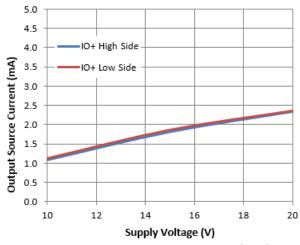














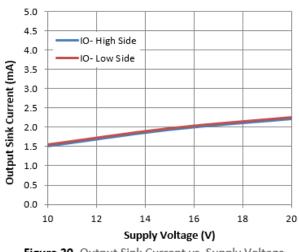
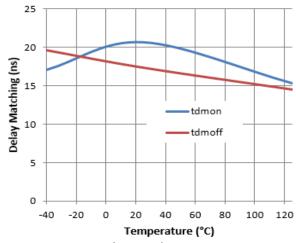
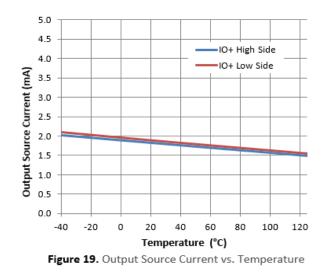
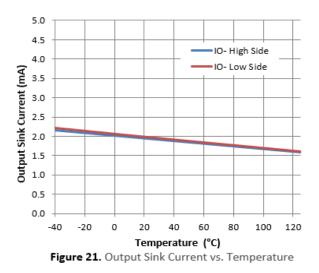


Figure 20. Output Sink Current vs. Supply Voltage

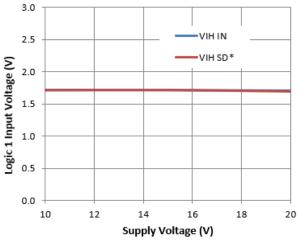




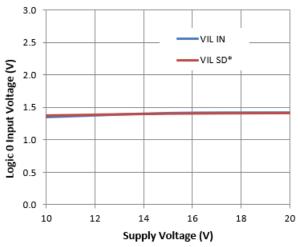




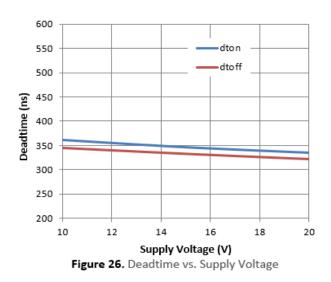












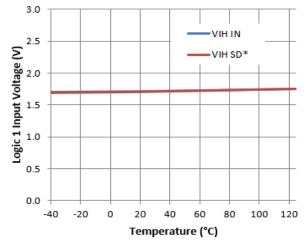


Figure 23. Logic 1 Input Voltage vs. Temperature

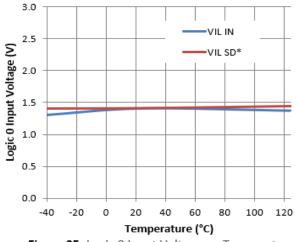
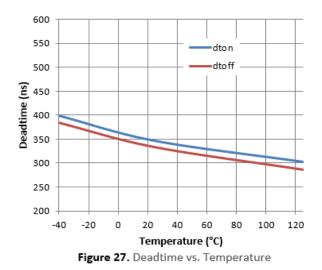
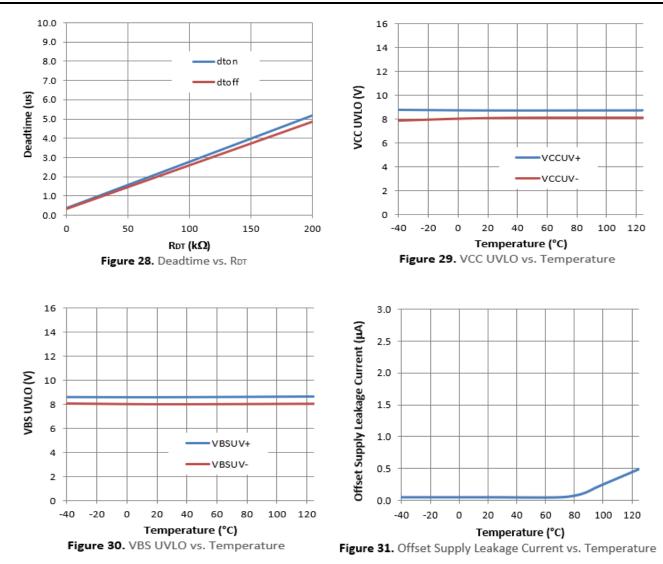


Figure 25. Logic 0 Input Voltage vs. Temperature



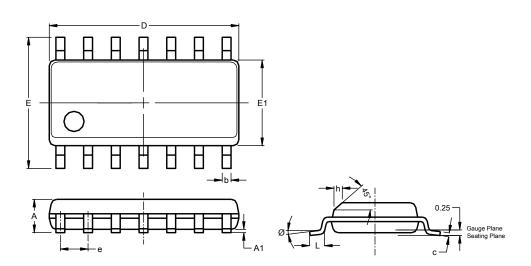






Package Outline Dimensions

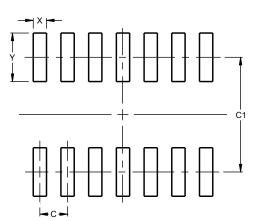
Please see http://www.diodes.com/package-outlines.html for the latest version.



SO-14 (Type TH)					
Dim	Min	Max	Тур		
Α	1.55	1.73			
A1	0.10	0.25			
b	0.35	0.51			
С	0.190	0.248			
D	8.56	8.74	8.61		
E	5.84	6.20	6.00		
E1	3.81	3.99	3.94		
е			1.27		
h			0.33		
L	0.41	0.89			
Ø	0°	8°			
All [Dimensi	ons in i	mm		

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.



SO-14 (Type TH)

Dimensions	Value (in mm)	
С	1.27	
C1	5.20	
Х	0.60	
Y	2.20	

SO-14 (Type TH)



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