

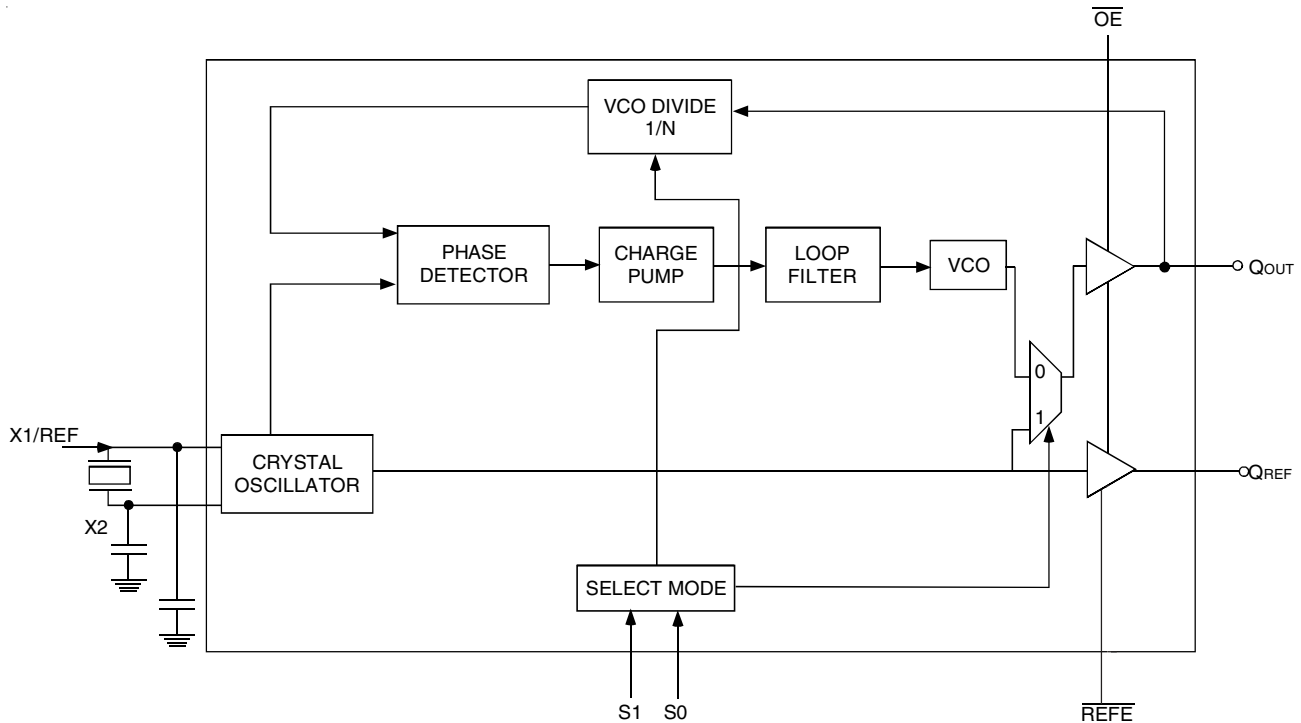
FEATURES:

- 3V to 3.6V operating voltage
- 48MHz to 160MHz output frequency range
- Input from fundamental crystal oscillator or external source
- Internal PLL feedback (loading the feedback output relative to the other outputs, will adjust the propagation delay between REF inputs and outputs)
- Select inputs (S[1:0]) for FB divide selection (multiply ratio of 2, 3, 4, 4.25, 5, 6, 6.25, and 8)
- Low jitter
- PLL bypass for testing and power-down control (S1 = H, S0 = H, powers part down <math><500\mu\text{A}</math>)
- Available in TSSOP package
- Pin and function compatible to IDT5V926

APPLICATIONS:

- Gigabit ethernet
- Router
- Network switches
- SAN
- Instrumentation
- Fibre channel

FUNCTIONAL BLOCK DIAGRAM

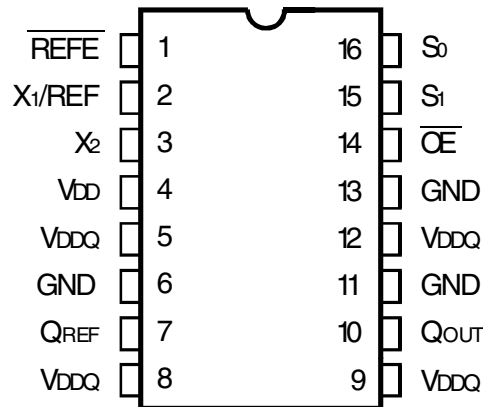


DESCRIPTION:

The IDT5V926A is a low-cost, low skew, low jitter, and high-performance clock multiplier with a reference clock from either a lower frequency crystal or clock input. It has been specially designed to interface with Gigabit Ethernet and Fast Ethernet applications by providing a 125MHz clock from 25MHz input. It can be programmed to provide output frequencies ranging from 48MHz to 160MHz, with input frequencies ranging from 6MHz to 80MHz.

The IDT5V926A includes an internal RC filter that provides excellent jitter characteristics and eliminates the need for external components. When using the optional crystal input, the device accepts a 10 - 40MHz fundamental mode crystal with a maximum equivalent series resistance of 50Ω.

PIN CONFIGURATION



TSSOP
TOP VIEW

CRYSTAL SPECIFICATION

The crystal oscillators should be fundamental mode quartz crystals; overtone crystals are not suitable. Crystal frequency should be specified for parallel resonance with 50Ω maximum equivalent series resonance. Crystal tuning capacitors should be connected from X1/REF to GND and from X2 to GND.

DIVIDE SELECTION TABLE⁽¹⁾

S1	S0	Divide-by-N Value	Mode
L	L	2	PLL
L	M	3	PLL
L	H	4	PLL
M	L	4.25	PLL
M	M	5	PLL
M	H	6	PLL
H	L	6.25	PLL
H	M	8	PLL
H	H	TEST	TEST (2)

NOTES:

- H = HIGH, M = MID, L = LOW
- Test mode for low frequency testing. In this mode, REF clock bypasses the VCO (VCO powered down) and the crystal oscillator is powered down.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Parameter	Max.	Unit
V _{DD} /V _{DDQ}	Supply Voltage to Ground	-0.5 to +4.6	V
V _I	Input Voltage	-0.5 to +4.6	V
I _O	Output Current	±50	mA
T _{STG}	Storage Temperature	-65 to +150	°C
T _J	Junction Temperature	150	°C

NOTE:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

PIN DESCRIPTION

Pin Name	Type	Description
S[1:0]	I	Three level divider/mode select pins. Float to MID.
$\overline{\text{OE}}$	I	Output enable bar. Outputs Qout and QREF are in a high-impedance state when HIGH. Set $\overline{\text{OE}}$ LOW for normal operation (has internal pull-down).
$\overline{\text{REFE}}$	I	QREF enable input. QREF stopped LOW when HIGH. When set $\overline{\text{REFE}}$ LOW, the QREF is enabled (has internal pull-down).
X1/REF	I	Crystal oscillator input or clock input.
X2	I	Crystal oscillator output. Leave unconnected for clock input.
QOUT	O	Output at N*REF frequency.
QREF	O	Output at REF frequency.
VDDQ	PWR	Power supply for the device outputs. Connect to VDD on PCB.
VDD	PWR	Power supply for the device core and inputs. Connect to VDD on PCB.
GND	PWR	Ground supply.

COMMON OUTPUT FREQUENCY EXAMPLES (MHz)

Output	48	60	64	72	75	80	90	100
Input	24	10	16	12	25	10	15	20
FB Divide Selection S[1:0]	LL	MH	LH	MH	LM	HM	MH	MM

Output	106.25	106.25	120	125	125	125	150	155.52
Input	17	25	15	20	25	62.5	25	19.44
FB Divide Selection S[1:0]	HL	ML	HM	HL	MM	LL	MH	HM

OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{DD} /V _{DDQ}	Power Supply Voltage	3	3.3	3.6	V
T _A	Operating Temperature	-40	25	+85	°C
C _{IN}	Input Capacitance, OE, F = 1MHz, V _{IN} = 0V, T _A = 25°C	—	5		pF

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Industrial: T_A = -40°C to +85°C, V_{DD}/V_{DDQ} = 3.3V ±0.3V

Symbol	Parameter	Test Conditions	Min.	Typ.	Max	Unit
V _{IL}	Input LOW Voltage		—	—	0.8	V
V _{IH}	Input HIGH Voltage		2	—	—	V
V _{IHH}	Input HIGH Voltage	3-level input only	V _{DD} - 0.6	—	—	V
V _{IMM}	Input MID Voltage	3-level input only	V _{DD} /2 - 0.3	—	V _{DD} /2 + 0.3	V
V _{ILL}	Input LOW Voltage	3-level input only	—	—	0.6	V
I ₃	3-Level Input DC Current, S[1:0]	V _{IN} = V _{DD} HIGH Level	—	—	+200	μA
		V _{IN} = V _{DD} /2 MID Level	-50	—	+50	
		V _{IN} = GND LOW Level	-200	—	—	
I _{IH}	Input HIGH Current	V _{IN} = V _{DD} \overline{OE} , \overline{REFE}	—	—	100	μA
		V _{IN} = V _{DD} , S[1:0] = HH X1/REF	—	2	4	mA
V _{OL}	Output LOW Voltage	I _{OL} = 12mA	—	—	0.4	V
V _{OH}	Output HIGH Voltage	I _{OH} = -12mA	2.4	—	—	V

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾	Min.	Typ.	Max	Unit
I _{DD_PD}	Power Down Current	V _{DD} = Max. S _[1:0] = HH $\overline{\text{OE}}$ = L; X1/REF = L All outputs unloaded	—	—	500	μA
ΔI _{DD}	Supply Current per Input	V _{DD} = Max., V _{IN} = 3V	—	—	30	μA
I _{DD}	Dynamic Supply Current	V _{DD} = 3.6V S _[1:0] = LL $\overline{\text{OE}}$ = L F _{OUT} = 160MHz All outputs unloaded	—	—	50	mA

NOTE:

- For conditions shown as Min. or Max., use the appropriate values specified under DC Electrical Characteristics.

AC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t _R , t _F	Rise Time, Fall Time	0.8V to 2V		0.7	1.5	ns
		Q _{OUT}				
				0.7	2.0	
d _T	Output/Duty Cycle	V _T = V _{DDQ} /2				%
		Q _{OUT} < 125MHz	45		55	
		Q _{OUT} > 125MHz	44		56	
		Q _{REF}	40		60	
t _J	Cycle - Cycle Jitter	F _{OUT} = 106.25MHz			100	ps
		F _{OUT} = 125MHz			90	
		F _{OUT} = 155.52MHz			125	
f _{OUT}	Output Frequency		48		160	MHz

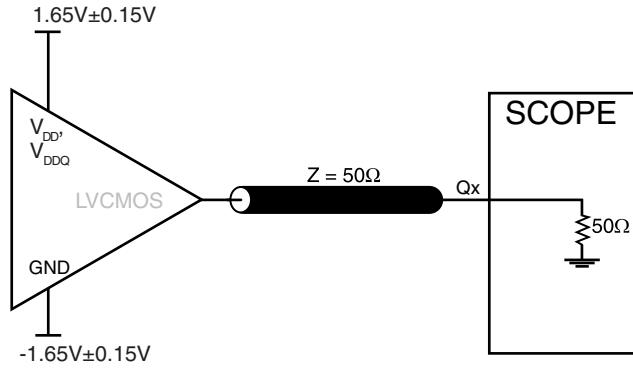
INPUT TIMING REQUIREMENTS

Symbol	Description ⁽¹⁾	Min.	Max.	Unit
t _R , t _F	Maximum input rise and fall time, 0.8V to 2V ⁽²⁾	—	10	ns/V
t _{PWC}	Input clock pulse, HIGH or LOW ⁽²⁾	2	—	ns
D _H	Input duty cycle ⁽²⁾	10	90	%
f _{OSC}	XTAL oscillator frequency	10	40	MHz
f _{IN}	Input frequency ⁽²⁾	48/N	160/N	MHz

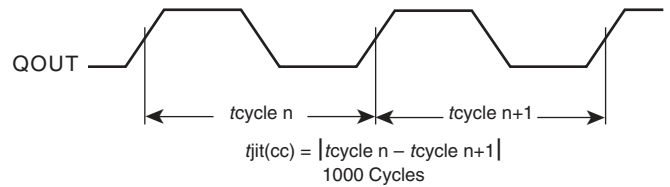
NOTES:

- Where pulse width implied by D_H is less than the t_{PWC} limit, t_{PWC} limit applies.
- When using a clock input.

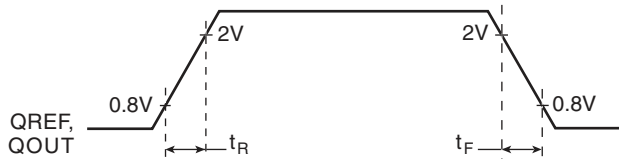
PARAMETER MEASUREMENT INFORMATION



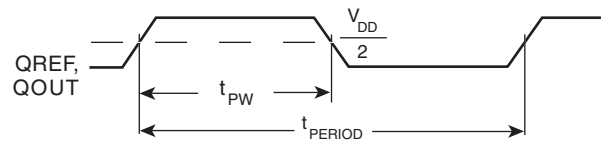
3.3V CORE/3.3V OUTPUT LOAD ACTEST CIRCUIT



CYCLE-TO-CYCLE JITTER



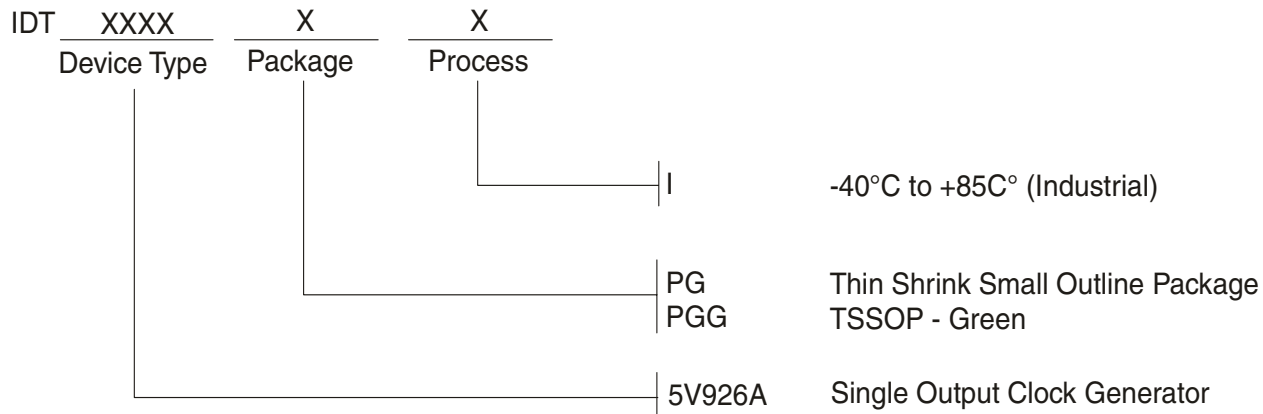
OUTPUT RISE/FALL TIME



$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

ORDERING INFORMATION



Innovate with IDT and accelerate your future networks. Contact:

www.IDT.com

For Sales

800-345-7015 (inside USA)
+408-284-8200 (outside USA)
Fax: 408-284-2775
www.IDT.com/go/contactIDT

For Tech Support

netcom@idt.com
+480-763-2056

Corporate Headquarters

Integrated Device Technology, Inc.
6024 Silver Creek Valley Road
San Jose, CA 95138
United States
800-345-7015 (inside USA)
+408-284-8200 (outside USA)