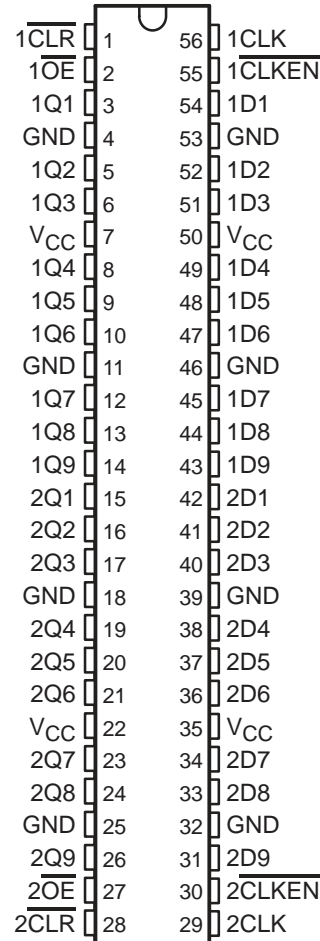


# SN54ABTH16823, SN74ABTH16823 18-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCBS664B – APRIL 1996 – REVISED MAY 1997

- Members of the Texas Instruments *Widebus™* Family
- State-of-the-Art *EPIC-II B™* BiCMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Typical  $V_{OLP}$  (Output Ground Bounce) < 1 V at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$
- High-Impedance State During Power Up and Power Down
- Distributed  $V_{CC}$  and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- High-Drive Outputs (–32-mA  $I_{OH}$ , 64-mA  $I_{OL}$ )
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

SN54ABTH16823 . . . WD PACKAGE  
SN74ABTH16823 . . . DGG OR DL PACKAGE  
(TOP VIEW)



## description

These 18-bit flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers with parity, and working registers.

The 'ABTH16823 can be used as two 9-bit flip-flops or one 18-bit flip-flop. With the clock-enable ( $\overline{\text{CLKEN}}$ ) input low, the D-type flip-flops enter data on the low-to-high transitions of the clock. Taking  $\overline{\text{CLKEN}}$  high disables the clock buffer, latching the outputs. Taking the clear ( $\overline{\text{CLR}}$ ) input low causes the Q outputs to go low independently of the clock.

A buffered output-enable ( $\overline{\text{OE}}$ ) input can be used to place the nine outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

$\overline{\text{OE}}$  does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
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# SN54ABTH16823, SN74ABTH16823 18-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

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## description (continued)

When  $V_{CC}$  is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN54ABTH16823 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74ABTH16823 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

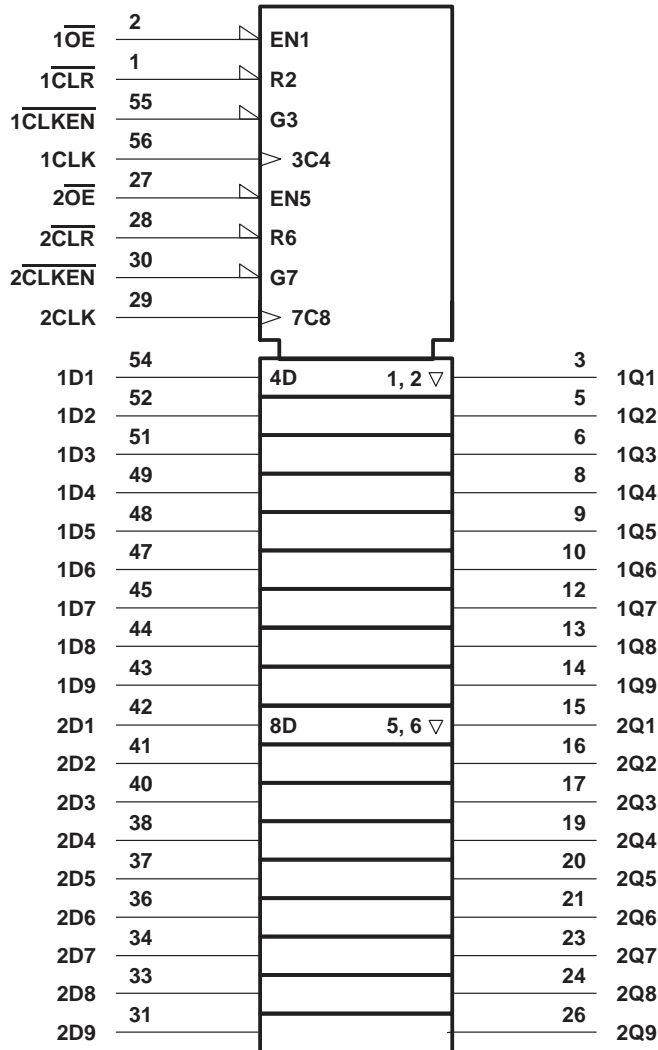
FUNCTION TABLE  
(each 9-bit flip-flop)

INPUTS					OUTPUT Q
$\overline{OE}$	$\overline{CLR}$	$\overline{CLKEN}$	CLK	D	
L	L	X	X	X	L
L	H	L	↑	H	H
L	H	L	↑	L	L
L	H	L	L	X	$Q_0$
L	H	H	X	X	$Q_0$
H	X	X	X	X	Z

SN54ABTH16823, SN74ABTH16823  
 18-BIT BUS-INTERFACE FLIP-FLOPS  
 WITH 3-STATE OUTPUTS

SCBS664B – APRIL 1996 – REVISED MAY 1997

logic symbol†

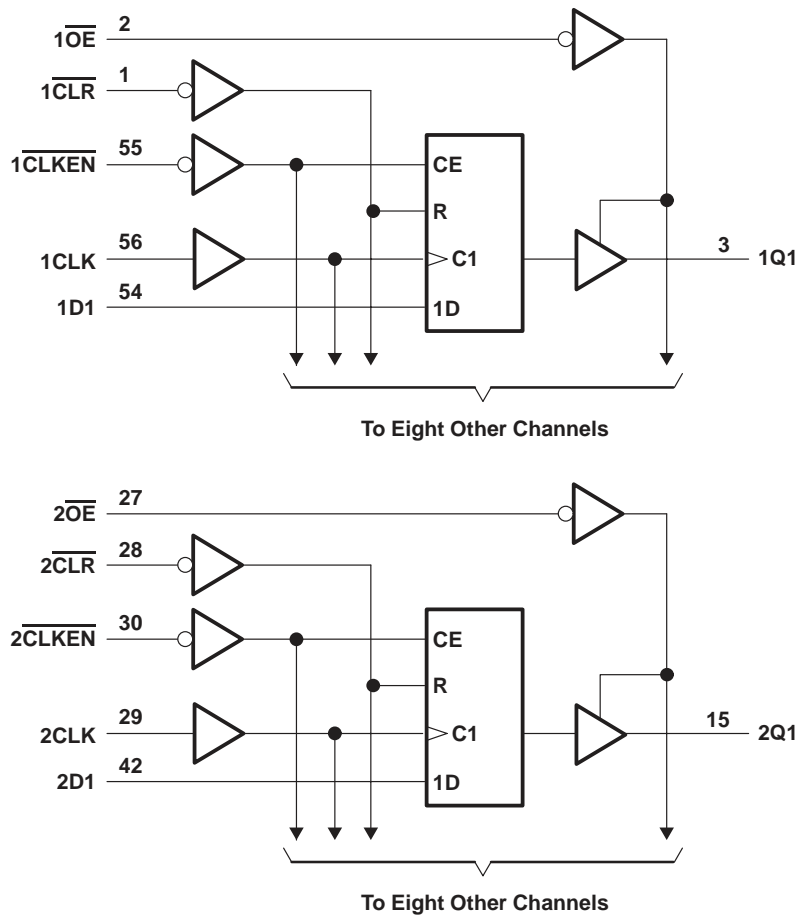


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

**SN54ABTH16823, SN74ABTH16823**  
**18-BIT BUS-INTERFACE FLIP-FLOPS**  
**WITH 3-STATE OUTPUTS**

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**logic diagram (positive logic)**



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range, $V_{CC}$ .....	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) .....	-0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, $V_O$ .....	-0.5 V to 5.5 V
Current into any output in the low state, $I_O$ : SN54ABTH16823 .....	96 mA
SN74ABTH16823 .....	128 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	-18 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ ) .....	-50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DGG package .....	81°C/W
DL package .....	74°C/W
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
 2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51.



# SN54ABTH16823, SN74ABTH16823 18-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

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## recommended operating conditions (see Note 3)

		SN54ABTH16823		SN74ABTH16823		UNIT
		MIN	MAX	MIN	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5.5	4.5	5.5	V
V <sub>IH</sub>	High-level input voltage	2		2		V
V <sub>IL</sub>	Low-level input voltage		0.8		0.8	V
V <sub>I</sub>	Input voltage	0	V <sub>CC</sub>	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current		-24		-32	mA
I <sub>OL</sub>	Low-level output current		48		64	mA
Δt/Δv	Input transition rise or fall rate	Outputs enabled		10	10	ns/V
Δt/ΔV <sub>CC</sub>	Power-up ramp rate	200		200		μs/V
T <sub>A</sub>	Operating free-air temperature	-55	125	-40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

**SN54ABTH16823, SN74ABTH16823**  
**18-BIT BUS-INTERFACE FLIP-FLOPS**  
**WITH 3-STATE OUTPUTS**

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	T <sub>A</sub> = 25°C			SN54ABTH16823		SN74ABTH16823		UNIT	
		MIN	TYP†	MAX	MIN	MAX	MIN	MAX		
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = -18 mA			-1.2		-1.2		-1.2	V	
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -3 mA		2.5		2.5		2.5		V	
	V <sub>CC</sub> = 5 V, I <sub>OH</sub> = -3 mA		3		3		3			
	V <sub>CC</sub> = 4.5 V	I <sub>OH</sub> = -24 mA	2		2					
		I <sub>OH</sub> = -32 mA	2*				2			
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V	I <sub>OL</sub> = 48 mA		0.55		0.55			V	
		I <sub>OL</sub> = 64 mA		0.55*			0.55			
V <sub>hys</sub>			100						mV	
I <sub>I</sub>	V <sub>CC</sub> = 0 to 5.5 V, V <sub>I</sub> = V <sub>CC</sub> or GND			±1		±1		±1	µA	
I <sub>I</sub> (hold)	V <sub>CC</sub> = -4.5 V	V <sub>I</sub> = 0.8 V	100		100		100		µA	
		V <sub>I</sub> = 2 V	-100		-100		-100			
I <sub>OZPU</sub> ‡	V <sub>CC</sub> = 0 to 2.1 V, V <sub>O</sub> = 0.5 V to 2.7 V, $\overline{OE} = X$			±50		±50		±50	µA	
I <sub>OZPD</sub> ‡	V <sub>CC</sub> = 2.1 V to 0, V <sub>O</sub> = 0.5 V to 2.7 V, $\overline{OE} = X$			±50		±50		±50	µA	
I <sub>OZH</sub>	V <sub>CC</sub> = 2.1 V to 5.5 V, V <sub>O</sub> = 2.7 V, $\overline{OE} \geq 2$ V			10**		50		10	µA	
I <sub>OZL</sub>	V <sub>CC</sub> = 2.1 V to 5.5 V, V <sub>O</sub> = 0.5 V, $\overline{OE} \geq 2$ V			-10**		-50		-10	µA	
I <sub>off</sub>	V <sub>CC</sub> = 0, V <sub>I</sub> or V <sub>O</sub> ≤ 4.5 V			±100				±100	µA	
I <sub>CEX</sub>	Outputs high	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 5.5 V		50		50		50	µA	
I <sub>O</sub> §		V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.5 V	-50	-100	-200	-50	-200	-50	-200	mA
I <sub>CC</sub>	Outputs high			0.5		0.5		0.5	mA	
	Outputs low	V <sub>CC</sub> = 5.5 V, I <sub>O</sub> = 0, V <sub>I</sub> = V <sub>CC</sub> or GND		80		80		80		
	Outputs disabled			0.5		0.5		0.5		
ΔI <sub>CC</sub> ¶		V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND		1.5		1.5		1.5	mA	
C <sub>i</sub>		V <sub>I</sub> = 2.5 V or 0.5 V		4					pF	
C <sub>o</sub>		V <sub>O</sub> = 2.5 V or 0.5 V		8.5					pF	

\* On products compliant to MIL-PRF-38535, this parameter does not apply.

\*\* These limits apply only to the SN74ABTH16823.

† All typical values are at V<sub>CC</sub> = 5 V.

‡ This parameter is characterized, but not production tested.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.



**SN54ABTH16823, SN74ABTH16823**  
**18-BIT BUS-INTERFACE FLIP-FLOPS**  
**WITH 3-STATE OUTPUTS**

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timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

		$V_{CC} = 5\text{ V},$ $T_A = 25^\circ\text{C}$		SN54ABTH16823		SN74ABTH16823		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$f_{\text{clock}}$	Clock frequency	0	150	0	150	0	150	MHz
$t_w$	Pulse duration	$\overline{\text{CLR}}$ low	3.3	3.3	3.3	3.3		ns
		CLK high or low	3.3	3.3	3.3			
$t_{\text{su}}$	Setup time before $\text{CLK}\uparrow$	$\overline{\text{CLR}}$ inactive	1.6	2	1.6		ns	
		Data	1.7	1.7	1.7			
		$\overline{\text{CLKEN}}$ low	2.8	2.8	2.8			
$t_h$	Hold time after $\text{CLK}\uparrow$	Data	1.2	1.2	1.2		ns	
		$\overline{\text{CLKEN}}$ low	0.6	0.6	0.6			

switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50\text{ pF}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ABTH16823					UNIT
			$V_{CC} = 5\text{ V},$ $T_A = 25^\circ\text{C}$			MIN	MAX	
			MIN	TYP	MAX			
$f_{\text{max}}$			150			150	MHz	
$t_{\text{PLH}}$	CLK	Q	1.6	3.9	5.5	1.6	7.7	ns
$t_{\text{PHL}}$			2.1	3.9	5.4	2.1	6.4	
$t_{\text{PHL}}$	$\overline{\text{CLR}}$	Q	1.9	4.1	6	1.9	6.9	ns
$t_{\text{PZH}}$	$\overline{\text{OE}}$	Q	1	3.1	4.2	1	5.1	ns
$t_{\text{PZL}}$			1.5	3.5	4.6	1.5	5.7	
$t_{\text{PHZ}}$	$\overline{\text{OE}}$	Q	2.2	4.3	6	2.2	6.8	ns
$t_{\text{PLZ}}$			1.6	4.3	6.4	1.6	9.9	

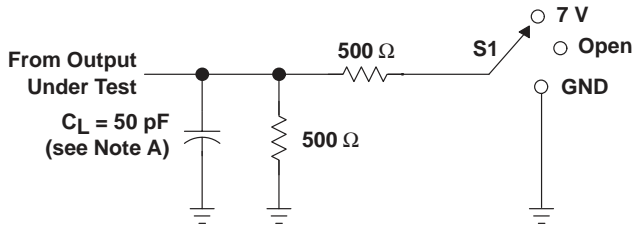
switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50\text{ pF}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74ABTH16823					UNIT
			$V_{CC} = 5\text{ V},$ $T_A = 25^\circ\text{C}$			MIN	MAX	
			MIN	TYP	MAX			
$f_{\text{max}}$			150			150	MHz	
$t_{\text{PLH}}$	CLK	Q	1.6	3.9	5.5	1.6	6.8	ns
$t_{\text{PHL}}$			2.1	3.9	5.4	2.1	6	
$t_{\text{PHL}}$	$\overline{\text{CLR}}$	Q	1.9	4.1	6	1.9	6.7	ns
$t_{\text{PZH}}$	$\overline{\text{OE}}$	Q	1	3.1	4.2	1	4.9	ns
$t_{\text{PZL}}$			1.5	3.5	4.6	1.5	5.5	
$t_{\text{PHZ}}$	$\overline{\text{OE}}$	Q	2.2	4.3	5.6	2.2	6.1	ns
$t_{\text{PLZ}}$			1.6	4.3	6.4	1.6	8.7	

**SN54ABTH16823, SN74ABTH16823**  
**18-BIT BUS-INTERFACE FLIP-FLOPS**  
**WITH 3-STATE OUTPUTS**

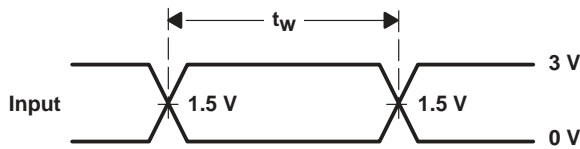
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**PARAMETER MEASUREMENT INFORMATION**

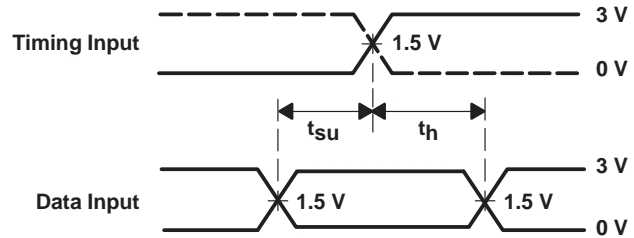


**LOAD CIRCUIT**

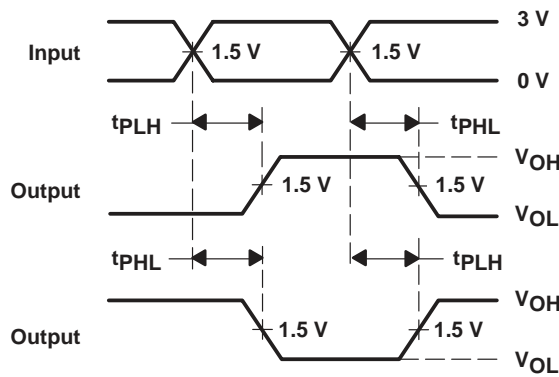
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	7 V
$t_{PHZ}/t_{PZH}$	Open



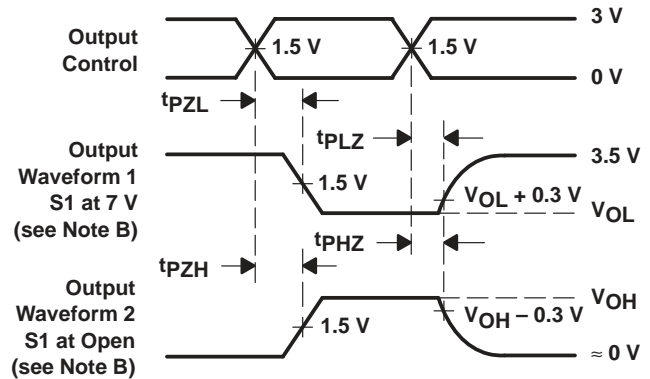
**VOLTAGE WAVEFORMS**  
**PULSE DURATION**



**VOLTAGE WAVEFORMS**  
**SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS**  
**PROPAGATION DELAY TIMES**  
**INVERTING AND NONINVERTING OUTPUTS**



**VOLTAGE WAVEFORMS**  
**ENABLE AND DISABLE TIMES**  
**LOW- AND HIGH-LEVEL ENABLING**

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .  
 D. The outputs are measured one at a time with one transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**



**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
74ABTH16823DGGRE4	ACTIVE	TSSOP	DGG	56		TBD	Call TI	Call TI	
74ABTH16823DGGRG4	ACTIVE	TSSOP	DGG	56		TBD	Call TI	Call TI	
74ABTH16823DLRG4	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ABTH16823DLR	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

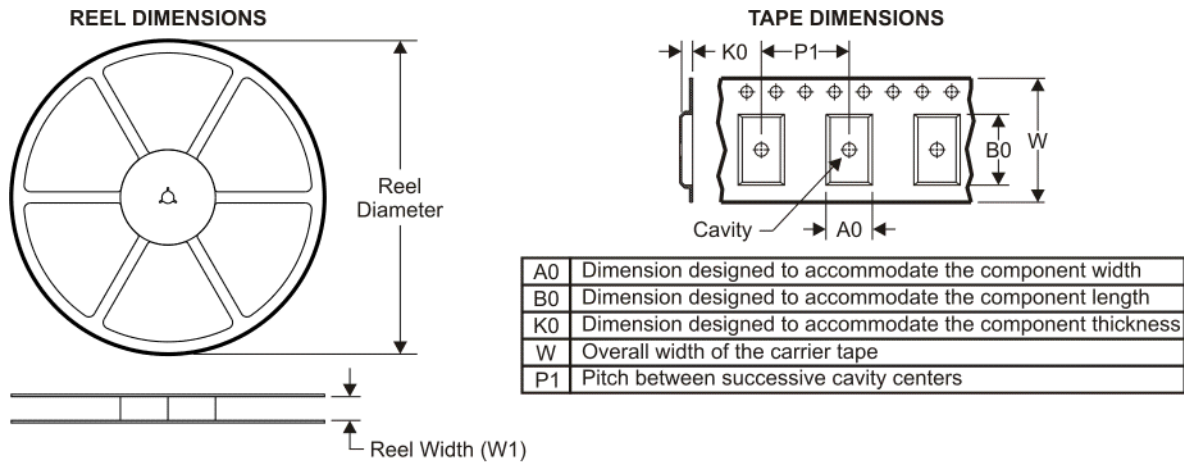
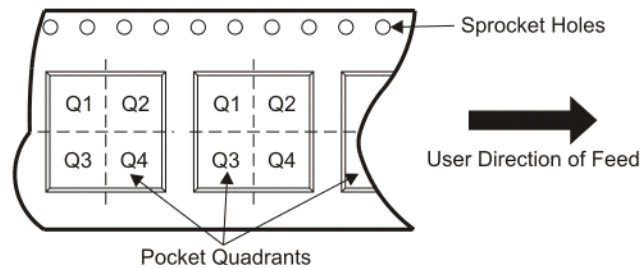
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ABTH16823DLR	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1

TAPE AND REEL BOX DIMENSIONS



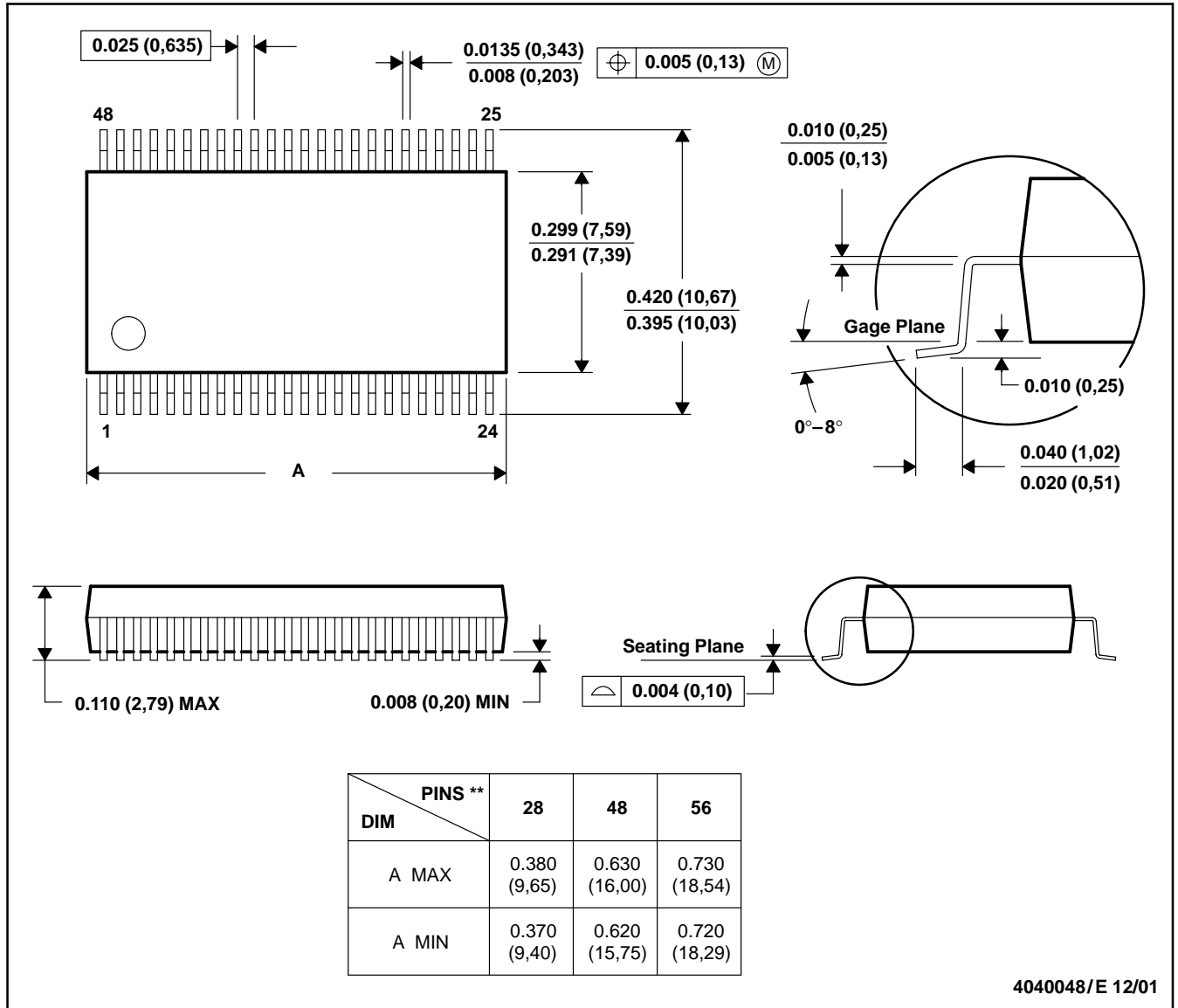
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ABTH16823DLR	SSOP	DL	56	1000	346.0	346.0	49.0

DL (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN

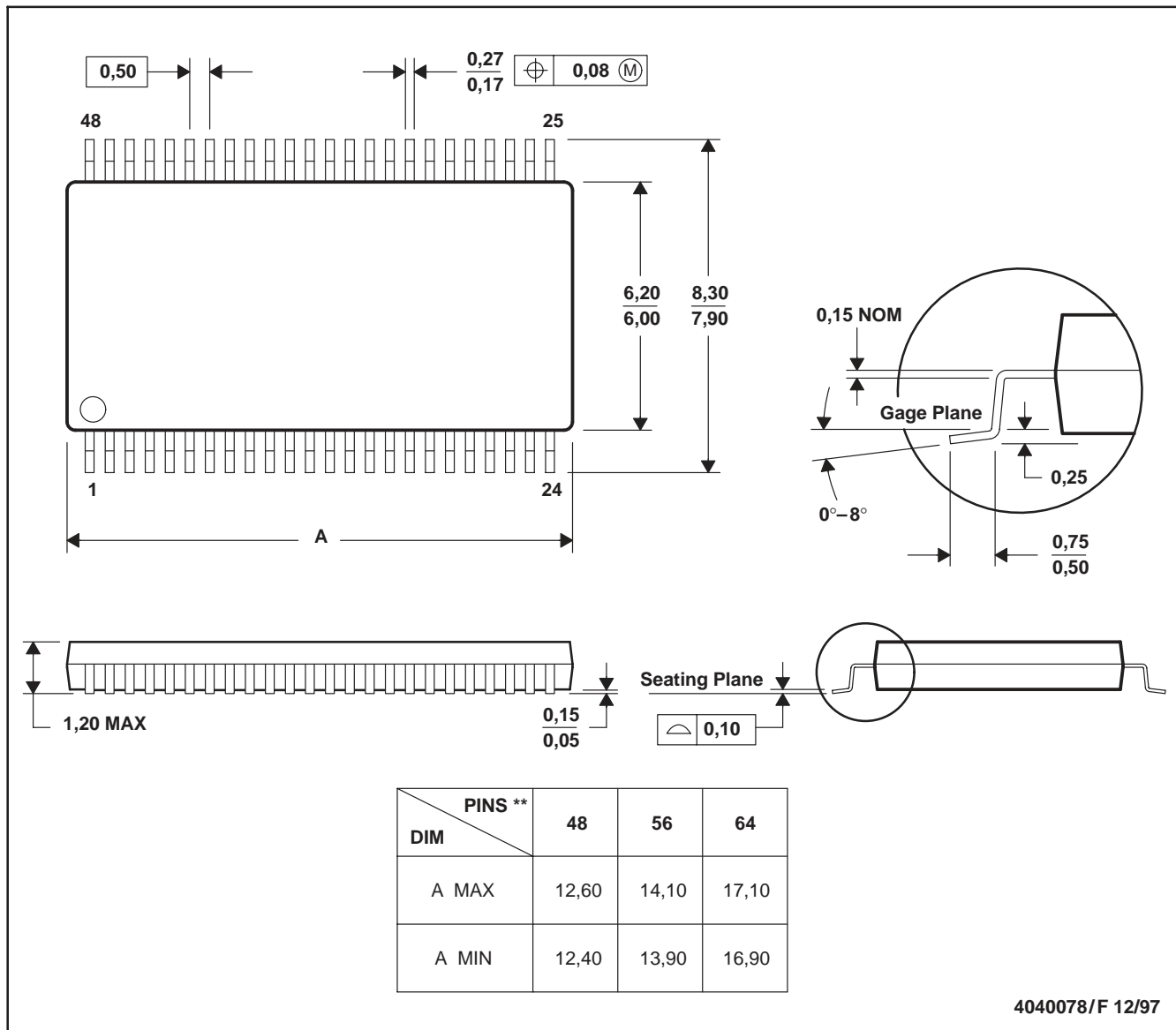


- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).  
 D. Falls within JEDEC MO-118

DGG (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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