FAN5019

6-Bit VID Controller 2-4 Phase VRM10.X Controller

Features

- Pin and Function Backward Compatible with FAN53168 and FAN53180 Controllers
- Precision Multi-Phase DC-DC Core Voltage Regulation
  - ±10mV Output Voltage Accuracy Over Temperature
- Differential Remote Voltage Sensing
- Selectable 2, 3, or 4 Phase Operation
- Selectable VRM9 or VRM10 Operation
- Up to 1MHz per Phase Operation (4MHz ripple Frequency)
- Lossless Inductor Current Sensing for Loadline Compensation
  - External Temperature Compensation
- Accurate Load-Line Programming (Meets Intel® VRM/VRD10.0 and 10.X CPU Specifications)
- Accurate Channel-Current Balancing for Thermal Optimization and Layout Compensation
- Convenient 12V Supply Biasing
- 6-bit Voltage Identification (VID) Input
  - .8375V to 1.600V in 12.5mV Steps
  - Dynamic VID Capability with Fault-Blanking for glitch-less Output voltage Changes
- Adjustable Over Current Protection with Programmable Latch-Off Delay. Latch-Off Function may be Disabled
- Over-Voltage Protection – Internal OVP Crowbar Protection

Applications

- Computer DC/DC Converter VRM/VRD10.0
- Computer DC/DC Converter VRM/VRD10.X
- Computer DC/DC Converter VRM/VRD9.X
- High Current, Low Voltage DC/DC Rail

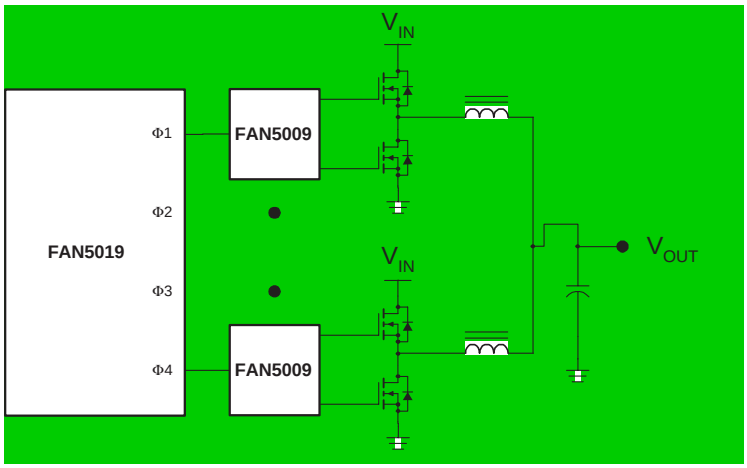
General Description

The FAN5019 is a multi-phase DC-DC controller for implementing high-current, low-voltage, CPU core power regulation circuits. It is part of a chipset that includes external MOSFET drivers and power MOSFETS. The FAN5019 drives up to four synchronous-rectified buck channels in parallel. The multi-phase buck converter architecture uses interleaved switching to multiply ripple frequency by the number of phases and reduce input and output ripple currents. Lower ripple results in fewer components, lower component cost, reduced power dissipation, and smaller board area.

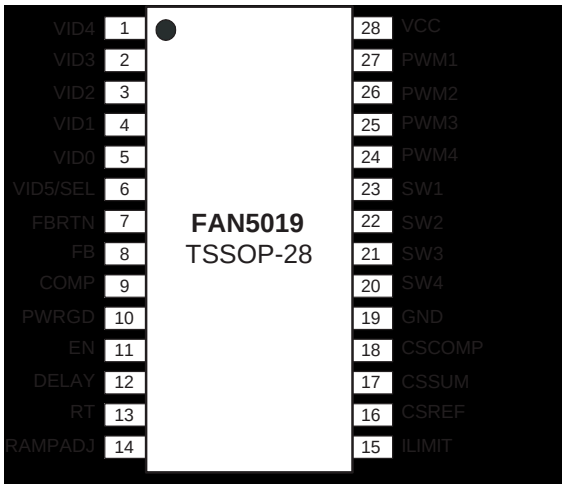
The FAN5019 features a high bandwidth control loop to provide optimal response to load transients. The FAN5019 senses current using lossless techniques: Phase current is measured through each of the output inductors. This current information is summed, averaged and used to set the loadline of the output via programmable "droop". The droop is temperature compensated to achieve precise loadline characteristics over the entire operating range. Additionally, individual phase current is measured using the $R_{DS(ON)}$ of the low-side MOSFETs. This information is used to dynamically balance/steer per-phase current. The phase currents are also summed and averaged for over-current detection.

Dynamic-VID technology allows on-the-fly VID changes with controlled, glitch-less output. Additionally, short-circuit protection, adjustable current limiting, over-voltage protection and power-good circuitry combine to ensure reliable and safe operation. The operating temperature range is 0°C to +85°C and the operating voltage is a single +12V supply, which simplifies the design. The FAN5019 is available in a TSSOP-28 package.

Block Diagram



Pin Assignments



Pin Definitions

Pin Number	Pin Name	Pin Function Description
1–5	VID [4:0]	**VID inputs.** Determines the output voltage via the internal DAC. These inputs comply to VRM10/VRD10 specifications for static and dynamic operation. All have internal pull-ups (1.25V for VRM10 and 2.5V for VRM9) so leaving them open results in logic high. Leaving VID[4:0] open results in a "No CPU" condition disabling the PWM outputs.
6	VID5/SEL	**VID5 Input/DAC Select.** Dual function pin that is either the 12.5mV DAC LSB for VRM10 or selects the VRM9 DAC codes when forced higher than Vtblsel(VRM9) voltage. The truth table is as follows: $V_{VID5/SEL}$ held > Vtblsel(VRM9); VRM9 DAC table is selected (See Table 3) $V_{ViD5/SEL}$ < Vtblsel(VRM10); VRM10 DAC table is selected (See Table 2) and $V_{ViD5/SEL}$ pin is used as VID5 input.
7	FBRTN	**Feedback Return.** Error Amp and DAC reference point.
8	FB	**Feedback Input.** Inverting input for Error Amp this pin is used for external compensation. This pin can also be used to introduce DC offset voltage to the output.
9	COMP	**Error Amp output.** This pin is used for external compensation.
10	PWRGD	**Power Good output.** This is an open-drain output that asserts when the output voltage is within the specified tolerance. It is expected to be pulled up to an external voltage rail.
11	EN	**Enable.** Logic signal that enables the controller when logic high.
12	DELAY	**Soft-start and Current Limit Delay.** An external resistor and capacitor sets the softstart ramp rate and the over-current latch off delay.
13	RT	**Switching Frequency Adjust.** This pin adjusts the output PWM switching frequency via an external resistor.
14	RAMPADJ	**PWM Current Ramp Adjust.** An external resistor to Vcc will adjust the amplitude of the internal PWM ramp.
15	ILIMIT	**Current Limit Adjust.** An external resistor sets the current limit threshold for the regulator circuit. This pin is internally pulled low when EN is low or the UVLO circuit is active. It is also used to enable the drivers.

Pin Definitions (continued)

Pin Number	Pin Name	Pin Function Description
16	CSREF	**Current Sense Reference.** Non-Inverting input of the current sense amp. Sense point for the output voltage used for OVP and PWRGD.
17	CSSUM	**Current Sense Summing node.** Inverting input of the current sense amp.
18	CSCOMP	**Current Sense Compensation node.** Output of the current sense amplifier. This pin is used, in conjunction with CSSUM to set the output droop compensation and current loop response.
19	GND	**Ground.** Signal ground for the device.
20–23	SW[4:1]	**Phase Current Sense/Balance inputs.** Phase-to-phase current sense and balancing inputs. Unused phases should be left open.
24–27	PWM[4:1]	**PWM outputs.** CMOS outputs for driving external gate drivers such as the FAN53418 or FAN5009. Unused phases should be grounded.
28	VCC	**Chip Power.** Bias supply for the chip. Connect directly to a +12V supply. Bypass with a 1µF MLCC capacitor.

Absolute Maximum Ratings

Absolute maximum ratings are the values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Parameter	Min.	Max.	Units
Supply Voltage: VCC to GND	-0.3	+15	V
Voltage on FBRTN pin	-0.3	+0.3	V
Voltage on SW1-SW4 (<250ns duration)	-5	+25	V
Voltage on SW1-SW4 (>=250ns duration)	-0.3	+15	V
Voltage on RAMPADJ, CSSUM	-0.3	VCC+0.3	V
Voltage on any other pin	-0.3	+5.5	V

Thermal Information

Parameter	Min.	Typ	Max.	Units
Operating Junction Temperature (T_J)	0		+150	°C
Storage Temperature	–65		+150	°C
Lead Soldering Temperature, 10 seconds			+300	°C
Vapor Phase, 60 seconds			+215	°C
Infrared, 15 seconds			+220	°C
Power Dissipation (P_D) @ T_A = 25°C			2	W
Thermal Resistance (Θ_{JA})*		50		°C/W

Recommended Operating Conditions (See Figure 8)

Parameter	Conditions	Min.	Typ.	Max.	Units
Supply Voltage VCC	VCC to GND	10.2	12	13.8	V
Ambient Operating Temperature		0		+85	°C
Operating Junction Temperature (T_J)		0		+125	

Note:

1: Θ_{JA} is defined as 1 oz. copper PCB with 1 in^2 pad.

Electrical Specifications

(V_{CC} = 12V, T_A = 0°C to +85°C and FBRTN=GND, using circuit in Figure 1, unless otherwise noted.)
The • denotes specifications which apply over the full operating temperature range.

Parameter	Symbol	Conditions			Min.	Typ.	Max.	Units
Error Amplifier								
Output Voltage Range	V_{COMP}			•	0.5		3.5	V
Accuracy	V_{FB}	Relative to DAC Setting, referenced to FBRTN, CSSUM = CSCOMP, Test Circuit 3	VRM10 VRM9	• •	-10 -12		+10 +12	mV
Line Regulation	ΔV_{FB}	VCC=10V to 14V				0.05		%
Input Bias Current	I_{FB}			•	-13	-15	-17	µA
FBRTN Current	I_{FBRTN}			•		150	180	µA
Output Current	$I_{O(ERR)}$	FB forced to V_{OUT} – 3%			300	500		µA
Gain Bandwidth Product	GBW	COMP = FB				20		MHz
DC Gain		C_{COMP} = 10pF				77		dB
VID Inputs								
Input Low Voltage	$V_{IL(VID)}$	VRM10 VRM9		• •			0.4 0.8	V V
Input High Voltage	$V_{IH(VID)}$	VRM10 VRM9		• •	0.8 2.0			V V
Input Current, VID Low	$I_{IL(VID)}$	VID(X) = 0V		•	-30	-20		µA
Input Current, VID High	$I_{IH(VID)}$	VID(X) = 1.25V		•	-2		2	µA
Pull-up Resistance	R_{VID}	Internal		•	35	60	115	kΩ
Internal Pull-up Voltage		VRM10 VRM9		• •	1.0 2.2	1.15 2.4	1.26 2.6	V V
VID Transition Delay Time[2]		VID Code Change to FB Change		•	400			ns
"No CPU" Detection Turn-off Delay Time[2]		VID Code Change to 11111X to PWM going low		•	400			ns
VID Table Select	Vtblsel	To select VRM9 table To select VRM10 table (becomes VID5)		• •	4		 3.5	V V
Oscillator								
Frequency	f_{OSC}			•	200		4000	kHz
Frequency Variation	f_{PHASE}	T_A = +25°C, R_T = 250kΩ, 4-Phase T_A = +25°C, R_T = 115kΩ, 4-Phase T_A = +25°C, R_T = 75kΩ, 4-Phase		•	155	200 400 600	245	kHz kHz kHz
Output Voltage	V_{RT}	R_T = 100kΩ to GND		•	1.9	2.0	2.1	V
RAMPADJ Pin Accuracy	$V_{RAMPADJ}$	$V_{RAMPADJ}$ = Vdac = +2K • (Vin–Vdac)/(Rr+2k)		•	-50		+50	mV
RAMPADJ Input Current	$I_{RAMPADJ}$	Current into RAMPADJ pin			0		100	µA
Current Sense Amplifier								
Offset Voltage	$V_{OS(CSA)}$	CSSUM–CSREF, Test Circuit 1		•	-1.5		+1.5	mV
Input Bias Current	$I_{BIAS(CSA)}$			•	-50		+50	nA
Gain Bandwidth Product	GBW	COMP = FB				10		MHz

Notes:
1. All limits at operating temperature extremes are guaranteed by design, characterization and statistical quality control
2. Guaranteed by design – NOT tested in production.

Electrical Specifications (continued)

(V_{CC} = 12V, T_A = 0°C to +85°C and FBRTN=GND, using circuit in Figure 1, unless otherwise noted.)
The • denotes specifications which apply over the full operating temperature range.

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Units
DC Gain					77		dB
Input Common Mode Range		CSSUM and CSREF	•	0		3	V
Positioning Accuracy	ΔV_{FB}	COMP = FB, Test Circuit 2	•	-84	-80	-76	mV
Output Voltage Range		I_{CSCOMP} = ±100µA	•	0.1		3.3	V
Output Current	$I_{O(CSA)}$	FB forced to V_{OUT} – 3% Source/Sink		300	375		µA
Current Balance Circuit							
Input Operating Range	$V_{SW(X)CM}$		•	-600		+200	mV
Input Resistance	$R_{SW(X)}$	SW(X) = 0V	•	20	30	40	kΩ
Input Current	$I_{SW(X)}$	SW(X) = 0V	•	4	7	10	µA
Input Current Matching	$\Delta I_{SW(X)}$	SW(X) = 0V	•	-5		+5	%
Current Limit Comparator							
ILIMIT Output Voltage Normal Mode In Shutdown	 $V_{ILIMIT(NM)}$ $V_{ILIMIT(SD)}$	 R_{ILIMIT} = 250kΩ I_{ILIMIT} = -100µA	 • •	 2.9	 3	 3.1 400	 V mV
Output Current, Normal Mode	$I_{ILIMIT(NM)}$	R_{ILIMIT} = 250kΩ			12		µA
Maximum Output Current		$V_{IILIMIT}$ = 3V	•	60			µA
Current Limit Threshold Voltage	V_{CL}	V_{CSREF}–V_{CSCOMP}, R_{ILIMIT} = 250kΩ	•	105	125	150	mV
Current Limit Setting Ratio		V_{CL}/I_{ILIMIT}			10.4		mV/µA
Latch-off Delay Threshold	V_{DELAY}	In Current Limit	•	1.7	1.8	1.9	V
Latch-off Delay Time	t_{DELAY}	R_{DELAY} = 250kΩ, C_{DELAY} = 4.7nF			600		µs
Soft Start							
Output Current, Soft start Mode	$I_{DELAY(SS)}$	During Start-up, DELAY < 2.8V	•	15	20	25	µA
Soft Start Delay Time	$T_{DELAY(SS)}$	R_{DELAY} = 250kΩ, C_{DELAY} = 4.7nF, VID = 011111 (1.475V)			400		µs
Enable Input							
Input Low Voltage	$V_{IL(EN)}$		•			0.4	V
Input High Voltage	$V_{IH(EN)}$		•	0.8			V
Input Current, EN Low	$I_{IL(EN)}$	EN = 0V	•	-1		1	µA
Input Current, EN High	$I_{IH(EN)}$	EN = 1.25V	•		10	25	µA
Power Good Comparator							
Under voltage Threshold	$V_{PWRGD(UV)}$	Relative to DAC Output	•	-325	-250	-200	mV
Over voltage Threshold	$V_{PWRGD(OV)}$	Relative to DAC Output	•	90	150	200	mV
Output Low Voltage	$V_{OL(PWRGD)}$	$I_{PWRGD(SINK)}$ = 4mA	•		225	400	mV

Notes:

1. All limits at operating temperature extremes are guaranteed by design, characterization and statistical quality control
2. Guaranteed by design – NOT tested in production.

Electrical Specifications (continued)

(V_{CC} = 12V, T_A = 0°C to +85°C and FBRTN=GND, using circuit in Figure 1, unless otherwise noted.)
The • denotes specifications which apply over the full operating temperature range.

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Units
Power Good Delay Time Initial Start Up VID Code Changing VID Code Static			•	 1 100	 250 200	 10 	 ms µs ns
Crowbar Trip Point	$V_{CROWBAR}$	Relative to Nominal DAC Output	•	90	150	200	mV
Crowbar Reset Point		Relative to FBRTN	•	450	550	650	mV
Crowbar Delay Time VID Code Changing VID Code Static	$t_{CROWBAR}$	Over voltage to PWM Going Low	•	100	 250 400	 500 600	 µs ns
PWM Outputs							
Output Voltage Low	$V_{OL(PWM)}$	$I_{PWM(SINK)}$ = 400µA	•		160	500	mV
Output Voltage High	$V_{OH(PWM)}$	$I_{PWM(SOURCE)}$ = 400µA	•	4	5	5.5	V
Input Supply							
DC Supply Current		EN = Logic High	•		5	10	mA
UVLO Threshold	V_{UVLO}	Vcc Rising (Vcc = 12V input)	•	6.5	6.9	7.8	V
UVLO Hysteresis			•	0.7			V
UVLO Threshold		Falling	•	5.6		7.0	

Notes:

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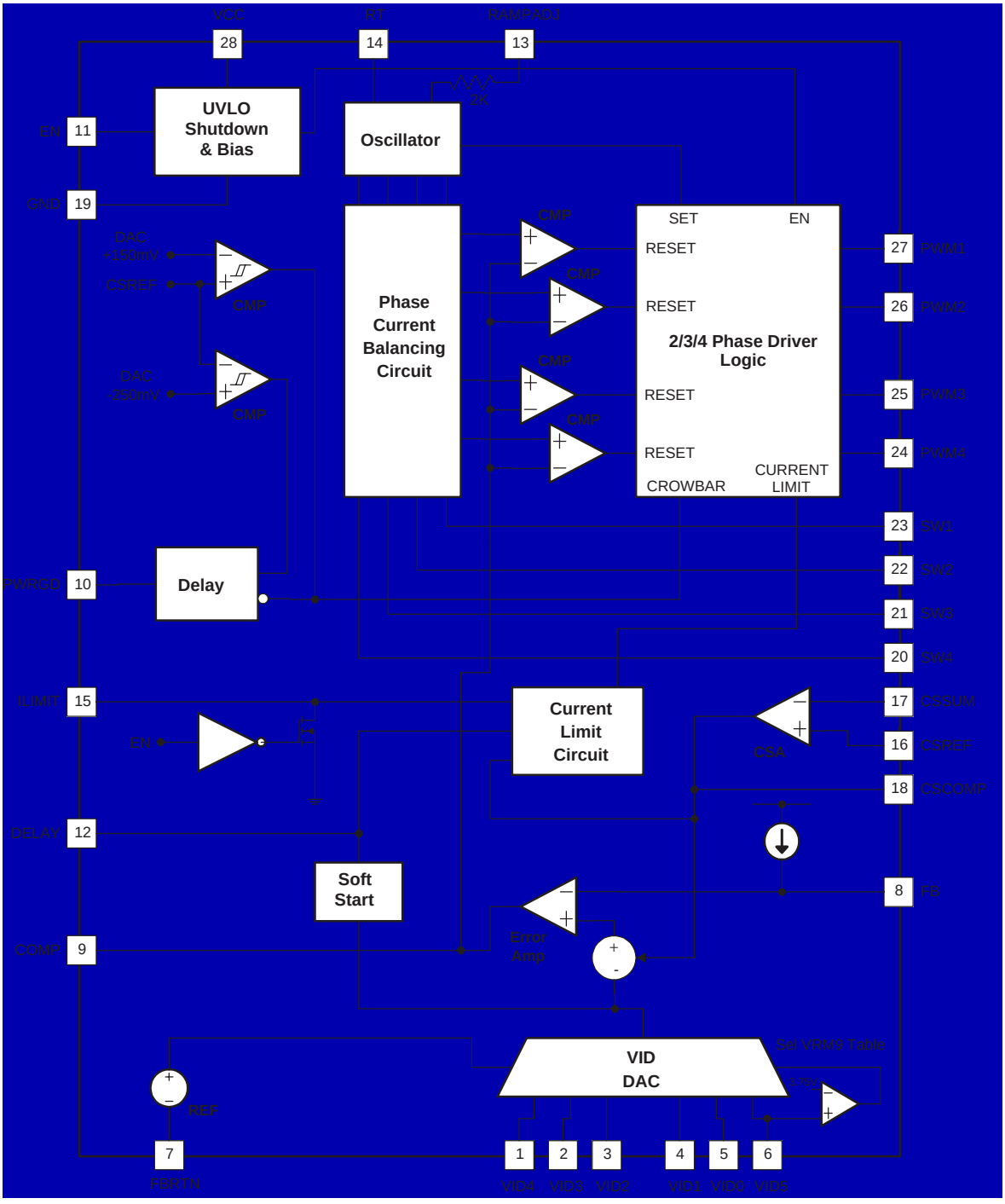
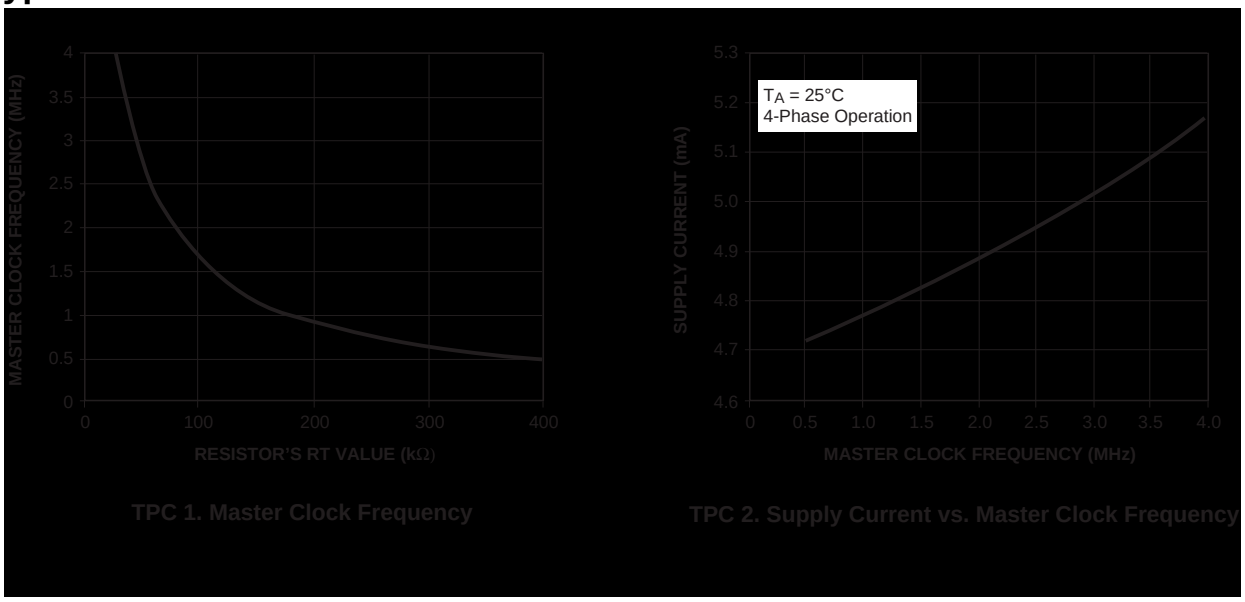
2. Guaranteed by design – NOT tested in production.

Internal Block Diagram



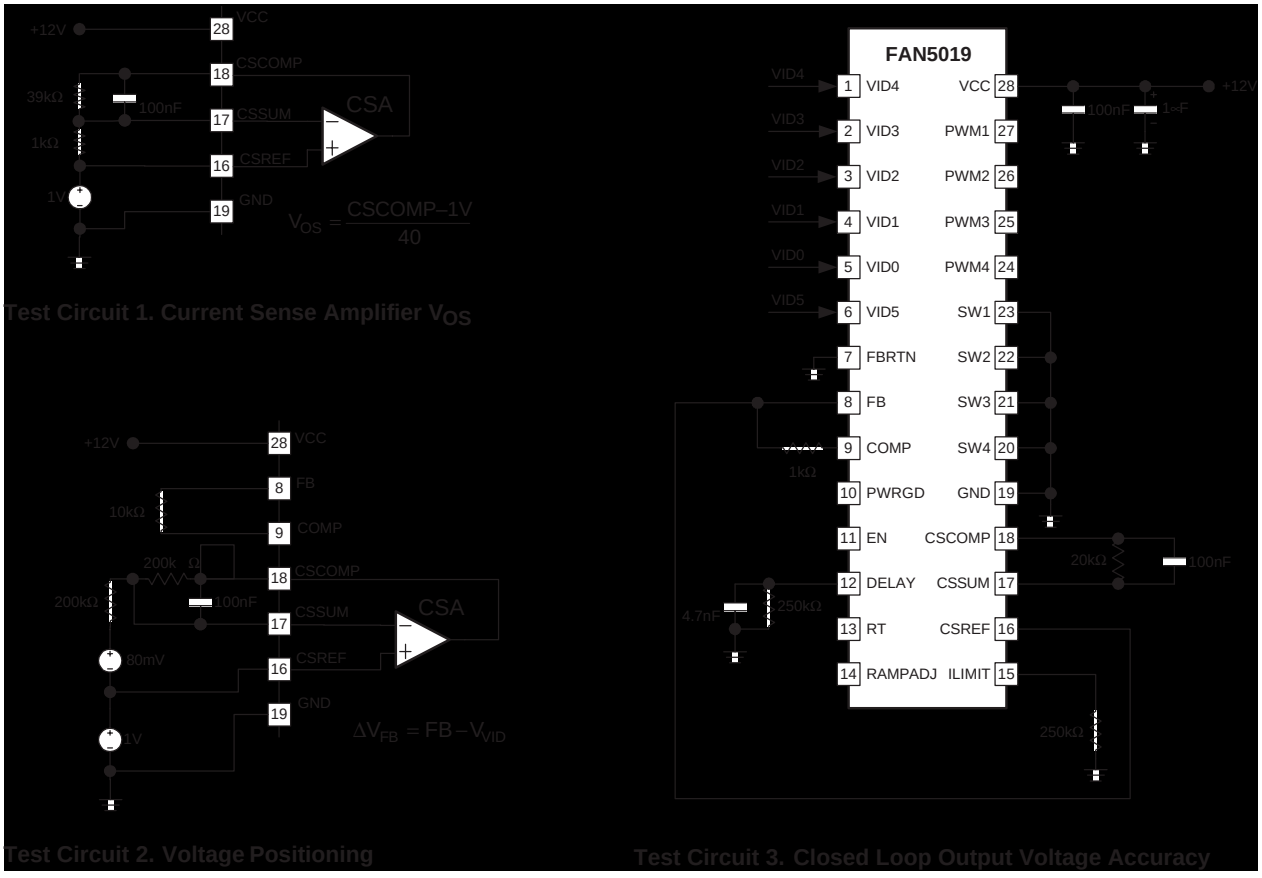
Typical Characteristics



TPC 1. Master Clock Frequency

TPC 2. Supply Current vs. Master Clock Frequency

Test Circuits



Test Circuit 1. Current Sense Amplifier V_{OS}

Test Circuit 2. Voltage Positioning

Test Circuit 3. Closed Loop Output Voltage Accuracy

Application Circuit

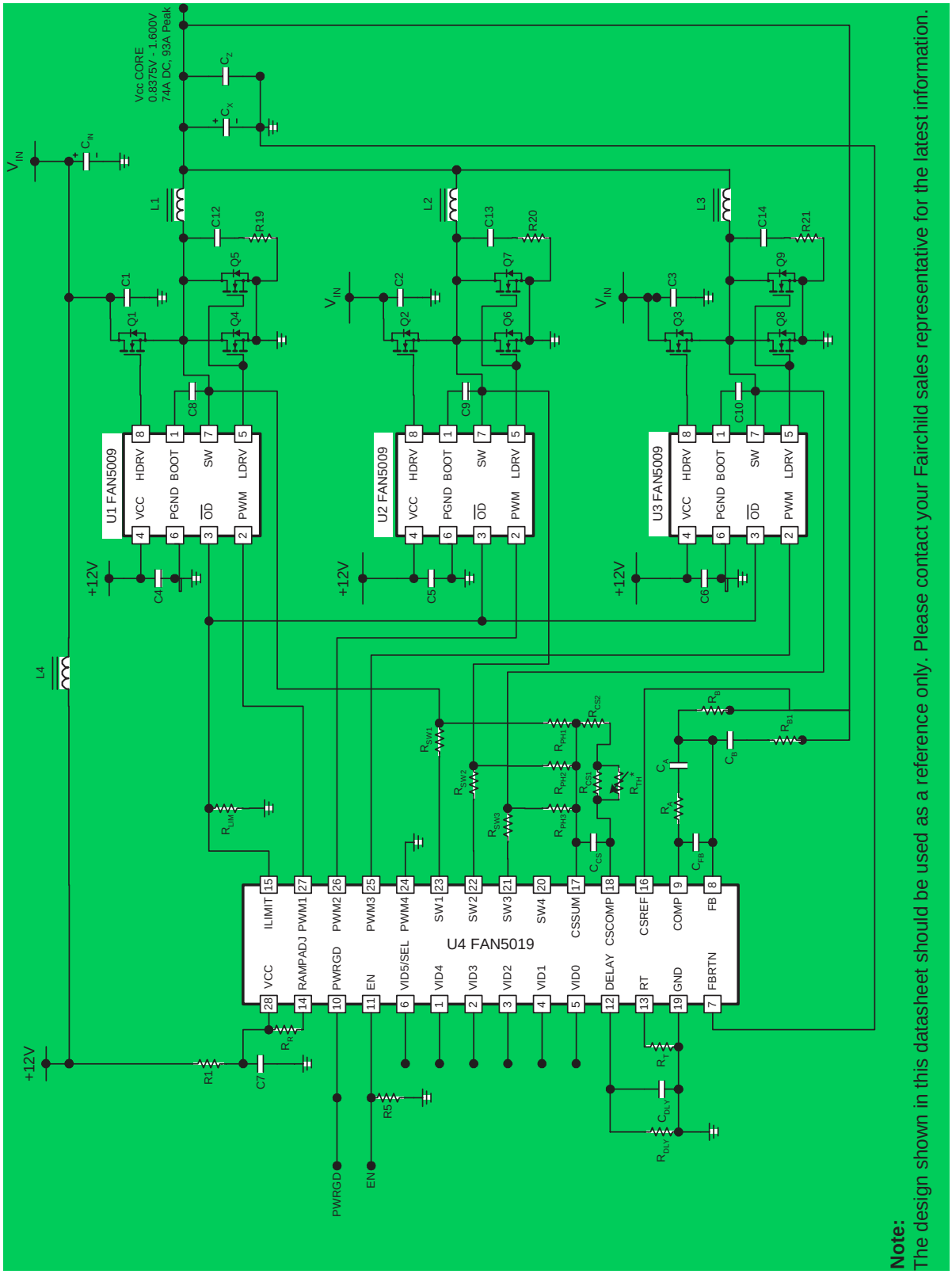


Figure 1. Typical Application – 3-phase, 65A (DC), 74A (Peak) VRD/VRM10 Design

Bill of Materials

Table 1. FAN5019 VRM/VRD10 Application Bill of Materials for Figure 1

Ref	Qty	Description	Manufacturer/Number
U4	1	VRM10, Multi-Phase Controller	Fairchild FAN5019
U1–3	3	Sync MOSFET Driver, 12V/12V	Fairchild FAN5009
Q1–3	3	N-MOSFET, 30V, 50A, 8mΩ	Fairchild FDD6696
Q4–9	6	N-MOSFET, 30V, 75A, 5mΩ	Fairchild FDD6682
L1–3	3	Inductor, 650nH, 26A, 1.6mΩ	Micrometals T50-8B/90, 5T, 16AWG
L4	1	Inductor, 630nH, 15A, 1.7mΩ	Inter-Technical AK1418160052A-R63M
R1	1	10Ω, 5%	
R_R R_{DLY}, R_T	3	301kΩ, 1%	
R5	1	15.0kΩ, 1%	
$R_{PH1–3}$	3	100kΩ, 1%	
R_A, R_{CS2}	2	24.9kΩ, 1%	
R_{B1}	1	10Ω, 1%	
R_B	1	1.33kΩ, 1%	
$R_{SW1–3}$	3	0Ω, 5%	
R_{CS1}	1	37.4kΩ, 1%	
R_{LIM}	1	200kΩ, 1%	
R19–21	3	1.5Ω, 5%	
R_{TH}	1	NTC Thermistor, 100kΩ, 5%	Panasonic ERT-J1V V104J
C1–7	7	1.0µF, 25V, 10% X7R	
C8–10	3	0.1µF, 50V, 10% X7R	
C12–14, C_{CS}	4	4700pF, 25V, 10% X7R	
C_{DLY}	1	0.047µF, 25V, 10% X7R	
C_B	1	2200pF, 25V, 10% X7R	
C_A	1	470pF, 50V, 10% X7R	
C_{FB}	1	100pF, 50V, 5% NPO	
C_X	8	820µF, 2.5V, 20% 7mΩ, POLY	Fujitsu FP-2R5RE821M
C_Z	22	10µF, 6.3V, 20% X5R	
C_{IN}	6	470µF, 16V, 20%, 36mΩ, Alum-Elec	Rubycon 16MBZ470M

Note:
The design shown in this datasheet should be used as a reference only. Please contact your Fairchild sales representative for the latest information.

Table 2. VRM10 VID Codes

VID4	VID3	VID2	VID1	VID0	VID5	V_{OUT} (nominal)
1	1	1	1	1	X	No CPU
0	1	0	1	0	0	0.8375 V
0	1	0	0	1	1	0.8500 V
0	1	0	0	1	0	0.8625 V
0	1	0	0	0	1	0.8750 V
0	1	0	0	0	0	0.8875 V
0	0	1	1	1	1	0.9000 V
0	0	1	1	1	0	0.9125 V
0	0	1	1	0	1	0.9250 V
0	0	1	1	0	0	0.9375 V
0	0	1	0	1	1	0.9500 V
0	0	1	0	1	0	0.9625 V
0	0	1	0	0	1	0.9750 V
0	0	1	0	0	0	0.9875 V
0	0	0	1	1	1	1.0000 V
0	0	0	1	1	0	1.0125 V
0	0	0	1	0	1	1.0250 V
0	0	0	1	0	0	1.0375 V
0	0	0	0	1	1	1.0500 V
0	0	0	0	1	0	1.0625 V
0	0	0	0	0	1	1.0750 V
0	0	0	0	0	0	1.0875 V
1	1	1	1	0	1	1.1000 V
1	1	1	1	0	0	1.1125 V
1	1	1	0	1	1	1.1250 V
1	1	1	0	1	0	1.1375 V
1	1	1	0	0	1	1.1500 V
1	1	1	0	0	0	1.1625 V
1	1	0	1	1	1	1.1750 V
1	1	0	1	1	0	1.1875 V
1	1	0	1	0	1	1.2000 V
1	1	0	1	0	0	1.2125 V
1	1	0	0	1	1	1.2250 V
1	1	0	0	1	0	1.2375 V
1	1	0	0	0	1	1.2500 V
1	1	0	0	0	0	1.2625 V
1	0	1	1	1	1	1.2750 V
1	0	1	1	1	0	1.2875 V
1	0	1	1	0	1	1.3000 V
1	0	1	1	0	0	1.3125 V
1	0	1	0	1	1	1.3250 V

Table 2. VRM10 VID Codes (continued)

VID4	VID3	VID2	VID1	VID0	VID5	V_{OUT} (nominal)
1	0	1	0	1	0	1.3375 V
1	0	1	0	0	1	1.3500 V
1	0	1	0	0	0	1.3625 V
1	0	0	1	1	1	1.3750 V
1	0	0	1	1	0	1.3875 V
1	0	0	1	0	1	1.4000 V
1	0	0	1	0	0	1.4125 V
1	0	0	0	1	1	1.4250 V
1	0	0	0	1	0	1.4375 V
1	0	0	0	0	1	1.4500 V
1	0	0	0	0	0	1.4625 V
0	1	1	1	1	1	1.4750 V
0	1	1	1	1	0	1.4875 V
0	1	1	1	0	1	1.5000 V
0	1	1	1	0	0	1.5125 V
0	1	1	0	1	1	1.5250 V
0	1	1	0	1	0	1.5375 V
0	1	1	0	0	1	1.5500 V
0	1	1	0	0	0	1.5625 V
0	1	0	1	1	1	1.5750 V
0	1	0	1	1	0	1.5875 V
0	1	0	1	0	1	1.6000 V

Table 3. VRM9 VID Codes

VID4	VID3	VID2	VID1	VID0	V_{OUT} (nominal)
1	1	1	1	1	No CPU
1	1	1	1	0	1.100 V
1	1	1	0	1	1.125 V
1	1	1	0	0	1.150 V
1	1	0	1	1	1.175 V
1	1	0	1	0	1.200 V
1	1	0	0	1	1.225 V
1	1	0	0	0	1.250 V
1	0	1	1	1	1.275 V
1	0	1	1	0	1.300 V
1	0	1	0	1	1.325 V
1	0	1	0	0	1.350 V
1	0	0	1	1	1.375 V
1	0	0	1	0	1.400 V
1	0	0	0	1	1.425 V
1	0	0	0	0	1.450 V
0	1	1	1	1	1.475 V
0	1	1	1	0	1.500 V
0	1	1	0	1	1.525 V
0	1	1	0	0	1.550 V
0	1	0	1	1	1.575 V
0	1	0	1	0	1.600 V
0	1	0	0	1	1.625V
0	1	0	0	0	1.650V
0	0	1	1	1	1.675V
0	0	1	1	0	1.700V
0	0	1	0	1	1.725V
0	0	1	0	0	1.750V
0	0	0	1	1	1.775V
0	0	0	1	0	1.800V
0	0	0	0	1	1.825V
0	0	0	0	0	1.850V

General Description

Note: The information in this section is intended to assist the user in their design and understanding of the FAN5019 functionality. For clarity and ease of understanding, device parameters have been included in the text. In the event of discrepancies between values stated in this section and the actual specification tables, the specification tables shall be deemed correct.

Theory of Operation

The FAN5019 combines a multi-mode, fixed frequency PWM control with multi-phase logic outputs for use in 2, 3 and 4 phase synchronous buck CPU core supply power converters. If VID5 is pulled up to a voltage greater than VTBLSEL, then the DAC code corresponds to VRM9.

Multi-phase operation is important for producing the high currents and low voltages demanded by today's microprocessors. Handling the high currents in a single-phase converter would place high thermal demands on the components in the system such as the inductors and MOSFETs. The internal 6-bit VID DAC conforms to Intel's VRD/VRM 10 specifications.

The multi-mode control of the FAN5019 ensures a stable, high performance topology for:

- Balancing currents and thermals between phases
- High speed response at the lowest possible switching frequency and output decoupling
- Minimizing thermal switching losses due to lower frequency operation
- Tight load line regulation and accuracy
- High current output from having up to 4 phase operation
- Reduced output ripple due to multi-phase cancellation
- PC board layout noise immunity
- Ease of use and design due to independent component selection
- Flexibility in operation for tailoring design to low cost or high performance

Number of Phases

The number of operational phases and their phase relationship is determined by internal circuitry which monitors the PWM outputs. Normally, the FAN5019 operates as a 4-phase PWM controller. Grounding the PWM4 pin programs three phase operation; grounding the PWM3 and PWM4 pins programs 2-phase operation.

When the FAN5019 is initially enabled, the controller outputs a voltage on PWM3 and PWM4 that is approximately 550 mV. An internal comparator checks each pin's voltage versus a threshold of 400mV. If the pin is grounded, then it will be below the threshold and the phase will be disabled. The output impedance of the PWM pin is approximately 5kΩ. Any external pull-down resistance connected to the PWM pin should not be less than 25kΩ to ensure proper operation. The phase detection is made prior to starting normal operation. After this time, if the PWM output was not grounded, then it will operate normally. If the PWM output was grounded, then it will remain off.

The PWM outputs become logic-level output devices once normal operation starts, and are intended for driving external gate drivers. Since each phase is monitored independently, operation approaching 100% duty cycle is possible. Also, more than one output can be on at a time for overlapping phases.

Master Clock Frequency

The clock frequency of the FAN5019 is set with an external resistor connected from the RT pin to ground. The frequency follows the graph shown in TPC 1. To determine the frequency per phase, the clock is divided by the number of phases in use. If PWM4 is grounded, then divide the master clock by 3 and if both PWM3 and 4 are grounded, then divide by 2. If all phases are in use, divide by 4.

Output Voltage Differential Sensing

The FAN5019 combines differential sensing with a high accuracy VID DAC and reference and a low offset error amplifier to maintain a worst-case specification of ±10 mV differential sensing error with a VID input of 1.600 V over its full operating output voltage and temperature range. The output voltage is sensed between the FB and FBRTN pins. FB should be connected through a resistor to the regulation point, usually the remote sense pin of the microprocessor. FBRTN should be connected directly to the remote sense ground point. The internal VID DAC and precision reference are referenced to FBRTN, which has a typical current of 150µA, to allow accurate remote sensing. The internal error amplifier compares the output of the DAC to the FB pin to regulate the output voltage.

Output Current Sensing

The FAN5019 provides a dedicated current sense amplifier (CSA) to monitor the total output current for proper voltage positioning versus load current and for current limit detection. Sensing the load current at the output gives the total average current being delivered to the load, which is an inherently more accurate method than peak current detection or sampling the current across a sense element such as the low side MOSFET. This amplifier can be configured several ways depending on the objectives of the system:

- Output inductor DCR sensing without thermistor for lowest cost
- Output inductor DCR sensing with thermistor for improved accuracy with tracking of inductor temperature
- Sense resistors for highest accuracy measurements

The positive input of the CSA is connected to the CSREF pin, which is connected to the output voltage. The inputs to the amplifier are summed together through resistors from the sensing element (such as the switch node side of the output

inductors) to the inverting input, CSSUM. The feedback resistor between CSCOMP and CSSUM sets the gain of the amplifier, and a filter capacitor is placed in parallel with this resistor. The gain of the amplifier is programmable by adjusting the feedback resistor to set the load line required by the microprocessor. The current information is then given as the difference of CSREF –CSCOMP. This difference signal is used internally to offset the VID DAC for voltage positioning and as a differential input for the current limit comparator.

To provide the best accuracy for the sensing of current, the CSA has been designed to have a low offset input voltage. Also, the sensing gain is determined by external resistors so that it can be made extremely accurate and flexible.

Active Impedance Control Mode

For controlling the output voltage droop as a function of output current, a voltage signal proportional to the total inductor currents is created by the current sense amplifier (CSA). The ratio of this voltage to the output current is determined by external components to allow it to be adjusted to set the required load line. Inside the chip the CSA output voltage is subtracted from the DAC voltage which then is used for the reference to the error amplifier. As the output current increases the reference to the error amp decreases causing the output voltage to decrease accordingly.

Current Control Mode and Thermal Balance

The FAN5019 has individual inputs for each phase which are used for monitoring the current in each phase. This information is combined with an internal ramp to create a current balancing feedback system that has been optimized for initial current balance accuracy and dynamic thermal balancing during operation. This current balance information is independent of the average output current information used for positioning described previously.

The magnitude of the internal ramp can be set to optimize the transient response of the system. It also monitors the supply voltage for feed-forward control for changes in the supply. A resistor connected from the power input voltage to the RAMPADJ pin determines the slope of the internal PWM ramp. Detailed information about programming the ramp is given in the applications section.

External resistors can be placed in series with individual phases to create an intentional current imbalance if desired, such as when one phase may have better cooling and can support higher currents. Resistors R_{SW1} through R_{SW4} (see the typical application circuit in Figure 4) can be used for adjusting FET thermal and current balance. Zero ohm placeholder resistors should be provided in the initial layout to allow the phase balance to be adjusted during design fine tuning.

To increase the current in any given phase, make R_{SW} for that phase larger (make R_{SW} = 0 for the hottest phase and do not change during balancing). Increasing R_{SW} to only 500Ω will make a substantial increase in phase current. Increase each R_{SW} value by small amounts to achieve balance, starting with the coolest phase first.

Voltage Control Mode

A high gain-bandwidth voltage mode error amplifier is used for the voltage-mode control loop. The control input voltage to the positive input is set via the VID 6-bit logic code according to the voltages listed in Table 1. This voltage is also offset by the droop voltage for active positioning of the output voltage as a function of current, commonly known as active voltage positioning. The output of the amplifier is the COMP pin, which sets the termination voltage for the internal PWM ramps.

The negative input (F_B) is tied to the output sense location with a resistor R_B and is used for sensing and controlling the output voltage at this point. A current source from the F_B pin flowing through R_B is used for setting the no-load offset voltage from the VID voltage. The no-load voltage will be negative with respect to the VID DAC. The main loop compensation is incorporated in the feedback network between FB and COMP.

Soft-Start

The power-on ramp up time of the output voltage is set with a capacitor and resistor in parallel from the DELAY pin to ground. The RC time constant also determines the current limit latch off time as explained in the following section. In UVLO or when EN is a logic low, the DELAY pin is held at ground. After the UVLO threshold is reached and EN is a logic high, the DELAY cap is charged up with an internal 20µA current source. The output voltage follows the ramping voltage on the DELAY pin, limiting the inrush current. The soft-start time depends on the value of VID DAC and C_{DLY}, with a secondary effect from R_{DLY}. Refer to the applications section for detailed information on setting C_{DLY}.

If EN is taken low or VCC drops below UVLO, the DELAY cap is reset to ground to be ready for another soft start cycle. Figure 1 shows a typical start-up sequence for the FAN5019.

Over Current Limit and Latch-off Protection

The FAN5019 compares a programmable current limit set point to the voltage from the output of the current sense amplifier. The level of current limit is set with the resistor from the ILIMIT pin to ground. During normal operation, the voltage on ILIMIT is 3V. The current through the external resistor is internally scaled to give a current limit threshold of approximately 10.4mV/µA. If the difference in voltage between CSREF and CSCOMP rises above the current limit threshold, the internal current limit amplifier will control the internal COMP voltage to maintain the average output current at the limit.

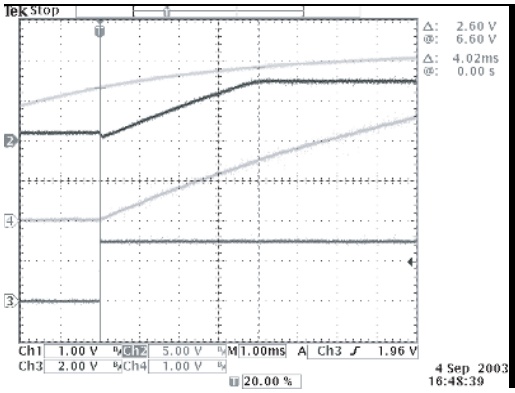


Figure 2. Start-Up Waveforms

Circuit of Figure 5
Channel 1 – Vout, Channel 2 – Vcc
Channel 3 – OD, Channel 4 – Delay pin

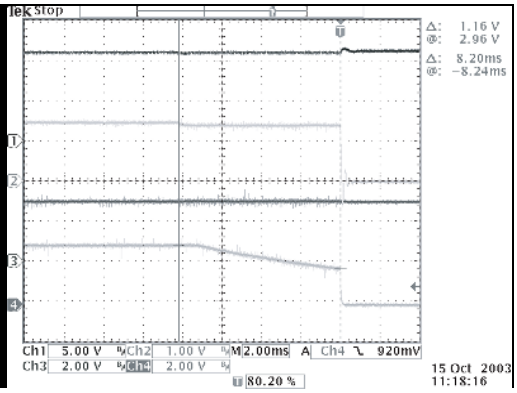


Figure 3. Overcurent Latch Off Waveform

Circuit of Figure 5
Channel 1 – Vcc, Channel 2 – Vout
Channel 3 – OD, Channel 4 – Delay pin

After the limit is reached, the 3V pull-up on the DELAY pin is disconnected, and the external delay capacitor is discharged through the external resistor. A comparator monitors the DELAY voltage and shuts off the controller when the voltage drops below 1.8V. The current limit latch off delay time is therefore set by the RC time constant discharging from 3V to 1.8V. The application section discusses the selection of C_{DLY} and R_{DLY}.

Because the controller continues to cycle the phases during the latch-off delay time, if the short is removed before the 1.8V threshold is reached, the controller will return to normal operation. The recovery characteristic depends on the state of PWRGD. If the output voltage is within the PWRGD window, the controller resumes normal operation. However, if short circuit has caused the output voltage to drop below the PWRGD threshold, then a soft-start cycle is initiated.

The latch-off function can be reset by either cycling VCC to the FAN5019, or by cycling the Enable pin low for a short time. To disable the short circuit latch off function, the external resistor to ground should be left open, and a 1MΩ resistor should be connected from VCC to the DELAY pin. This prevents the DELAY capacitor from discharging, so the 1.8V threshold is never reached. The resistor will have an impact on the soft-start time because the current through it will add to the internal 20µA current source.

During start-up when the output voltage is below 200mV, a secondary current limit is active. This is necessary because the voltage swing of CSCOMP cannot go below ground. This secondary current limit controls the internal COMP voltage to the PWM comparators to 2V. This will limit the voltage drop across the low side MOSFETs through the current balance circuitry.

There is also an inherent per phase current limit that will protect individual phases in the case where one or more phases may stop functioning because of a faulty component. This limit is based on the maximum normal-mode COMP voltage.

Dynamic VID

The FAN5019 incorporates the ability to dynamically change the VID input while the controller is running. This allows the output voltage to change while the supply is running and supplying current to the load. This is commonly referred to as VID-on-the-fly (OTF). A VID-OTF can occur under either light load or heavy load conditions. The processor signals the controller by changing the VID inputs in multiple steps from the start code to the finish code. This change can be either positive or negative.

When a VID input changes state, the FAN5019 detects the change and ignores the DAC inputs for a minimum of 400ns. This time is to prevent a false code due to logic skew while the six VID inputs are changing. Additionally, the first VID change initiates the PWRGD and CROWBAR blanking functions for a minimum of 250µs to prevent a false PWRGD or CROWBAR event. Each VID change will reset the internal timer. Figure 4 shows the VID on-the-fly performance when the output voltage is stepping up and the output current is switching between minimum and maximum values which is the worst-case situation.

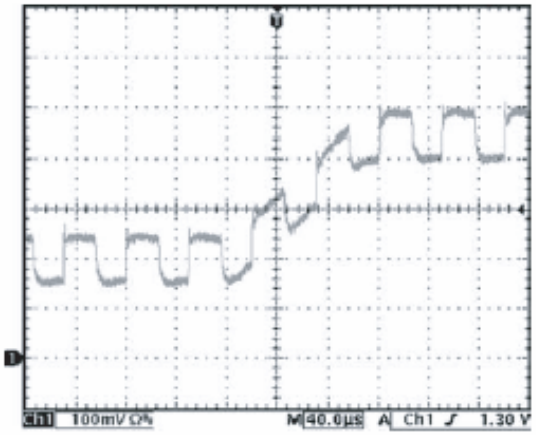


Figure 4. VID On-the-Fly Waveforms, Circuit of Figure 5, VID Change = 5mV, 5µs, 50 steps, I_{OUT} Change = 5A to 65A

Power Good Monitoring

The Power Good comparator monitors the output voltage via the CSREF pin. The PWRGD pin is an open drain output whose high level (when connected to a pull-up resistor) indicates that the output voltage is within the nominal limits specified in the specifications table based on the VID voltage setting. PWRGD will go low if the output voltage is outside of this specified range. PWRGD is blanked during a VID OTF event for a period of 250µs to prevent false signals during the time the output is changing.

Output Crowbar

As part of the protection for the load and output components of the supply, the PWM outputs will be driven low (turning on the low-side MOSFETs) when the output voltage exceeds the upper Power Good threshold. This crowbar action will stop once the output voltage has fallen below the release threshold of approximately 550mV.

Turning on the low-side MOSFETs pulls down the output voltage as the reverse current builds up in the inductors. If the output overvoltage is due to a short of the high side MOSFET, this action will current limit the input supply or blow its fuse, protecting the microprocessor from destruction.

Output Enable and UVLO

The input supply (VCC) to the controller must be higher than the UVLO threshold and the EN pin must be higher then its logic threshold for the FAN5019 to begin switching. If UVLO is less than the threshold or the EN pin is a logic low, the FAN5019 is disabled. This holds the PWM outputs at ground, shorts the DELAY capacitor to ground, and holds the ILIMIT pin at ground.

In the application circuit, the ILIMIT pin should be connected to the output disable pins of the FAN5009 drivers. Because ILIMIT is grounded, this disables the drivers such that both DRVH and DRVL are grounded. This feature is important to prevent discharging of the output capacitors when the controller is shut off. If the driver outputs were not disabled, then a negative voltage could be generated on the output due to the high current discharge of the output capacitors through the inductors.

Application Information

The design parameters for a typical Intel VRD10.x compliant CPU application are as follows:

- Input voltage (V_{IN}) = 12V
- VID setting voltage (V_{VID}) = 1.500V
- Duty cycle (D) = 0.125
- Nominal output voltage at no load (V_{ONL}) = 1.480V
- Nominal output voltage at 65 A load (V_{OFL}) = 1.3955V
- Static output voltage drop based on a 1.3 mΩ load line (R_O) from no load to full load
- (V_D) = $V_{ONL} – V_{OFL}$ = 1.480V – 1.3955V = 84.5mV
- Maximum Output Current (I_O) = 65A
- Maximum Output Current Step (ΔI_O) = 60A
- Number of Phases (n) = 3
- Switching frequency per phase (f_{SW}) = 228 kHz

Setting the Clock Frequency

The FAN5019 uses a fixed-frequency control architecture with the frequency being set by an external timing resistor (R_T). The clock frequency and the number of phases determine the switching frequency per phase, which relates directly to switching losses and the sizes of the inductors and input and output capacitors. With n = 3 for three phases, a clock frequency of 684kHz sets the switching frequency of each phase, f_{SW}, to 228kHz, which represents a practical trade-off between the switching losses and the sizes of the output filter components. TPC 1 shows that to achieve a 684kHz oscillator frequency, the correct value for R_T is 301kΩ. Alternatively, the value for R_T can be calculated using:

$$R_T = \frac{1}{(n \cdot f_{sw} \cdot 5pF) - 110nS} \quad (1)$$

where 5.0pF and 110nS are internal IC component values. For good initial accuracy and frequency stability, it is recommended to use a 1% resistor.

Soft-Start and Current Limit Latch-Off Delay Times

Because the soft-start and current limit latch off delay functions share the DELAY pin, these two parameters must be considered together. The first step is to set C_{DLY} for the soft-start ramp. This ramp is generated with a 20µA internal current source. The value of R_{DLY} will have a second order impact on the soft-start time because it sinks part of the current source to ground. However, as long as R_{DLY} is kept greater than 200kΩ, this effect is minor. The value for C_{DLY} can be approximated using:

$$C_{DLY} = \left\{20 \mu A - \frac{V_{VID}}{2 \cdot R_{DLY}}\right\} \cdot \frac{t_{SS}}{V_{VID}} \quad (2)$$

Where t_{SS} is the desired soft-start time. Assuming an R_{DLY} of 301kΩ and a desired a soft-start time of 3ms, C_{DLY} is 35nF. A close standard value for C_{DLY} is 47nF. Once C_{DLY} has been chosen, R_{DLY} can be calculated for the current limit latch-off time using:

$$R_{DLY} = \frac{1.96 \cdot t_{DELAY}}{C_{DLY}} \quad (3)$$

If the result for R_{DLY} is less than 200kΩ, then a smaller soft-start time should be considered by recalculating the equation for C_{DLY} or a longer latch-off time should be used. In no case should R_{DLY} be less than 200kΩ. In this example, a delay time of 8ms gives R_{DLY} = 334kΩ. A close standard 1% value is 301kΩ.

Inductor Selection

The choice of inductance value for the inductor determines the ripple current in the inductor. Less inductance leads to more ripple current, which increases the output ripple voltage and conduction losses in the MOSFETs, but allows using smaller-size inductors and, for a specified peak-to-peak transient deviation, less total output capacitance. Conversely, a higher inductance means lower ripple current and reduced conduction losses, but requires larger-size inductors and more output capacitance for the same peak-to-peak transient deviation. In any multi-phase converter, a practical value for the peak-to-peak inductor ripple current is less than 50% of the maximum DC current in the same inductor. Equation 4 shows the relationship between the inductance, oscillator frequency, and peak-to-peak ripple current in the inductor. Equation 5 can be used to determine the minimum inductance based on a given output ripple voltage:

$$I_R = \frac{V_O \cdot (1 - D)}{f_{SW} \cdot L} \quad (4)$$

$$L \geq \frac{V_{VID} \cdot R_O \cdot (1 - (n \cdot D))}{f_{SW} \cdot V_{RIPPLE}} \quad (5)$$

Solving Equation 5 for a 10 mV_{p-p} output ripple voltage yields:

$$L \geq \frac{1.5V \cdot 1.3m\Omega \cdot (1 - 0.375)}{228kHz \cdot 10mV} = 534nH$$

If the ripple voltage ends up less than that designed for, the inductor can be made smaller until the ripple value is met. This will allow optimal transient response and minimum output decoupling.

The smallest possible inductor should be used to minimize the number of output capacitors. Choosing a 650nH inductor is a good choice for a starting point and gives a calculated ripple current of 8.86A. The inductor should not saturate at the peak current of 26.1A and should be able to handle the sum of the power dissipation caused by the average current of 21.7A in the winding and core loss.

Another important factor in the inductor design is the DC Resistance (DCR), which is used for measuring the phase currents. A large DCR will cause excessive power losses, while too small a value will lead to increased measurement error. A good rule of thumb is to have the DCR be about 1 to 1 1/2 times the droop resistance (R_O). For our example, we are using an inductor with a DCR of 1.6 mΩ.

Designing an Inductor

Once the inductance and DCR are known, the next step is either to design an inductor or find a standard inductor that comes as close as possible to meeting the overall design goals. It is also important to have the inductance and DCR tolerance specified to keep the accuracy of the system controlled. Using 15% for the inductance and 8% for the DCR (at room temperature) are reasonable tolerances that most manufacturers can meet.

The first decision in designing the inductor is to choose the core material. There are several possibilities for providing low core loss at high frequencies. Two examples are the powder cores (e.g., Kool-Mm® from Magnetics, Inc. or Micrometals) and the gapped soft ferrite cores (e.g., 3F3 or 3F4 from Philips). Low frequency powdered iron cores should be avoided due to their high core loss, especially when the inductor value is relatively low and the ripple current is high.

The best choice for a core geometry is a closed-loop types, such as pot cores, PQ, U, and E cores, or toroids. A good compromise between price and performance are cores with a toroidal shape.

There are many useful references for quickly designing a power inductor, such as:

Magnetics Design References

1. Magnetic Designer Software Intusoft (www.intusoft.com)

2. *Designing Magnetic Components for High-Frequency DC-DC Converters*, by William T. McLyman, Kg Magnetics, Inc. ISBN 1883107008

Selecting a Standard Inductor

The companies listed below can provide design consultation and deliver power inductors optimized for high power applications upon request.

Power Inductor Manufacturers

- Coilcraft
  (847)639-6400
  www.coilcraft.com

- Coiltronics
  (561)752-5000
  www.coiltronics.com

- Sumida Electric Company
  (510) 668-0660
  www.sumida.com

- Vishay Intertechnology
  (402) 563-6866
  www.vishay.com

Output Droop Resistance

The design requires that the regulator output voltage measured at the CPU pins drops when the output current increases. The specified voltage drop corresponds to a DC output resistance (R_O).

The output current is measured by summing together the voltage across each inductor and then passing the signal through a low-pass filter. This summer-filter is the CS amplifier configured with resistors $R_{PH(X)}$ (summers), and R_{CS} and C_{CS} (filter). The output resistance of the regulator is set by the following equations, where R_L is the DCR of the output inductors:

$$R_O = \frac{R_{CS}}{R_{PH(X)}} \cdot R_L \quad (6)$$

$$C_{CS} = \frac{L}{R_L \cdot R_{CS}} \quad (7)$$

One has the flexibility of choosing either R_{CS} or $R_{PH(X)}$. It is best to select R_{CS} equal to 100kΩ, and then solve for $R_{PH(X)}$ by rearranging Equation 6.

$$R_{PH(X)} = \frac{R_L}{R_O} \cdot R_{CS}$$

$$R_{PH(X)} = \frac{1.6m\Omega}{1.3m\Omega} \cdot 100k\Omega = 123k\Omega$$

Next, use Equation 7 to solve for C_{CS}:

$$C_{CS} = \frac{650nH}{1.6m\Omega \cdot 100k\Omega} = 4.06nF$$

It is best to have a dual location for C_{CS} in the layout so standard values can be used in parallel to get as close to the value desired. For this example, choosing C_{CS} to be 4.7nF is a good choice. For best accuracy, C_{CS} should be a 5% or 10% NPO capacitor. A close standard 1% value for $R_{PH(X)}$ is 100kΩ.

Inductor DCR Temperature Correction

With the inductor's DCR being used as the sense element, and copper wire being the source of the DCR, one needs to compensate for temperature changes of the inductor's winding. Fortunately, copper has a well-known temperature coefficient (TC) of 0.39%/°C.

If R_{CS} is designed to have an opposite and equal percentage change in resistance to that of the wire, it will cancel the temperature variation of the inductor's DCR. Due to the non-linear nature of NTC thermistors, resistors R_{CS1} and R_{CS2} are needed (see Figure 5) to linearize the NTC and produce the desired temperature tracking.

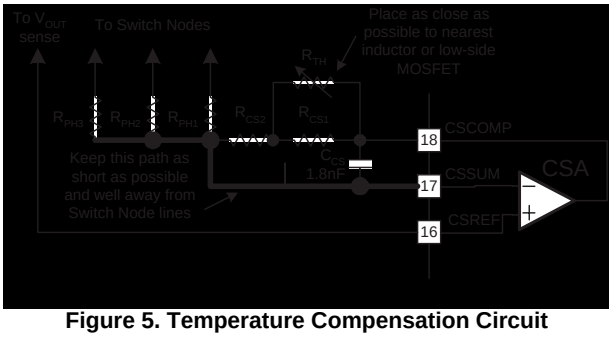


Figure 5. Temperature Compensation Circuit

The following procedure and expressions will yield values to use for R_{CS1}, R_{CS2}, and R_{TH} (the thermistor value at 25°C) for a given R_{CS} value.

1. Select an NTC to be used based on type and value. Since we do not have a value yet, start with a thermistor with a value close to R_{CS}. The NTC should also have an initial tolerance of better than 5%.

2. Based on the type of NTC, find its relative resistance value at two temperatures. The temperatures to use that work well are 50°C and 90°C. We will call these resistance values A (A is $R_{TH(50°C)}/R_{TH(25°C)}$) and B (B is $R_{TH(90°C)}/R_{TH(25°C)}$). Note that the NTC's relative value is always 1 at 25°C.

3. Next, find the relative value of R_{CS} required for each of these temperatures. This is based on the percentage change needed, which we will initially make 0.39%/°C. We will call these r_1 and r_2 where:

$$r_1 = \frac{1}{(1 + TC \cdot (T_1 - 25))}$$

$$r_2 = \frac{1}{(1 + TC \cdot (T_2 - 25))}$$

$TC = 0.0039$
$T_1 = 50°C$
$T_2 = 90°C$

4. Compute the relative values for R_{CS1}, R_{CS2}, and R_{TH} using:

$$r_{CS2} = \frac{(A \cdot B) \cdot r_1 - r_2 \cdot A - (1 - B) \cdot r_1 - B \cdot (1 - A) \cdot r_1}{\cdot A - (1 - B) \cdot r_1 - B \cdot (1 - A) \cdot r_2 - (A - B)}$$

$$r_{CS1} = \frac{(1 - A)}{\frac{1}{1 - r_{CS2}} - \frac{A}{r_1 - r_{CS2}}} \quad (8)$$

$$r_{TH} = \frac{1}{\frac{1}{1 - r_{CS2}} - \frac{1}{r_{CS1}}}$$

5. Calculate $R_{TH} = r_{TH} \times R_{CS}$, then select the closest value of thermistor available. Also compute a scaling factor k based on the ratio of the actual thermistor value used relative to the computed one:

$$k = \frac{R_{TH(ACTUAL)}}{R_{TH(CALCULATED)}} \quad (9)$$

6. Finally, calculate values for R_{CS1} and R_{CS2} using the following:

$$R_{CS1} = R_{CS} \cdot k \cdot r_{CS1} \quad (10)$$

$$R_{CS2} = R_{CS} \cdot ((1 - k) + (k \cdot r_{CS2}))$$

For this example, R_{CS} has been chosen to be 100kΩ, so we start with a thermistor value of 100kΩ. Looking through available 0603 size thermistors, we find a Panasonic ERT-J1VV104J NTC thermistor with A = 0.2954 and B = 0.05684. From these we compute R_{CS1} = 0.3304, R_{CS2} = 0.7426 and R_{TH} = 1.165. Solving for R_{TH} yields 116.5 kΩ, so we choose 100kΩ, making k = 0.8585. Finally, we find R_{CS1} and R_{CS2} to be 28.4kΩ and 77.9kΩ. Choosing the closest 1% resistor values yields a choice of 35.7kΩ and 73.2kΩ.

Output Offset

Intel's specification requires that at no load the nominal output voltage of the regulator be offset to a lower value than the nominal voltage corresponding to the VID code. The offset is set by a constant current source flowing out of the FB pin (IFB) and flowing through RB. The value of RB can be found using Equation 11:

$$R_B = \frac{V_{VID} - V_{ONL}}{I_{FB}} \quad (11)$$

$$R_B = \frac{1.5V - 1.480V}{15\mu A} = 1.33k\Omega$$

The closest standard 1% resistor value is 1.33 kΩ.

C_{OUT} Selection

The required output decoupling for the regulator is typically recommended by Intel for various processors and platforms. One can also use some simple design guidelines to determine what is required. These guidelines are based on having both bulk and ceramic capacitors in the system.

The first thing is to select the total amount of ceramic capacitance. This is based on the number and type of capacitor to be used. The best location for ceramics is inside the socket, with 12 to 18 of size 1206 being the physical limit. Others can be placed along the outer edge of the socket as well.

Combined ceramic values of 200µF–300µF are recommended, usually made up of multiple 10µF or 22µF capacitors. Select the number of ceramics and find the total ceramic capacitance (C_Z).

Next, there is an upper limit imposed on the total amount of bulk capacitance (C_X) when one considers the VID on-the-fly voltage stepping of the output (voltage step V_V in time t_V with error V_{ERR}) and a lower limit based on meeting the critical capacitance for load release for a given maximum load step ΔI_O:

$$C_{X(MIN)} \geq \left(\frac{L \cdot \Delta I_O}{n \cdot R_O \cdot V_{VID}} - C_Z \right) \quad (12)$$

$$C_{X(MAX)} \leq \frac{L}{nK^2 R_O^2} \cdot \frac{V_V}{V_{VID}} \cdot \left(\sqrt{1 + \left(t_V \frac{V_{VID}}{V_V} \cdot \frac{nKR_O}{L} \right)^2} - 1 \right) - C_Z \quad (13)$$

where

$$K = -\ln\left(\frac{V_{VERR}}{V_V} \right)$$

To meet the conditions of these expressions and transient response, the ESR of the bulk capacitor bank (R_X) should be less than two times the droop resistance, R_O. If the $C_{X(MIN)}$ is larger than $C_{X(MAX)}$, the system will not meet the VID on-the-fly specification and may require the use of a smaller inductor or more phases (and may have to increase the switching frequency to keep the output ripple the same).

For our example, 22 10µF 1206 MLC capacitors (C_Z = 220µF) were used. The VID on-the-fly step change is 250mV in 150µs with a setting error of 2.5mV. Solving for the bulk capacitance yields:

$$C_{X(MAX)} \le \frac{650nH \cdot 250mV}{3 \cdot 4.6^2 \cdot (1.3m\Omega)^2 \cdot 1.5V} \cdot \left(\sqrt{1+\left(\frac{150\mu s \cdot 1.5V \cdot 3 \cdot 4.6 \cdot 1.3m\Omega}{250mV \cdot 650nH} \right)^2} - 1 \right) - 220\mu F = 23.9mF$$

$$C_{X(MIN)} \ge \left(\frac{650nH \cdot 60A}{3 \cdot 1.3m\Omega \cdot 1.5V} - 220\mu F \right) = 6.45mF$$

where K=4.6

Using eight 820µF A1-Polys with a typical ESR of 8mΩ, each yields CX = 6.56µF with an RX = 1.0mΩ. One last check should be made to ensure that the ESL of the bulk capacitors (LX) is low enough to limit the initial high-frequency transient spike. This can be tested using:

$$L_X \le C_Z \cdot R_o^2 \qquad (14)$$

$$L_X \le 220\mu F \cdot (1.3m\Omega)^2 = 372\,pH$$

In this example, L_X is 375pH for the eight A1-Poly capacitors, which satisfies this limitation. If the L_X of the chosen bulk capacitor bank is too large, the number of MLC capacitors must be increased. One should note for this multi-mode control technique, ***"all-ceramic" designs can be used as long as the conditions of Equations 11, 12 and 13 are satisfied.***

Power MOSFETs

For this example, the N-channel power MOSFETs have been selected for one high-side switch and two low-side switches per phase. The main selection parameters for the power MOSFETs are $V_{GS(TH)}$, Q_G, C_{ISS}, C_{RSS} and $R_{DS(ON)}$. The minimum gate drive voltage (the supply voltage to the FAN5009) dictates whether standard threshold or logic-level threshold MOSFETs must be used. With V_{GATE} ~10V, logic-level threshold MOSFETs ($V_{GS(TH)}$ < 2.5V) are recommended. The maximum output current I_O determines the $R_{DS(ON)}$ requirement for the low-side (synchronous) MOSFETs. With the FAN5019, currents are balanced between phases, thus the current in each low-side MOSFET is the output current divided by the total number of MOSFETs (n_{SF}). With conduction losses being dominant, the following expression shows the total power being dissipated in each synchronous MOSFET in terms of the ripple current per phase (I_R) and average total output current (I_O):

$$P_{SF} = (1 - D) \cdot \left[\left(\frac{I_O}{n_{SF}} \right)^2 + \frac{1}{12} \cdot \left(\frac{n \cdot I_R}{n_{SF}} \right)^2 \right] \cdot R_{DS(SF)} \qquad (15)$$

Knowing the maximum output current being designed for and the maximum allowed power dissipation, one can find the required $R_{DS(ON)}$ for the MOSFET. For D-PAK MOSFETs up to an ambient temperature of 50ºC, a safe limit for P_{SF} is 1W–1.5W at 125ºC junction temperature. Thus, for our example (65A maximum), we find $R_{DS(SF)}$ (per MOSFET) < 8.7mΩ. This $R_{DS(SF)}$ is also at a junction temperature of about 125ºC, so we need to make sure we account for this when making this selection. For our example, we selected two lower side MOSFETs at 8.6mΩ each at room temperature, which gives 8.4mΩ at high temperature.

Another important factor for the synchronous MOSFET is the input capacitance and feedback capacitance. The ratio of the feedback to input needs to be small (less than 10% is recommended), to prevent accidental turn-on of the synchronous MOSFETs when the switch node goes high.

Also, the time to switch the synchronous MOSFETs off should not exceed the non-overlap dead time of the MOSFET driver (40ns typical for the FAN5009). The output impedance of the driver is about 2Ω and the typical MOSFET input gate resistances are about 1Ω–2Ω, so a total gate capacitance of less than 6000pF should be adhered to. Since there are two MOSFETs in parallel, we should limit the input capacitance for each synchronous MOSFET to 3000pF.

The high-side (main) MOSFET has to be able to handle two main power dissipation components; conduction and switching losses. The switching loss is related to the amount of time it takes for the main MOSFET to turn on and off, and to the current and voltage that are being switched. Basing the switching speed on the rise and fall time of the gate driver impedance and MOSFET input capacitance, the following expression provides an approximate value for the switching loss per main MOSFET, where n_{MF} is the total number of main MOSFETs:

$$P_{S(MF)} = 2 \cdot f_{SW} \cdot \frac{V_{CC} \cdot I_O}{n_{MF}} \cdot R_G \cdot \frac{n_{MF}}{n} \cdot C_{ISS} \qquad (16)$$

Here, R_G is the total gate resistance (2Ω for the FAN5009 and about 1Ω for typical high speed switching MOSFETs, making R_G = 3Ω) and CISS is the input capacitance of the main MOSFET. It is interesting to note that adding more main MOSFETs (nMF) does not really help the switching loss per MOSFET since the additional gate capacitance slows down switching. The best way to reduce switching loss is to use lower gate capacitance devices.

The conduction loss of the main MOSFET is given by the following, where $R_{DS(MF)}$ is the ON-resistance of the MOSFET:

$$P_{C(MF)} = D \cdot \left[\left(\frac{I_O}{n_{MF}} \right)^2 + \frac{1}{12} \cdot \left(\frac{n \cdot I_R}{n_{MF}} \right)^2 \right] \cdot R_{DS(MF)} \qquad (17)$$

Typically, for main MOSFETs, one wants the highest speed (low C_{ISS}) device, but these usually have higher ON-resistance. One must select a device that meets the total power dissipation (about 1.5 W for a single D-PAK) when combining the switching and conduction losses.

For our example, we have selected a Fairchild FD6696 as the main MOSFET (three total; n_{MF} = 3), with a C_{iss} = 2058 pF (max) and $R_{DS(MF)}$ = 15m (max at T_J = 125ºC) and an Fairchild FDD6682 as the synchronous MOSFET (six total; n_{SF} = 6), with C_{iss} = 2880pF (max) and $R_{DS(SF)}$ = 11.9mΩ (max at T_J = 125ºC). The synchronous MOSFET C_{iss} is less than 3000 pF, satisfying that requirement. Solving for the power dissipation per MOSFET at I_O = 65A and I_R = 8.86A yields 1.24W for each synchronous MOSFET and 1.62W for each main MOSFET. These numbers work well considering there is usually more PCB area available for each main MOSFET versus each synchronous MOSFET.

One last thing to look at is the power dissipation in the driver for each phase. This is best described in terms of the Q_G for the MOSFETs and is given by the following, where Q_{GMF} is the total gate charge for each main MOSFET and Q_{GSF} is the total gate charge for each synchronous MOSFET:

$$P_{DRV} = \left[\frac{f_{SW}}{2 \cdot n} \cdot (n_{MF} \cdot Q_{GMF} + n_{SF} \cdot Q_{GSF}) + I_{CC}\right] \cdot V_{CC} \quad (18)$$

Also shown is the standby dissipation factor (I_{CC} times the V_{CC}) for the driver. For the FAN5009, the maximum dissipation should be less than 400 mW. For our example, with I_{CC} = 7 mA, Q_{GMF} = 24nC (max) and Q_{GSF} = 31nC (max), we find 202 mW in each driver, which is below the 400 mW dissipation limit. See the FAN5009 data sheet for more details.

Ramp Resistor Selection

The ramp resistor (R_R) is used for setting the size of the internal PWM ramp. The value of this resistor is chosen to provide the best combination of thermal balance, stability, and transient response. The following expression is used for determining the optimum value:

$$R_R = \frac{A_R \cdot L}{3 \cdot A_D \cdot R_{DS} \cdot C_R} \quad (19)$$

$$R_R = \frac{0.2 \cdot 650nH}{3 \cdot 5 \cdot 5.95m\Omega \cdot 5pF} = 291k\Omega$$

where A_R is the internal ramp amplifier gain, A_D is the current balancing amplifier gain, R_{DS} is the total low-side MOSFET ON-resistance, and C_R is the internal ramp capacitor value. A close standard 1% resistor value is 301kΩ.

The internal ramp voltage magnitude can be calculated using:

$$V_R = \frac{A_R \cdot (1 - D) \cdot V_{VID}}{R_R \cdot C_R \cdot f_{SW}} \quad (20)$$

$$V_R = \frac{0.2 \cdot (1 - 0.125) \cdot 1.5V}{301k\Omega \cdot 5pF \cdot 228kHz} = 0.765V$$

The size of the internal ramp can be made larger or smaller. If it is made larger, stability and transient response will improve, but thermal balance will degrade. Likewise, if the ramp is made smaller, thermal balance will improve at the sacrifice of transient response and stability. The factor of three in the denominator of equation 19 sets a ramp size that gives an optimal balance for good stability, transient response, and thermal balance.

COMP Pin Ramp

There is a ramp signal on the COMP pin due to the droop voltage and output voltage ramps. This ramp amplitude adds to the internal ramp to produce the following overall ramp signal at the PWM input.

$$V_{RT} = \frac{V_R}{\left(1 - \frac{2 \cdot (1 - n \cdot D)}{n \cdot f_{SW} \cdot C_X \cdot R_O}\right)} \quad (21)$$

For this example, the overall ramp signal is found to be 0.974V.

Current Limit Set Point

To select the current limit set point, we need to find the resistor value for R_{LIM}. The current limit threshold for the FAN5019 is set with a 3V source (V_{LIM}) across R_{LIM} with a gain of 10.4mV/mA (A_{LIM}). R_{LIM} can be found using the following:

$$R_{LIM} = \frac{A_{LIM} \cdot V_{LIM}}{I_{LIM} \cdot R_O} \quad (22)$$

For values of R_{LIM} greater than 500kΩ, the current limit may be lower than expected, so some adjustment of R_{LIM} may be needed. Here, I_{LIM} is the average current limit for the output of the supply. For our example, choosing 120A for I_{LIM}, we find R_{LIM} to be 200kΩ, for which we chose 200kΩ as the nearest 1% value.

The per phase current limit described earlier has its limit determined by the following:

$$I_{PHLIM} \cong \frac{V_{COMP(MAX)} - V_R - V_{BIAS}}{A_D \cdot R_{DS(MAX)}} - \frac{I_R}{2} \quad (23)$$

For the FAN5019, the maximum COMP voltage ($V_{COMP(MAX)}$) is 3.3 V, the COMP pin bias voltage (V_{BIAS}) is 1.2V, and the current balancing amplifier gain (A_D) is 5. Using V_R of 0.765V, and $R_{DS(MAX)}$ of 5.95mΩ (low-side ON-resistance at 125°C), we find a per-phase limit of 40.44A.

This limit can be adjusted by changing the ramp voltage V_R. But make sure not to set the per-phase limit lower than the average per-phase current ($I_{LIM/n}$).

There is also a per phase initial duty cycle limit determined by:

$$D_{MAX} = D \cdot \frac{V_{COMP(MAX)} - V_{BIAS}}{V_{RT}} \quad (24)$$

For this example, the maximum duty cycle is found to be 0.2696.

Feedback Loop Compensation Design

Optimized compensation of the FAN5019 allows the best possible response of the regulator's output to a load change. The basis for determining the optimum compensation is to make the regulator and output decoupling appear as an output impedance that is entirely resistive over the widest possible frequency range, including DC, and equal to the droop resistance (R_O). With the resistive output impedance, the output voltage will droop in proportion with the load current at any load current slew rate; this ensures the optimal positioning and allows the minimization of the output decoupling.

With the multimode feedback structure of the FAN5019, one needs to set the feedback compensation to make the converter's output impedance work in conjunction with the output decoupling to meet this goal. There are several poles and zeros created by the output inductor and decoupling capacitors (output filter) that need to be compensated for.

A type-III compensator on the voltage feedback is adequate for proper compensation of the output filter. The expressions given in Equations 25–29 are intended to yield an optimal starting point for the design; some adjustments may be necessary to account for PCB and component parasitic effects (see the Tuning Procedure for the FAN5019 section).

The first step is to compute the time constants for all of the poles and zeros in the system:

$$R_E = n \cdot R_O + A_D \cdot R_{DS} + \frac{R_L \cdot V_{RT}}{V_{VID}} + \frac{2 \cdot L \cdot (1 - n \cdot D) \cdot V_{RT}}{n \cdot C_X \cdot R_O \cdot V_{VID}} \quad (25)$$

$$R_E = 3 \cdot 1.3m\Omega + 5 \cdot 5.95m\Omega + \frac{1.6m\Omega \cdot 0.974V}{1.5V} + \frac{2 \cdot 650nH \cdot (1 - 0.375) \cdot 0.974V}{3 \cdot 6.56mF \cdot 1.3m\Omega \cdot 1.5V} = 55.3m\Omega$$

$$T_A = C_X \cdot (R_O - R') + \frac{L_X}{R_O} \cdot \frac{R_O - R'}{R_X} \quad (26)$$

$$T_A = 6.56mF \cdot (1.3m\Omega - 0.6m\Omega) + \frac{375pH}{1.3m\Omega} \cdot \frac{1.3m\Omega - 0.6m\Omega}{1.0m\Omega} = 4.79\mu s$$

$$T_B = (R_X + R' - R_O) \cdot C_X \quad (27)$$

$$T_B = (1.0m\Omega + 0.6m\Omega - 1.3m\Omega) \cdot 6.56mF = 1.97\mu s$$

$$T_C = \frac{V_{RT} \cdot \left(L - \frac{A_D \cdot R_{DS}}{2 \cdot f_{SW}}\right)}{V_{VID} \cdot R_E} \quad (28)$$

$$T_C = \frac{0.974V \cdot \left(650nH - \frac{5 \cdot 6.95m\Omega}{2 \cdot 228kHz}\right)}{1.5V \cdot 55.3m\Omega} = 6.86\mu s$$

$$T_D = \frac{C_X \cdot C_Z \cdot R_O^2}{C_X \cdot (R_O - R') + C_Z \cdot R_O} \quad (29)$$

$$T_D = \frac{6.56mF \cdot 220\mu F \cdot (1.3m\Omega)^2}{6.56mF \cdot (1.3m\Omega - 0.6m\Omega) + 220\mu F \cdot 1.3m\Omega} = 500ns$$

where, for the FAN5019, R' is the PCB resistance from the bulk capacitors to the ceramics and where R_{DS} is approximately the total low-side MOSFET ON resistance per phase at 25ºC. For this example, A_D is 5, V_{RT} equals 0.974V, R' is approximately 0.6mΩ (assuming a 4-layer motherboard) and L_X is 375pH for the eight Al-Poly capacitors.

The compensation values can then be solved for using the following:

$$C_A = \frac{n \cdot R_O \cdot T_A}{R_E \cdot R_B} \quad (30)$$

$$C_A = \frac{3 \cdot 1.3m\Omega \cdot 4.79\mu s}{55.3m\Omega \cdot 1.33k\Omega} = 253pF$$

$$R_A = \frac{T_C}{C_A} = \frac{6.86\mu s}{253pF} = 27.1k\Omega \quad (31)$$

$$C_B = \frac{T_B}{R_B} = \frac{1.97\mu s}{1.33k\Omega} = 1.48nF \quad (32)$$

$$C_{FB} = \frac{T_D}{R_A} = \frac{500ns}{27.1k\Omega} = 18.5pF \quad (33)$$

Choosing the closest standard values for these components yields: C_A = 390pF, R_A = 16.9kΩ, C_B = 1.5nF, and C_{FB} = 33pF.

C_{IN} Selection and Input Current di/dt Reduction

In continuous inductor-current mode, the source current of the high-side MOSFET is approximately a square wave with a duty ratio equal to n (V_{OUT}/V_{IN}) and an amplitude of one-nth of the maximum output current. To prevent large voltage transients, a low ESR input capacitor sized for the maximum rms current must be used. The maximum rms capacitor current is given by:

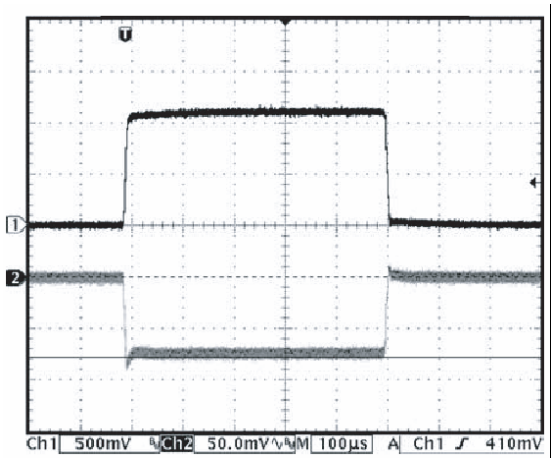


Figure 6. Typical Transient Response for Design Example

$$I_{CRMS} = D \cdot I_O \cdot \sqrt{\frac{1}{n \cdot D} - 1} \quad (34)$$

$$I_{CRMS} = 0.125 \cdot 65A \cdot \sqrt{\frac{1}{3 \cdot 0.125} - 1} = 10.5A$$

Note that the capacitor manufacturer's ripple current ratings are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor, or to choose a capacitor rated at a higher temperature than required. Several capacitors may be placed in parallel to meet size or height requirements in the design. In this example, the input capacitor bank is formed by three 2200µF, 16V Nichicon capacitors with a ripple current rating of 3.5A each.

To reduce the input-current di/dt to below the recommended maximum of 0.1A/µs, an additional small inductor (L > 1µH @ 15A) should be inserted between the converter and the supply bus. That inductor also acts as a filter between the converter and the primary power source.

$$R_{CS2(NEW)} = R_{CS2(OLD)} \cdot \frac{(V_{NL} - V_{FLCOLD})}{(V_{NL} - V_{FLHOT})} \quad (35)$$

Tuning Procedure for the FAN5019

DC Load line Setting

1. Build circuit based on compensation values computed from design spreadsheet.

2. Hook up DC load to circuit, turn on and verify operation. Also check for jitter at no-load and full-load.

3. Measure output voltage at no-load (V_{NL}). Verify it is within tolerance.

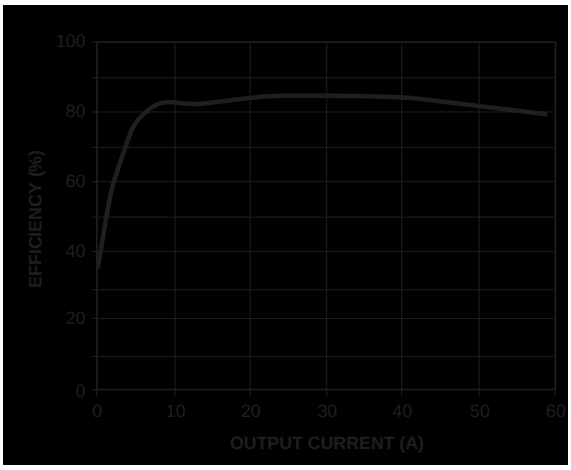


Figure 7. Efficiency vs. Output Current (Circuit of Figure 5)

4. Measure output voltage at full-load cold (V_{FLCOLD}). Let board soak for ~10 minutes at full-load and measure output (V_{FLHOT}). If there is a change of more than a couple of millivolts, adjust R_{CS1} and R_{CS2} using Equations 35 and 37.

5. Repeat Step 4 until cold and hot voltage measurements remain the same.

6. Measure output voltage from no-load to full-load using 5 Amp steps. Compute the loadline slope for each change and then average to get overall loadline slope (R_{OMEAS}).

7. If R_{OMEAS} is off from R_O by more than 0.05 mΩ, use the following to adjust the R_{PH} values:

$$R_{PH(NEW)} = R_{PH(OLD)} \cdot \frac{R_{OMEAS}}{R_O} \quad (36)$$

8. Repeat Steps 6 and 7 to check loadline and repeat adjustments if necessary.

9. Once complete with DC loadline adjustment, do not change R_{PH}, R_{CS1}, R_{CS2}, or R_{TH} for rest of procedure.

$$R_{CS(NEW)} = \frac{1}{\frac{R_{CS(OLD)} + R_{TH(25^\circ C)}}{R_{CS1(OLD)} \cdot R_{TH(25^\circ C)} + \left(R_{CS2(OLD)} - R_{CS2(NEW)}\right) \cdot \left(R_{CS1(OLD)} - R_{TH(25^\circ C)}\right)} - \frac{1}{R_{TH(25^\circ C)}}} \quad (37)$$

10. Measure the output ripple at no-load and full-load with scope and make sure it is within spec.

AC Loadline Setting

11. Remove DC load from circuit and hook up dynamic load.

12. Hook up scope to output voltage and set to DC coupling with a time scale at 100µs/div.

13. Set dynamic load for a transient step of about 40A at 1kHz with 50% duty cycle.

14. Measure output waveform (may have to use DC offset on scope to see waveform). Try to use vertical scale of 100 mV/div or finer.

15. You will see a waveform that looks something like Figure 8. Use the horizontal cursors to measure V_{ACDRP} and V_{DCDRP} as shown.

DO NOT MEASURE THE UNDERSHOOT OR OVER-SHOOT THAT HAPPENS IMMEDIATELY AFTER THE STEP.

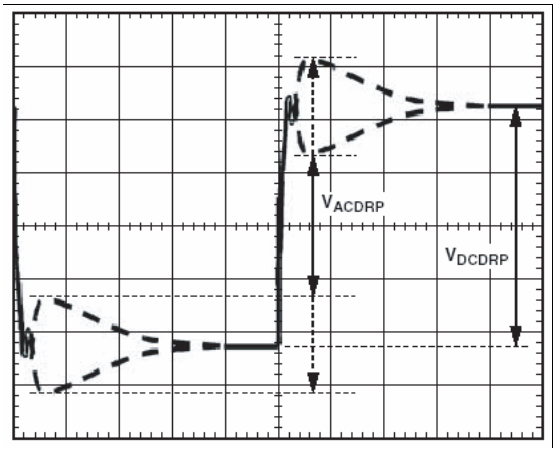


Figure 8. AC Loadline Waveform

16. If the V_{ACDRP} and V_{DCDRP} are different by more than a couple of millivolts, use Equation 38 to adjust C_{CS}. You may need to parallel different values to get the right one since there are limited standard capacitor values available (it is a good idea to have locations for two capacitors in the layout for this).

$$C_{CS(NEW)} = C_{CS(OLD)} \cdot \frac{V_{ACDRP}}{V_{DCDRP}} \quad (38)$$

17. Repeat Steps 11 to 13 and repeat adjustments if necessary. Once complete, do not change C_{CS} for the rest of the procedure.

18. Set dynamic load step to maximum step size (do not use a step size larger than needed) and verify that the output waveform is square (which means VACDRP and VDCDRP are equal). **NOTE:** MAKE SURE LOAD STEP SLEW RATE AND TURN-ON ARE SET FOR A SLEW RATE OF ~150–250A/µs (for example, a load step of 50A should take 200ns–300ns) WITH NO OVERSHOOT. Some dynamic loads will have an excessive turn-on overshoot if a minimum current is not set properly (this is an issue if using a VTT tool).

Initial Transient Setting

19. With dynamic load still set at maximum step size, expand scope time scale to see 2µs/div to 5µs/div. You will see a waveform that may have two overshoots and one minor undershoot (see Figure 9). Here, V_{DROOP} is the final desired value.

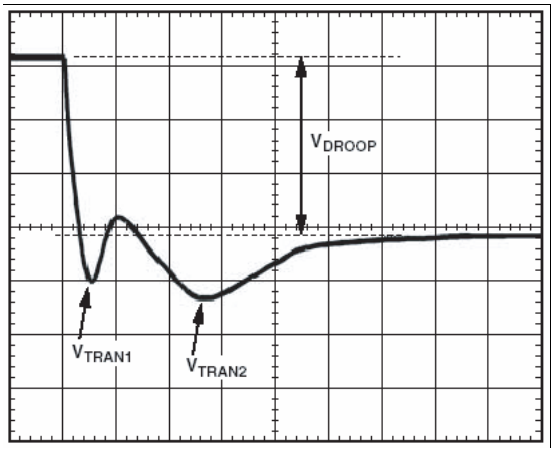


Figure 9. Transient Setting Waveform

20. If both overshoots are larger than desired, try making the following adjustments in this order. (**NOTE**: If these adjustments do not change the response, you are limited by the output decoupling.) Check the output response each time you make a change as well as the switching nodes (to make sure it is still stable).
    a. Make ramp resistor larger by 25% (R_{RAMP}).
    b. For V_{TRAN1}, increase CB or increase switching frequency.
    c. For V_{TRAN2}, increase R_A and decrease C_A by 25%.

21. For load release (see Figure 10), if $V_{TRANREL}$ is larger than V_{TRAN1} (see Figure 9), you do not have enough output capacitance. You will either need more capacitance or to make the inductor values smaller (if you change inductors, you need to start the design over using the spreadsheet and this tuning procedure).

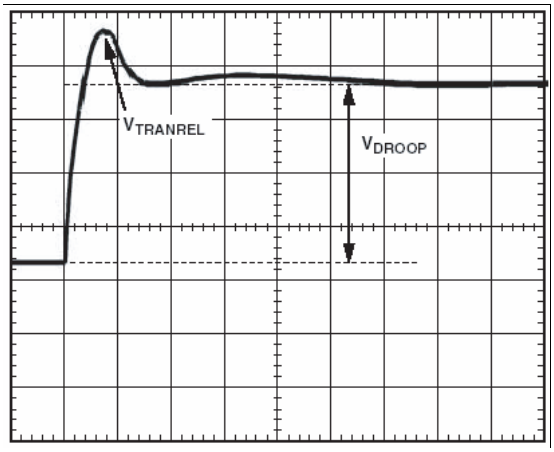


Figure 10. Transient Setting Waveform

Since the FAN5019 turns off all of the phases (switches inductors to ground), there is no ripple voltage present during load release. Thus, you do not have to add headroom for ripple, allowing your load release $V_{TRANREL}$ to be larger than V_{TRAN1} by that amount and still be meeting spec. If V_{TRAN1} and $V_{TRANREL}$ are less than the desired final droop, this implies that capacitors can be removed. When removing capacitors, make sure to check the output ripple voltage as well to make sure it is still within spec.

Layout and Component Placement

The following guidelines are recommended for optimal performance of a switching regulator in a PC system. Key layout issues are illustrated in Figure 11.

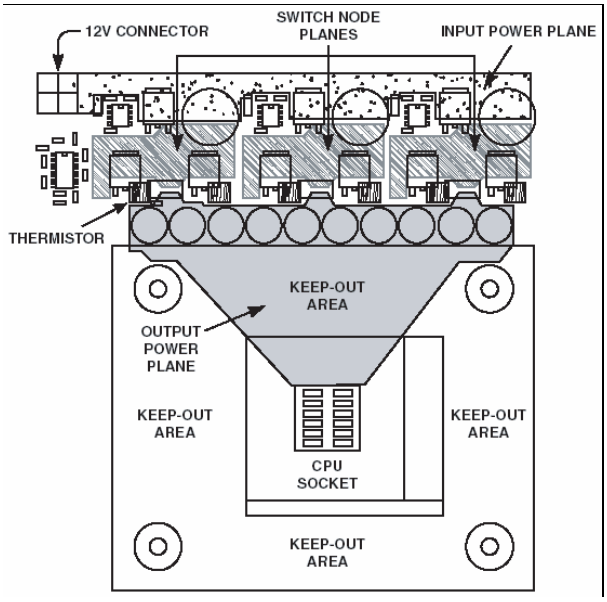


Figure 11. Layout Recommendations

General Recommendations

- For good results, at least a four-layer PCB is recommended. This should allow the needed versatility for control circuitry interconnections with optimal placement, power planes for ground, input, and output power, and wide interconnection traces in the rest of the power delivery current paths. Keep in mind that each square unit of 1 ounce copper trace has a resistance of ~0.53 mΩ at room temperature.

- Whenever high currents must be routed between PCB layers, vias should be used liberally to create several parallel current paths so that the resistance and inductance introduced by these current paths is minimized and the via current rating is not exceeded.

- If critical signal lines (including the output voltage sense lines of the FAN5019) must cross through power circuitry, it is best if a signal ground plane can be interposed between those signal lines and the traces of the power circuitry to serves as a shield to minimize noise injection into the signals..

- An analog ground plane should be used both around and under the FAN5019 for ground connections to the components associated with the controller. This plane should be tied to the nearest output decoupling capacitor ground and should not tie to any other power circuitry to prevent power currents from flowing in it.

- The components around the FAN5019 should be located close to the controller with short traces. The most important traces to keep short and away from other traces are the FB and CSSUM pins.

- The output capacitors should be connected as close as possible to the load (or connector) that receives the power (e.g., a microprocessor core). If the load is distributed, the capacitors should also be distributed, and generally in proportion to where the load tends to be more dynamic.

Power Circuitry

- The switching power path should be routed on the PCB to encompass the shortest possible length in order to minimize radiated switching noise energy (i.e., EMI) and conduction losses in the board. Failure to take proper precautions often results in EMI problems for the entire PC system as well as noise related operational problems in the power converter control circuitry. The switching power path is the loop formed by the current path through the input capacitors and the power MOSFETs including all interconnecting PCB traces and planes. The use of short and wide interconnection traces is especially critical in this path for two reasons: it minimizes the inductance in the switching loop, which can cause high-energy ringing, and it accommodates the high current demand with minimal voltage loss. Avoid crossing any signal lines over the switching power path loop, described below.

- Whenever a power dissipating component (e.g., a power MOSFET) is soldered to a PCB, the liberal use of vias, both directly on the mounting pad and immediately surrounding it, is recommended. Two important reasons for this are: improved current rating through the vias, and improved thermal performance from vias extended to the opposite side of the PCB where a plane can more readily transfer the heat to the air. Make a mirror image of any pad being used to heatsink the MOSFETs on the opposite side of the PCB to achieve the best thermal dissipation to the air around the board. To further improve thermal performance, the largest possible pad area should be used.

- The output power path should also be routed to encompass a short distance. The output power path is formed by the current path through the inductor, the output capacitors, and the load.

- For best EMI containment, a solid power ground plane should be used as one of the inner layers extending fully under all the power components.

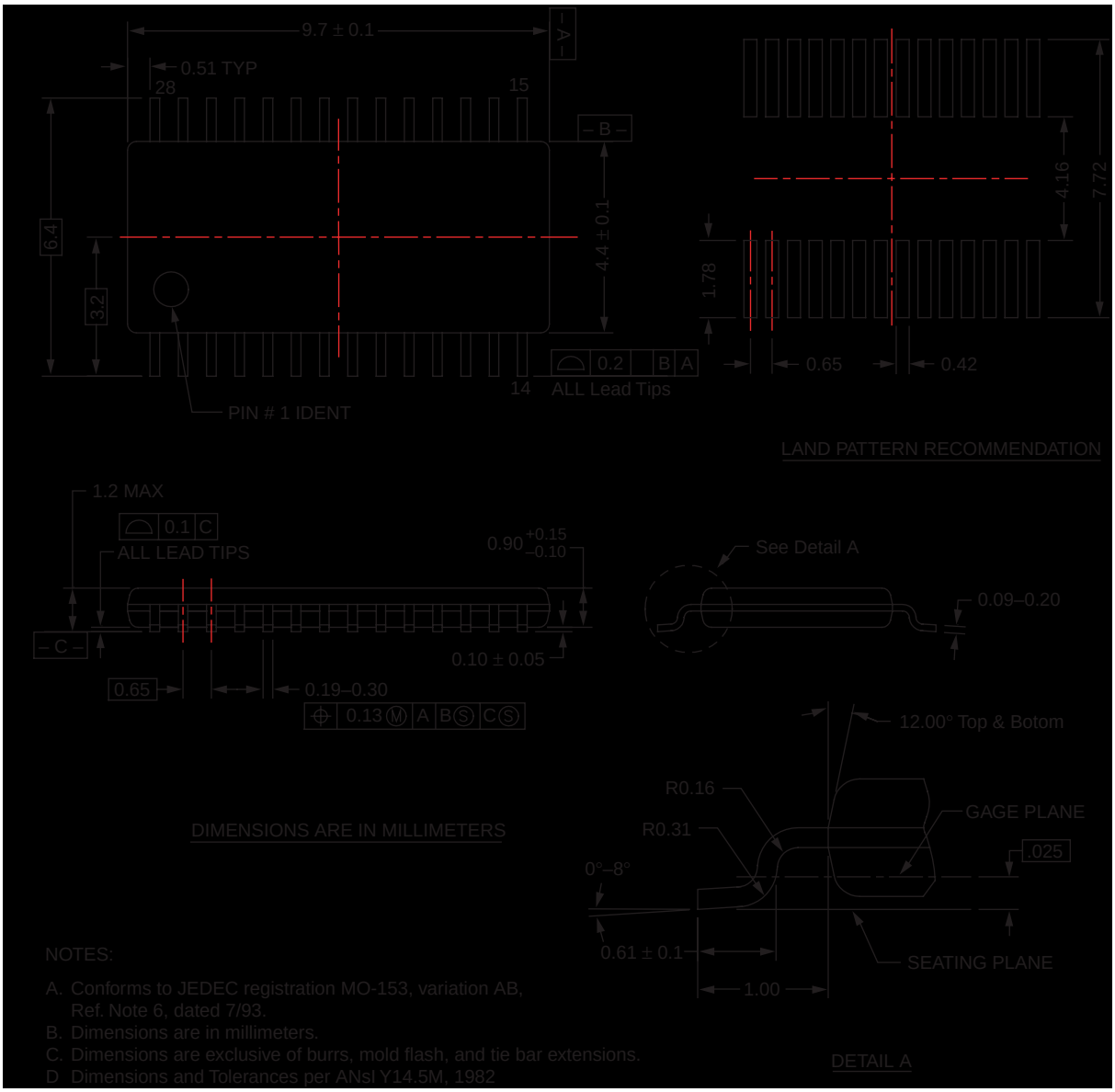
Signal Circuitry

- The output voltage is sensed and regulated between the FB pin and the FBRTN pin (which connects to the signal ground at the load). In order to avoid differential mode noise pickup in the sensed signal, the loop area should be small. Thus the FB and FBRTN traces should be routed adjacent to each other atop the power ground plane back to the controller.

- The feedback traces from the switch nodes should be connected as close as possible to the inductor. The CSREF signal should be connected to the output voltage at the nearest inductor to the controller.

Mechanical Dimensions

28-Pin TSSOP



Ordering Information

Part Number	Temperature Range	Package	Packing
FAN5019MTC	0°C to +85°C	TSSOP-28	Rail
FAN5019MTCX	0°C to +85°C	TSSOP-28	Tape and Reel