



Integrated Device Technology, Inc.

OCTAL BUS SWITCH

IDT74FST3245
IDT74FST32245
PRELIMINARY

FEATURES:

- Bus switches provide zero delay paths
- Extended commercial range of -40°C to $+85^{\circ}\text{C}$
- Low switch on-resistance:
 FST3xxx – 5Ω
 FST32xxx – 28Ω
- TTL-compatible input and output levels
- ESD > 2000V per MIL-STD-883, Method 3015;
 > 200V using machine model (C = 200pF, R = 0)
- Available in QSOP, TSSOP, SOIC and PDIP
- Pin-compatible with FCT245/FCT245T

DESCRIPTION:

The FST3245/32245 belong to IDT's family of Bus switches. Bus switch devices perform the function of connecting or isolating two ports without providing any inherent current sink or source capability. Thus they generate little or no noise of their own while providing a low resistance path for an external driver. These devices connect input and output ports through

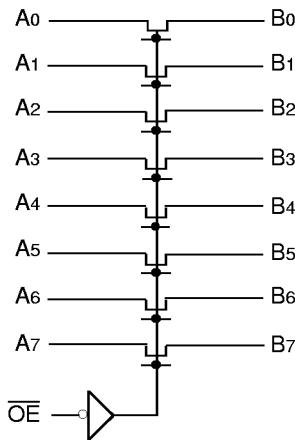
an n-channel FET. When the gate-to-source junction of this FET is adequately forward-biased the device conducts or the resistance between input and output ports is small. Without adequate bias on the gate-to-source junction of the FET, the FET is turned off, therefore with no Vcc applied, the device has hot insertion capability.

The low on-resistance and simplicity of the connection between input and output ports reduces the delay in this path to close to zero.

The FST32245 integrates terminating resistors in the device, thus eliminating the need for external 25Ω series resistors.

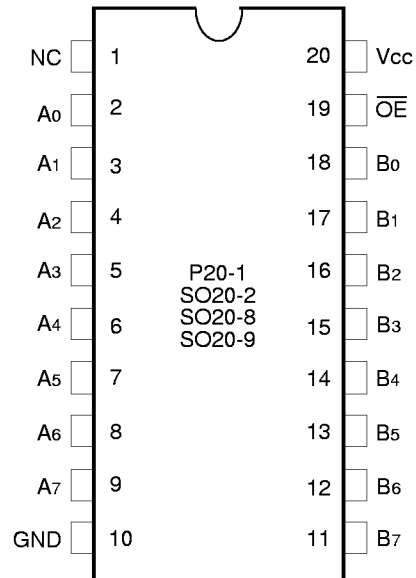
The FST3245 and FST32245 are octal TTL-compatible bus switches. The $\overline{\text{OE}}$ pin provides output enable control for all 8 bits. The direction control pin (DIR) of the FCT245/FCT245T is replaced with a "No connect" (NC) in the FST3245/32245. Bus switch devices provide an inherently bidirectional connection between ports, thus eliminating the purpose of the direction control pin.

FUNCTIONAL BLOCK DIAGRAM



3256 drw 01

PIN CONFIGURATION



DIP/SOIC/
 QSOP/TSSOP
 TOP VIEW

3256 drw 02

PIN DESCRIPTION

Pin Names	Description
$\overline{\text{OE}}$	Output Enable Input (Active LOW)
NC	No connect
A0-A7	A Port Bits
B0-B7	B Port Bits

3256 tbl 01

The IDT logo is a registered trademark of Integrated Device Technology, Inc.

COMMERCIAL TEMPERATURE RANGES

AUGUST 1996

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max.	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
TSTG	Storage Temperature	-65 to +150	°C
IOUT	Maximum Continuous Channel Current	128	mA

NOTES: 3256 Ink 02

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- Vcc, Control and Switch terminals.

FUNCTION TABLE

\overline{OE}	B0-7	Description
H	X	Disconnect
L	A0-7	Connect

NOTE: 3256 tbl 03

- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

CAPACITANCE⁽¹⁾

Symbol	Parameter	Conditions ⁽²⁾	Typ.	Unit
CIN	Control Input Capacitance		4	pF
CI/O	Switch Input/Output Capacitance	Switch Off		pF

NOTES: 3256 tbl 04

- Capacitance is characterized but not tested
- TA = 25°C, f = 1MHz, VIN = 0V, VOUT = 0V

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Commercial: TA = -40°C to +85°C, Vcc = 5.0V ±5%

Symbol	Parameter	Test Conditions ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Unit	
VIH	Input HIGH Voltage	Guaranteed Logic HIGH for Control Inputs	2.0	—	—	V	
VIL	Input LOW Voltage	Guaranteed Logic LOW for Control Inputs	—	—	0.8	V	
IiH	Input HIGH Current	VCC = Max.	—	—	±1	μA	
IiL	Input LOW Current						VI = VCC
IoZH	High Impedance Output Current (3-State Output pins)	VCC = Max.	—	—	±1	μA	
							Vo = VCC
IoZL			—	—	±1		
							Vo = GND
IOS	Short Circuit Current	VCC = Max., Vo = GND ⁽³⁾	—	300	—	mA	
VIK	Clamp Diode Voltage	VCC = Min., IIN = -18mA	—	-0.7	-1.2	V	
RON	Switch On Resistance ⁽⁴⁾	VCC = Min. VIN = 0.0V ION = 30mA	3xxx	—	5	7	Ω
			32xxx	17	28	40	
		VCC = Min. VIN = 2.4V ION = 15mA	3xxx	—	10	15	Ω
			32xxx	20	35	48	
IOFF	Input/Output Power Off Leakage	VCC = 0V, VIN or Vo ≤ 4.5V	—	—	±1	μA	
ICC	Quiescent Power Supply Current	VCC = Max., VI = GND or VCC	—	0.1	3	μA	

NOTES: 3256 Ink 05

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at Vcc = 5.0V, +25°C ambient.
- Not more than one output should be tested at one time. Duration of the test should not exceed one second.
- Measured by voltage drop between ports at indicated current through the switch.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V _{CC} = Max. V _{IN} = 3.4V ⁽³⁾		—	0.5	1.5	mA
I _{CCD}	Dynamic Power Supply Current ⁽⁴⁾	V _{CC} = Max. Outputs Open Enable Pin Toggling 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND	—	30	40	μA/ MHz/ Switch
I _C	Total Power Supply Current ⁽⁶⁾	V _{CC} = Max. Outputs Open Enable Pin Toggling (8 Switches Toggling) f _i = 10MHz 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND V _{IN} = 3.4 V _{IN} = GND	—	2.4 2.7	3.2 4.0	mA

NOTES:

3256 tbl 06

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V_{CC} = 5.0V, +25°C ambient.
- Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}
I_C = I_{CC} + ΔI_{CC} D_HN_T + I_{CCD} (f_{IN})
I_{CC} = Quiescent Current
 ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
D_H = Duty Cycle for TTL Inputs High
N_T = Number of TTL Inputs at D_H
I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
f_i = Input Frequency
N = Number of Switches Toggling at f_i
All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Commercial: TA = -40°C to +85°C, V_{CC} = 5.0V ±5%

Symbol	Description	Condition ⁽¹⁾	Min. ⁽²⁾	Typ.	3245	32245	Unit
					Max.		
t _{PLH} t _{PHL}	Data Propagation Delay A _i to B _i , B _i to A _i ^(3,4)	C _L = 50pF R _L = 500Ω	—	—	0.25	1.25	ns
t _{PZH} t _{PZL}	Switch Turn on Delay \overline{OE} to A _i , B _i		1.5	—	6.5	7.5	ns
t _{PHZ} t _{PLZ}	Switch Turn off Delay \overline{OE} to A _i , B _i ⁽³⁾		1.5	—	5.5	5.5	ns
Q _C	Charge Injection ^(5,6)		—	1.5	—	—	pC

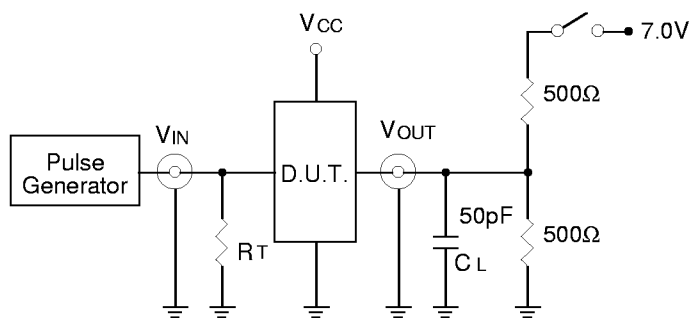
NOTES:

3256 tbl 07

- See test circuit and waveforms.
- Minimum limits guaranteed but not tested.
- This parameter is guaranteed by design but not tested.
- The bus switch contributes no propagation delay other than the RC delay of the on resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25 ns for 50 pF load. Since this time is constant and much smaller than the rise/fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.
- Measured at switch turn off, load = 50 pF in parallel with 10 MΩ scope probe, V_{IN} = 0.0 volts.
- Characterized parameter. Not 100% tested.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



3256 Ink 04

SWITCH POSITION

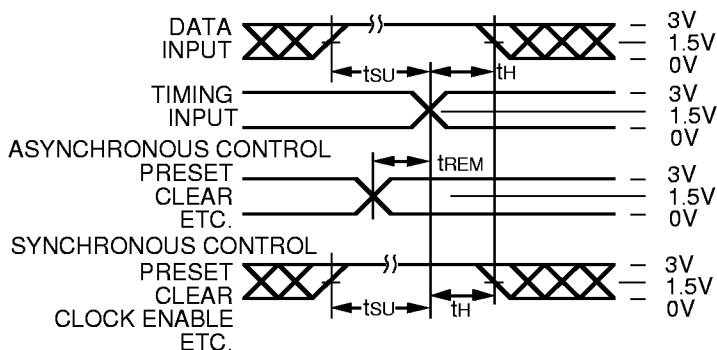
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

DEFINITIONS:

CL = Load capacitance: includes jig and probe capacitance.
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

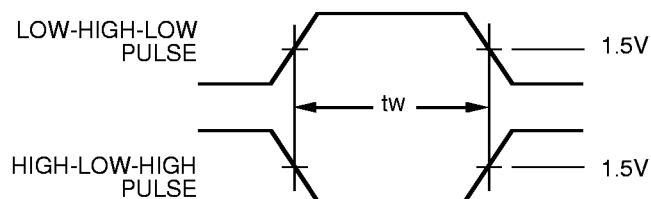
3256 Ink 08

SET-UP, HOLD AND RELEASE TIMES



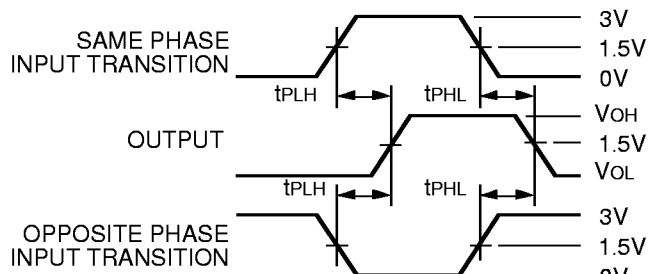
3256 Ink 03

PULSE WIDTH



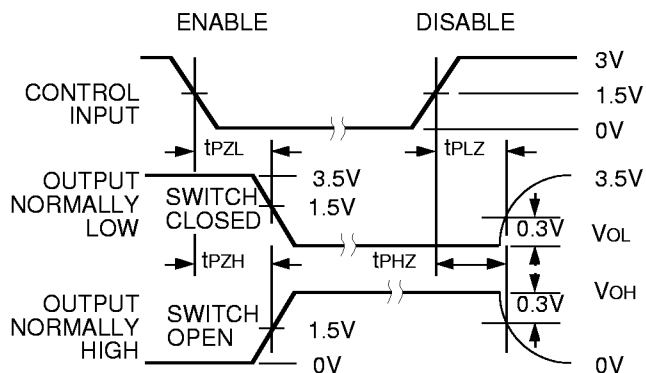
3256 Ink 06

PROPAGATION DELAY



3256 Ink 07

ENABLE AND DISABLE TIMES

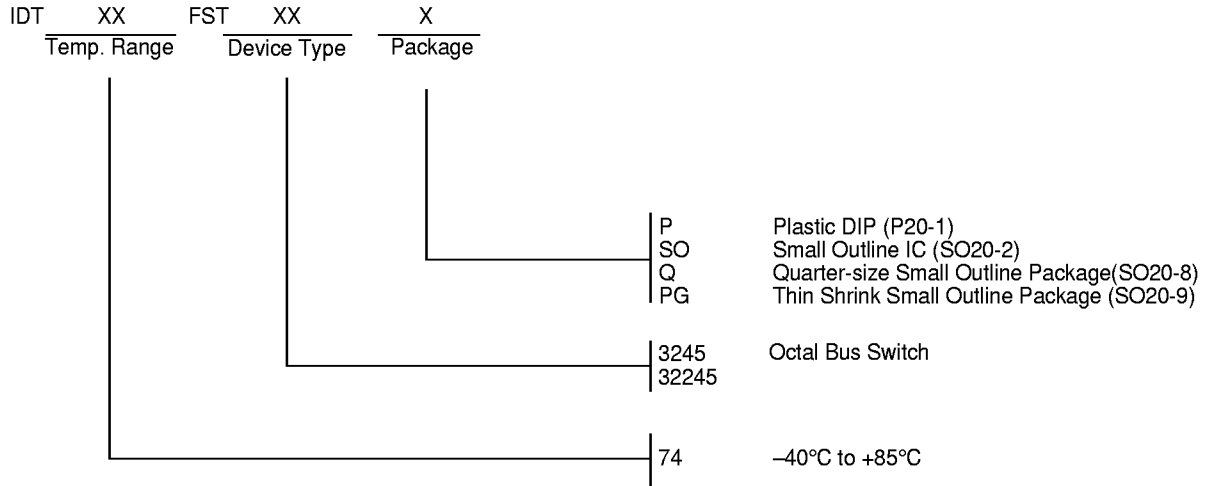


3256 Ink 05

NOTES:

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
- Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; $t_f \leq 2.5\text{ns}$; $t_r \leq 2.5\text{ns}$

ORDERING INFORMATION



3256 Ink 09