BLC2425M10LS250

Power LDMOS transistor

Rev. 3 — 19 April 2019

AMPLEON

Product data sheet

1. Product profile

1.1 General description

250 W LDMOS-based power transistor suitable for use in a variety of commercial and consumer cooking, industrial, scientific and medical applications at frequencies from 2400 MHz to 2500 MHz.

The BLC2425M10LS250 is designed for high-power CW applications and is assembled in a high performance plastic package.

Table 1. Typical performance

RF performance at V_{DS} = 32 V; I_{Dq} = 100 mA; T_{case} = 25 °C in a class-AB application circuit.

Test signal	f	V_{DS}	$P_{L(AV)}$	G_p	η_D
	(MHz)	(V)	(W)	(dB)	(%)
CW	2450	32	260	15.2	68.5
CW pulsed [1]	2450	32	260	15.3	68.8

[1] t_p = 100 μs; δ = 10 %.

1.2 Features and benefits

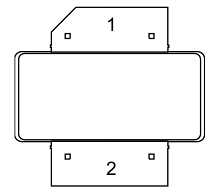
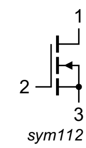
- High efficiency
- Excellent ruggedness
- Integrated ESD protection
- Designed for broadband operation (2400 MHz to 2500 MHz)
- Internally input and output matched
- For RoHS compliance see the product details on the Ampleon website

1.3 Applications

- RF power amplifiers for CW applications in the 2400 MHz to 2500 MHz frequency range such as commercial and consumer cooking, industrial, scientific and medical applications

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	drain		
2	gate		
flange	source		

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLC2425M10LS250	-	air cavity plastic earless flanged package; 2 leads	SOT1270-1

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		–6	+13	V
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature	[1]	-	225	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-case)}$	thermal resistance from junction to case	T_{case} = 80 °C; P_L = 250 W	0.33	K/W

6. Characteristics

Table 6. DC characteristics

T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 2.7 mA	65.00	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 32 V; I_D = 20 mA	1.68	2.15	2.68	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 32 V	-	-	2.8	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	-	59.7	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	280	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 15.2 A	-	22.6	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 10.64 A	-	40.5	-	mΩ

Table 7. RF characteristics

Test signal: pulsed at 2450 MHz; RF performance at V_{DS} = 32 V; I_{Dq} = 10 mA; T_{case} = 25 °C; unless otherwise specified; in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	P_L = 260 W	13.2	14.4	-	dB
RL_{in}	input return loss	P_L = 260 W	-	–15	–5	dB
η_D	drain efficiency	P_L = 260 W	64	68.7	-	%

7. Test information

7.1 Ruggedness in class-AB operation

The BLC2425M10LS250 is capable of withstanding a load mismatch corresponding to VSWR = 20 : 1 through all phases with a time rate of 55 ms/degree under the following conditions: V_{DS} = 32 V; I_{Dq} = 10 mA; P_L = 260 W (CW); f = 2450 MHz; T_{case} = 25 °C.

7.2 Impedance information

Table 8. Typical impedance

Measured load-pull data. Typical values unless otherwise specified. I_{Dq} = 10 mA; V_{DS} = 32 V.

f	Z_S [1]	Z_L [1]
(MHz)	(Ω)	(Ω)
2400	3.43 – 6.80j	2.31 – 2.00j
2450	3.31 – 6.57j	2.14 – 1.70j
2500	3.20 – 6.29j	1.98 – 1.43j

[1] Z_S and Z_L defined in Figure 1.

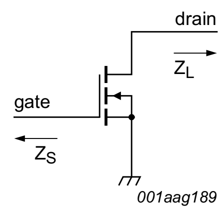
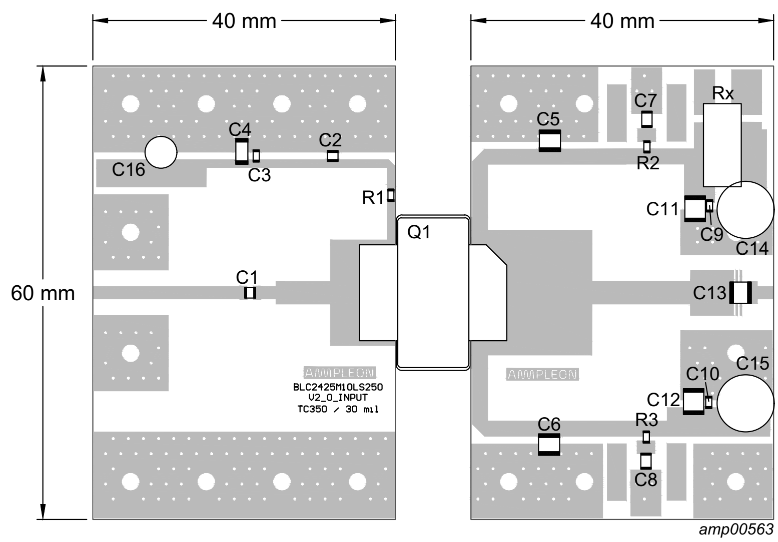


Fig 1. Definition of transistor impedance

7.3 Test circuit



Printed-Circuit Board (PCB): Rogers TC350; thickness = 0.762 mm; thickness copper plating = 35 μm.

See Table 9 for a list of components.

Fig 2. Component layout for production test circuit

Table 9. List of components

See Figure 2 for component layout.

Component	Description	Value	Remarks
C1, C2	multilayer ceramic chip capacitor	22 pF	ATC 800A
C3, C9, C10	multilayer ceramic chip capacitor	1000 pF, 50 V	C0805
C4	multilayer ceramic chip capacitor	1 μF, 50 V	C1206
C5, C6, C13	multilayer ceramic chip capacitor	22 pF	ATC 800B
C7, C8	multilayer ceramic chip capacitor	560 pF	ATC 100B
C11, C12	multilayer ceramic chip capacitor	4.7 μF, 50 V	C1210
C14, C15	electrolytic capacitor	100 μF, 63 V	
C16	electrolytic capacitor	22 μF, 63 V	
L1, L2	inductor	79 nH, 17.8 A [1]	1010VS-79NMEB
Q1	LDMOS transistor		BLC2425M10LS250

Table 9. List of components *...continued*

See Figure 2 for component layout.

Component	Description	Value	Remarks
R1	chip resistor	10 Ω	R0603
R2, R3	chip resistor	1.5 Ω	R1206
Rx	shunt resistor	0.01 Ω	Ohmite: FC4L110R010FER

[1] Optional component.

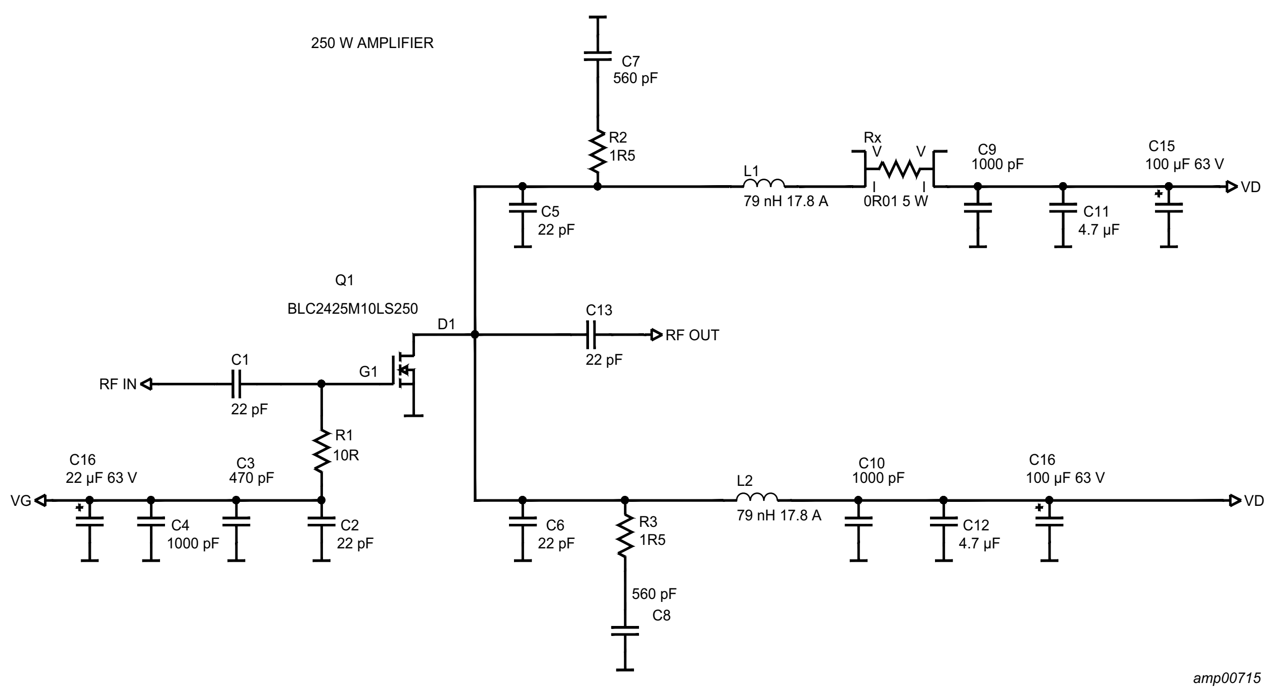
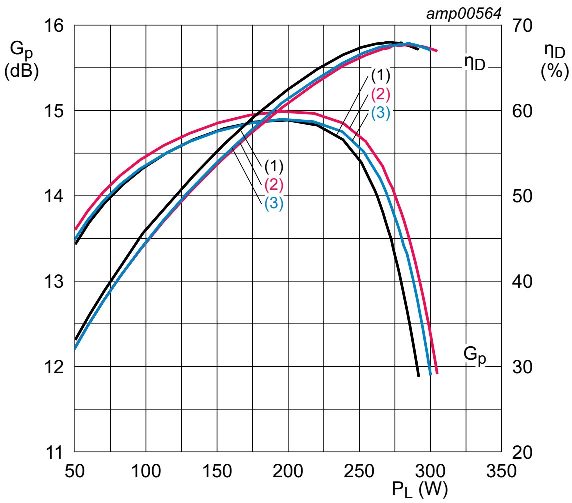


Fig 3. Electrical schematic

7.4 Graphical data



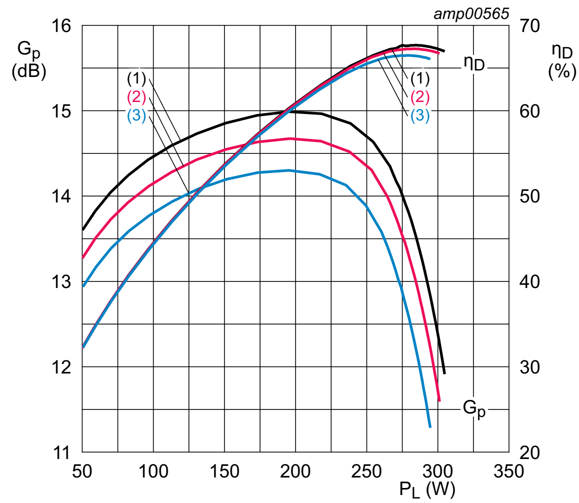
V_{DS} = 32 V; I_{Dq} = 10 mA.

(1) f = 2400 MHz

(2) f = 2450 MHz

(3) f = 2500 MHz

Fig 4. Power gain and drain efficiency as function of output power; typical values



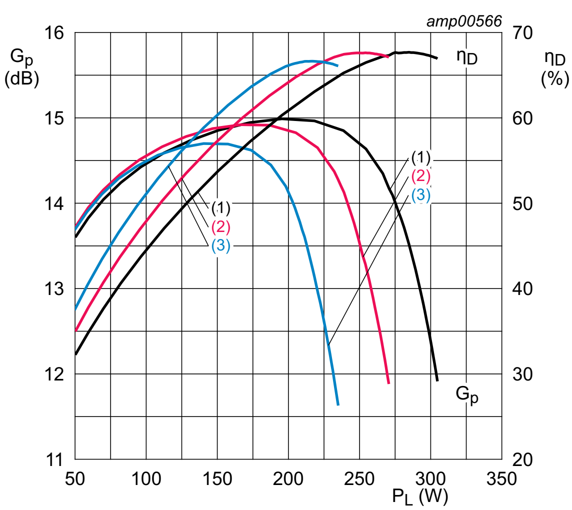
Performance derating at frequency of 2450 MHz.
V_{DS} = 32 V; I_{Dq} = 10 mA.

(1) T = 25 °C

(2) T = 45 °C

(3) T = 65 °C

Fig 5. Power gain and drain efficiency as function of output power; typical values



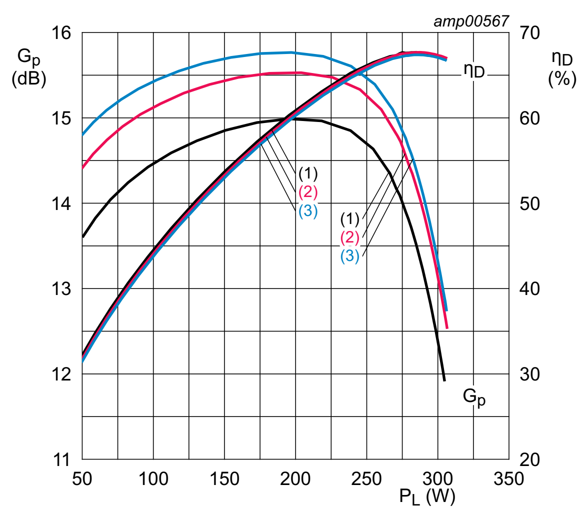
Performance derating at frequency of 2450 MHz.
I_{Dq} = 10 mA.

(1) V_{DS} = 32 V

(2) V_{DS} = 30 V

(3) V_{DS} = 28 V

Fig 6. Power gain and drain efficiency as function of output power; typical values



Performance derating at frequency of 2450 MHz.
V_{DS} = 32 V.

(1) I_{Dq} = 10 mA

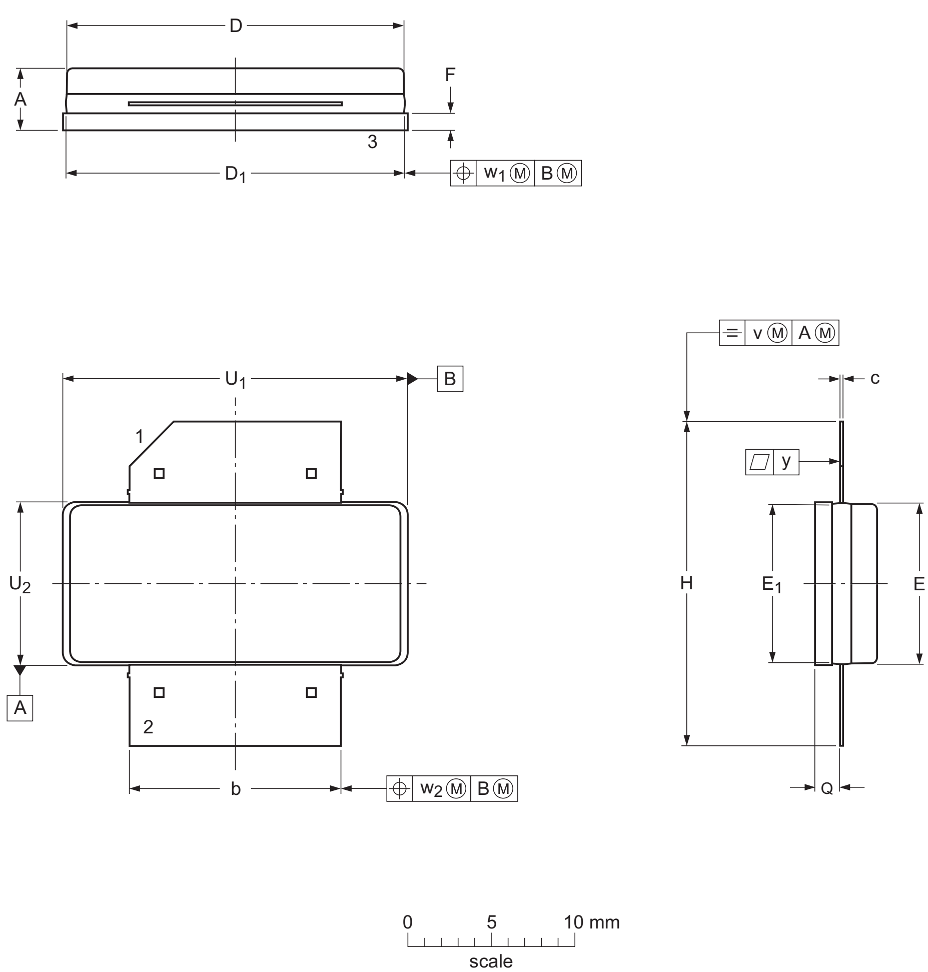
(2) I_{Dq} = 50 mA

(3) I_{Dq} = 100 mA

Fig 7. Power gain and drain efficiency as function of output power; typical values

8. Package outline

Air cavity plastic earless flanged package; 2 leads **SOT1270-1**



Dimensions

Unit		A	b	c	D	D_1	E	E_1	F	H	$Q^{(1)}$	U_1	U_2	v	w_1	w_2	y
mm	max	4.01	12.80	0.18	20.42	20.37	9.80	9.75	1.14	19.53	1.68	20.70	9.91	0.50	0.50	0.50	0.10
	nom																
	min	3.40	12.60	0.13	20.12	20.17	9.50	9.55	0.94	19.33	1.45	20.50	9.70				

Note
1. Dimension Q is measured 0.1 mm away from the flange.
2. Ringframe and/or ringframe glue shall not overhang at the side of the flange.

sot1270-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1270-1						~~16-09-28~~ 16-11-15

Fig 8. Package outline SOT1270-1

9. Handling information

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

Table 10. ESD sensitivity

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C1 [1]
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	1C [2]

[1] CDM classification C1 is granted to any part that passes after exposure to an ESD pulse of 250 V.

[2] HBM classification 1C is granted to any part that passes after exposure to an ESD pulse of 1000 V.

10. Abbreviations

Table 11. Abbreviations

Acronym	Description
CW	Continuous Wave
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MTF	Median Time to Failure
RoHS	Restriction of Hazardous Substances
VSWR	Voltage Standing Wave Ratio

11. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLC2425M10LS250 v.3	20190419	Product data sheet	-	BLC2425M10LS250 v.2
Modifications	• Figure 5 on page 6: figure note list updated			
BLC2425M10LS250 v.2	20180726	Product data sheet	-	BLC2425M10LS250 v.1
BLC2425M10LS250 v.1	20180710	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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14. Contents

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