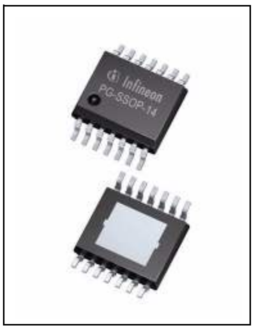
OPTIREG™ linear TLS820D2ELVSE

Low dropout linear voltage regulator



Features

- Wide input voltage range from 3.0 V to 40 V
- Selectable output voltage 5 V or 3.3 V
- Output voltage accuracy ≤ ±2%
- Output current capability up to 200 mA
- Ultra low current consumption, typical 20 µA
- Very low dropout voltage, typical 100 mV, at output currents below 100 mA
- Stable with ceramic output capacitor of 1 µF
- Enable
- Reset output
- Adjustable reset threshold down to 2 V
- Overtemperature shutdown
- Output current limitation
- Wide temperature range
- Green Product (RoHS compliant)

Potential applications

- Automotive or other supply systems that are connected to the battery permanently
- Automotive supply systems that need to operate in cranking condition

Product validation

Qualified for automotive applications. Product validation according to AEC-Q100.

Description

The OPTIREG™ linear TLS820D2ELVSE is a linear voltage regulator with high performance, very low dropout voltage and very low quiescent current.

With an input voltage range of 3 V to 40 V and very low quiescent current of only 20 µA, this regulator is perfectly suitable for automotive or other supply systems permanently connected to the battery.

The new loop concept combines fast regulation and very high stability while requiring only one small ceramic capacitor of 1 µF at the output. At output currents below 100 mA the device has a very low dropout voltage of only 100 mV (for an output voltage of 5 V) and 120 mV (for an output voltage of 3.3 V). The operating range starts at an input voltage of only 3 V (extended operating range). This makes the TLS820D2ELVSE suitable for automotive systems that need to operate during cranking condition.

The device can be switched on and off by the enable feature.

The output voltage of the TLS820D2ELVSE can be selected between 5 V and 3.3 V by connecting the SEL pin to V_Q or GND. When the SEL pin is connected to V_Q, the regulator's output is set to 5 V; when the SEL pin is connected to GND, the regulator's output is set to 3.3 V.

The reset feature supervises the output voltage, including undervoltage reset, delayed reset at power-on and an adjustable lower reset threshold.

Internal protection features such as output current limitation and overtemperature shutdown, protect the device from immediate damage caused by failure such as output shorted to GND, overcurrent or overtemperature conditions.

External components

An input capacitor C_I is recommended to compensate for line influences. The output capacitor C_Q is necessary for the stability of the regulating circuit. The TLS820D2ELVSE is designed to be stable with low ESR ceramic capacitors.

Type	Package	Marking
TLS820D2ELVSE	PG-SSOP-14	820D2VSE

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1 Block diagram

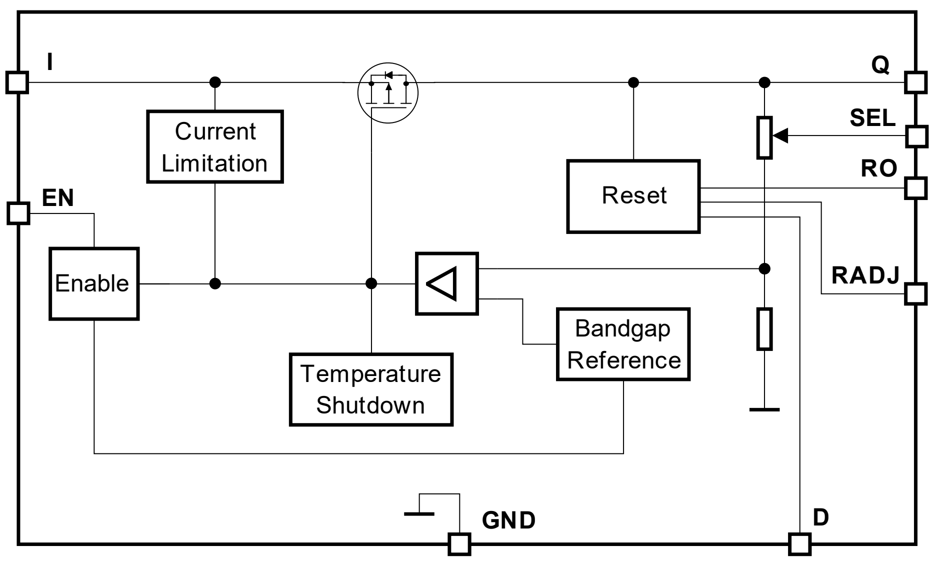


Figure 1 Block diagram TLS820D2ELVSE

2 Pin configuration

2.1 Pin assignment TLS820D2ELVSE

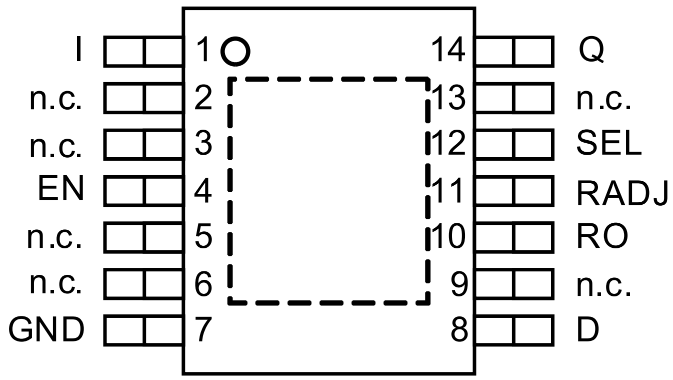


Figure 2 Pin configuration TLS820D2ELVSE

2.2 Pin definitions and functions TLS820D2ELVSE

Pin	Symbol	Function
1	I	**Input** It is recommended to place a small ceramic capacitor to GND, close to the pins, in order to compensate line influences.
2	n. c.	**Not connected** Leave open or connect to GND.
3	n. c.	**Not connected** Leave open or connect to GND.
4	EN	**Enable input** (integrated pull-down resistor) “High” enables the device. “Low” disables the device.
5	n. c.	**Not connected** Leave open or connect to GND.
6	n. c.	**Not connected** Leave open or connect to GND.
7	GND	**Ground**
8	D	**Reset delay timing** Connect a ceramic capacitor to GND for adjusting the reset delay time. If the reset function is not needed, then leave this pin open.
9	n. c.	**Not connected** Leave open or connect to GND.
10	RO	**Reset output** (integrated pull-up resistor to Q) Open collector output. Leave open if the reset function is not needed.

Pin configuration

Pin	Symbol	Function
11	RADJ	**Reset threshold adjustment** Connect to GND to use standard value. Connect an external voltage divider to adjust reset threshold.
12	SEL	**Output voltage selection** Connect to Q to select 5 V output voltage. Connect to GND to select 3.3 V output voltage.
13	n. c.	**Not connected** Leave open or connect to GND.
14	Q	**Output voltage** Connect output capacitor C_Q to GND close to the pin, respecting the values specified for its capacitance and ESR in **"Functional range" on Page 8**.
Pad	–	**Exposed pad** Connect to heatsink area. Connect to GND.

3 General product characteristics

3.1 Absolute maximum ratings

Table 1 Absolute maximum ratings[1)]

T_j = -40°C to 150°C; all voltages with respect to ground (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input I, enable EN							
Voltage	V_I, V_{EN}	-0.3	–	45	V	–	P_3.1.1
Output Q, reset output RO							
Voltage	V_Q, V_{RO}	-0.3	–	7	V	–	P_3.1.2
Select SEL							
voltage	V_{SEL}	-0.3	–	7	V	–	P_3.1.3
Reset delay D, reset adjust RADJ							
Voltage	V_D, V_{RADJ}	-0.3	–	7	V	–	P_3.1.4
Temperatures							
Junction temperature	T_j	-40	–	150	°C	–	P_3.1.5
Storage temperature	T_{stg}	-55	–	150	°C	–	P_3.1.6
ESD absorption							
ESD susceptibility	$V_{ESD,HBM}$	-2	–	2	kV	Human Body Model (HBM)[2)]	P_3.1.7
ESD susceptibility	$V_{ESD,CDM}$	-750	–	750	V	Charged Device Model (CDM)[3)] at all pins	P_3.1.8

1) Not subject to production test, specified by design.
2) ESD susceptibility, HBM according to ANSI/ESDA/JEDEC JS001 (1.5 kΩ, 100 pF)
3) ESD susceptibility, Charged Device Model “CDM” ESDA STM5.3.1 or ANSI/ESD S.5.3.1

Notes

1. *Exceeding the absolute max ratings may cause permanent damage to the device and affects the device’s reliability.*
2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as operation outside the normal operating range. Protection functions are not designed for continuous repetitive operation.*

3.2 Functional range

Table 2 Functional range

T_j = -40°C to 150°C; all voltages with respect to ground (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input voltage range	V_I	$V_{Q,nom} + V_{dr}$	–	40	V	[1] –	P_3.2.1
Extended input voltage range	$V_{I,ext}$	3.0	–	40	V	[2] –	P_3.2.2
Enable voltage range	V_{EN}	0	–	40	V	–	P_3.2.3
Capacitance of output capacitor for stability	C_Q	1	–	–	µF	[3][4] –	P_3.2.4
Equivalent Series Resistance of output capacitor	$ESR(C_Q)$	–	–	50	Ω	[3] –	P_3.2.6
Junction temperature	T_j	-40	–	150	°C	–	P_3.2.7

1) Output current is limited internally and depends on the input voltage, see electrical characteristics for more details.
2) If $V_{I,ext,min} \leq V_I \leq V_{Q,nom} + V_{dr}$, then $V_Q = V_I - V_{dr}$. If $V_I < V_{I,ext,min}$, then V_Q can drop to 0 V.
3) Not subject to production test, specified by design.
4) The minimum output capacitance requirement is applicable for a worst case capacitance tolerance of 30%.

Note: Within the functional or operating range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the electrical characteristics table.

3.3 Thermal resistance

Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to ***www.jedec.org****.*

Table 3 Thermal resistance TLS820D2ELVSE in PG-SSOP-14 package

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Junction to case	R_{thJC}	–	15	–	K/W	[1] –	P_3.3.16
Junction to ambient	R_{thJA}	–	50	–	K/W	[1][2] 2s2p board	P_3.3.17
Junction to ambient	R_{thJA}	–	150	–	K/W	[1][3] 1s0p board, footprint only	P_3.3.18
Junction to ambient	R_{thJA}	–	74	–	K/W	[1][3] 1s0p board, 300 mm^2 heatsink area on PCB	P_3.3.19
Junction to ambient	R_{thJA}	–	62	–	K/W	[1][3] 1s0p board, 600 mm^2 heatsink area on PCB	P_3.3.20

1) Not subject to production test, specified by design.
2) Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board. The product (chip + package) was simulated on a 76.2 × 114.3 × 1.5 mm^3 board with 2 inner copper layers (2 × 70 µm Cu, 2 × 35 µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.
3) Specified R_{thJA} value is according to JEDEC JESD 51-3 at natural convection on FR4 1s0p board. The product (chip + package) was simulated on a 76.2 × 114.3 × 1.5 mm^3 board with 1 copper layer (1 × 70 µm Cu).

4 Block description and electrical characteristics

4.1 Voltage regulation

The output voltage V_Q is divided by a resistor network. The TLS820D2ELVSE compares this fractional voltage to an internal voltage reference and drives the pass transistor accordingly.

The control loop stability depends on the following factors:

- output capacitor C_Q
- load current
- chip temperature
- internal circuit design

Output capacitor

To ensure stable operation, the capacitance of the output capacitor and its equivalent series resistor (ESR) requirements as specified in **“Functional range” on Page 8** must be maintained. The output capacitor must be sized according to the requirements of the application to be able to buffer load steps.

Input capacitors, reverse polarity protection diode

An input capacitor C_I is recommended to compensate for line influences.

In order to block influences such as pulses and high frequency distortion at the input, an additional reverse polarity protection diode and a combination of several capacitors for filtering should be used. Connect the capacitors close to the component’s terminals.

Smooth ramp-up

In order to prevent overshoots during startup, a smooth ramp-up function is implemented. This ensures a reduced output voltage overshoot during startup, mostly independent from load and output capacitance.

Output current limitation

If the load current exceeds the specified limit, due to a short-circuit for example, then the device limits the output current and the output voltage decreases.

Overtemperature shutdown

The overtemperature shutdown circuit prevents the device from immediate destruction in case of a fault condition, for example due to a permanent short-circuit at the output, by switching off the power stage. After the device has cooled down, the regulator restarts. This leads to an oscillatory behavior of the output voltage until the fault is removed. However, any junction temperature above 150°C is outside the maximum ratings and therefore significantly reduces the lifetime of the device.

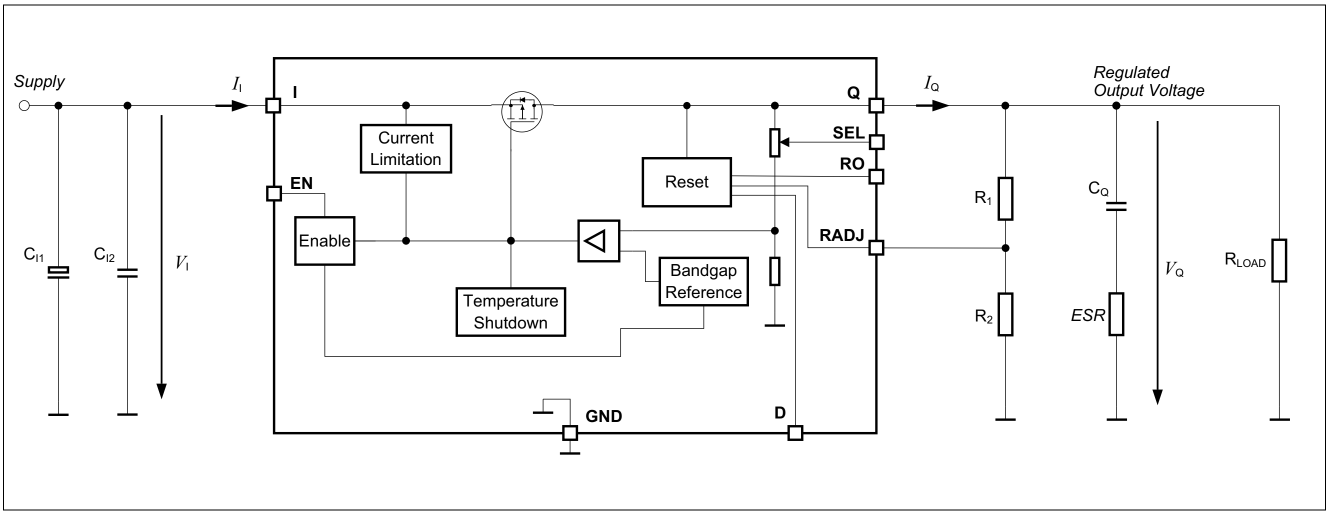


Figure 3 Voltage regulation

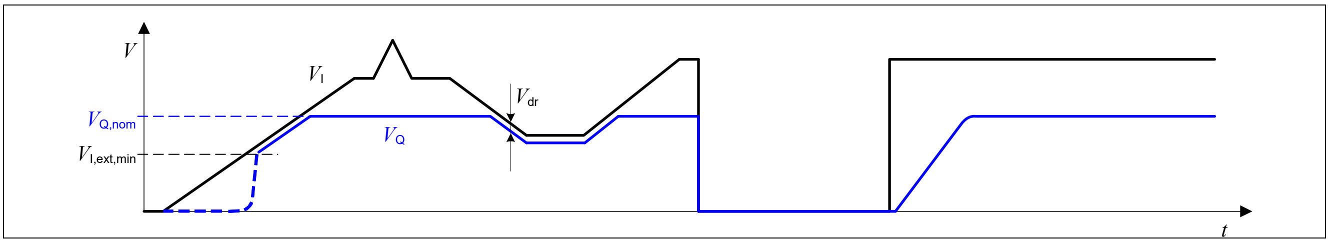


Figure 4 Output voltage versus input voltage

Table 4 Electrical characteristics voltage regulator

T_j = -40°C to 150°C, V_I = 13.5 V, all voltages with respect to ground (unless otherwise specified)
Typical values are given at T_j = 25°C

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
5 V output voltage							
Output voltage accuracy	V_Q	4.9	5.0	5.1	V	0.05 mA ≤ I_Q ≤ 200 mA 5.5 V ≤ V_I ≤ 28 V SEL connected to Q	P_4.1.1
Output voltage accuracy	V_Q	4.9	5.0	5.1	V	0.05 mA ≤ I_Q ≤ 100 mA 5.3 V ≤ V_I ≤ 40 V SEL connected to Q	P_4.1.2
Dropout voltage $V_{dr} = V_I - V_Q$	V_{dr}	–	200	400	mV	1) I_Q = 200 mA, SEL connected to Q	P_4.1.9
Dropout voltage $V_{dr} = V_I - V_Q$	V_{dr}	–	100	200	mV	1) I_Q = 100 mA, SEL connected to Q	P_4.1.10
Power Supply Ripple Rejection	*PSRR*	–	60	–	dB	2) f_{ripple} = 100 Hz V_{ripple} = 0.5 V_{pp} I_Q = 10 mA SEL connected to Q	P_4.1.11
3.3 V output voltage							
Output voltage accuracy	V_Q	3.23	3.3	3.37	V	0.05 mA ≤ I_Q ≤ 200 mA 3.85 V ≤ V_I ≤ 28 V SEL connected to GND	P_4.1.13
Output voltage accuracy	V_Q	3.23	3.3	3.37	V	0.05 mA ≤ I_Q ≤ 100 mA 3.61 V ≤ V_I ≤ 40 V SEL connected to GND	P_4.1.14
Dropout voltage $V_{dr} = V_I - V_Q$	V_{dr}	–	240	480	mV	1) I_Q = 200 mA, SEL connected to GND	P_4.1.21
Dropout voltage $V_{dr} = V_I - V_Q$	V_{dr}	–	120	240	mV	1) I_Q = 100 mA, SEL connected to GND	P_4.1.22
Power Supply Ripple Rejection	*PSRR*	–	63	–	dB	2) f_{ripple} = 100 Hz V_{ripple} = 0.5 V_{pp} I_Q= 10 mA SEL connected to GND	P_4.1.23
Other electrical characteristics							
Output current limitation	$I_{Q,max}$	201	350	550	mA	0 V < V_Q < $V_{Q,nom}$ - 0.1 V	P_4.1.25
Load regulation steady-state	$\Delta V_{Q,load}$	-15	-5	–	mV	I_Q = 0.05 mA to 200 mA V_I = 6.5 V	P_4.1.31
Line regulation steady-state	$\Delta V_{Q,line}$	–	1	10	mV	V_I = 8 V to 32 V I_Q = 5 mA	P_4.1.32

Table 4 Electrical characteristics voltage regulator (cont'd)

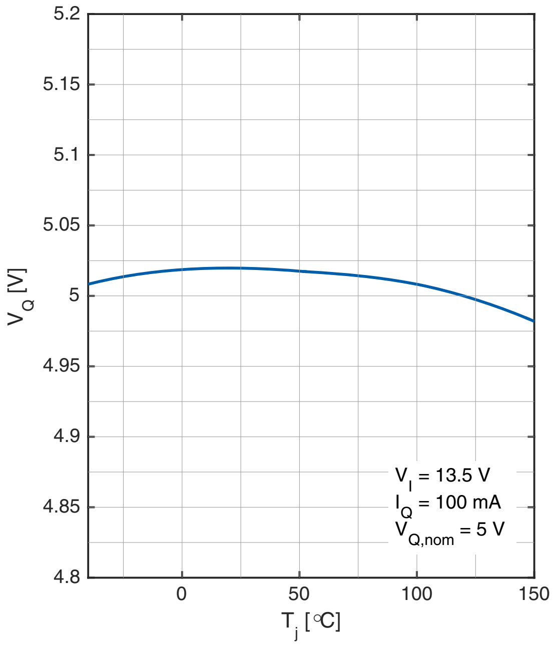
T_j = -40°C to 150°C, V_I = 13.5 V, all voltages with respect to ground (unless otherwise specified)
Typical values are given at T_j = 25°C

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Overtemperature shutdown threshold	$T_{j,sd}$	151	175	200	°C	[2] T_j increasing	P_4.1.33
Overtemperature shutdown threshold hysteresis	$T_{j,sdh}$	–	15	–	K	[2] T_j decreasing	P_4.1.34

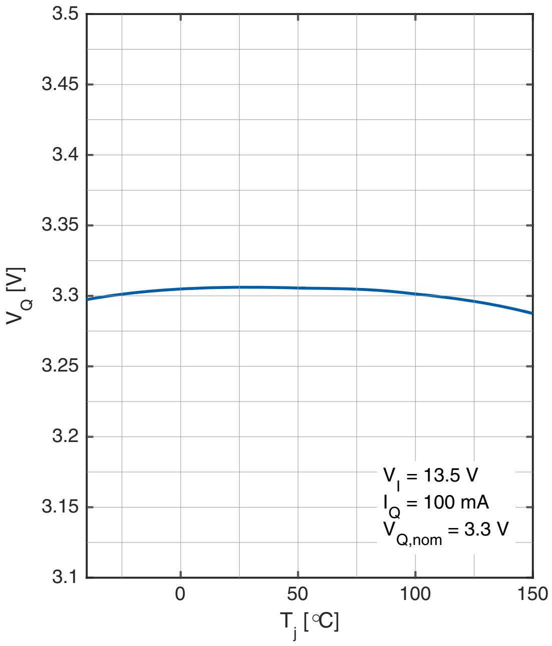
1) Measured when the output voltage V_Q drops by 100 mV during gradual decrease of input voltage.
2) Not subject to production test, specified by design.

4.2 Typical performance characteristics voltage regulator

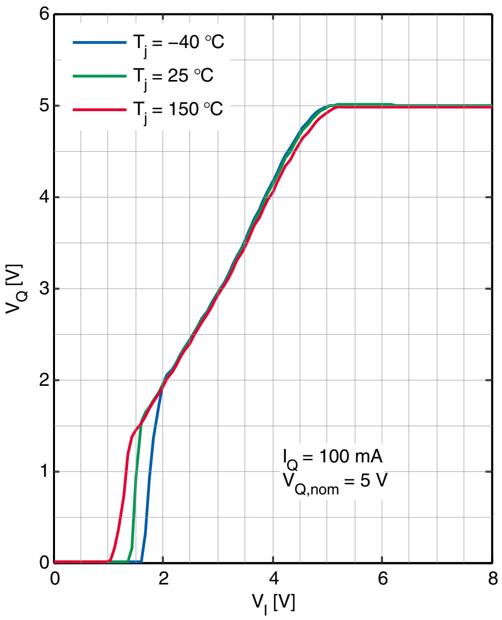
Output voltage V_Q versus junction temperature T_j



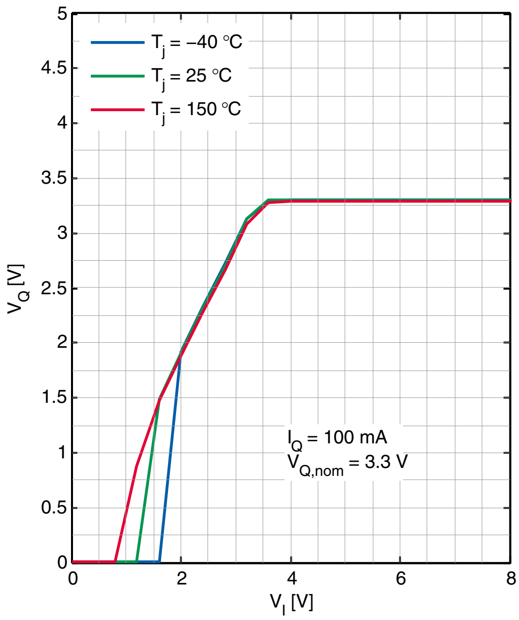
Output voltage V_Q versus junction temperature T_j



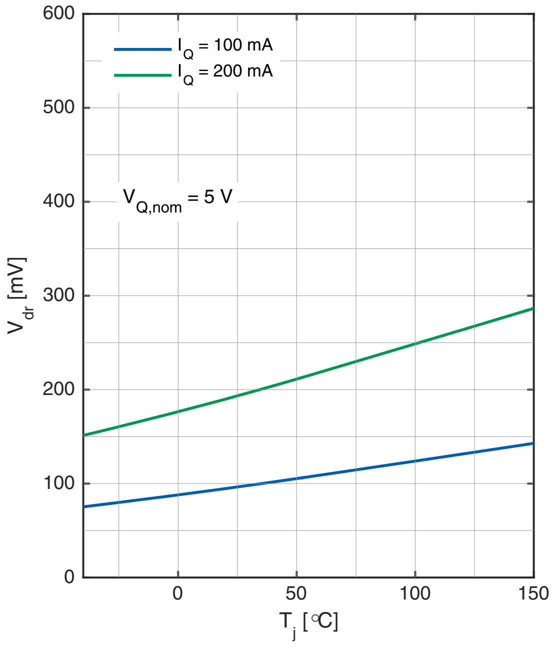
Output Voltage V_Q versus Input Voltage V_I



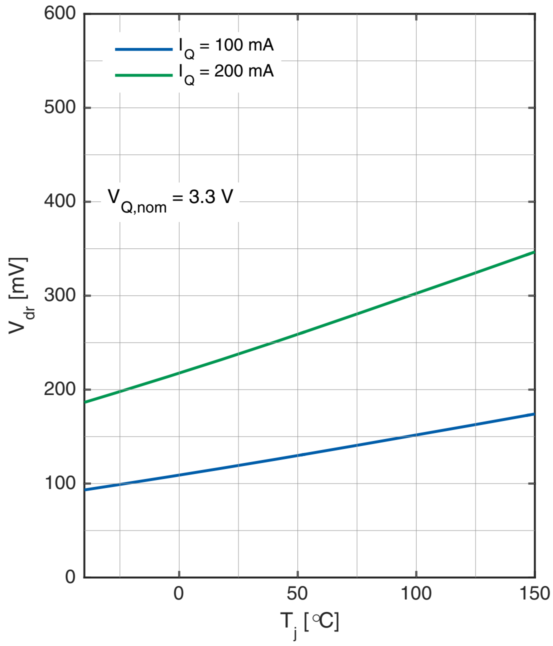
Output Voltage V_Q versus Input Voltage V_I



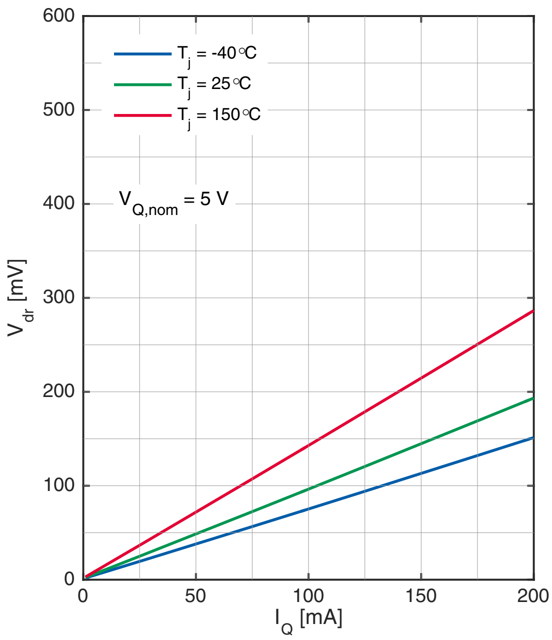
Dropout voltage V_{dr} versus junction temperature T_j



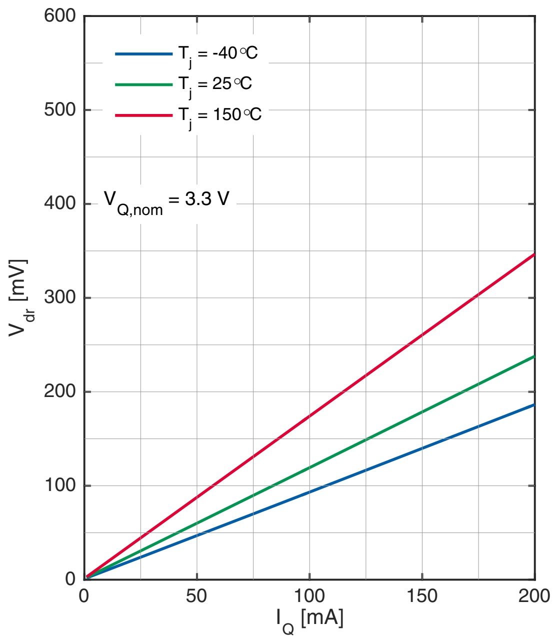
Dropout voltage V_{dr} versus junction temperature T_j



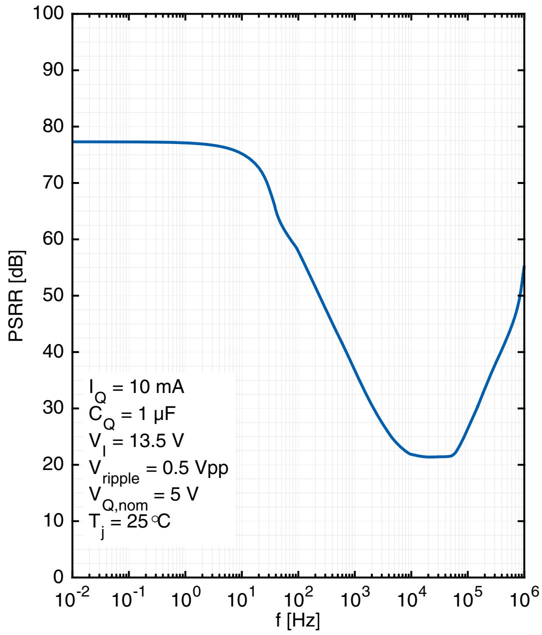
Dropout voltage V_{dr} versus Output Current I_Q



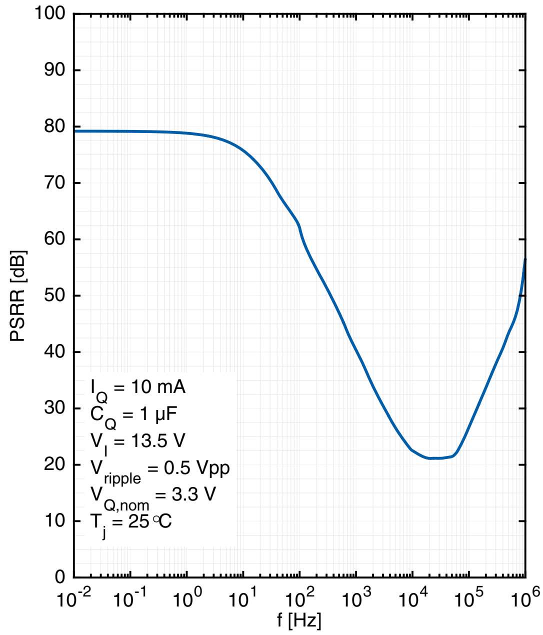
Dropout voltage V_{dr} versus Output Current I_Q



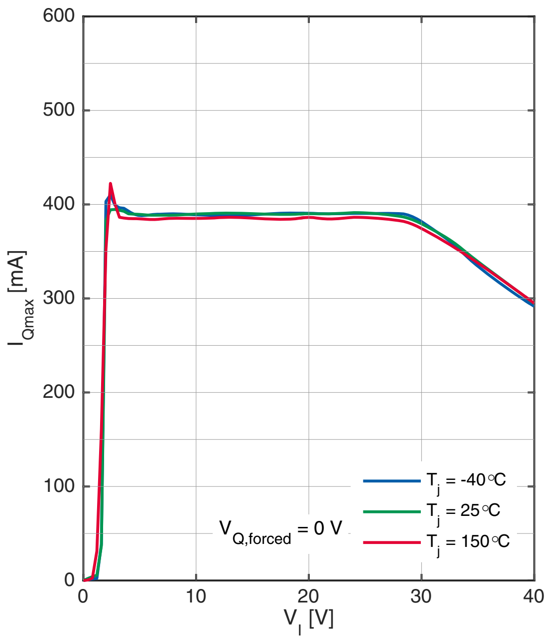
Power Supply Ripple Rejection *PSRR* versus ripple frequency *f*



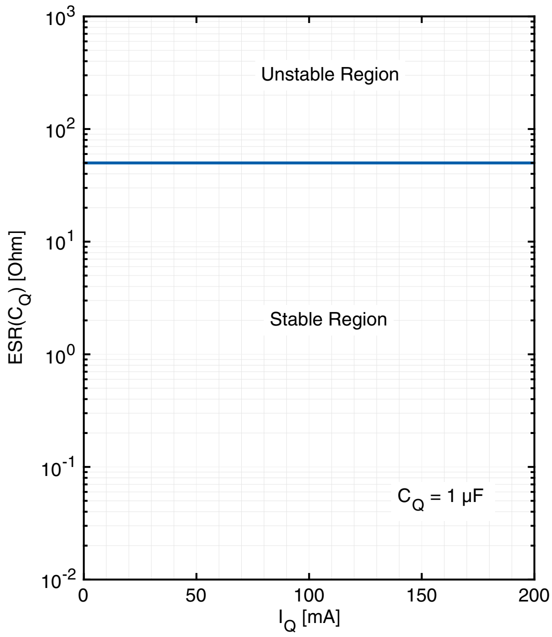
Power Supply Ripple Rejection *PSRR* versus ripple frequency *f*



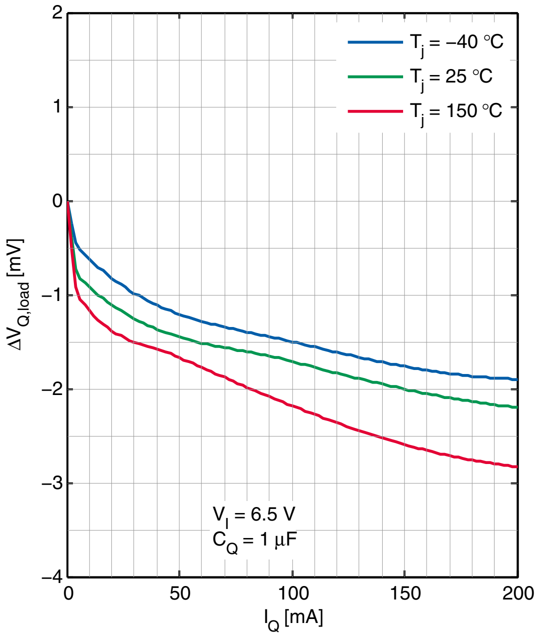
Maximum output current I_Q versus input voltage V_I



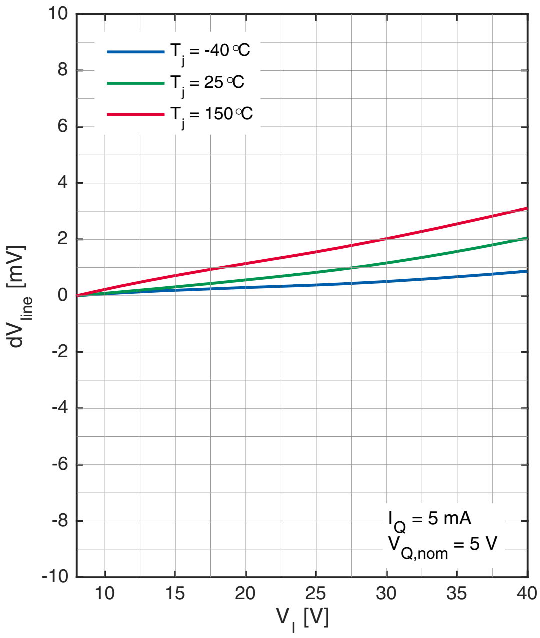
Equivalent Series Resistance of output capacitor $ESR(C_Q)$ versus output current I_Q



Load regulation $\Delta V_{Q,load}$ versus output current change I_Q



Line regulation $\Delta V_{Q,line}$ versus input voltage V_I



4.3 Current consumption

Table 5 Electrical characteristics current consumption

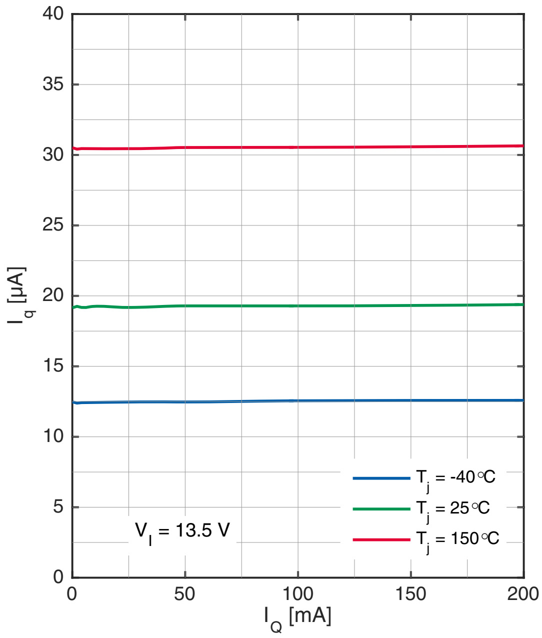
T_j = -40°C to 150°C, V_I = 13.5 V (unless otherwise specified)
Typical values are given at T_j = 25°C

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Current consumption $I_q = I_I$	$I_{q,off}$	–	–	1	µA	V_{EN}= 0 V; T_j < 105°C	P_4.7.1
Current consumption $I_q = I_I$	$I_{q,off}$	–	–	2	µA	V_{EN} = 0.4 V; T_j < 125°C	P_4.7.3
Current consumption $I_q = I_I - I_Q$	I_q	–	20	30	µA	I_Q = 0.05 mA T_j = 25°C	P_4.7.4
Current consumption $I_q = I_I - I_Q$	I_q	–	23	36	µA	I_Q = 0.05 mA T_j < 125°C	P_4.7.5
Current consumption $I_q = I_I - I_Q$	I_q	–	25	42	µA	[1] I_Q = 200 mA T_j < 125°C	P_4.7.6

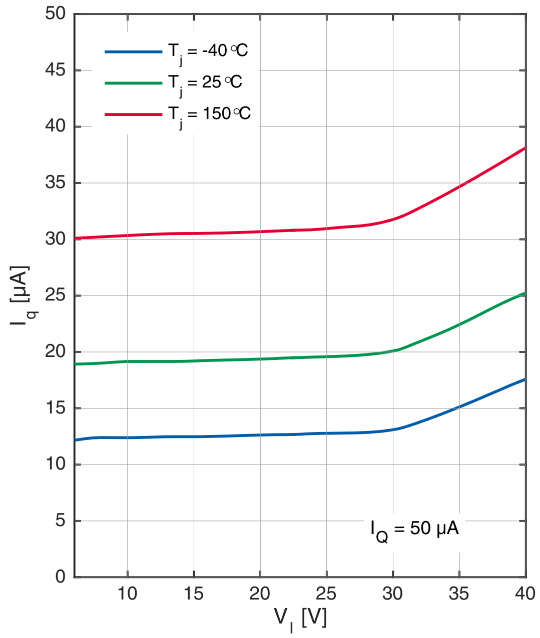
1) Not subject to production test, specified by design

4.4 Typical performance characteristics current consumption

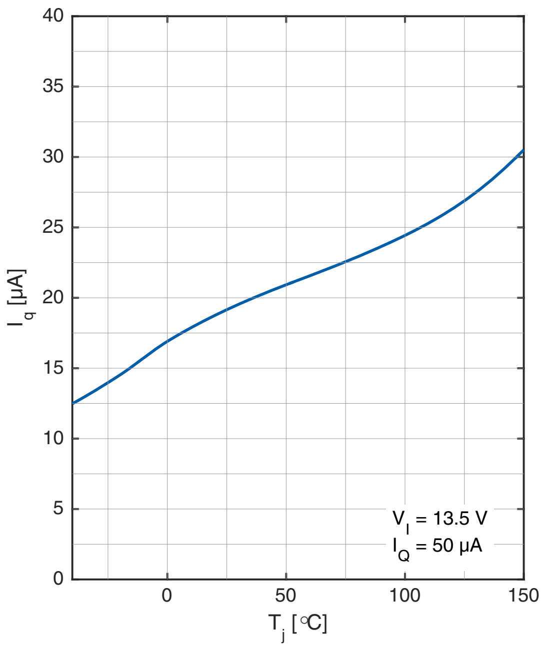
Current consumption I_q versus output current I_Q



Current consumption I_q versus input voltage V_I



Current consumption I_q versus junction temperature T_j



4.5 Enable

The TLS820D2ELVSE can be switched on and off by the enable feature. Applying a “high” level as specified below with V_{EN} ≥ 2 V to the EN pin enables the device. Applying a “low” level as specified below with V_{EN} ≤ 0.8 V shuts down the device. The enable feature has a built-in hysteresis to avoid toggling between the ON/OFF state, when a signal with slow slope is applied to the EN pin.

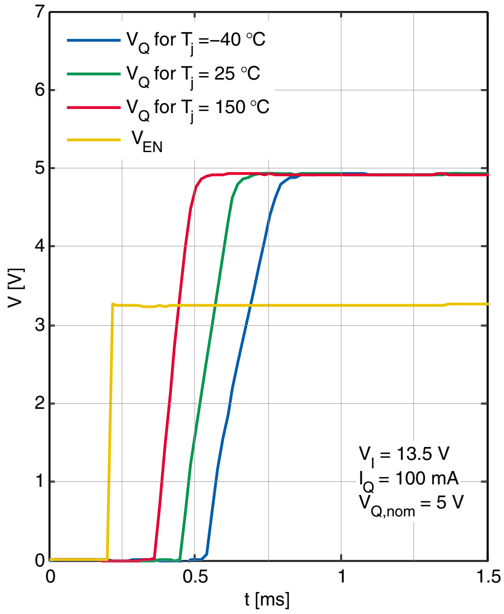
Table 6 Electrical characteristics enable

T_j = -40°C to 150°C, V_I = 13.5 V, all voltages with respect to ground (unless otherwise specified)
Typical values are given at T_j = 25°C

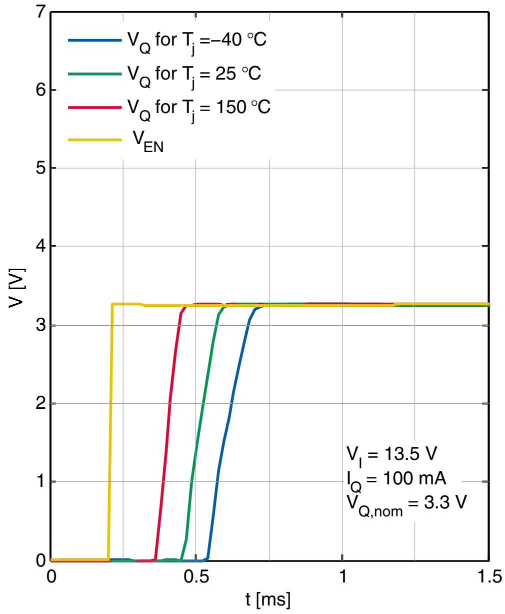
Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Enable “high” input voltage	$V_{EN,H}$	2	–	–	V	–	P_4.14.1
Enable “low” input voltage	$V_{EN,L}$	–	–	0.8	V	–	P_4.14.2
Enable threshold hysteresis	$V_{EN,Hy}$	90	–	–	mV	–	P_4.14.3
Enable “high” input current	$I_{EN,H}$	–	–	1	µA	V_{EN} = 5 V	P_4.14.4
Enable “high” input current	$I_{EN,H}$	–	–	6	µA	V_{EN} ≤ 18 V	P_4.14.5
Enable internal pull-down resistor	R_{EN}	2.8	10	20	MΩ	–	P_4.14.6

4.6 Typical performance characteristics enable

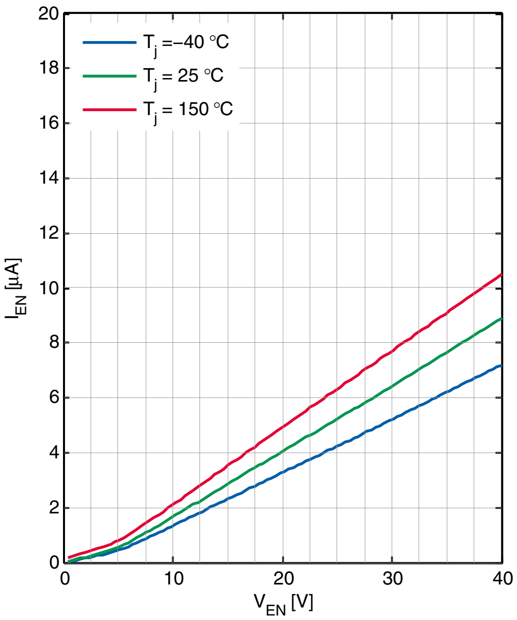
Output voltage V_Q versus time t (EN switched on)



Output voltage V_Q versus time t (EN switched on)



Enable input current I_{EN} versus Enable input voltage V_{EN}



4.7 Output voltage selection

The output voltage V_Q of TLS820D2ELVSE can be selected by the SEL pin:
SEL pin connected to Q: V_Q = 5 V;
SEL pin connected to GND: V_Q = 3.3 V.

4.8 Reset function

The reset function monitors the output voltage V_Q and indicates a potential imminent loss of power. This then allows enough time for the system to shut down or do the transition into a safe state. To meet the requirements of the application, some reset parameters can be adjusted by measures described below.

Output undervoltage reset

The reset output RO is an open collector stage. It is internally pulled up to V_Q via a resistor **Reset output internal pull-up resistor** (**Table 7**). In case of an undervoltage event at V_Q, RO is pulled to "low". This signal can then be used to reset a microcontroller during low supply voltage.

Optional reset output pull-up resistor $R_{RO,ext}$

Although the reset output RO is an open collector output with an integrated pull-up resistor, an additional external pull-up resistor can be added to the output Q, if needed. **Table 7** specifies a minimum value for the external resistor $R_{RO,ext}$ for this option.

Power-on reset delay time

The power-on reset delay time t_{rd} allows a microcontroller and oscillator to start up. This delay time is the time interval from exceeding the reset switching threshold $V_{RT,high}$ until the reset is released by switching the reset output RO from "low" to "high". The power-on reset delay time t_{rd} is defined by an external delay capacitor C_D connected to pin D. The delay capacitor charge current $I_{D,ch}$ charges C_D by starting from V_D = 0 V.

If the application requires a power-on reset delay time t_{rd} that differs from the default value specified in **Table 7**, then the required value of the delay capacitor can be derived from the specified value and the desired power-on delay time as follows:

$$C_D = \frac{t_{rd}}{t_{rd,100\,nF}} \cdot C_{D,100\,nF} \tag{4.1}$$

where

- C_D: required capacitance of the delay capacitor
- t_{rd}: desired power-on reset delay time
- $t_{rd,100\ nF}$: **Power-on reset delay time** (**Table 7**) for C_D = 100 nF as specified in the data sheet

For a precise calculation, the tolerance of the delay capacitor must also be considered.

Reset reaction time

The reset reaction time ensures that short undervoltage spikes do not trigger an unwanted reset "low" signal. The reset reaction time $t_{rr,total}$ comprises the internal reaction time $t_{rr,int}$ and the discharge time $t_{rr,d}$ defined by the external delay capacitor C_D. Therefore, the total reset reaction time becomes:

$$t_{rr,total} = t_{rr,int} + t_{rr,d} \tag{4.2}$$

where

- $t_{rr,total}$: **Reset reaction time**
- $t_{rr,int}$: **Internal reset reaction time**
- $t_{rr,d}$: **Delay capacitor discharge time**

Reset adjust function

To select the default switching threshold as specified in **Table 7** under $V_{RT,low}$ connect the RADJ pin to GND.

To adjust the undervoltage reset lower switching threshold according to the requirements of the application, an external voltage divider (R_{ADJ1}, R_{ADJ2}) is required at pin RADJ. In this case, it should be considered that the resistors of the voltage divider dissipate additional current.

With a voltage divider connected, the adjusted undervoltage reset lower switching threshold $V_{RT,low,new}$ can be calculated according to the following equation:

$$V_{RT,low,new} = V_{RADJ,th}\left(\frac{R_{ADJ1}}{R_{ADJ2}} + 1\right) \tag{4.3}$$

where

- $V_{RT,low,new}$: the desired new undervoltage reset switching lower threshold
- R_{ADJ1}, R_{ADJ2}: resistors of the external voltage divider
- $V_{RADJ,th}$: reset adjustment switching threshold given in **Table 7**

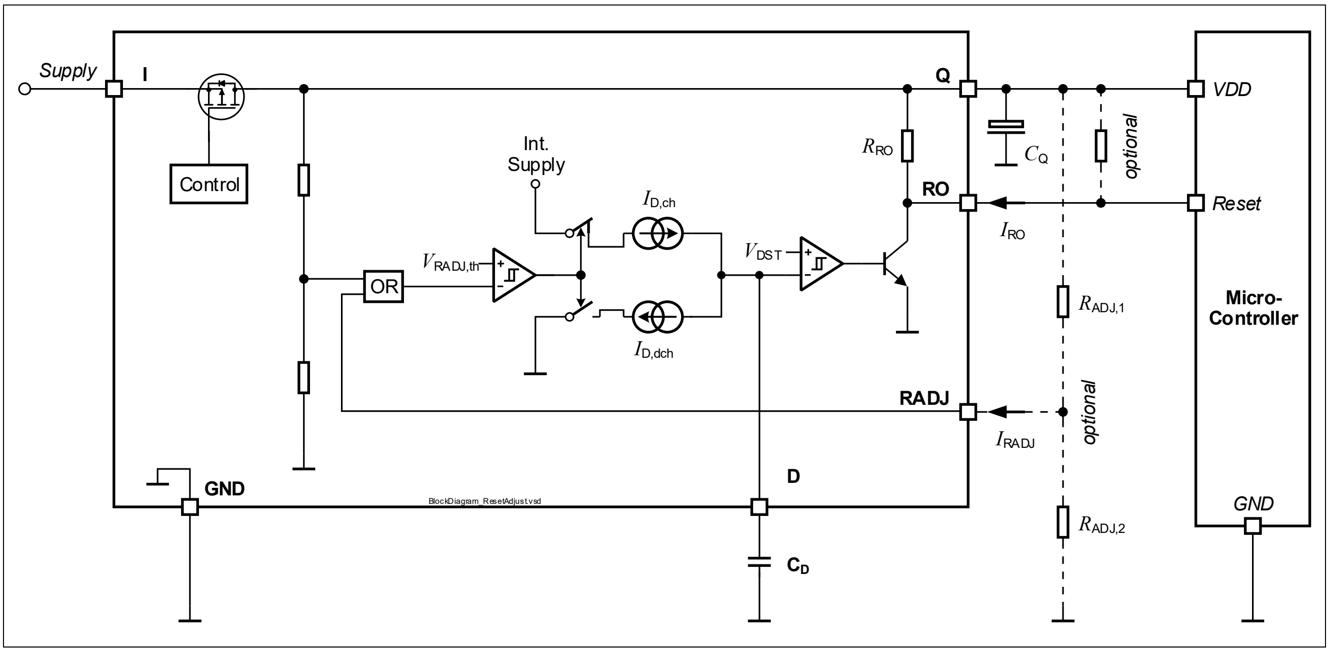


Figure 5 Block diagram reset function

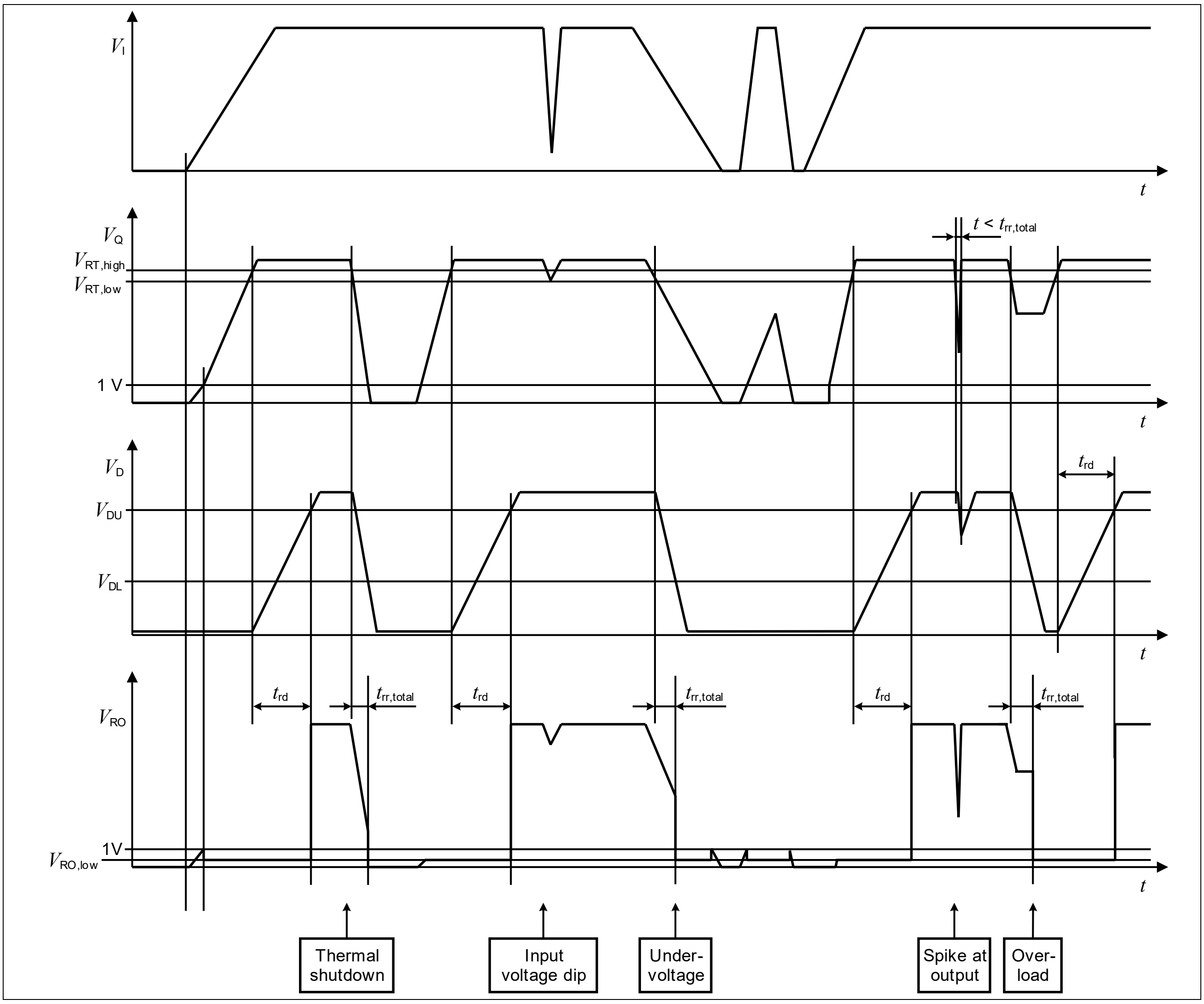


Figure 6 Timing diagram reset

Table 7 Electrical characteristics reset

T_j = -40°C to 150°C, V_I = 13.5 V, all voltages with respect to ground (unless otherwise specified).
Typical values are given at T_j = 25°C, V_I = 13.5 V.

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Output undervoltage reset (5 V output voltage)							
Output undervoltage reset upper switching threshold	$V_{RT,high}$	4.55	4.70	4.85	V	V_Q increasing, *V_{EN} ≥ 2.0 V, RADJ connected to GND*, SEL connected to Q	P_4.19.1
Output undervoltage reset lower switching threshold	$V_{RT,low}$	4.45	4.60	4.75	V	V_Q decreasing, *V_{EN} ≥ 2.0 V, RADJ connected to GND*, SEL connected to Q	P_4.19.2

Table 7 Electrical characteristics reset (cont'd)

T_j = -40°C to 150°C, V_I = 13.5 V, all voltages with respect to ground (unless otherwise specified).
Typical values are given at T_j = 25°C, V_I = 13.5 V.

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Reset adjustment switching threshold	$V_{RADJ,th}$	0.85	0.9	0.95	V	SEL connected to Q	P_4.19.4
Reset threshold adjustment range	$V_{RT,range}$	2	–	4.2	V	SEL connected to Q	P_4.19.5
Output undervoltage reset (3.3 V output voltage)							
Output undervoltage reset upper switching threshold	$V_{RT,high}$	3.00	3.10	3.20	V	V_Q increasing, $V_{EN} \geq 2.0$ *V, RADJ connected to GND*, SEL connected to GND	P_4.19.6
Output undervoltage reset lower switching threshold	$V_{RT,low}$	2.93	3.03	3.13	V	V_Q decreasing, $V_{EN} \geq 2.0$ V, RADJ connected to GND, SEL connected to GND	P_4.19.7
Reset adjustment switching threshold	$V_{RADJ,th}$	0.85	0.9	0.95	V	SEL connected to GND	P_4.19.9
Reset threshold adjustment range	$V_{RT,range}$	2	–	2.75	V	SEL connected to GND	P_4.19.10
Reset output RO							
Reset output "low" voltage	$V_{RO,low}$	–	0.2	0.4	V	$1 V \leq V_Q \leq V_{RT}$; $R_{RO} > 4.7$ kΩ	P_4.19.11
Reset output internal pull-up resistor	$R_{RO,int}$	13	20	36	kΩ	internally connected to Q	P_4.19.12
Reset output external pull-up resistor to V_Q	$R_{RO,ext}$	4.7	–	–	kΩ	$1 V \leq V_Q \leq V_{RT}$; $V_{RO} \leq 0.4$ V	P_4.19.13
Reset delay timing							
Power-on reset delay time	t_{rd}	17	25	37	ms	C_D = 100 nF Calculated value	P_4.19.15
Upper delay switching threshold	V_{DU}	–	0.9	–	V	–	P_4.19.16
Lower delay switching threshold	V_{DL}	–	0.6	–	V	–	P_4.19.17
Delay capacitor charge current	$I_{D,ch}$	–	3.6	–	µA	V_D = 1 V	P_4.19.18
Delay capacitor discharge current	$I_{D,dch}$	–	210	–	mA	V_D = 1 V	P_4.19.19
Delay capacitor discharge time	$t_{rr,d}$	–	2	6	µs	C_D = 100 nF Calculated value	P_4.19.20

Table 7 Electrical characteristics reset (cont'd)

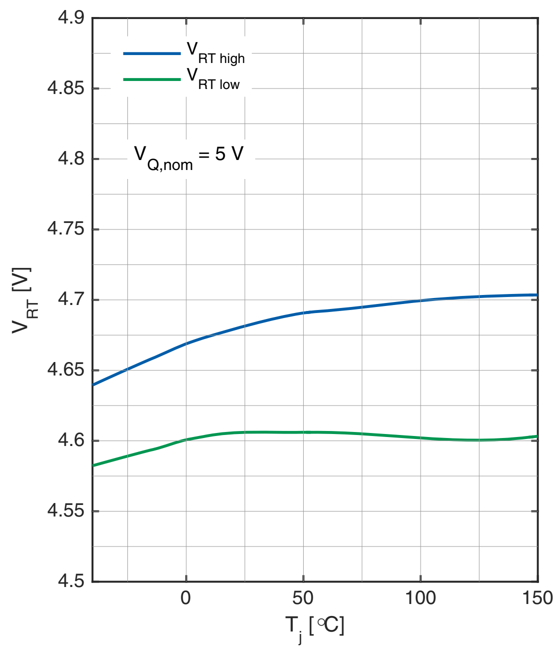
T_j = -40°C to 150°C, V_I = 13.5 V, all voltages with respect to ground (unless otherwise specified).
Typical values are given at T_j = 25°C, V_I = 13.5 V.

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Internal reset reaction time	$t_{rr,int}$	–	15	44	µs	1) C_D = 0 nF	P_4.19.21
Reset reaction time	$t_{rr,total}$	–	17	50	µs	C_D = 100 nF Calculated value	P_4.19.22

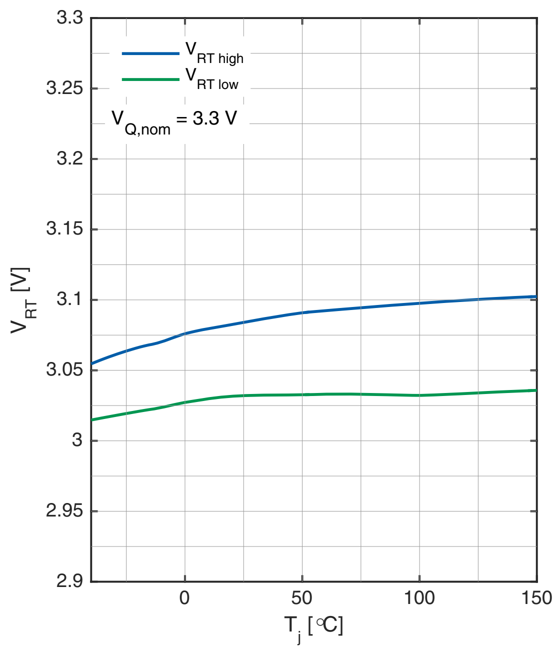
1) Parameter not subject to production test; specified by design.

4.9 Typical performance characteristics reset

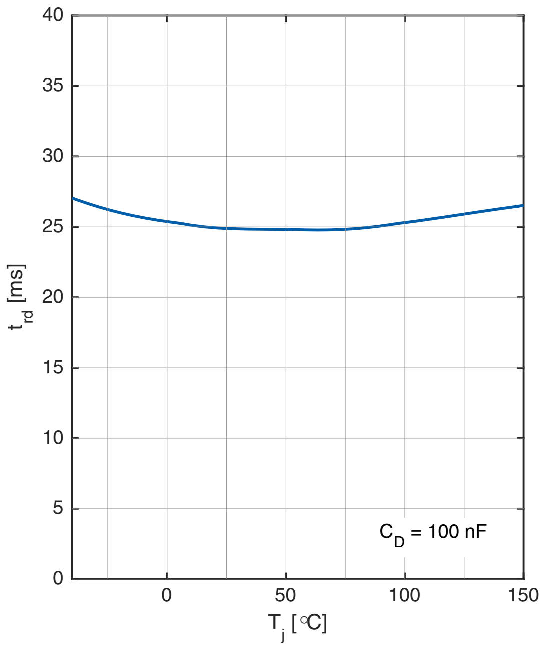
Undervoltage reset threshold V_{RT} versus junction temperature T_j



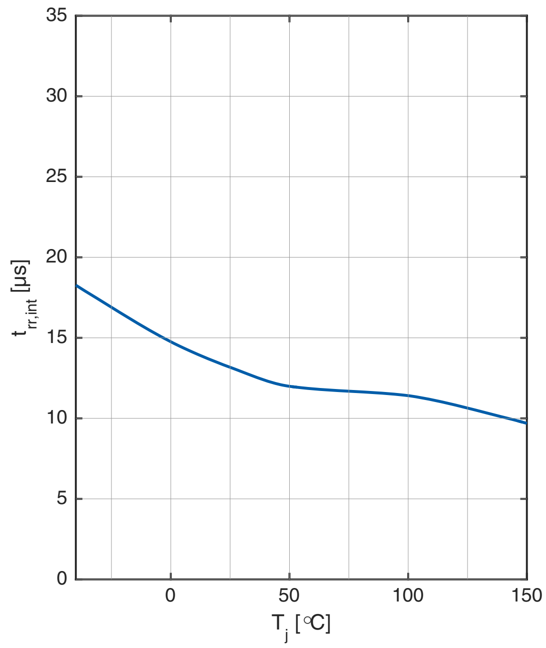
Undervoltage reset threshold V_{RT} versus junction temperature T_j



Power-on reset delay time t_{rd} versus junction temperature T_j



Internal Reset reaction time $t_{rr,int}$ versus junction temperature T_j



5 Application information

5.1 Application diagram

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

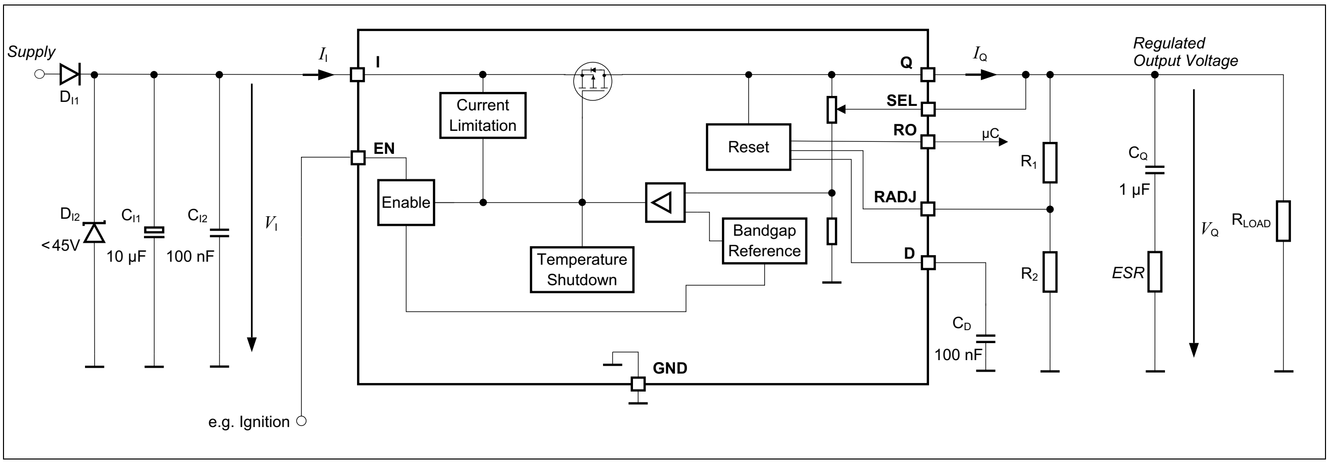


Figure 7 Application diagram

Note: This is a very simplified example of an application circuit. The function must be verified in the real application.

5.2 Selection of external components

5.2.1 Input pin

Figure 7 shows an example of the input circuitry for a linear voltage regulator. A ceramic capacitor at the input, in the range of 100 nF to 470 nF, is recommended to filter out the high frequency disturbances imposed by the line, for example ISO pulses 3a/b. This capacitor must be placed very close to the input pin of the linear voltage regulator on the PCB.

An aluminum electrolytic capacitor in the range of 10 µF to 470 µF is recommended as an input buffer to smooth out high energy pulses, such as ISO pulse 2a. This capacitor must be placed close to the input pin of the linear voltage regulator.

An overvoltage suppressor diode can be used to further suppress any high voltage beyond the maximum rating of the linear voltage regulator and to protect the device from damage due to overvoltage.

The external components at the input pin are optional, but they are recommended to deal with possible external disturbances.

5.2.2 Output pin

An output capacitor is mandatory for the stability of linear voltage regulators. Furthermore it serves as an energy buffer during load jumps, to compensate and maintain a constant output voltage potential. It must be dimensioned according to the specific requirements of the application. The requirements for the output capacitor are given in **"Functional range" on Page 8**.

The TLS820D2ELVSE is designed to be stable with low ESR capacitors as well. According to automotive requirements, ceramic capacitors with X5R or X7R dielectrics are recommended.

The output capacitor should be placed as close as possible to the voltage regulator's output pin and GND pin and on the same side of the PCB as the regulator itself.

In case of transients of input voltage or load current, the capacitance should be dimensioned accordingly. The configuration must be verified in the real application to ensure that the output stability requirements are fulfilled.

5.3 Thermal considerations

From the known input voltage, the output voltage and the load profile of the application, the total power dissipation can be calculated as follow:

$$P_D = (V_I - V_Q)I_Q + V_I I_q \tag{5.1}$$

with

- P_D: continuous power dissipation
- V_I: input voltage
- V_Q: output voltage
- I_Q: output current
- I_q: quiescent current

The maximum acceptable thermal resistance R_{thJA} is given by:

$$R_{thJA} = \frac{T_{j,max} - T_a}{P_D} \tag{5.2}$$

with

- $T_{j,max}$: maximum allowed junction temperature
- T_a: ambient temperature

Based on the above calculation the proper PCB type and the necessary heat sink area can be determined by referencing to the specification for **"Thermal resistance" on Page 9**.

5.4 Reverse polarity protection

The TLS820D2ELVSE is not protected against reverse polarity faults and must be protected by external components against negative supply voltage. An external reverse polarity diode is necessary. The absolute maximum ratings of the device as specified in **"Absolute maximum ratings" on Page 7** must be maintained.

5.5 Further application information

For further information you may contact **http://www.infineon.com/**

6 Package information

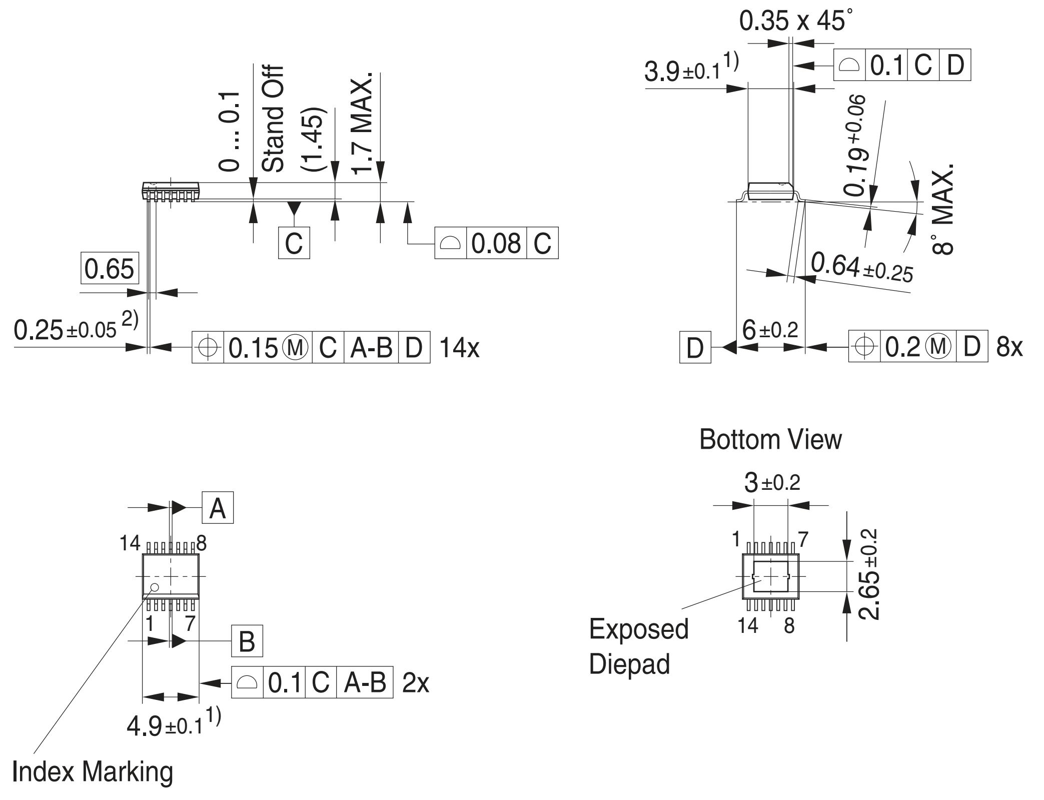


Figure 8 PG-SSOP-14[1)]

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

Further information on packages

https://www.infineon.com/packages

1) Dimensions in mm

7 Revision history

Revision	Date	Changes
1.0	2020-07-27	Initial version

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