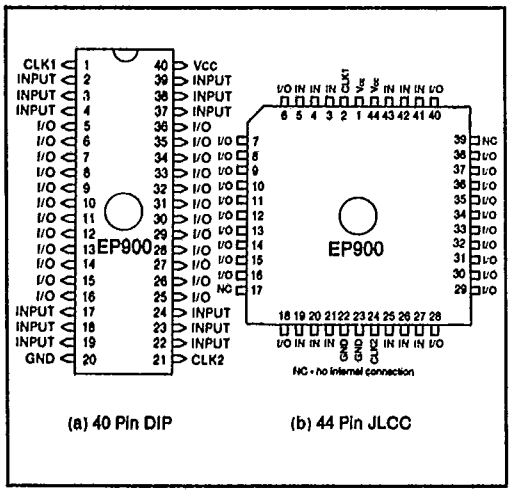
ALTERA 24-MACROCELL EPLD EP900

FEATURES

- High density logic replacement for TTL and 74HC.
- Functional and pin compatible with the Altera EP910.
- High speed, tpd = 45 ns.
- Asynchronous clocking of all registers or banked register operation from 2 synchronous clocks.
- 24 Macrocells with configurable I/O architecture allowing 36 inputs and 24 outputs.
- "Zero Power" (typically 20μA standby).
- Programmable registers providing D,T,SR or JK flipflops with individual Asynchronous Clear control.
- 100% generically testable—provides 100% programming yield.
- Programmable "Security Bit" allows total protection of proprietary designs.
- Package options include both a 40 pin, 600 mil DIP and a 44 pin J-leaded chip carrier
- Full software support featuring Schematic Capture, Netlist, Boolean Equation and State Machine design entry methods.

CONNECTION DIAGRAM



(a) 40 Pin DIP (b) 44 Pin JLCC

GENERAL DESCRIPTION

The Altera EP900 is a pin-compatible version of the popular EP910 Erasable Programmable Logic Device (EPLD). Available in 40-pin DIP and 44-pin J-leaded chip carrier packages, the EP900 contains 24 Macrocells with user-configurable I/O architecture, allowing up to 36 inputs and 24 outputs.

Each of the 24 Macrocells contains a programmable AND and fixed OR PLA structure, see Figure 1, with a maximum eight product terms for logic implementation. In addition, single product terms control Output Enable/Asynchronous Clock and Asynchronous Clear functions.

The Altera proprietary programmable I/O architecture allows the EP900 user to program output and feedback paths for both combinatorial or registered operation, active high or active low.

For increased flexibility, the EP900 also includes programmable registers. Each of the 24 internal registers may be programmed to be D, T, SR or JK flipflop. In addition, each register may be clocked asynchronously on an individual basis or synchronously on a banked register basis.

For proper operation, standard high performance design practices should be followed. It is recommended that opaque labels be placed over device window. Input and output pins must be constrained to the range GND ≤ (V_{IN} or V_{OUT}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic level (e.g. either V_{CC} or GND). Each set of V_{CC} and GND pins must be shorted together directly at the device. Power supply decoupling capacitors of at least .2μF must be connected between each V_{CC} pin and GND. For the most effective decoupling, connect one capacitor between each set of V_{CC} and GND pins, directly at the device.

Programming the EP900 is accomplished by using the Altera A+PLUS PC-based development software which supports schematic capture, netlist, state machine and Boolean equation design entry methods. Once the design is entered, A+PLUS automatically performs translation into logical equations, Boolean minimization, and design fitting directly to an EP900. The device may then be programmed to achieve customized working silicon within minutes at the designer's own desktop.

For full EP900 functional description please consult the EP910 datasheet.

REV 4.0

ABSOLUTE MAXIMUM RATINGS

COMMERCIAL, INDUSTRIAL, MILITARY OPERATING RANGES

Note: See Design Recommendations

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{CC}	Supply voltage	With respect to GND note (3)	-2.0	7.0	V
V_{PP}	Programming supply voltage		-2.0	13.5	V
V_I	DC INPUT voltage		-2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current		-150	+150	mA
I_{OUT}	DC OUTPUT current, per pin		-25	+25	mA
P_D	Power dissipation			750	mW
T_{STG}	Storage temperature	No bias	-65	+150	°C
T_{AMB}	Ambient temperature	Under bias	-65	+135	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{CC}	Supply Voltage	note (6)	4.75 (4.5)	5.25 (5.5)	V
V_I	INPUT voltage		0	V_{CC}	V
V_O	OUTPUT voltage		0	V_{CC}	V
T_A	Operating temperature	For Commercial	0	70	°C
T_A	Operating temperature	For Industrial	-40	85	°C
T_C	Case temperature	For Military	-55	125	°C
T_R	INPUT rise time	note (9)		500	ns
T_F	INPUT fall time	note (9)		500	ns

DC OPERATING CHARACTERISTICS

(V_{CC} = 5V ±5%, T_A = 0°C to 70°C for Commercial)
(V_{CC} = 5V ± 10%, T_A = -40°C to 85°C for Industrial)
(V_{CC} = 5V ±10%, T_C = -55°C to 125°C for Military)*
Note (1) and (6)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	HIGH level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	LOW level input voltage		-0.3		0.8	V
V_{OH}	HIGH level TTL output voltage	I_{OH} = -4mA DC	2.4			V
V_{OH}	HIGH level CMOS output voltage	I_{OH} = -2mA DC	3.84			V
V_{OL}	LOW level output voltage	I_{OL} = 4mA DC			0.45	V
I_I	Input leakage current	V_I = V_{CC} or GND	-10		+10	μA
I_{OZ}	3-state output off-state current	V_O = V_{CC} or GND	-10		+10	μA
I_{CC1}	V_{CC} supply current (standby)	V_I = V_{CC} or GND No load note (8)		35	150	μA
I_{CC2}	V_{CC} supply current (non-turbo)	V_I = V_{CC} or GND No load, f = 1.0 MHz note (7)		5	15 (25)	mA
I_{CC3}	V_{CC} supply current (turbo)	V_I = V_{CC} or GND No load, f = 1.0 MHz note (7)		45	75 (100)	mA

CAPACITANCE

Note (4)

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V f = 1.0 MHz		20	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V f = 1.0 MHz		20	pF
C_{CLK}	Clock Pin Capacitance	V_{IN} = 0V f = 1.0 MHz		20	pF

AC CHARACTERISTICS

EP900, EP900-2, EP900-3

T-46-13-47

(V_{CC} = 5V ± 5%, T_A = 0°C to 70°C for Commercial)
(V_{CC} = 5V ± 10%, T_A = -40°C to 85°C for Industrial)
(V_{CC} = 5V ± 10%, T_C = -55°C to 125°C for Military)*

SYMBOL	PARAMETER	CONDITIONS	EP900-2 MIN	EP900-2 MAX	EP900-3 MIN	EP900-3 MAX	EP900 MIN	EP900 MAX	NON-TURBO ADDER note (5)	UNIT
t_{PD1}	Input to non-registered output	C_1 = 50pF		45		50		55	25	ns
t_{PD2}	I/O input to non-registered output			50		55		60	25	ns
t_{PZX}	Input or I/O input to output enable			50		55		60	25	ns
t_{PXZ}	Input or I/O input to output disable	C_1 = 5pF note (2)		50		55		60	25	ns
t_{CLR}	Asynchronous output clear time	C_1 = 50pF		50		55		60	25	ns
t_{IO}	I/O input buffer delay			5		5		5	0	ns

SYNCHRONOUS CLOCK MODE

SYMBOL	PARAMETER	CONDITIONS	EP900-2 MIN	EP900-2 MAX	EP900-3 MIN	EP900-3 MAX	EP900 MIN	EP900 MAX	NON-TURBO ADDER note (5)	UNIT
f_{MAX}	Maximum frequency		26.3		23.8		21.7		0	MHz
t_{SU}	Input or I/O input setup time		38		42		46		25	ns
t_H	Input or I/O input hold time		0		0		0		0	ns
t_{CH}	Clock high time		17.5		20		23		0	ns
t_{CL}	Clock low time		17.5		20		23		0	ns
t_{CO1}	Clock to output delay			23		25		28	0	ns
t_{CNT}	Minimum clock period (register output feedback to register input - internal path)			50		55		60	0	ns
f_{CNT}	Internal maximum frequency ($1/t_{CNT}$)	note (7)	20.0		18.2		16.7		0	MHz

ASYNCHRONOUS CLOCK MODE

SYMBOL	PARAMETER	CONDITIONS	EP900-2 MIN	EP900-2 MAX	EP900-3 MIN	EP900-3 MAX	EP900 MIN	EP900 MAX	NON-TURBO ADDER note (5)	UNIT
f_{MAX}	Maximum frequency		26.3		23.8		21.7		0	MHz
t_{ASU}	Input or I/O input setup time		13		14		15		25	ns
t_{AH}	Input or I/O input hold time		15		15		15		0	ns
t_{ACH}	Clock high time		17.5		20		23		0	ns
t_{ACL}	Clock low time		17.5		20		23		0	ns
t_{ACO1}	Clock to output delay			48		53		59	25	ns
t_{ACNT}	Minimum clock period (register output feedback to register input - internal path)			50		55		60	0	ns
f_{ACNT}	Internal maximum frequency ($1/t_{ACNT}$)	note (7)	20.0		18.2		16.7		0	MHz

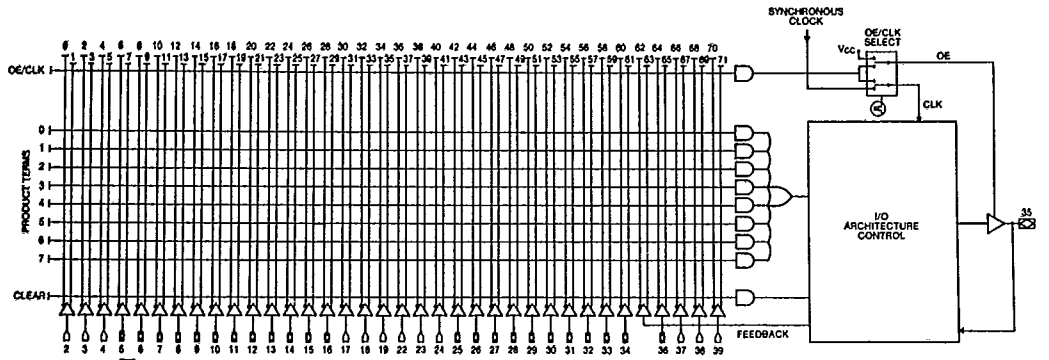
Notes:

1. Typical values are for T_A = 25°C, V_{CC} = 5V
2. Sample tested only for an output change of 500mV.
3. Minimum DC input is -0.3V. During transitions, the inputs may undershoot to -2.0V for periods less than 20ns.
4. Capacitance measured at 25°C. Sample tested only. Clock pin capacitance for dedicated clock inputs only. Pin 21, (high voltage pin during programming), has capacitance of 80 pF max.
5. See TURBO-BIT™, page 29.
6. Figures in ( ) pertain to military and industrial temperature version.
7. Measured with device programmed as a 24 bit counter.
8. EPLD automatically goes into standby mode if logic transitions do not occur when in non-turbo mode (approximately 100 ns after last transition).
9. Clock t_R, t_F = 250ns (100ns).
10. The f_{MAX} values shown represent the highest frequency for pipelined data.

GRADE	AVAILABILITY
Commercial (0°C to 70°C)	EP900-2 EP900-3 EP900
Industrial (-40°C to 85°C)	EP900
Military (-55°C to 125°C)	EP900

* The specifications noted above apply to military operating range devices. MIL-STD-883 compliant product specifications are provided in military product drawings available on request from Altera marketing at 408/984-2805, ext. 101. These military product drawings should be used for the preparation of source control drawings.

Figure 1. Logic Array Macrocell



*Note ⊠ = I/O Pin, In which Logic Array Input is from feedback path.
Pin numbers reflect 40 pin DIP.

Figure 2. I_{CC} vs. F_{MAX}

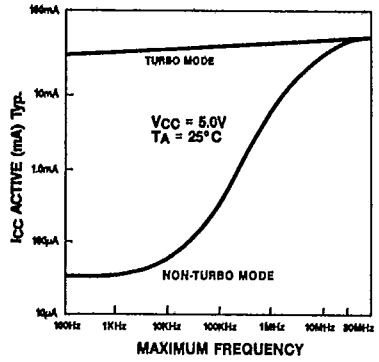


Figure 3. Output Drive Currents