3 kV RMS, Signal and Power Isolated, CAN Transceiver for CAN FD

Enhanced Product

ADM3057E-EP

FEATURES

- 3 kV rms signal and power isolated CAN transceiver
- *iso*Power integrated isolated dc-to-dc converter
- V_{IO} pin for 1.7 V to 5.5 V logic levels
- ISO 11898-2:2016 compliant (CAN FD)
- Data rates up to 12 Mbps for CAN FD
- Low maximum loop propagation delay: 150 ns
- Extended common-mode range (V_{CANx}): ±25 V
- Bus fault protection: ±40 V on CANH and CANL pins
- Low power standby support remote wake request
- Extra isolated signal for control (such as termination switches)
- Passes EN 55022 Class B by 6 dB
- Slope control for reduced EMI
- Safety and regulatory approvals
  - VDE certificate of conformity, VDE V 0884-10 (pending)
    - V_{IORM} = 849 V_{PEAK}
  - UL: 5000 V rms for 1 minute per UL 1577 (pending)
  - CSA Component Acceptance Notice 5A (pending)
    - IEC 60950-1, IEC 61010-1
- Creepage and clearance
  - 7.8 mm minimum with 20-lead SOIC_W
- High common-mode transient immunity: >75 kV/µs

ENHANCED PRODUCT FEATURES

- Supports defense and aerospace applications (AQEC standard)
- Military temperature range: −55°C to +105°C
- Controlled manufacturing baseline
- 1 assembly/test site
- Product change notification
- Qualification data available on request

APPLICATIONS

- CANOpen, DeviceNet, and other CAN bus implementations
- Industrial automation
- Military and aerospace (MILA) avionics for sensors, actuators, and engine control

GENERAL DESCRIPTION

The ADM3057E-EP is a 3 kV rms isolated controller area network (CAN) physical layer transceiver with integrated isolated dc-to-dc converter. The ADM3057E-EP meets flexible data rate (CAN FD) requirements for operation to 5 Mbps and higher and complies with the ISO 11898-2: 2016 standard. The ADM3057E-EP is capable of supporting data rates as high as 12 Mbps.

The device employs Analog Devices, Inc., *i*Coupler® technology to combine a 3-channel isolator, a CAN transceiver, and an Analog Devices *iso*Power® dc-to-dc converter into a single, surface-mount, small outline integrated circuit (SOIC) package. The device is powered by a single 5 V supply, realizing a fully isolated solution for CAN and CAN FD. Radiated emissions from the high frequency switching of the dc-to-dc convertors are kept below EN 55022 Class B limits by continuous adjustments to the switching frequency.

FUNCTIONAL BLOCK DIAGRAM

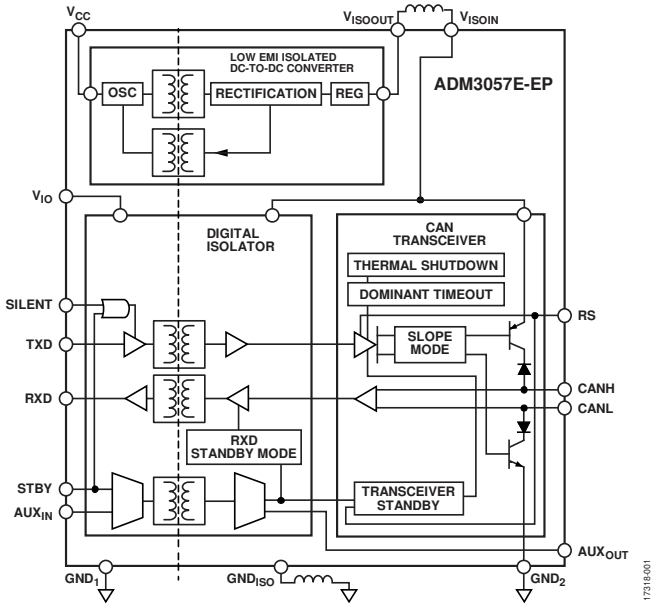

Figure 1.

The ADM3057E-EP provides complete isolation between the CAN controller and physical layer bus. Safety and regulatory approvals (pending) for 3 kV rms isolation voltage, 10 kV surge test, and 7.8 mm creepage and clearance ensure the ADM3057E-EP meets application reinforced isolation requirements.

Low propagation delays through the isolation support longer bus cables. Slope control mode is available for standard CAN at low data rates. Standby mode minimizes power consumption when the bus is idle or if the node goes offline. Silent mode allows the TXD input to be ignored for listen only mode.

Dominant timeout functionality protects against bus lockup in a fault condition. The current limiting and thermal shutdown features protect against output short circuits. The device is fully specified over a temperature range of −55°C to +105°C.

Additional application and technical information can be found in the ADM3057E data sheet.

Rev. 0 Document Feedback

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TABLE OF CONTENTS

Features 1
Enhanced Product Features 1
Applications 1
General Description 1
Functional Block Diagram 1
Revision History 2
Specifications 3
Timing Specifications 5
Insulation and Safety Related Specifications 7
Package Characteristics 7
Regulatory Information 8
DIN V VDE V 0884-10 (VDE V 0884-10) Insulation Characteristics 9
Absolute Maximum Ratings 10
Thermal Resistance 10
ESD Caution 10
Pin Configuration and Function Descriptions 11
Operational Truth Table 12
Typical Performance Characteristics 13
Test Circuits 17
Outline Dimensions 18
Ordering Guide 18

REVISION HISTORY

2/2019—Revision 0: Initial Version

SPECIFICATIONS

All voltages are relative to their respective ground. 4.5 V ≤ V_{CC} ≤ 5.5 V, 1.7 V ≤ V_{IO} ≤ 5.5 V, −55°C ≤ T_A ≤ +105°C, and STBY low, unless otherwise noted. Typical specifications are at V_{CC} = V_{IO} = 5 V and T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY CURRENT						
Logic Side *iso*Power Current	I_{CC}					
Standby			13.5	30	mA	STBY high, AUX_{IN} low, load resistance (R_L) = 60 Ω
Recessive State (or Silent)			27	40	mA	TXD and/or SILENT high, R_L = 60 Ω
Dominant State			180	260	mA	Fault condition, R_L = 60 Ω
70% Dominant/30% Recessive						Worst case, R_L = 60 Ω
1 Mbps			138		mA	
5 Mbps			151	200	mA	
12 Mbps			177	220	mA	
Switching Frequency	f_{OSC}		180		MHz	Frequency hopping center
Logic Side *i*Coupler Current	I_{IO}					
Normal Mode			3.6	5	mA	TXD high, low or switching, AUX_{IN} low
Standby Mode			1.2	2	mA	STBY high
DRIVER						
Differential Outputs						See Figure 27
Recessive State, Normal Mode						TXD high, R_L and common-mode filter capacitor (C_F) open
CANH, CANL Voltage	V_{CANL}, V_{CANH}	2.0		3.0	V	
Differential Output Voltage	V_{OD}	−500		+50	mV	
Dominant State, Normal Mode						TXD and SILENT low, C_F open
CANH Voltage	V_{CANH}	2.75		4.5	V	50 Ω ≤ R_L ≤ 65 Ω
CANL Voltage	V_{CANL}	0.5		2.0	V	50 Ω ≤ R_L ≤ 65 Ω
Differential Output Voltage	V_{OD}	1.5		3.0	V	50 Ω ≤ R_L ≤ 65 Ω
		1.4		3.3	V	45 Ω ≤ R_L ≤ 70 Ω
		1.5		5.0	V	R_L = 2240 Ω
Standby Mode						STBY high, R_L and C_F open
CANH, CANL Voltage	V_{CANL}, V_{CANH}	−0.1		+0.1	V	
Differential Output Voltage	V_{OD}	−200		+200	mV	
Output Symmetry (V_{ISOIN} − V_{CANH} − V_{CANL})	V_{SYM}	−0.55		+0.55	V	R_L = 60 Ω, C_F = 4.7 nF, RS low
Short-Circuit Current	$\|I_{SC}\|$					R_L open
Absolute						
CANH				115	mA	V_{CANH} = −3 V
CANL				115	mA	V_{CANL} = 18 V
Steady State						
CANH				115	mA	V_{CANH} = −24 V
CANL				115	mA	V_{CANL} = 24 V
Logic Inputs (TXD, SILENT, STBY, AUX_{IN})						
Input Voltage						
High	V_{IH}	0.65 × V_{IO}			V	
Low	V_{IL}			0.35 × V_{IO}	V	
Complementary Metal-Oxide Semiconductor (CMOS) Logic Input Currents	$\|I_{IH}\|$, $\|I_{IL}\|$			10	μA	Input high or low

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
RECEIVER						
Differential Inputs						
Differential Input Voltage Range	V_{ID}					See Figure 28, C_{RXD} open, $-25\ V < V_{CANL}, V_{CANH} < +25\ V$
Recessive		−1.0		+0.5	V	
		−1.0		+0.4	V	STBY high
Dominant		0.9		5.0	V	
		1.15		5.0	V	STBY high
Input Voltage Hysteresis	V_{HYS}		150		mV	
Unpowered Input Leakage Current	$\lvert I_{IN\ (OFF)}\rvert$			10	µA	$V_{CANH}, V_{CANL} = 5\ V, V_{CC} = 0\ V$
Input Resistance						
CANH, CANL	R_{INH}, R_{INL}	6		25	kΩ	
Differential	R_{DIFF}	20		100	kΩ	
Matching	m_R	−0.03		+0.03	Ω/Ω	$m_R = 2 \times (R_{INH} - R_{INL})/(R_{INH} + R_{INL})$
Input Capacitance						
CANH, CANL	C_{INH}, C_{INL}		35		pF	
Differential	C_{DIFF}		12		pF	
Logic Outputs (RXD, AUX_{OUT})						
Output Voltage						
Low	V_{OL}		0.2	0.4	V	Output current (I_{OUT}) = 2 mA
High	V_{OH}					
RXD		$V_{IO} - 0.2$			V	$I_{OUT} = -2$ mA
AUX_{OUT}		+2.4			V	$I_{OUT} = -2$ mA
Short-Circuit Current	I_{OS}					
RXD		7		85	mA	Output voltage (V_{OUT}) = GND_1 or V_{IO}
COMMON-MODE TRANSIENT IMMUNITY[1]						Common-mode voltage (V_{CM}) ≥ 1 kV, transient magnitude ≥ 800 V
Input High, Recessive	$\lvert CM_H\rvert$	75	100		kV/µs	$V_{IN} = V_{IO}$ (AUX_{IN}, TXD) or CANH/CANL recessive
Input Low, Dominant	$\lvert CM_L\rvert$	75	100		kV/µs	$V_{IN} = 0\ V$ (AUX_{IN}, TXD) or CANH/CANL dominant
SLOPE CONTROL						
Input Voltage for Standby Mode	V_{STB}	4.0			V	
Current for Slope Control Mode	I_{SLOPE}			−240	µA	RS voltage (V_{RS}) = 0 V
Slope Control Mode Voltage	V_{SLOPE}	2.1			V	RS current (I_{RS}) = 10 µA
Input Voltage for High Speed Mode	V_{HS}			1	V	

[1] $\lvert CM_H\rvert$ is the maximum common-mode voltage slew rate that can be sustained while maintaining $AUX_{OUT} \geq 2.4$ V, CANH/CANL recessive, or RXD ≥ $V_{IO} - 0.2$ V. $\lvert CM_L\rvert$ is the maximum common-mode voltage slew rate that can be sustained while maintaining $AUX_{OUT} \leq 0.4$ V, CANH/CANL dominant, or RXD ≤ 0.4 V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

TIMING SPECIFICATIONS

All voltages are relative to their respective ground. 4.5 V ≤ V_{CC} ≤ 5.5 V, 1.7 V ≤ V_{IO} ≤ 5.5 V, −55°C ≤ T_A ≤ +105°C, and STBY low, unless otherwise noted. Typical specifications are at V_{CC} = V_{IO} = 5 V and T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DRIVER						SILENT low, bit time on the TXD pin as transmitted by the CAN controller (t_{BIT_TXD}) = 200 ns, see Figure 2 and Figure 29, slope resistance (R_{SLOPE}) = 0 Ω, R_L = 60 Ω, load capacitance (C_L) = 100 pF
Maximum Data Rate		12			Mbps	
Propagation Delay from TXD to Bus (Recessive to Dominant)	t_{TXD_DOM}		35	60	ns	
Propagation Delay from TXD to Bus (Dominant to Recessive)	t_{TXD_REC}		46	70	ns	
Transmit Dominant Timeout	t_{DT}	1175		4000	µs	TXD low, see Figure 5
RECEIVER						SILENT low, see Figure 2 and Figure 29, R_L = 60 Ω, C_L = 100 pF, RXD capacitance (C_{RXD}) = 15 pF
Falling Edge Loop Propagation Delay (TXD to RXD)	t_{LOOP_FALL}					
Full Speed Mode				150	ns	R_{SLOPE} = 0 Ω, t_{BIT_TXD} = 200 ns
Slope Control Mode				300	ns	R_{SLOPE} = 47 kΩ, t_{BIT_TXD} = 1 µs
Rising Edge Loop Propagation Delay (TXD to RXD)	t_{LOOP_RISE}					
Full Speed Mode				150	ns	R_{SLOPE} = 0 Ω, t_{BIT_TXD} = 200 ns
Slope Control Mode				300	ns	R_{SLOPE} = 47 kΩ, t_{BIT_TXD} = 1 µs
Loop Delay Symmetry (Minimum Recessive Bit Width)	t_{BIT_RXD}					
2 Mbps		450		550	ns	t_{BIT_TXD} = 500 ns
5 Mbps		160		220	ns	t_{BIT_TXD} = 200 ns
8 Mbps		85		140	ns	t_{BIT_TXD} = 125 ns
12 Mbps		50		91.6	ns	t_{BIT_TXD} = 83.3 ns
CANH, CANL SLEW RATE	|SR|		7		V/µs	SILENT low, see Figure 29, R_L = 60 Ω, C_L = 100 pF, R_{SLOPE} = 47 kΩ
STANDBY MODE						
Minimum Pulse Width Detected (Receiver Filter Time)	t_{FILTER}	1		5	µs	STBY high, see Figure 4
Wake-Up Pattern Detection Reset Time	t_{WUPR}	1175		4000	µs	STBY high, see Figure 4
Normal Mode to Standby Mode Time	t_{STBY_ON}			25	µs	
Standby Mode to Normal Mode Time	t_{STBY_OFF}			25	µs	Time until RXD valid
AUXILIARY SIGNAL						
Maximum Switching Rate	f_{AUX}	20			kHz	
AUX_{IN} to AUX_{OUT} Propagation Delay	t_{AUX}			25	µs	
SILENT MODE						
Normal Mode to Silent Mode Time	t_{SILENT_ON}		40	100	ns	TXD low, R_{SLOPE} = 0 Ω, see Figure 3
Silent Mode to Normal Mode Time	t_{SILENT_OFF}		50	100	ns	TXD low, R_{SLOPE} = 0 Ω, see Figure 3

Timing Diagrams

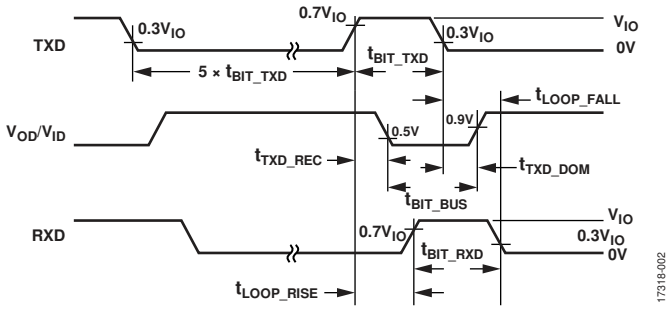

Figure 2. Transceiver Timing Diagram

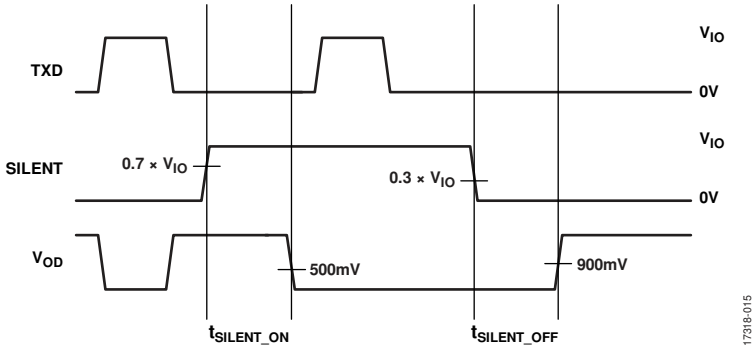

Figure 3. Silent Mode Timing Diagram

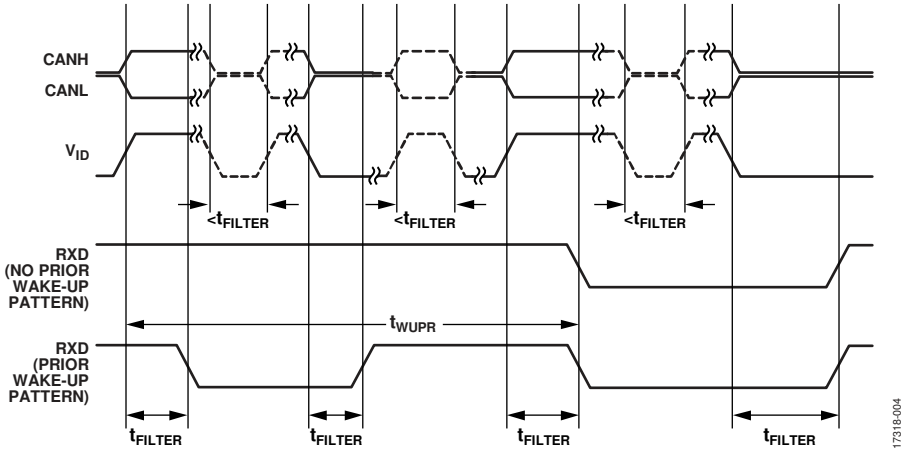

Figure 4. Wake-Up Pattern Detection and Filtered RXD in Standby Mode Timing Diagram

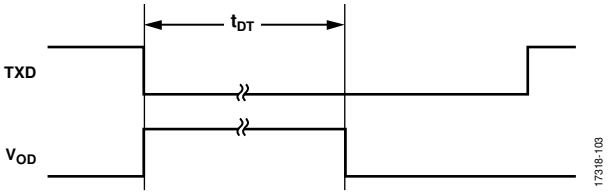

Figure 5. Dominant Timeout

INSULATION AND SAFETY RELATED SPECIFICATIONS

For additional information, see www.analog.com/icouplersafety.

Table 3.

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		3000	V rms	1-minute duration
Minimum External Air Gap (Clearance)	L (I01)	7.8	mm min	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L (I02)	7.8	mm min	Measured from input terminals to output terminals, shortest distance path along body
Minimum Clearance in the Plane of the Printed Circuit Board (PCB Clearance)	L (PCB)	7.8	mm min	Measured from input terminals to output terminals, shortest distance through air, line of sight, in the PCB mounting plane
Minimum Internal Gap (Internal Clearance)		21	µm min	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>600	V	IEC 60112
Material Group		I		Material Group (IEC 60664-1)

PACKAGE CHARACTERISTICS

Table 4.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Resistance (Input to Output)[1]	R_{I-O}		10^{13}		Ω	
Capacitance (Input to Output)[1]	C_{I-O}		3.7		pF	f = 1 MHz
Input Capacitance[2]	C_I		4.0		pF	

[1] The device is considered a 2-terminal device: Pin 1 through Pin 10 are shorted together, and Pin 11 through Pin 20 are shorted together.
[2] Input capacitance is from any input data pin to ground.

REGULATORY INFORMATION

See Table 9 for details regarding maximum working voltages for specific cross isolation waveforms and insulation levels. The ADM3057E-EP is approved or pending approval by the organizations listed in Table 5.

Table 5.

UL (Pending)[1]	CSA (Pending)	VDE (Pending)[2]	CQC (Pending)
Recognized Under UL 1577 Component Recognition Program Single Protection, 3000 V rms Isolation Voltage	Approved under CSA Component Acceptance Notice 5A CSA 60950-1-07+A1+A2 and IEC 60950-1, second edition, +A1+A2 Basic insulation at 780 V rms (1103 V_{PEAK}) Reinforced insulation at 390 V rms (552 V_{PEAK}) IEC 60601-1 Edition 3.1: Basic insulation (1 MOPP), 490 V rms (693 V_{PEAK}) Reinforced insulation (2 MOPP), 250 V rms (353 V_{PEAK}) CSA 61010-1-12 and IEC 61010-1 third edition Basic insulation at 300 V rms mains, 780 V secondary (1103 V_{PEAK}) Reinforced insulation at 300 V rms mains, 390 V secondary (552 V_{PEAK})	DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 Reinforced insulation 849 V_{PEAK}, surge isolation voltage (V_{IOTM}) = 6000 V_{PEAK}	Certified under CQC11-471543-2012 GB4943.1-2011: basic insulation at 780 V rms (1103 V_{PEAK}) Reinforced insulation at 390 V rms (552 V_{PEAK})
File E214100	File 205078	File 2471900-4880-0001	File (pending)

[1] In accordance with UL 1577, each ADM3057E-EP is proof tested by applying an insulation test voltage ≥ 3600 V rms for 1 sec.
[2] In accordance with DIN V VDE V 0884-10, each ADM3057E-EP is proof tested by applying an insulation test voltage ≥ 1592 V_{PEAK} for 1 sec (partial discharge detection limit = 5 pC). The * marking branded on the component designates DIN V VDE V 0884-10 approval.

DIN V VDE V 0884-10 (VDE V 0884-10) INSULATION CHARACTERISTICS

These isolators are suitable for reinforced electrical isolation only within the safety limit data. The protective circuits ensure the maintenance of the safety data. The asterisk (*) marking on packages denotes DIN V VDE V 0884-10 approval.

Table 6. VDE Characteristics

Description	Test Conditions/Comments	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 150 V rms			I to IV	
For Rated Mains Voltage ≤ 300 V rms			I to IV	
For Rated Mains Voltage ≤ 400 V rms			I to III	
Climatic Classification			55/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Working Insulation Voltage		V_{IORM}	849	V_{PEAK}
Input to Output Test Voltage, Method B1	$V_{IORM} \times 1.875 = V_{PR}$, 100% production test, t_m = 1 sec, partial discharge < 5 pC	$V_{pd(m)}$	1592	V_{PEAK}
Input to Output Test Voltage, Method A				
After Environmental Tests Subgroup 1	$V_{IORM} \times 1.5 = V_{pd(m)}$, t_{ini} = 60 sec, t_m = 10 sec, partial discharge < 5 pC	$V_{pd(m)}$	1273	V_{PEAK}
After Input or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{pd(m)}$, t_{ini} = 60 sec, t_m = 10 sec, partial discharge < 5 pC	$V_{pd(m)}$	1018	V_{PEAK}
Highest Allowable Overvoltage	Transient overvoltage, t_{TR} = 10 sec	V_{IOTM}	6000	V_{PEAK}
Surge Isolation Voltage Reinforced	$V_{IOSM(TEST)}$ = 10 kV, 1.2 µs rise time, 50 µs, 50% fall time	V_{IOSM}	6000	V_{PEAK}
Safety Limiting Values	Maximum value allowed in the event of a failure (see Figure 6)			
Case Temperature		T_S	150	°C
Total Power Dissipation at 25°C		P_S	2.35	W
Insulation Resistance at T_S	V_{IO} = 500 V	R_S	$>10^9$	Ω

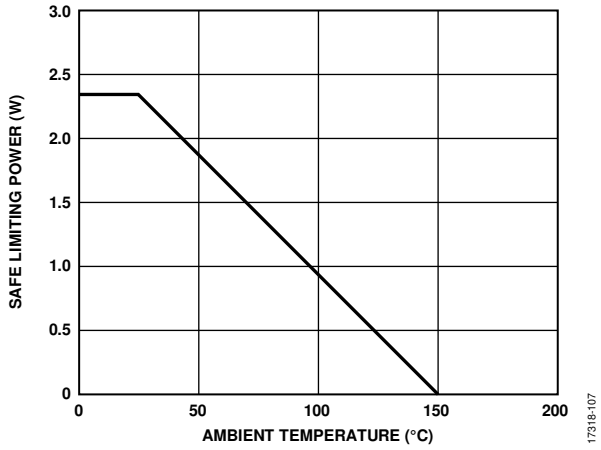

Figure 6. Thermal Derating Curve, Dependence of Safety Limiting Values with Ambient Temperature per DIN V VDE V 0884-10

ABSOLUTE MAXIMUM RATINGS

Pin voltages with respect to GND_x are on the same side, unless otherwise noted.

Table 7.

Parameter	Rating
V_{CC}	−0.5 V to +6 V
V_{IO}	−0.5 V to +6 V
Logic Side Input/Output: TXD, RXD, AUX_{IN}, SILENT, STBY	−0.5 V to V_{IO} + 0.5 V
CANH, CANL	−40 V to +40 V
AUX_{OUT}, RS	−0.5 V to V_{ISOIN} + 0.5 V
Operating Temperature Range	−55°C to +105°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (T_J Maximum)	150°C
Power Dissipation	(T_J maximum − T_A)/θ_{JA}
Electrostatic Discharge (ESD)	
IEC 61000-4-2, CANH/CANL	
Across Isolation Barrier to GND_1	±8 kV
Contact Discharge to GND_2	±8 kV
Air Discharge to GND_2	±15 kV
Human Body Model (HBM), All Pins, 1.5 kΩ, 100 pF	4 kV
Moisture Sensitivity Level (MSL)	MSL3

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to PCB design and operating environment. Careful attention to PCB thermal design is required.

The thermal resistance value specified in Table 8 is simulated based on JEDEC specifications (unless specified otherwise) and must be used in compliance with JESD51-12.

Table 8. Thermal Resistance

Package Type	θ_{JA}	Unit
RW-20[1]	53	°C/W

[1] The θ_{JA} value is based on simulations of a devices mounted on a JEDEC standard, 4-layer board with fine width traces and still air. See the ADM3057E data sheet for thermal model definitions.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Table 9. Maximum Continuous Working Voltage[1]

Parameter	Rating	Unit	Constraint
AC Voltage			
Bipolar Waveform			
Basic Insulation	566	V_{PEAK}	Lifetime limited by insulation lifetime per VDE-0884-11
Reinforced Insulation	467	V_{PEAK}	Lifetime limited by insulation lifetime per VDE-0884-11
Unipolar Waveform			
Basic Insulation	1131	V_{PEAK}	Lifetime limited by insulation lifetime per VDE-0884-11
Reinforced Insulation	933	V_{PEAK}	Lifetime limited by insulation lifetime per VDE-0884-11
DC Voltage			
Basic Insulation	1560	V_{PEAK}	Lifetime limited by package creepage per IEC 60664-1
Reinforced Insulation	780	V_{PEAK}	Lifetime limited by package creepage per IEC 60664-1

[1] Maximum continuous working voltage refers to the continuous voltage magnitude imposed across the isolation barrier. See the ADM3057E data sheet for more details.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

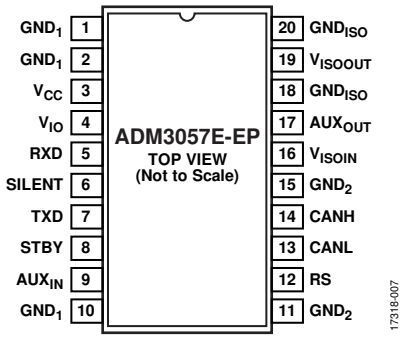

Figure 7. Pin Configuration

Table 10. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 2, 10	GND_1	Ground, Logic Side.
3	V_{CC}	*iso*Power Power Supply, 4.5 V to 5.5 V. This pin requires 0.1 µF and 10 µF decoupling capacitors.
4	V_{IO}	*i*Coupler Power Supply, 1.7 V to 5.5 V. This pin requires 0.01 µF and 0.1 µF decoupling capacitors.
5	RXD	Receiver Output Data.
6	SILENT	Silent Mode Select with Input High. Bring this input low or leave the pin unconnected (internal pull-down) for normal mode.
7	TXD	Driver Input Data. This pin has a weak internal pull-up resistor to V_{IO}.
8	STBY	Standby Mode Select with Input High. Bring this input low or leave the pin unconnected (internal pull-down) for normal mode.
9	AUX_{IN}	Auxiliary Channel Input. This pin sets the AUX_{OUT} output.
11, 15	GND_2	Ground, Bus Side.
12	RS	Slope Control Pin. Short this pin to ground for full speed operation or use a weak pull-down resistor (for example, 47 kΩ) for slope control mode. An input high signal places the CAN transceiver in standby mode.
13	CANL	CAN Low Input/Output.
14	CANH	CAN High Input/Output.
16	V_{ISOIN}	Isolated Power Supply Input for the CAN Transceiver Bus Side Digital Isolator. This pin requires 0.01 µF and 0.1 µF decoupling capacitors.
17	AUX_{OUT}	Isolated Auxiliary Channel Output. The state of AUX_{OUT} is latched when STBY is high. By default, AUX_{OUT} is low at startup or when V_{IO} is unpowered.
18, 20	GND_{ISO}	Ground for the Isolated DC-to-DC Converter. Connect these pins together through one ferrite bead to PCB ground (bus side).
19	V_{ISOOUT}	Isolated Power Supply Output. This pin requires 0.22 µF and 10 µF capacitors to GND_{ISO}. Connect this pin through a ferrite bead and short the PCB trace to V_{ISOIN} for operation.

OPERATIONAL TRUTH TABLE

Table 11. Truth Table

Power		Inputs[1, 2]						Outputs[2]		Input/Output
V_{CC}	V_{IO}	TXD	SILENT	STBY	AUX_{IN}	RS	Mode	RXD[3]	AUX_{OUT}	CANH/CANL
On	On	Low	Low	Low	Low	Low/ pull-down	Normal/ slope mode	Low	Low	Dominant[4]
On	On	Low	Low	Low	High	Low/ pull-down	Normal/ slope mode	Low	High	Dominant[4]
On	On	High	Low	Low	Low	Low/ pull-down	Normal/ slope mode	High/per bus	Low	Recessive/set by bus
On	On	High	Low	Low	High	Low/ pull-down	Normal/ slope mode	High/per bus	High	Recessive/set by bus
On	On	X	High	Low	Low	X	Listen only	High/per bus	Low	Recessive/set by bus
On	On	X	High	Low	High	X	Listen only	High/per bus	High	Recessive/set by bus
On	On	X	X	High	X	X	Standby	High/WUP/filtered	Last state	Bias to GND_2/set by bus
On	On	X	X	X	Low	Pull-up	Standby[5]	High/WUP/filtered	Low	Bias to GND_2/set by bus
On	On	X	X	X	High	Pull-up	Standby[5]	High/WUP/filtered	High	Bias to GND_2/set by bus
On	Off	Z	Z	Z	Z	Low/ pull-down	Normal/ slope mode	Z	Low	Recessive/set by bus
Off	On	X	X	X	X	X	Transceiver off	High	Z	High impedance/set by bus
Off	Off	Z	Z	Z	Z	Z	Transceiver off	Z	Z	High impedance/set by bus

[1] X means irrelevant.
[2] Z means high impedance within one diode drop of ground.
[3] WUP means remote wake-up pattern.
[4] Limited by t_{DT}.
[5] RS can only set the transceiver to standby mode. RS does not control the digital isolator.

TYPICAL PERFORMANCE CHARACTERISTICS

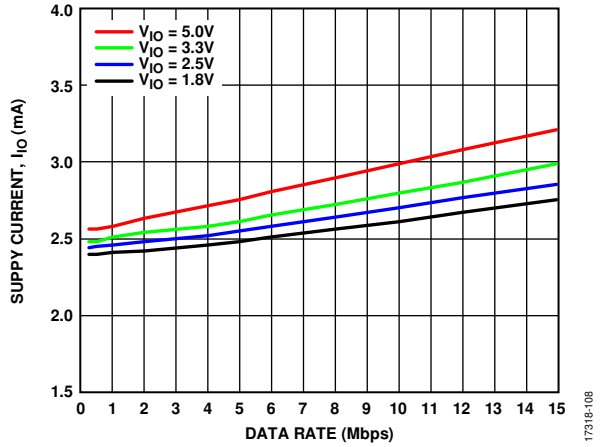

Figure 8. Supply Current, I_{IO} vs. Data Rate

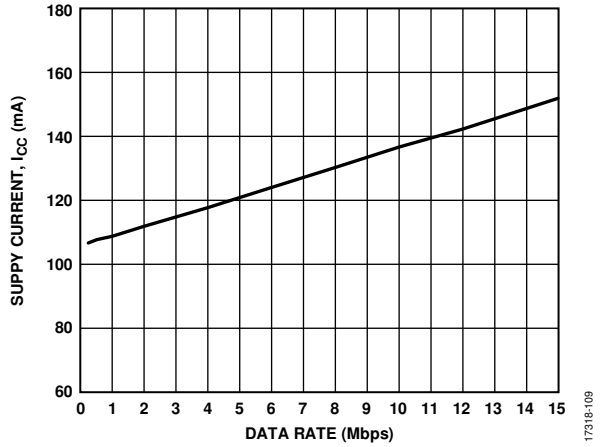

Figure 9. Supply Current, I_{CC} vs. Data Rate

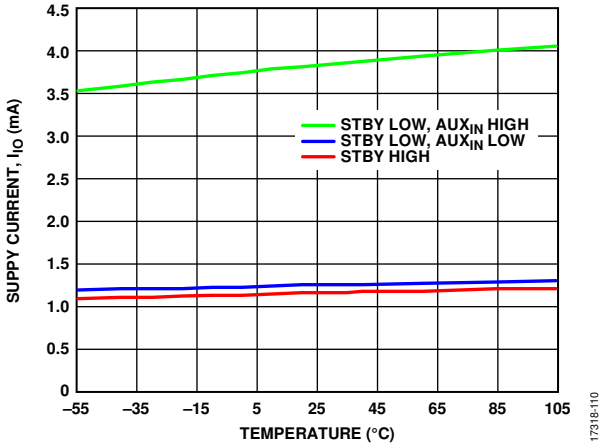

Figure 10. Supply Current, I_{IO} vs. Temperature (Inputs Idle)

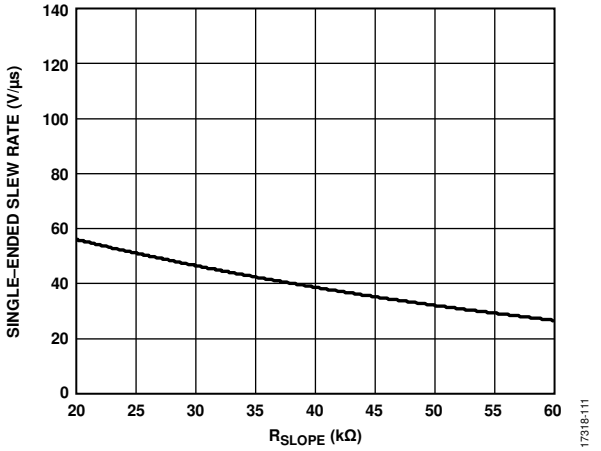

Figure 11. Single-Ended Slew Rate vs. R_{SLOPE}

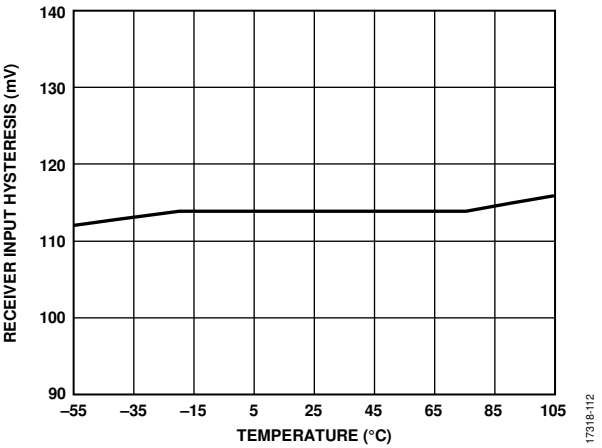

Figure 12. Receiver Input Hysteresis vs. Temperature

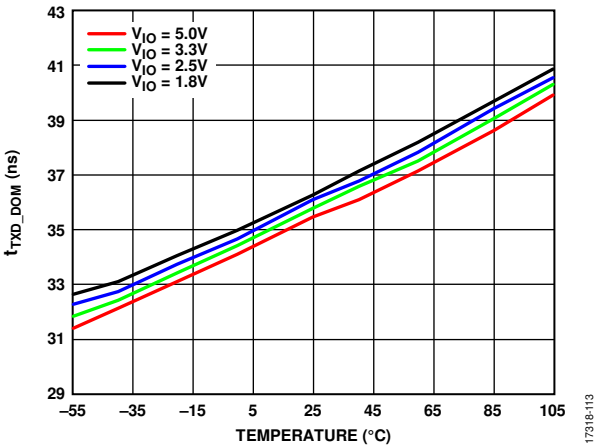

Figure 13. t_{TXD_DOM} vs. Temperature

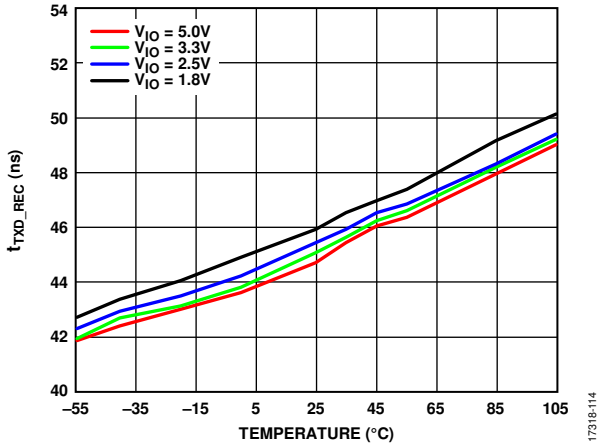

Figure 14. t_{TXD_REC} vs. Temperature

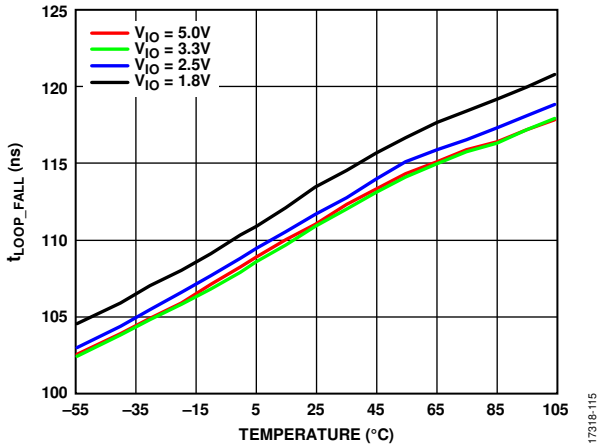

Figure 15. t_{LOOP_FALL} vs. Temperature (R_{SLOPE} = 0 Ω)

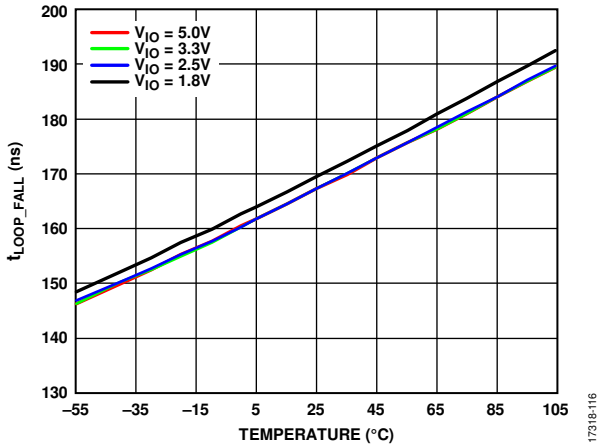

Figure 16. t_{LOOP_FALL} vs. Temperature (R_{SLOPE} = 47 kΩ)

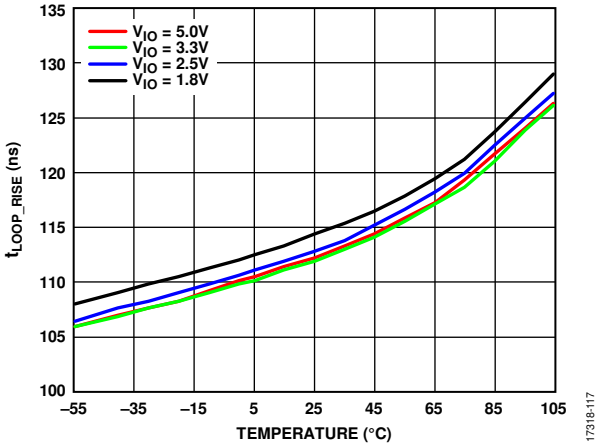

Figure 17. t_{LOOP_RISE} vs. Temperature (R_{SLOPE} = 0 Ω)

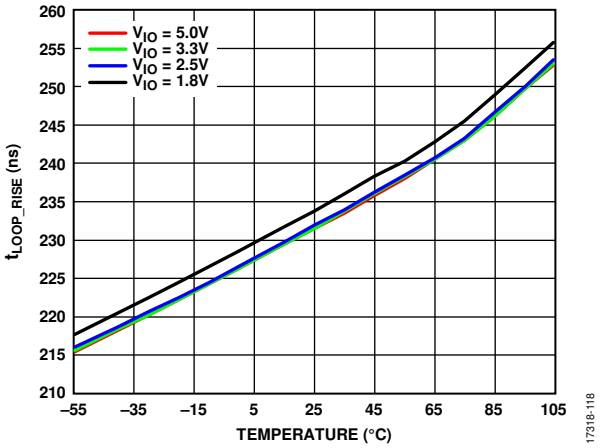

Figure 18. t_{LOOP_RISE} vs. Temperature (R_{SLOPE} = 47 kΩ)

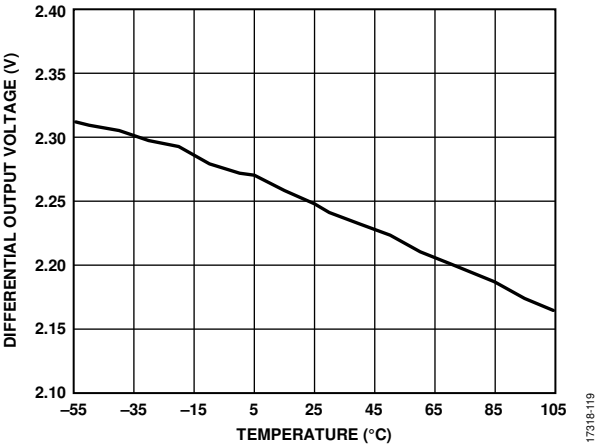

Figure 19. Differential Output Voltage (V_{OD}) vs. Temperature

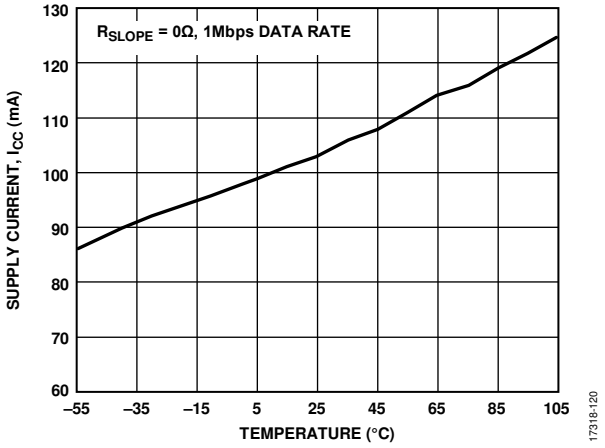

Figure 20. Supply Current, I_{CC} vs. Temperature

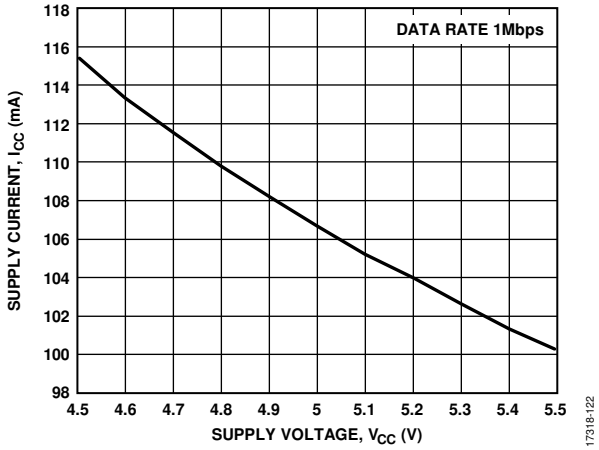

Figure 22. Supply Current, I_{CC} vs. Supply Voltage, V_{CC}, RS = 0 Ω, 1 Mbps

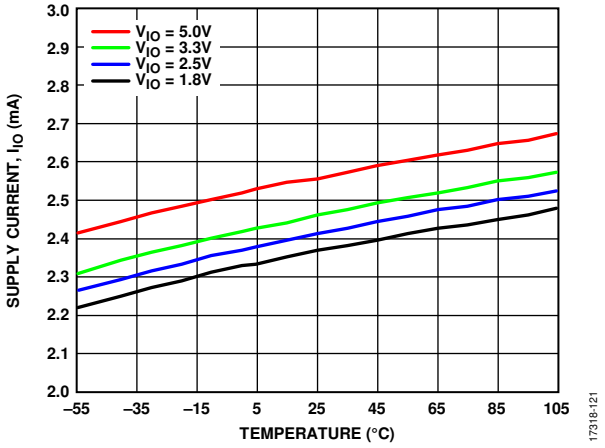

Figure 21. Supply Current, I_{IO} vs. Temperature, RS = 0 Ω, 1 Mbps

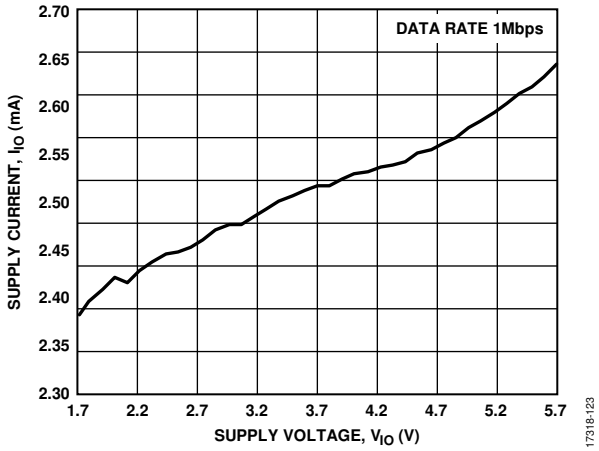

Figure 23. Supply Current, I_{IO} vs. Supply Voltage, V_{IO}, Data Rate = 1 Mbps

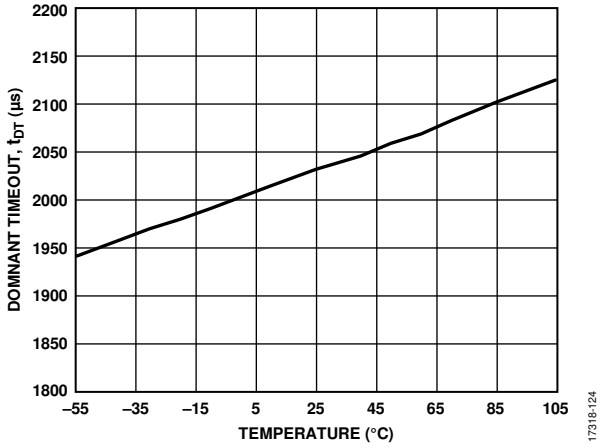

Figure 24. Dominant Timeout, t_{DT} vs. Temperature

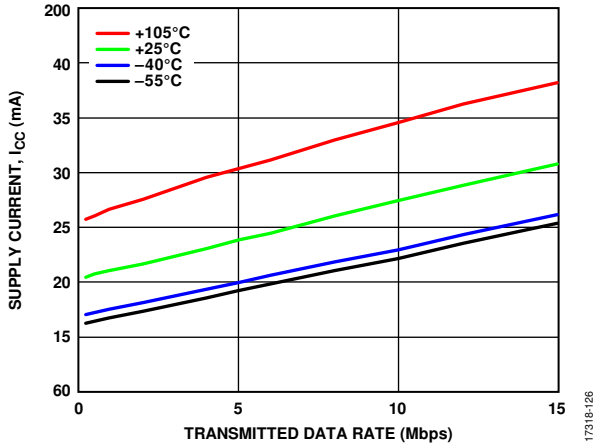

Figure 26. Supply Current, I_{CC} vs. Transmitted Data Rate

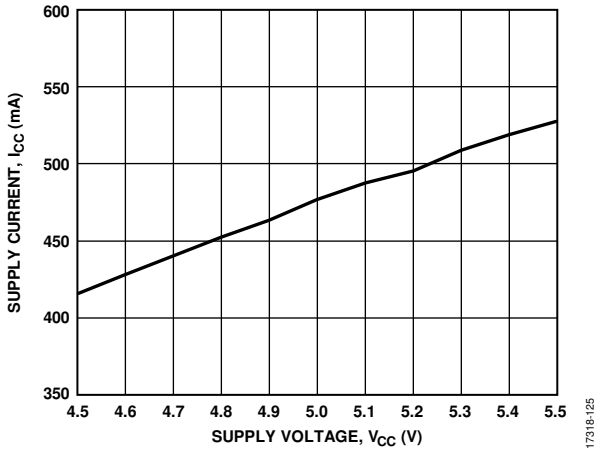

Figure 25. Supply Current, I_{CC} vs. Supply Voltage, V_{CC} (V_{ISOOUT} Shorted to GND_{ISO})

TEST CIRCUITS

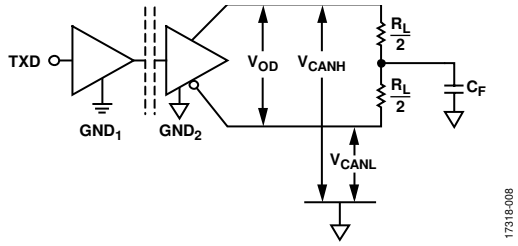

Figure 27. Driver Voltage Measurement

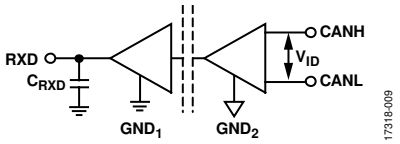

Figure 28. Receiver Voltage Measurement

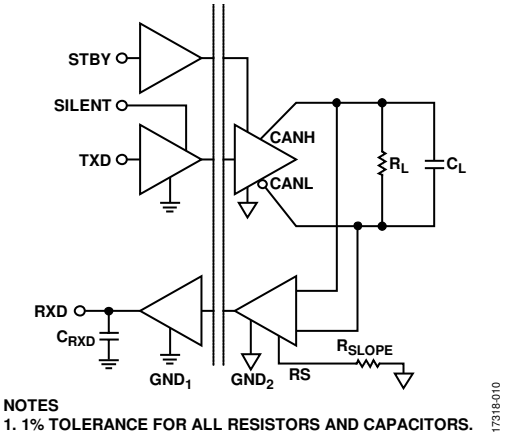

Figure 29. Switching Characteristics Measurements

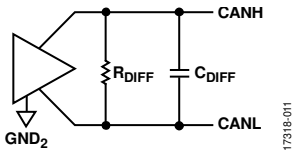

Figure 30. R_{DIFF} and C_{DIFF} Measured in Recessive State, Bus Disconnected

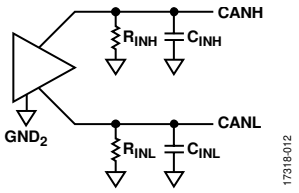

Figure 31. R_{INx} and C_{INx} Measured in Recessive State, Bus Disconnected

OUTLINE DIMENSIONS

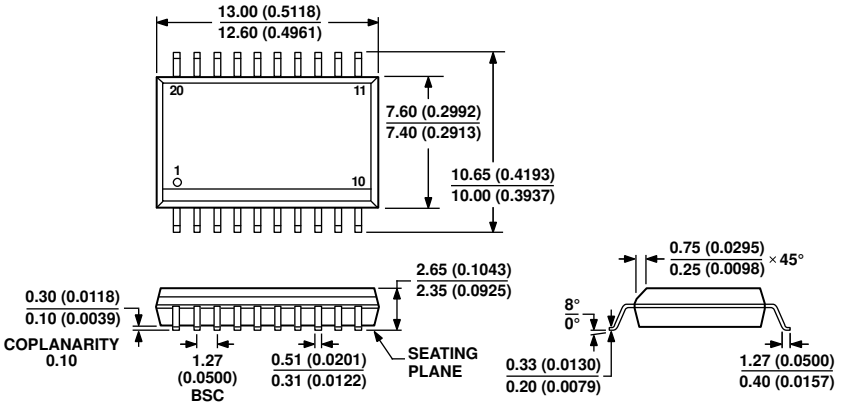

Figure 32. 20-Lead Standard Small Outline Package [SOIC_W]
Wide Body
(RW-20)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model[1, 2]	Temperature Range	Package Description	Package Option
ADM3057ETRWZ-EP	−55°C to +105°C	20-Lead Standard Small Outline Package [SOIC_W]	RW-20
ADM3057ETRWZ-EP-RL	−55°C to +105°C	20-Lead Standard Small Outline Package [SOIC_W]	RW-20
EVAL-ADM3055EEBZ		ADM3055E Evaluation Board	

[1] Z = RoHS Compliant Part.
[2] Use the EVAL-ADM3055EEBZ evaluation board to evaluate the ADM3057E-EP.

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