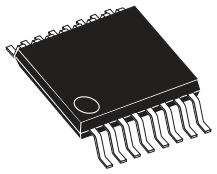
L5989D

4 A continuous (more than 5 A pulsed) step-down switching regulator with synchronous rectification

Features

- 4 A output current (more than 5 pulsed)
- Operating input voltage from 2.9 V to 18 V
- External 1.8 V ± 2% reference voltage
- Output voltage from 0.6 to input voltage
- MLCC compatible
- 200 ns T_{ON}
- Programmable UVLO matches 3.3 V, 5 V and 12 V bus
- F_{SW} programmable up to 1 MHz
- Voltage feed-forward
- Zero load current operation
- Programmable current limit on both switches
- Programmable sink current capability
- Pre-bias start up capability
- Thermal shutdown

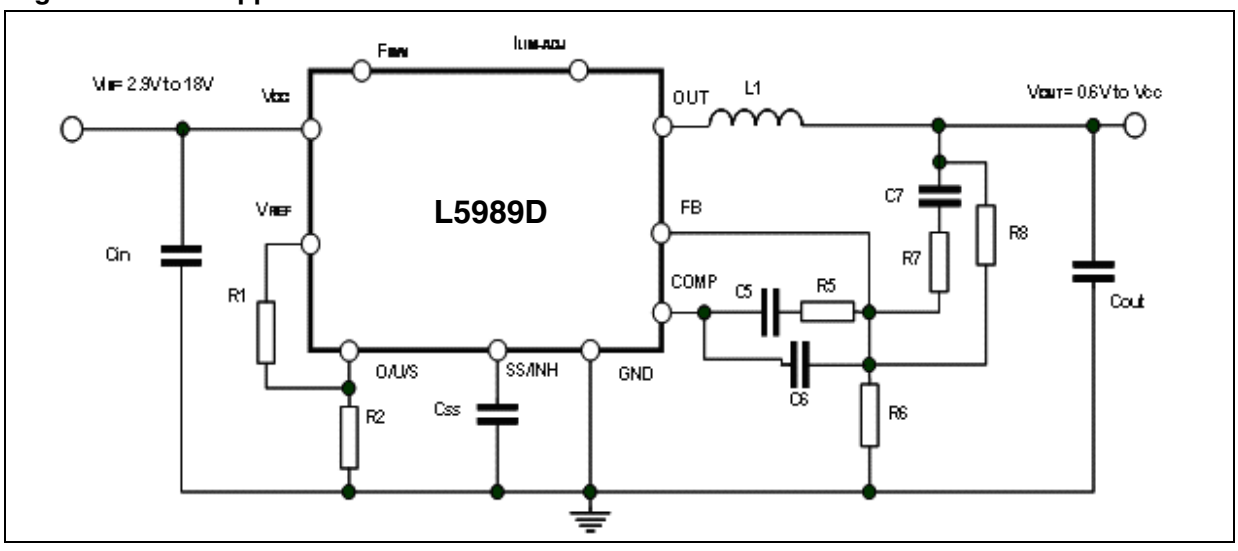


HTSSOP 16

Applications

- Consumer: STB, DVD, LCD TV, VCR, car radio, LCD monitors
- Networking: XDSL, modems, routers and switches
- Computer and peripherals: printers, audio / graphic cards, optical storage, hard disk drive
- Industrial: DC-DC modules, factory automation
- HC LED driving

Figure 1. Test application circuit



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1 Description

The L5989D is a monolithic step down power switching regulator able to deliver a continuos output current of 4 A to the load in most of the application conditions limited only by the thermal performance (see *Chapter 6.5* for details). The device is able to deliver more than 5 A to the load for a maximum time which is dependent on the thermal impedance of the system and the specific operating conditions (see *Chapter 6.6*).

The input voltage can range from 2.9 V to 18 V. The device is capable of 100% duty cycle operation thanks to the embedded high side PMOS switch which doesn't need external bootstrap capacitor to be driven.

The internal switching frequency is adjustable by external resistor and can be set continuously from 100 kHz to 1 MHz.

The multifunction UOS pin allows to set-up properly the additional embedded features depending on the value of the voltage level.

- U (UVLO): two UVLO thresholds can be selected to match the 3.3 V and 5 V or 12 V input buses
- O (OVP): latched or not latched OVP protection selectable. In latched mode the switching activity is interrupted until an UVLO or INH event happens
- S (SINK): the sink capability is always disabled during soft-start time to support pre-biased output voltage. Afterwards the sink capability can be enabled or not depending on the voltage set on the multifunction pin.

During soft-start phase a constant current protection is active to deliver extra current necessary to load the output capacitor. The current limit protection is achieved by sensing the current flowing in both embedded switches to assure an effective protection even at extreme duty cycle operations. Finished the soft-start phase the current protection feature triggers the "HICCUP" mode forcing the soft-start capacitor to be discharged and recharged. The current thresholds of both switches can be adjusted in tracking by using an external resistor to dimension the current protection accordingly to the local application.

The soft-start time is based on a constant current charge of an external capacitor. As a consequence the time can be set accordingly to the value of the output capacitor.

The latest smart power technology BCD6 (Bipolar-CMOS-DMOS version 6) features a low resistance of the embedded switches (35 mΩ typical for a NMOS, 50 mΩ typical for a PMOS), achieving high efficiency levels.

The HTSSOP16 package with exposed pad accomplishes low R_{thJA} (40°C/W), useful in dissipating power internally generated during high output current / high frequency operations.

2 Pin function

Figure 2. Pin connection

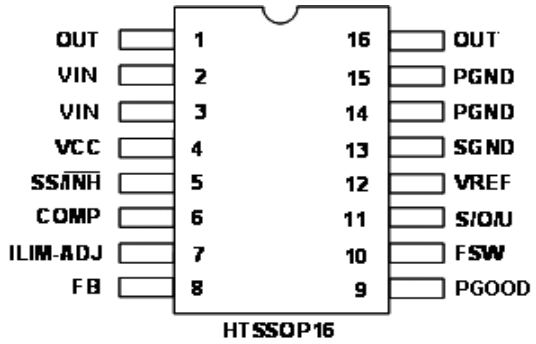


Table 1. Pinout description

N.	Name	Description
1, 16	OUT	Regulator output
2, 3	VIN	Unregulated DC input voltage
4	VCC	Unregulated DC signal input voltage
5	SS/$\overline{\text{INH}}$	An external logic signal (active LOW) disables the device. In case the pin is floating the device deliver a constant current (22 µA typ.) to charge the soft-start capacitor (see *Chapter 5.4*)
6	COMP	Error amplifier output for frequency compensation
7	ILIM-ADJ	Connecting a pull-up resistor to VREF or a pull-down resistor to GND the internal current limit thresholds can be tuned to match the local application. In case the pin is left floating no changes are applied to the default current limit thresholds
8	FB	Feedback input. Connecting the output voltage directly to this pin results in a regulation voltage of 600 mV. An external resistive divider is required for higher output voltages
9	PGOOD	Open collector output; low impedance if the feedback voltage is lower than 0.85 times the internal reference of the error amplifier. An hysteresis is provided
10	FSW	Connecting a pull-up resistor to VREF or a pull-down resistor to GND the internal oscillator frequency will be increased or decreased respectively. In case the pin is left floating the predefined oscillator frequency (400 kHz ± 10%) is active
11	U/O/S	Multifunction pin used to program additional features: UVLO thresholds, OVP latched/not latched, SINK enabled/disabled
12	VREF	1.8 V voltage reference
13	SGND	Signal ground
14, 15	PGND	Power ground

3 Maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
VCC	Input voltage	20	V
VOUT	Output DC voltage	-0.3 (1) to VCC	V
U/O/S, SS/$\overline{INH}$, COMP, PGOOD, Fsw, ILIM-ADJ	Analog pins	-0.3 to 4	V
FB	Feedback voltage	1.5	V
P_{tot}	Power dissipation at T_A < 60 °C	2.25	W
T_J	Junction temperature range	-40 to 150	°C
T_{STG}	Storage temperature range	-55 to 150	°C

1. During the switching activity the negative peak voltage could reach -1.5 V without any damage for the device

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction to ambient max	40 (1)	°C/W

1. HTSSOP16 package mounted on ST demonstration board

4 Electrical characteristics

V_{CC} = 12 V, T_J = 25 °C unless otherwise specified.

Table 4. Electrical characteristic

Symbol	Parameter	Test condition		Min	Typ	Max	Unit
Vcc	Operating input voltage range	Vout = 0.6 V; Iout = 3 A		2.9		18	V
Rdson HS	High side MOSFET on resistance	Iout = 1.0 A		75	85	95	mΩ
			(1)	111	120	132	mΩ
Rdson LS	Low side MOSFET on resistance	Iout = 1.0 A		62	67	72	mΩ
			(1)	92	100	106	mΩ
$I_{L\ HIGH\ SIDE}$	Maximum peak limiting current	$I_{LIM-ADJ}$ = float		3.6	4	4.4	A
$I_{L\ LOW\ SIDE}$	Maximum valley limiting current	$I_{LIM-ADJ}$ = float		4.14	4.6	5.06	A
f_{SW}	Switching frequency	FSW = floating		360	400	440	kHz
$f_{SW\ ADJ}$	Adjusted switching frequency	$R_{FSW\ PULL\ DWN}$ = 27 kΩ			1000		kHz
D	Duty cycle			0		100	%
Selectable undervoltage lock-out (UVLO)							
3.3 V BUS	Turn ON Vcc threshold				2.7	2.8	V
	Turn OFF Vcc threshold			2.4	2.5		V
	Hysteresis				200		mV
12 V BUS	Turn ON Vcc threshold				8	8.6	V
	Turn OFF Vcc threshold			6.8	7		V
	Hysteresis				1		V
DC characteristic							
I_{SS}	Soft-start current	$V_{SS/\overline{INH}}$ = 2 V			22		µA
		$V_{SS/\overline{INH}}$ = 0			5		µA
INH	Device ON level			0.8			V
	Device OFF level					0.3	V
I_q	Quiescent current	Duty Cycle = 0; V_{FB} = 1 V				3	mA
$I_{q\ st-by}$	Total stand-by quiescent current					35	µA

Table 4. Electrical characteristic (continued)

Symbol	Parameter	Test condition		Min	Typ	Max	Unit
Dynamic characteristic (see figure 1)							
V_{FB}	Voltage feedback in regulation	2.9 V < VCC < 18 V		0.595	0.6	0.605	V
			(1)	0.592	0.6	0.609	
Error amplifier							
V_{OH}	High level output voltage	V_{FB} = 0.2 V; SS floating		3.1			V
V_{OL}	Low level output voltage	V_{FB} = 1.0 V				0.1	V
$I_{O\ SOURCE}$	Source output current	V_{FB} = 0.2 V	(2)		25		mA
$I_{O\ SRCE\ LIM}$	Source current limitation	V_{FB} = 0.2 V, V_{COMP}=3 V			2		mA
$I_{O\ SINK}$	Sink output current	V_{FB} = 1.0 V, V_{COMP}=0.5 V			30		mA
A_{V0}	DC open loop gain		(2)		100		dB
PGOOD							
V_{FB_PGOOD}	Up threshold (V_{FB_PGOOD} / V_{FB})	V_{FB} rising		81	85	90	% V_{FB}
	Low threshold (V_{FB_PGOOD} / V_{FB})	V_{FB} falling		77	82	86	
	V_{PGOOD}	I_{PGOOD} = -1 mA			0.4		V
Reference section							
V_{REF}	Reference voltage	Vcc = 2.9 V to 18 V		1.756	1.8	1.837	V
			(1)	1.754	1.8	1.852	V
	Line regulation	Vcc = 2.9 V to 18 V I_{REF} = 0 mA			6	12	mV
	Load regulation	I_{REF} = 0 to 5 mA			7.5	15	mV
	Short circuit current			12	18	24	mA
Protections							
V_{FB_OVP}	Overvoltage trip (V_{FB_OVP} - V_{FB}) / V_{FB}	V_{FB} rising		15	20	24	%
Bus thresholds							
TH1	- UVLO 3.3 V bus - OVP not latched - No sink		(3)	0		0.2	V
TH2	- UVLO 3.3 V bus - OVP not latched - Sink		(3)	0.26		0.425	V
TH3	- UVLO 3.3 V bus - OVP latched - No sink		(3)	0.48		0.65	V

Table 4. Electrical characteristic (continued)

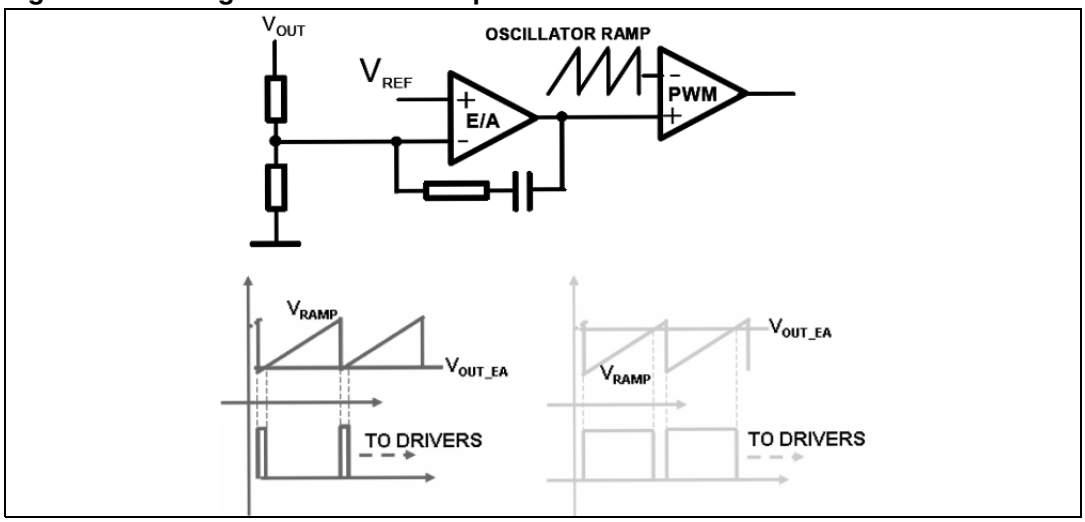
Symbol	Parameter	Test condition		Min	Typ	Max	Unit
TH4	- UVLO 3.3 V bus - OVP latched - Sink		(3)	0.71		0.875	V
TH5	- UVLO 12 V bus - OVP not latched - No sink		(3)	0.93		1.085	V
TH6	- UVLO 12 V bus - OVP not latched - Sink		(3)	1.16		1.31	V
TH7	- UVLO 12 V bus - OVP latched - No sink		(3)	1.385		1.525	V
TH8	- UVLO 12 V bus - OVP latched - Sink		**(3)**	1.615		VREF	V

1. Specification over the junction temperature range (T_J) of -40 to +125 °C are guaranteed by design, characterization and statistical correlation
2. Guaranteed by design
3. V_{CC} = 4 V

5 Functional description

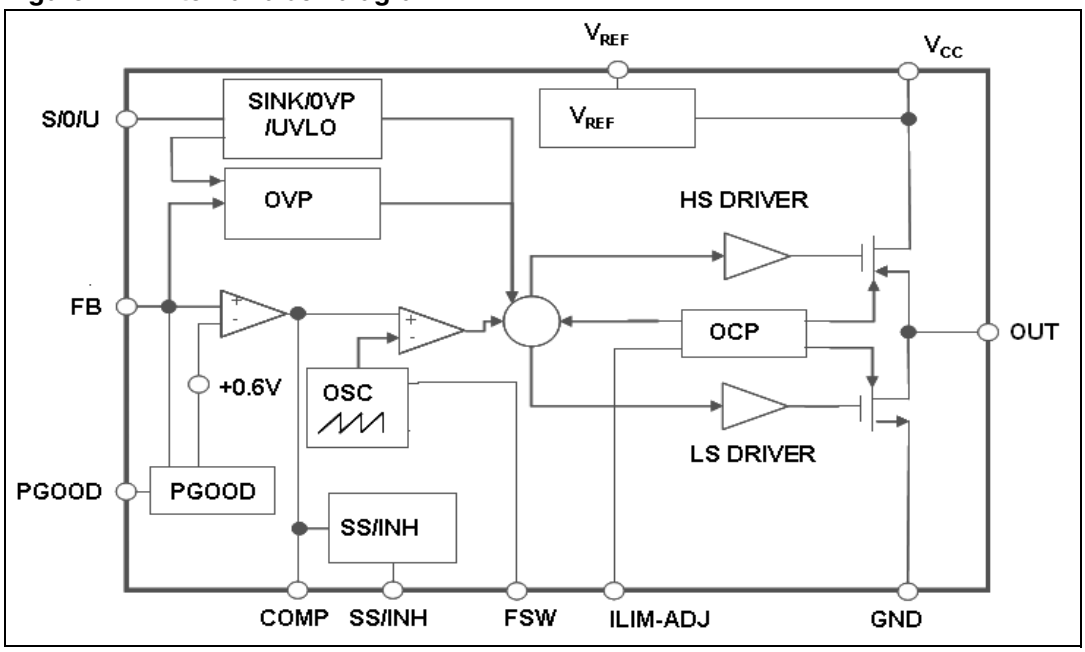
The L5989D is based on a voltage mode control loop. Therefore the duty ratio of the internal switch is obtained through a comparison between a saw-tooth waveform (generated by an oscillator) and the output voltage of the error amplifier as shown in *Figure 3.* The advantage of this technique is the very short conduction time of the power elements thanks to the proper operation of the control loop without a precise current sense, which instead is required in current mode regulators. Thanks to this architecture the L5989D supports extremely low conversion ratio (D = V_{OUT}/V_{IN}) even at very high switching frequency (up to 1 MHz).

Figure 3. Voltage mode control loop



The main internal blocks are represented in *Figure 4.*

Figure 4. Internal block diagram



Below follows a brief description of the main blocks:

- A voltage pre-regulator supplies the internal circuitry. The external 1.8 V voltage reference is supplied by this regulator.
- A voltage monitor circuit that checks the input and internal voltages
- A fully integrated sawtooth oscillator whose frequency is 400 kHz ± 10% when the Fsw pin is floating. Its frequency can be increased/decreased connecting a proper resistor to GND or VREF
- The internal current limitation circuitry monitors the current flowing in both embedded switches to guarantee an effective protection even in extreme duty cycle conditions
- The over voltage protection (OVP) monitors the feedback voltage. If the voltage of this pin overcomes the 20% of the internal reference value (600 mV ± 1%) it will force the conduction of the low side switch until the overshoot is present
- A voltage mode amplifier. The inverting input and the output are externally available for compensation
- A pulse width modulator (PWM) comparator and the relative logic to drive the embedded switches
- The soft-start circuit charges an external capacitor with a constant current equal to 20 µA (typ.). The soft-start feature is realized clamping the output of the error amplifier until the voltage across the capacitor is below 2.7 V
- The PGOOD is an open collector output: low impedance if the feedback voltage is lower than 0.85 times the internal reference of the error amplifier. An hysteresis is provided
- The circuitry related to the UOS multifunction pin is composed of a 3 bit A/D converter and the decoding logic. It recognizes eight different voltage windows of a VREF voltage magnitude for selecting additional features.
- An inhibit block for stand-by operation
- A circuit to realize the thermal protection function

5.1 Multifunction pin

The UOS pin is used to configure the device additional features accordingly to the voltage bias imposed through VREF voltage partitioning.

The selectable options are:

- UVLO level: two pre-defined the under voltage lock out thresholds can be selected to match the 3.3 V and 5 V or 12 V power bus
- SINK capability: this feature is always disabled during the soft-start period to be compatible with pre-biased output voltages. After the soft-start phase, the synchronous rectification can be enabled or not depending on the status of the UOS pin. Anyway, in case an overvoltage is detected, the sink capability is always enabled to bring the FB back to regulation as fast as possible
- OVP management: in case the latched mode is selected and an overvoltage event recurs, the switching activity will be suspended until VCC is reapplied or the SS/$\overline{\text{INH}}$ pin is toggled. Otherwise when the overvoltage transient is ended the regulator will work accordingly to the load request without regulation discontinuity

The circuitry related to the UOS multifunction pin is composed of a 3 bit A/D converter and the decoding logic. *Table 5* shows the internal thresholds of each voltage window

composing the VREF magnitude. The voltage biasing of the multifunction can be set accordingly to table *Table 6.*

Table 5. A/D voltage windows

	UVLO	OVP	SINK
1.8 V	12 V BUS	Latch	Sink
1.575 V	12 V BUS	Latch	No sink
1.35 V	12 V BUS	No latch	Sink
1.125 V	12 V BUS	No latch	No sink
0.9 V	3.3 V BUS	Latch	Sink
0.675 V	3.3 V BUS	Latch	No sink
0.45 V	3.3 V BUS	No latch	Sink
0.225 V	3.3 V BUS	No latch	No sink
0 V			

Table 6. UOS voltage biasing

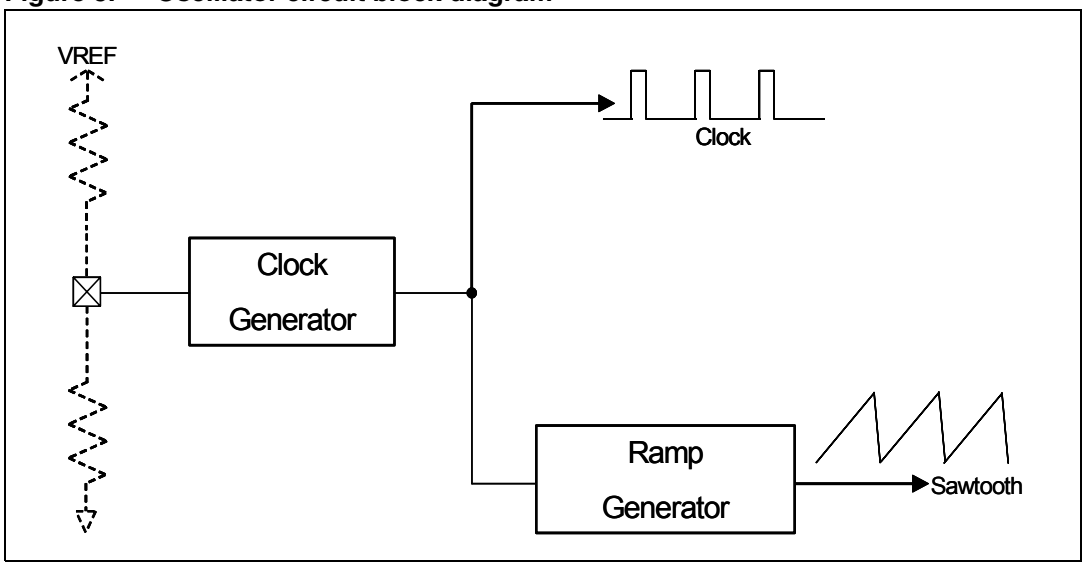
R1 (kΩ)	R2 (kΩ)	V_{OUS}(V)	UVLO	OVP	SINK
0	N.C.	1.8	12 V bus	Latch	Sink
0.68	2.7	1.438	12 V bus	Latch	No sink
1.2	2.7	1.246	12 V bus	No latch	Sink
2	2.7	1.034	12 V bus	No latch	No sink
3.3	2.7	0.810	3.3 V bus	Latch	Sink
6.2	2.7	0.546	3.3 V bus	Latch	No sink
11	2.7	0.355	3.3 V bus	No latch	Sink
N.C.	0	0	3.3 V bus	No latch	No sink

5.2 Oscillator

The generation of the internal saw-tooth waveform is based on the constant current charge / discharge of an internal capacitor. The current generator is designed to get a switching frequency of 400 kHz ± 10% in case the FSW pin is left floating.

The current mirror connected to FSW (see *Figure 5*) pin acts increasing / decreasing the value of the internal charging current to adjust the oscillator frequency. Since the internal circuitry forces the FSW voltage bias at 1.235 V, the user can easily source / sink current in this pin connecting a pull up resistor to VREF or a pull down to GND respectively.

Figure 5. Oscillator circuit block diagram



The value of the pull up resistor versus VREF to decrease the oscillator frequency follows the formula:

$$R_1(K\Omega) = \frac{8.5 \cdot 10^3}{400 - F_{SW}(KHz)} + 0.95$$

In the same way to increase the switching frequency the pull down resistor is selected using the formula:

$$R_2(K\Omega) = \frac{18 \cdot 10^3}{F_{SW}(KHz) - 400} - 2.1$$

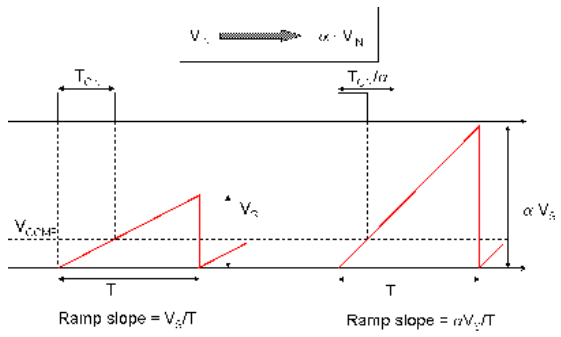
Table 10 shows some resistor values to adjust the oscillator frequency

Table 7. FSW resistor examples

R1 (kΩ)	f_{SW} (kHz)	R2 (kΩ)	f_{SW} (kHz)
43	198	360	450
47	215	180	499
56	245	120	548
62	261	91	594
82	295	56	711
110	322	43	801
150	343	33	915
220	361	27	1022

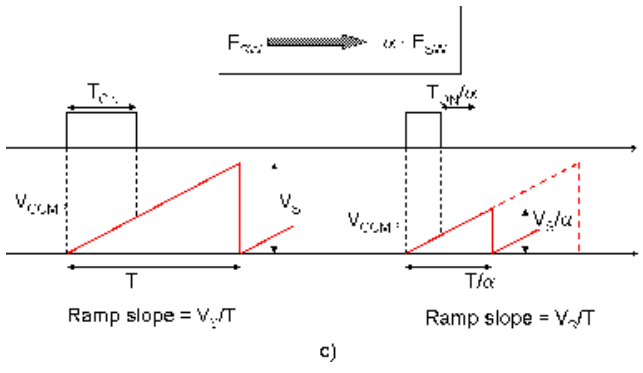
To improve the line transient performance, the voltage feed forward is implemented by changing the slope of the sawtooth according to the input voltage change (see *Figure 6* a).

Figure 6. Sawtooth: voltage feed forward



The slope of the sawtooth does not change if the oscillator frequency is increased by an external signal or adjusted by the external resistor (see *Figure 7*). As a consequence the gain of the PWM stage is a function of the switching frequency and its contribution must be taken in account when performing the calculations of the compensation network (see *Chapter 6.4.1* and *Chapter 6.4.2*).

Figure 7. Sawtooth: frequency adjust



5.3 External voltage reference

An external 1.8 V regulated voltage is provided. This reference is useful to set the voltage at the multifunction pin (see *Chapter 5.1*) or to source current to ILIM-ADJ and FSW pins (see and *Chapter 5.5.2*). The typical current capability is 4 mA.

5.4 Soft-start

When VCC is above the selected UVLO threshold the start-up phase takes place. At start-up, a voltage ramp is generated charging the external capacitor C_{SS} with an internal current generator. The device is in inhibit mode as long as SS/$\overline{INH}$ pin is below the INH threshold.

The L5989D implements the soft-start phase by clamping the output of the error amplifier and, being based on a voltage mode control, the duty cycle. In fact the comparison between the output of the error amplifier and the internal saw tooth waveform generates the duty cycle needed to keep the output voltage in regulation.

Two different current sources charge the external capacitor depending on the pin voltage in order to reduce the power consumption in INH mode.

$$I_{SS} = \begin{cases} I_{SS1} = 5\mu A & 0 < V_{SS/INH} < 1 \\ I_{SS2} = 22\mu A & 1 < V_{SS/INH} < 2.9 \end{cases}$$

The equation for the soft-start time is:

$$T_{SS} = \Delta T_1 + \Delta T_2 = \frac{C_{SS}}{I_{SS1}} \times (1-0) + \frac{C_{SS}}{I_{SS2}} \times (2.9-1)$$

Considering I_{SS2}/I_{SS1} = 22/5 = 4.4, the proper soft-start capacitor is simply calculated as follows:

$$C(nF) = Tss(mS) \times 3.5$$

During the soft-start phase (V_{SS} < 2.9 V):

- the sink capability is always disabled (independently from the multifunction pin settings) to be compatible with pre-biased output voltage
- in case the overcurrent limit is detected, a constant current protection is provided in order to deliver extra current for charging the output capacitor (see *Chapter 5.5.2* for description of current protection management).

During normal operation the C_{SS} is discharged with a constant current of 22 µA (typ.) only if:

- HICCUP mode is triggered (see *Chapter 5.5.2*)
- the input voltage goes below the UVLO threshold (see *Chapter 5.5.3*)
- the internal temperature is over 150°C (see *Chapter 5.5.4*)

A new SS cycle will start when the V_{SS} drops below the INH threshold.

New high performance ICs often require more than one supply voltage. Most of these applications require well defined start-up sequencing, in order to avoid potential damage and latch-up of the processing core. Sharing the same soft-start capacitor for a set of regulators, the output voltages increase with the same slew rate implementing a “simultaneous start-up” sequencing method.

5.5 Monitoring and protections

5.5.1 Overvoltage

The device provides the overvoltage protection monitoring the output voltage through the FB pin. If the voltage sensed on FB pin reaches a value 20% (typ.) greater than the reference of the error amplifier, the low-side MOSFET is turned on to discharge as fast as possible the output capacitor. It is possible to set two different behaviors in case of OVP:

- In case the OVP latched mode is active (see *Chapter 5.1*), the internal oscillator is suspended and the low side switch will be kept on until the input voltage goes below the selected UVLO threshold or the SS/$\overline{\text{INH}}$ pin is forced below the INH threshold.
- In case of NOT latched OVP mode is active, the low side MOS is forced ON until the feedback voltage is higher than the OVP threshold (20% greater than the reference of the error amplifier).

Figure 8. OVP not latched

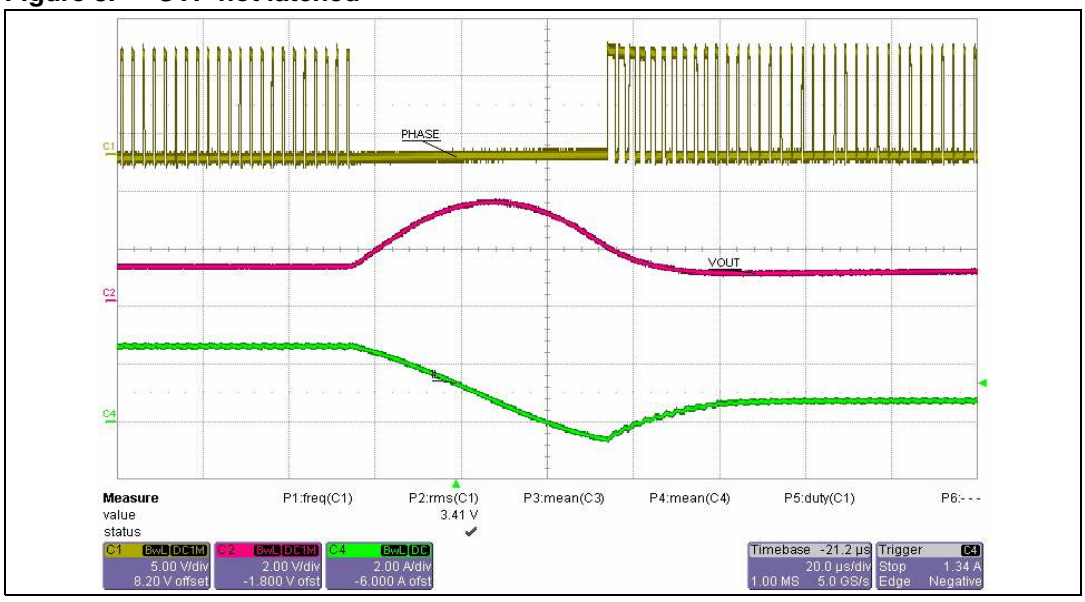
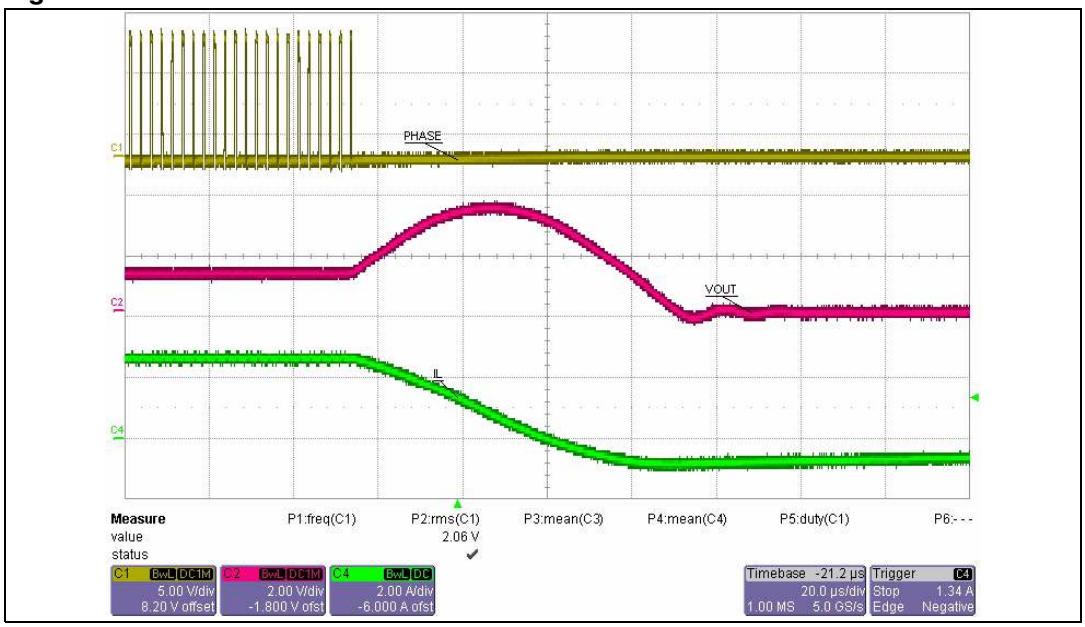


Figure 9. OVP latched



5.5.2 Current limiting

The current limiting feature acts in different ways depending on the operative conditions.

- In case an overcurrent detection happens after the soft-start phase, the internal logic will trigger the “HICCUP” mode. Both switches are turned off and the soft-start capacitor is discharged with a constant current of 22 µA (typ.). When the SS/$\overline{\text{INH}}$ voltage drops below the INH threshold a new SS cycle will start.
- During the soft-start phase the overcurrent information is used to provide a constant current protection. In this way additional current is available to charge the output capacitor during power up.

The most common way is to sense the current flowing through the power MOSFETs. However, due to the noise created by the switching activity of the power MOSFETs, the current sense is disabled during the initial phase of the conduction time. This avoids an erroneous detection of a fault condition. This interval is generally known as “masking time” or “blanking time”. For this reason, the current cannot be sensed through the high-side MOSFET in the case of extremely low duty cycles, nor through the low-side MOSFET in the case of very high duty cycles.

The L5989D assures the effective protection sensing the current flowing in both embedded switches. The protection achieved by sensing the current in the high-side MOSFET is called “peak overcurrent protection”, while the protection achieved by sensing the current in the low-side MOSFET is called “valley overcurrent protection”. When the current limit is reached during normal operation, the so called HICCUP mode is triggered, and the soft-start cap is discharged and recharged. However, during the start-up phase, additional current is required to charge the output capacitor. This could continuously trigger the HICCUP intervention preventing the system from reaching a steady working condition. For this reason the HICCUP feature is disabled during the start-up phase and a constant current mode is active to charge the output capacitor. In this case, when the peak current limit is triggered after a conduction time equal to the “masking time”, the high-side MOSFET is turned off and the low side MOSFET is kept on until the flowing current goes below the “valley” current limit. If necessary, some switching pulses are skipped, as illustrated in *Figure 10*. Thus, the combination of the “peak” and “valley” current limits assure the effectiveness of the overcurrent protection even in extreme duty cycle conditions. The current threshold of the low side is designed higher than the high side one to guarantee the proper protection.

The constant current mode during the soft-start phase limits the maximum current up to:

$$I_{MAX} = I_{VALLEY\_TH} + \frac{V_{IN} - V_{OUT}}{L} \cdot T_{MASK}$$

The overcurrent limit protection is adjustable (higher or lower than the nominal value) through an external resistor. To guarantee effective protection, both thresholds (valley and peak) are in tracking.

The typical active thresholds in case of ILIM-ADJ pin left floating are I_{PEAK_TH} = 4.0 A, I_{VALLEY_TH} = 4.58 A. The dimensioning of the pull up resistor versus VREF to decrease the peak (and valley) thresholds follows the formula:

$$R_3(k\Omega) = \frac{270.6}{Ipk(A) - 4.026}, \qquad Ivy(A) = \left(\frac{287}{R_3(k\Omega)}\right) + 4.58$$

In the same way the pull down resistor is selected using the following formula to increase the maximum current thresholds:

$$R_9(k\Omega) = \frac{120}{4.026 - Ipk(A)}, \qquad Ivy(A) = 4.58 - \left(\frac{127}{R_9(k\Omega)}\right)$$

Figure 10. Constant current protection at extreme duty cycles

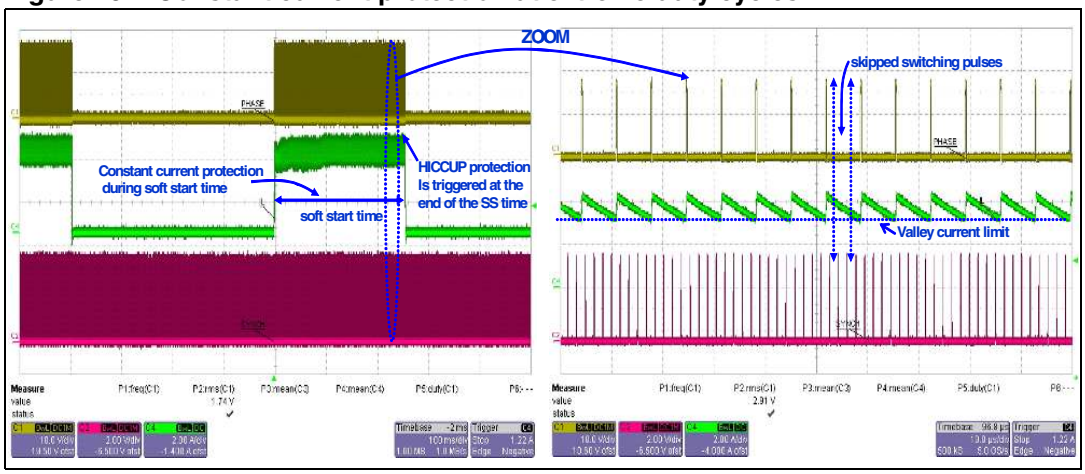


Table 8 shows some resistor values to adjust the current limits

Table 8. ILIM-ADJ resistor examples

R9(kΩ)	$I_{LIM\ PEAK}$(A)	$I_{LIM\ VALLEY}$(A)	R3(kΩ)	$I_{LIM\ PEAK}$(A)	$I_{LIM\ VALLEY}$(A)
43	1.24	1.62	1500	4.2	4.75
47	1.47	1.87	750	4.38	4.95
56	1.88	2.31	470	4.6	5.18
68	2.26	2.71	330	4.8	5.42
91	2.71	3.18	270	5.0	5.62
120	3.03	3.52	220	5.20	5.82
200	3.43	3.94	180	5.50	6.12
560	3.81	4.35	160	5.70	6.30

5.5.3 UVLO

The under-voltage-lock-out (UVLO) is adjustable by the multifunction pin (see *Chapter 5.1*). It is possible to set two different thresholds:

- 2.9 V for 3.3 V BUS
- 8 V for 12 V BUS

5.5.4 Thermal shutdown

When the junction temperature reaches 150 °C the device enters in thermal shutdown. Both MOSFETs are turned off and the soft-start capacitor is discharged with a current of 22 µA. The device doesn't restart until the junction temperature goes down to 120 °C.

5.6 Power Good

An internal comparator monitors the FB to drive the PGOOD open collector output.

The voltage reference of the comparator is 85% typ. of the nominal FB voltage (0.6V) and an hysteresis of 5% typ. is provided to increase the noise immunity of the circuitry.

$$V_{RISING} = 0.85 \cdot V_{FB} \cdot \left(1 + \frac{R_8}{R_6}\right)$$

$$V_{FALLING} = 0.80 \cdot V_{FB} \cdot \left(1 + \frac{R_8}{R_6}\right)$$

The PGOOD output is driven in low impedance state as long as the output voltage is lower than V_{RISING} threshold, otherwise released in high impedance.

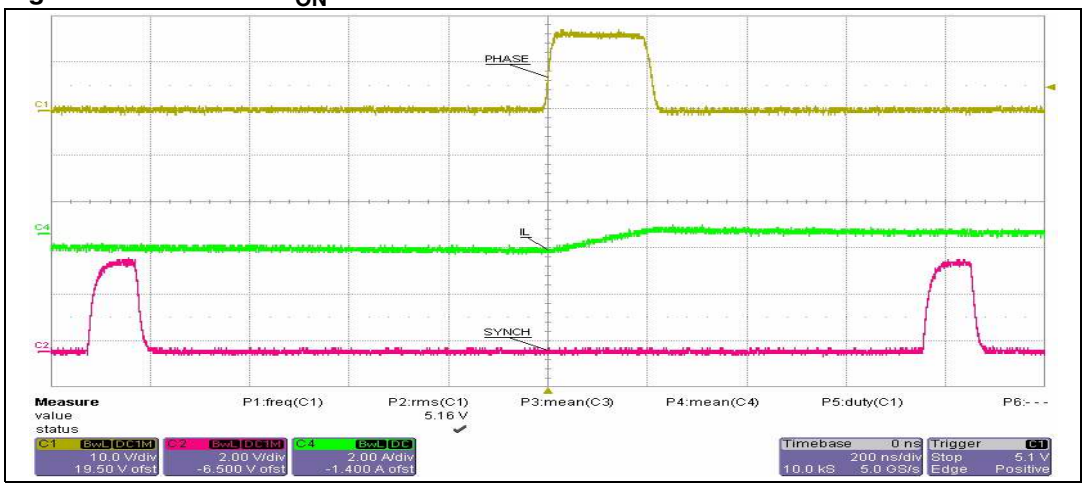
In case the output voltage drops below the $V_{FALLING}$ threshold the PGOOD output goes in low impedance.

In case an external type III compensation network is used (see *Chapter 6.4.1*), the leading network across the resistor R_8 could introduce a phase shift of the sensed FB voltage respect to the output voltage during load transitions.

5.7 Minimum on time

The L5989D is based on a voltage mode control loop. The advantage of this technique is the very short conduction time of the power elements thanks to the proper functioning of the control loop without a current sense (that is challenging with low conduction times), which instead is required in current mode regulators. The optimized architecture, the design solutions and the high performance fabrication technique allow power elements to achieve extremely short conduction times. This allows very high switching frequency operation even in very low duty cycle applications. *Figure 11* shows how the L5989D can easily manage a minimum conduction time of 200 ns. Moreover, thanks to the embedded P-MOS used for the high-side, no bootstrap capacitor is required. This means that the device is able to manage a duty cycle of 100%.

Figure 11. Minimum T_{ON}



5.8 Error amplifier

The error amplifier (E/A) provides the error signal to be compared with the sawtooth to perform the Pulse Width Modulation. Its non-inverting input is internally connected to a 0.6 V voltage reference, while its inverting input (FB) and output (COMP) are externally available for feedback and frequency compensation. In this device the error amplifier is a voltage mode operational amplifier so with high DC gain and low output impedance.

The uncompensated error amplifier characteristics are the following:

Table 9. Uncompensated error amplifier

Low frequency gain	100 dB
GBWP	4.5 MHz
Slew rate	7 V/µs
Output voltage swing	0 to 3.3 V
Maximum source/sink current	25 mA / 40 mA

In continuos conduction mode (CCM), the transfer function of the power section has two poles due to the LC filter and one zero due to the ESR of the output capacitor. Different kinds of compensation networks can be used depending on the ESR value of the output capacitor. In case the zero introduced by the output capacitor helps to compensate the double pole of the LC filter a type II compensation network can be used. Otherwise, a type III compensation network has to be used (see *Chapter 6.4* for details about the compensation network selection).

Anyway the methodology to compensate the loop is to introduce zeros to obtain a safe phase margin.

6 Application information

6.1 Input capacitor selection

The capacitor connected to the input has to be capable to support the maximum input operating voltage and the maximum RMS input current required by the device. The input capacitor is subject to a pulsed current, the RMS value of which is dissipated over its ESR, affecting the overall system efficiency.

So the input capacitor must have a RMS current rating higher than the maximum RMS input current and an ESR value compliant with the expected efficiency.

The maximum RMS input current flowing through the capacitor can be calculated as:

$$I_{RMS} = I_O \cdot \sqrt{D - \frac{2 \cdot D^2}{\eta} + \frac{D^2}{\eta^2}}$$

Where Io is the maximum DC output current, D is the duty cycles, η is the efficiency. This function has a maximum at D = 0.5 and, considering η = 1, it is equal to Io/2.

In a specific application the range of possible duty cycles has to be considered in order to find out the maximum RMS input current. The maximum and minimum duty cycles can be calculated as:

$$D_{MAX} = \frac{V_{OUT} + \Delta V_{LOW\_SIDE}}{V_{INMIN} + \Delta V_{LOW\_SIDE} - \Delta V_{HIGH\_SIDE}}$$

and

$$D_{MIN} = \frac{V_{OUT} + \Delta V_{LOW\_SIDE}}{V_{INMAX} + \Delta V_{LOW\_SIDE} - \Delta V_{HIGH\_SIDE}}$$

Where ΔV_{HIGH_SIDE} and ΔV_{LOW_SIDE} are the voltage drops across the embedded switches.

The peak to peak voltage across the input filter can be calculated as:

$$V_{PP} = \frac{I_O}{C_{IN} \cdot f_{SW}} \cdot \left[\left(1 - \frac{D}{\eta}\right) \cdot D + \frac{D}{\eta} \cdot (1 - D)\right] + ESR \cdot I_O$$

Given a physical dimension, ceramic capacitors can met well the requirements of the input filter substaining an higher input current than electrolytic / tantalum types. In this case the equation of C_{IN} as a function of the target V_{PP} can be written as follows:

$$C_{IN} = \frac{I_O}{V_{PP} \cdot f_{SW}} \cdot \left[\left(1 - \frac{D}{\eta}\right) \cdot D + \frac{D}{\eta} \cdot (1 - D)\right]$$

Considering $\eta=1$ this function has its maximum in D = 0.5:

$$C_{IN\_MIN} = \frac{I_O}{2 \cdot V_{PP\_MAX} \cdot f_{SW}}$$

Typically C_{IN} is dimensioned to keep the maximum peak-peak voltage across the input filter in the order of 1% V_{IN_MAX}

Table 10. Input capacitors

Manufacture	Series	Cap value (µF)	Rated voltage (V)
MURATA	GRM31	10	25
	GRM55	10	25
TDK	C3225	10	25

6.2 Inductor selection

The inductance value fixes the current ripple flowing through the output capacitor. So the minimum inductance value in order to have the expected current ripple has to be selected. The rule to fix the current ripple value is to have a ripple at 20%-40% of the output current. The inductance value can be calculated by the following equation:

$$\Delta I_L = \frac{V_{IN} - V_{OUT}}{L} \cdot T_{ON} = \frac{V_{OUT}}{L} \cdot T_{OFF}$$

Where T_{ON} and T_{OFF} are the on and off time of the internal power switch. The maximum current ripple, at fixed Vout, is obtained at maximum T_{OFF} that is at minimum duty cycle (see previous section to calculate minimum duty). So fixing ΔI_L = 20% to 40% of the maximum output current, the minimum inductance value can be calculated:

$$L_{MIN} = \frac{V_{OUT} + V_F}{\Delta I_{MAX}} \cdot \frac{1 - D_{MIN}}{F_{SW}}$$

where F_{SW} is the switching frequency $1/(T_{ON} + T_{OFF})$.

For example for V_{OUT} = 3.3 V, V_{IN} = 12 V, I_O = 4 A and F_{SW} = 400 kHz the minimum inductance value to have ΔI_L = 30% of I_O is about 4.7 µH.

The peak current through the inductor is given by:

$$I_{L,PK} = I_O + \frac{\Delta I_L}{2}$$

So if the inductor value decreases, the peak current (that has to be lower than the current limit of the device) increases. The higher is the inductor value, the higher is the average output current that can be delivered, without reaching the current limit.

In the table below some inductor part numbers are listed.

Table 11. Inductors

Manufacturer	Series	Inductor value (µH)	Saturation current (A)
Coilcraft	XPL7030	2.2 to 4.7	6.8 to 10.5
	MSS1048	2.2 to 6.8	4.14 to 6.62
	MSS1260	10	5.5
Panasonic	ETQP5M4R7YFM	4.7	8
Wurth	WE-HC/HCA	3.3 to 4.7	7 to 11
	WE-TPC type XLH	3.6 to 6.2	4.5 to 6.4
	WE-PD type L	10	5.6
Coiltronics	DR74	3.3 to 4.7	4.3 to 5.4
	DR125	10	5.3
BI	HM78-60	4.7 to 10	5.4 to 6.8
SUMIDA	HM78-60	4.7 to 10	5.4 to 6.8

6.3 Output capacitor selection

The current in the capacitor has a triangular waveform (with zero average value) which generates a voltage ripple across it. This ripple is due to the capacitive component and the resistive component (ESR). So the output capacitor has to be selected in order to have a voltage ripple compliant with the application requirements.

The amount of the voltage ripple can be calculated starting from the current ripple obtained by the inductor selection.

$$\Delta V_{OUT} = ESR \cdot \Delta I_{MAX} + \frac{\Delta I_{MAX}}{8 \cdot C_{OUT} \cdot f_{SW}}$$

Usually the resistive component of the ripple is much higher than the capacitive one, if the output capacitor adopted is not a multi layer ceramic capacitor (MLCC) with very low ESR value.

The output capacitor is important also for loop stability: it fixes the double LC filter pole and the zero due to its ESR. In *Chapter 6.4*, it will be illustrated how to consider its effect in the system stability.

For example with V_{OUT} = 3.3 V, V_{IN} = 12 V, ΔI_L = 0.6 A (resulting by the inductor value), in order to have a $\Delta V_{OUT} = 0.01 \cdot V_{OUT}$, if the multi layer capacitor are adopted, 10 µF are needed and the ESR effect on the output voltage ripple can be neglected. In case of not negligible ESR (electrolytic or tantalum capacitors), the capacitor is chosen taking into account its ESR value. So 100 µF with ESR = 40 mΩ is compliant with the requested output voltage ripple.

The output capacitor is also important to sustain the output voltage when a load transient with high slew rate is required by the load. When the load transient slew rate exceeds the

system bandwidth the output capacitor provides the current to the load. So if the high slew rate load transient is required by the application the output capacitor and system bandwidth have to be chosen in order to sustain load transient and to have a fast response to the transient.

In the table below some capacitor series are listed.

Table 12. Output capacitors

Manufacturer	Series	Cap value (µF)	Rated voltage (V)	ESR (mΩ)
MURATA	GRM32	22 to 100	6.3 to 25	< 5
	GRM31	10 to 47	6.3 to 25	< 5
PANASONIC	ECJ	10 to 22	6.3	< 5
	EEFCD	10 to 68	6.3	15 to 55
SANYO	TPA/B/C	100 to 470	4 to 16	40 to 80
TDK	C3225	22 to 100	6.3	< 5

6.4 Compensation network

The compensation network has to assure stability and good dynamic performance. The loop of the L5989D is based on the voltage mode control. The error amplifier is a voltage operational amplifier with high bandwidth. So selecting the compensation network the E/A will be considered as ideal, that is, its bandwidth is much larger than the system one.

The transfer functions of PWM modulator and the output LC filter are studied. The transfer function PWM modulator, from the error amplifier output (COMP pin) to the OUT pin, results:

$$G_{PW0}(f_{SW0}) = \frac{V_{IN}}{V_s} \cdot H(f_{SW0})$$

where V_S is the sawtooth amplitude and H represent its reliance on the switching frequency. As seen in *Chapter 5.2*, the voltage feed forward generates a sawtooth amplitude directly proportional to the input voltage, that is:

$$V_S(f_{SW0}) = K \cdot V_{IN} \cdot H(f_{SW0})$$

The internal saw tooth is designed in order to have the maximum amplitude at the natural switching frequency of the device.

At f_{SW0} = 400 kHz the PWM modulator can be written as:

$$G_{PW0}(400\ kHz) = \frac{1}{K} = \frac{V_{IN}}{V_S(400\ kHz)} = 9$$

The adjustment of the switching frequency through the FSW pin modify the gain of the internal saw tooth (see *Chapter 5.2*).

The PWM modulator gain is a function of the switching frequency:

$$G_{PW0}(f_{SW}) = G_{PW0}(400\ kHz) \cdot \frac{f_{SW}(kHz)}{400} = 9 \cdot \frac{f_{SW}(kHz)}{400}$$

The transfer function on the LC filter is given by:

$$G_{LC}(s) = \frac{1 + \frac{s}{2\pi \cdot f_{zESR}}}{1 + \frac{s}{2\pi \cdot Q \cdot f_{LC}} + \left(\frac{s}{2\pi \cdot f_{LC}}\right)^2}$$

where:

$$f_{LC} = \frac{1}{2\pi \cdot \sqrt{L \cdot C_{OUT}} \cdot \sqrt{1 + \frac{ESR}{R_{OUT}}}}, \qquad f_{zESR} = \frac{1}{2\pi \cdot ESR \cdot C_{OUT}}$$

$$Q = \frac{\sqrt{R_{OUT} \cdot L \cdot C_{OUT} \cdot (R_{OUT} + ESR)}}{L + C_{OUT} \cdot R_{OUT} \cdot ESR}, \qquad R_{OUT} = \frac{V_{OUT}}{I_{OUT}}$$

Two different kind of networks can compensate the loop depending on the output capacitor.

Type II network is used to compensate the loop with high ESR output capacitors, type III with low ESR output capacitors (MLCC). In the two following paragraph the guidelines to select the Type II and Type III compensation network are illustrated.

6.4.1 Type III compensation network

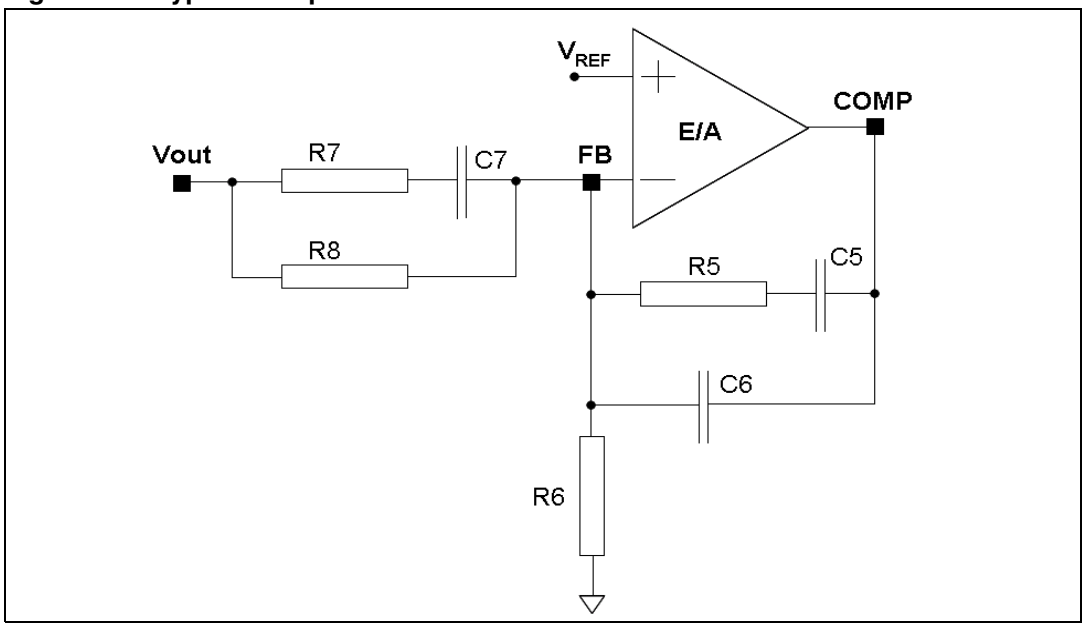
The methodology to stabilize the loop consists of placing two zeros to compensate the effect of the LC double pole, so increasing phase margin; then to place one pole in the origin to minimize the dc error on regulated output voltage; finally to place other poles far away the zero dB frequency.

In *Figure 12* the type III compensation network is shown. This network introduces two zeros (f_{Z1}, f_{Z2}) and three poles (f_{P0}, f_{P1}, f_{P2}). They expression are:

$$f_{Z1} = \frac{1}{2\pi \cdot C_7 \cdot (R_8 + R_7)}, \qquad f_{Z2} = \frac{1}{2\pi \cdot R_5 \cdot C_5}$$

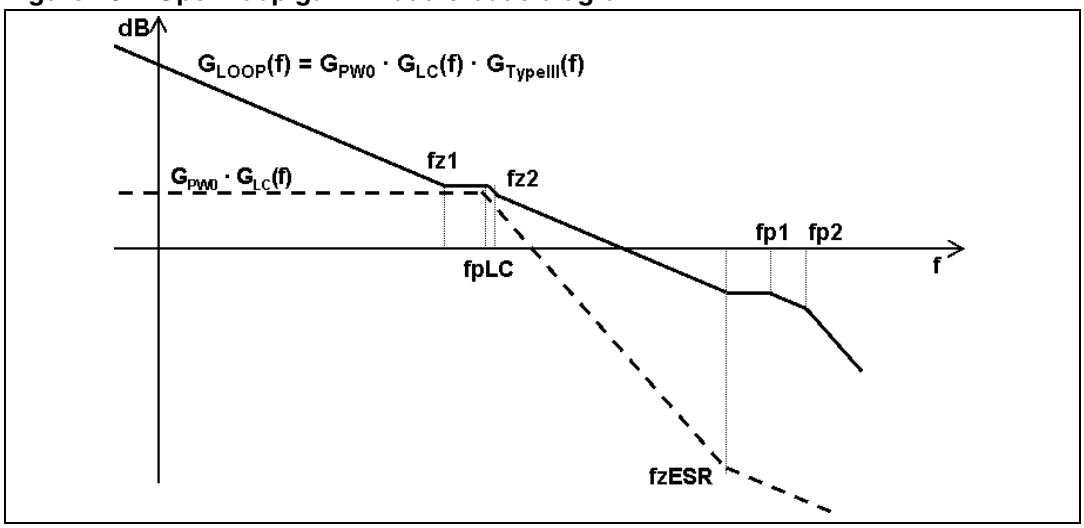
$$f_{P0} = 0, \qquad f_{P1} = \frac{1}{2\pi \cdot R_7 \cdot C_7}, \qquad f_{P2} = \frac{1}{2\pi \cdot R_5 \cdot \frac{C_5 \cdot C_6}{C_5 + C_6}}$$

Figure 12. Type III compensation network



In *Figure 13* the bode diagram of the PWM and LC filter transfer function ($G_{PW0} \cdot G_{LC}(f)$) and the open loop gain ($G_{LOOP}(f) = G_{PW0} \cdot G_{LC}(f) \cdot G_{TYPEIII}(f)$) are drawn.

Figure 13. Open loop gain: module bode diagram



The guidelines for positioning the poles and the zeroes and for calculating the component values can be summarized as follow:

1. Choose a value for R_1, usually between 1 kΩ and 5 kΩ.
2. Choose a gain (R_5/R_8) in order to have the required bandwidth (BW), that means:

$$R_5 = \frac{BW}{f_{LC}} \cdot K \cdot R_8$$

where K is the feed forward constant and 1/K is equals to 9.

3. Calculate C_5 by placing the zero at 50% of the output filter double pole frequency (f_{LC}):

$$C_5 = \frac{1}{\pi \cdot R_5 \cdot f_{LC}}$$

4. Calculate C_6 by placing the second pole at four times the system bandwidth (BW):

$$C_6 = \frac{C_5}{2\pi \cdot R_5 \cdot C_5 \cdot 4 \cdot BW - 1}$$

5. Set also the fist pole at four times the system bandwidth and also the second zero at the output filter double pole:

$$R_7 = \frac{R_8}{\frac{4 \cdot BW}{f_{LC}} - 1}, \qquad C_7 = \frac{1}{2\pi \cdot R_7 \cdot 4 \cdot BW}$$

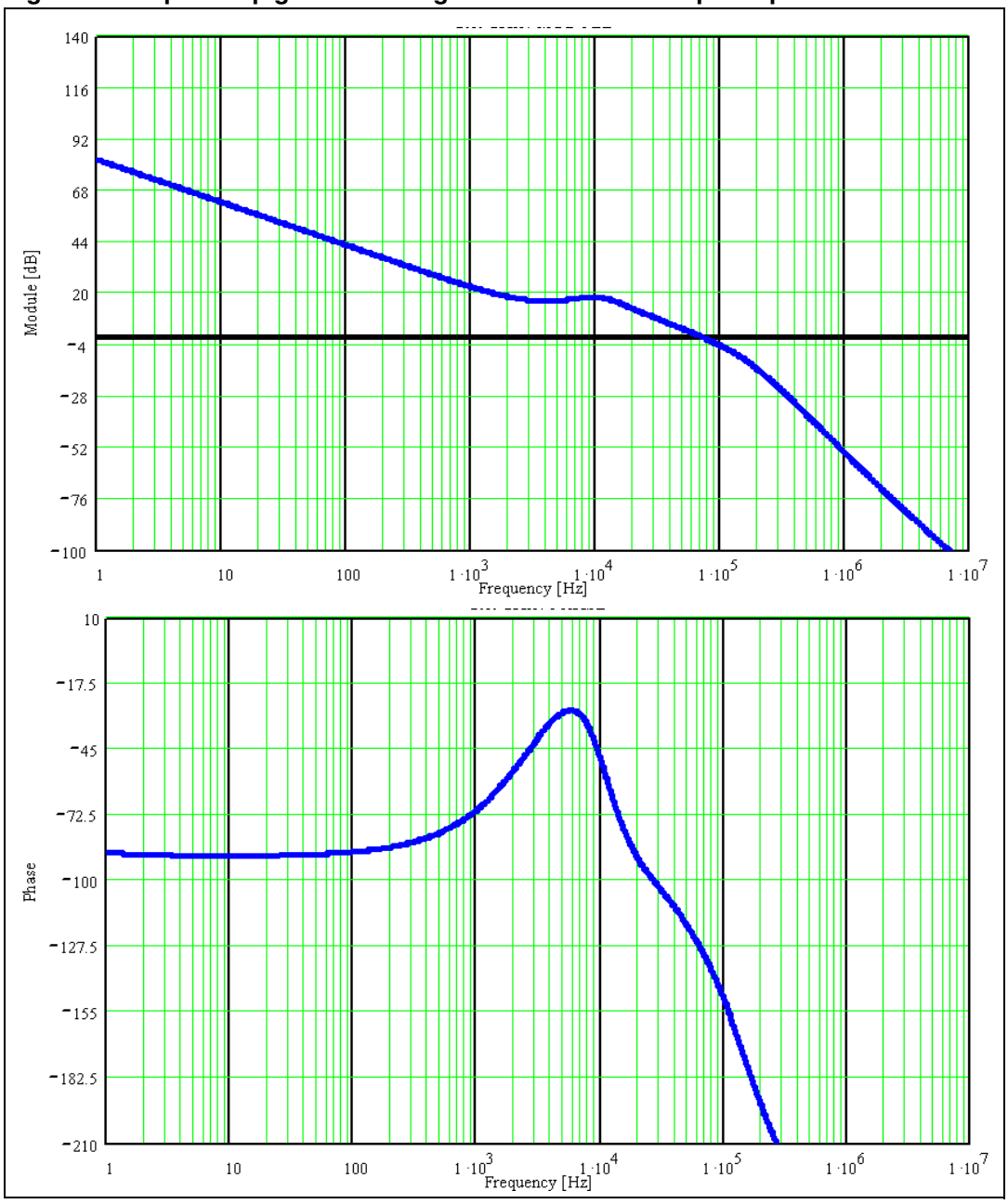
The suggested maximum system bandwidth is equals to the switching frequency divided by 3.5 ($F_{SW}/3.5$), anyway lower than 120kHz if the F_{SW} is set higher than 500 kHz.

For example with V_{OUT} = 1.2 V, V_{IN} = 12 V, I_O = 4 A, L = 4.7 µH, C_{OUT} = 47 µF, the type III compensation network is:

$R_8 = 4.7k\Omega$, $R_6 = 4.7k\Omega$, $R_7 = 180\Omega$, $R_5 = 3.3K\Omega$, $C_7 = 3.3nF$, $C_5 = 10nF$, $C_6 = 150pF$

In *Figure 14* is shown the module and phase of the open loop gain. The bandwidth is about 68 kHz and the phase margin is 50°.

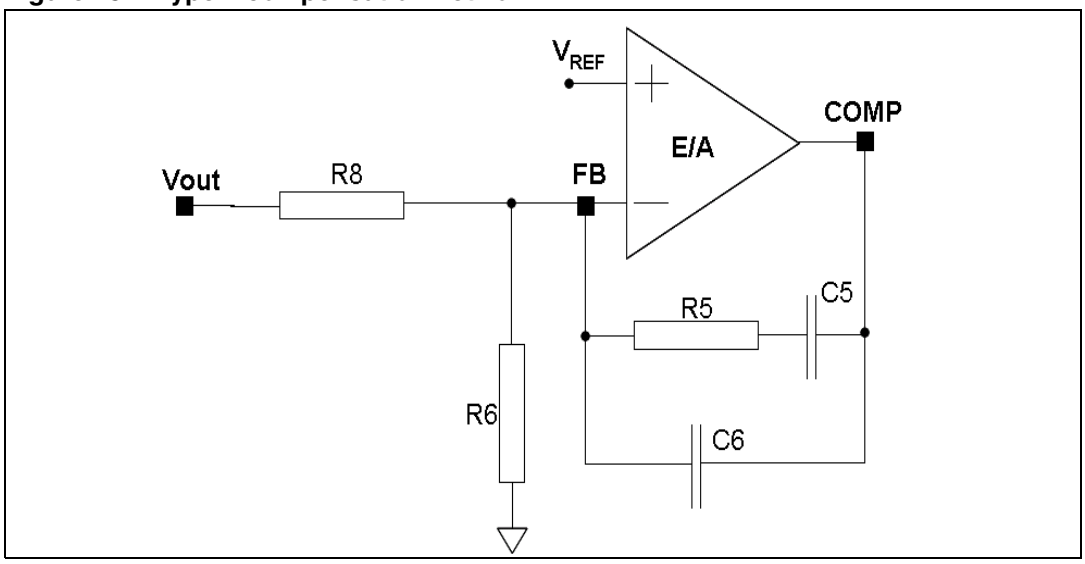
Figure 14. Open loop gain bode diagram with ceramic output capacitor



6.4.2 Type II compensation network

In *Figure 15* the type II network is shown.

Figure 15. Type II compensation network

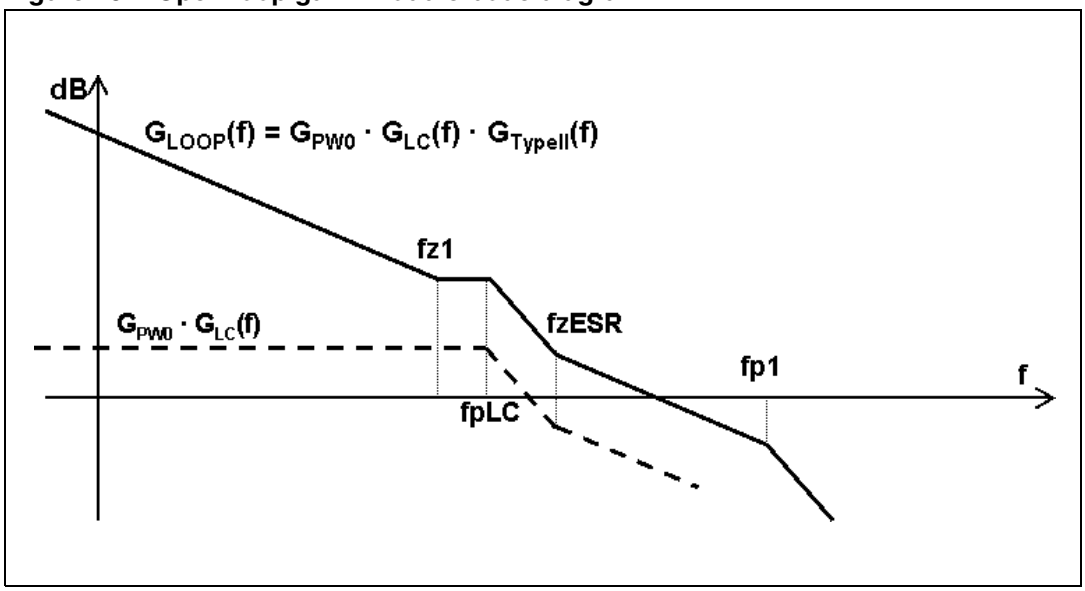


The singularities of the network are:

$$f_{Z1} = \frac{1}{2\pi \cdot R_5 \cdot C_5}, \quad f_{P0} = 0, \quad f_{P1} = \frac{1}{2\pi \cdot R_5 \cdot \frac{C_5 \cdot C_6}{C_5 + C_6}}$$

In *Figure 16* the bode diagram of the PWM and LC filter transfer function ($G_{PW0} \cdot G_{LC}(f)$) and the open loop gain ($G_{LOOP}(f) = G_{PW0} \cdot G_{LC}(f) \cdot G_{TYPEII}(f)$) are drawn.

Figure 16. Open loop gain: module bode diagram



The guidelines for positioning the poles and the zeroes and for calculating the component values can be summarized as follow:

1. Choose a value for R_8, usually between 1 kΩ and 5 kΩ, in order to have values of C5 and C6 not comparable with parasitic capacitance of the board.
2. Choose a gain (R_5/R_8) in order to have the required bandwidth (BW), that means:

$$R_5 = \left(\frac{f_{ESR}}{f_{LC}}\right)^2 \cdot \frac{BW}{f_{ESR}} \cdot \frac{V_S}{V_{IN}} \cdot R_8$$

Where f_{ESR} is the ESR zero:

$$f_{ESR} = \frac{1}{2\pi \cdot ESR \cdot C_{OUT}}$$

and Vs is the saw-tooth amplitude. The voltage feed forward keeps the ratio Vs/Vin constant.

3. Calculate C_5 by placing the zero one decade below the output filter double pole:

$$C_5 = \frac{10}{2\pi \cdot R_5 \cdot f_{LC}}$$

4. Then calculate C_7 in order to place the second pole at four times the system bandwidth (BW):

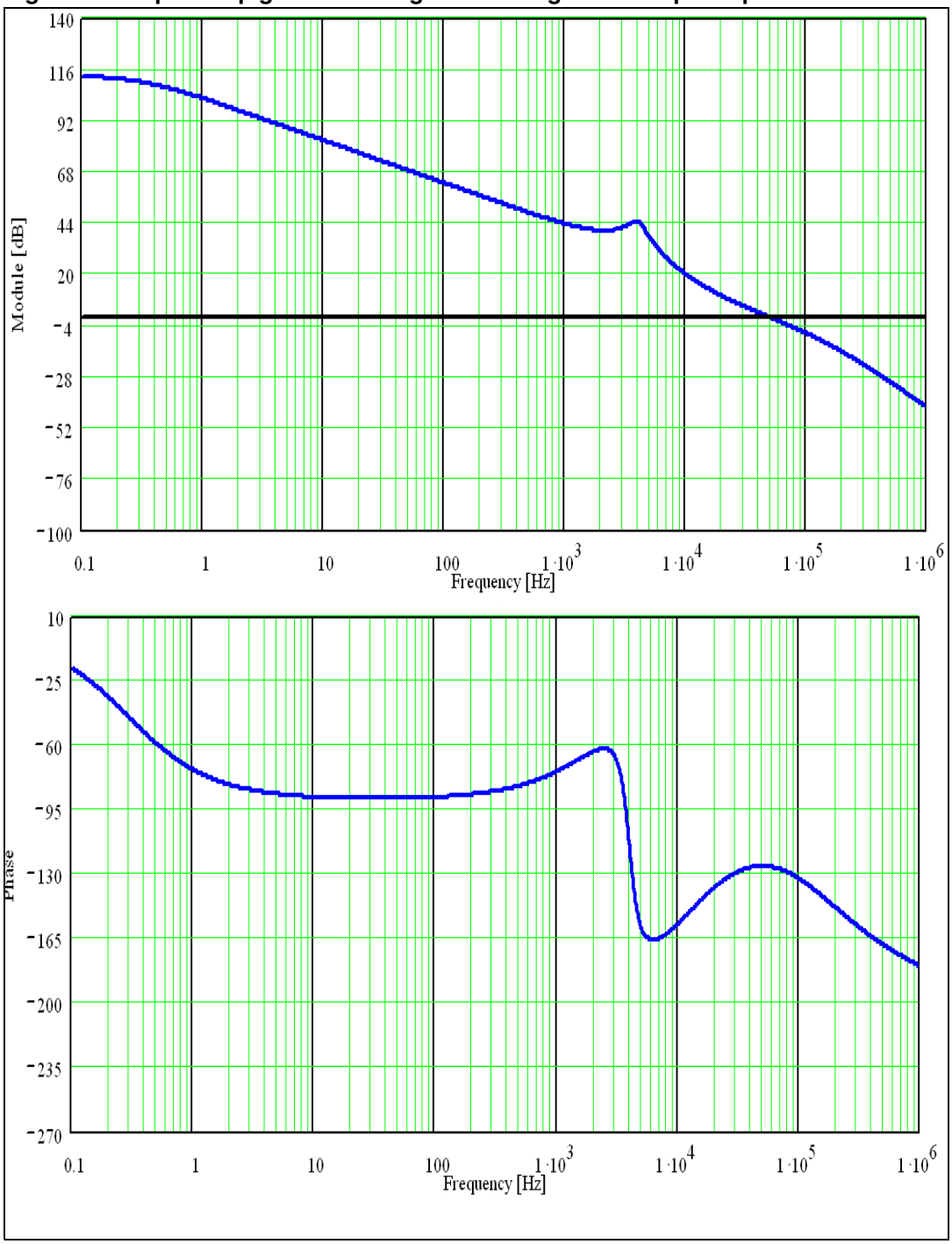
$$C_7 = \frac{C_5}{2\pi \cdot R_5 \cdot C_5 \cdot 4 \cdot BW - 1}$$

For example with V_{OUT} = 1.2V, V_{IN} = 12 V, I_O = 4 A, L = 4.7 µH, C_{OUT} = 330 µF, ESR = 35 mΩ, the type II compensation network is:

$$R_8 = 4.7k\Omega, \quad R_6 = 4.7K\Omega, \quad R_5 = 22k\Omega, \quad C_5 = 2.2nF, \quad C_6 = 33pF$$

In *Figure 17* is shown the module and phase of the open loop gain. The bandwidth is about 42 kHz and the phase margin is 56°.

Figure 17. Open loop gain bode diagram with high ESR output capacitor



The response of the system to a load transition in terms of output voltage regulation is affected not only by the designed compensation network but it also rely on the selection of the power components (the inductor value, for example, limits the slew rate of the current).

Some measurements of the output regulation during load transient for the examples are provided at the end of this document.

6.5 R.M.S. current of the embedded power MOSFETs

The L5989D integrates both the power elements (high side and low side) and so the power dissipation is often the bottleneck for the output current capability (refer to *Chapter 6.6* for the estimation of the operating temperature).

Nevertheless, as mentioned in *Description on page 6* the device can manage a continuos output current of 4 A in most of the application conditions.

However the rated continuos current is 5 A and the rated RMS current of the power elements is 4.5 A, where:

$$I_{RMS\ HS} = I_{LOAD} \cdot \sqrt{D}$$

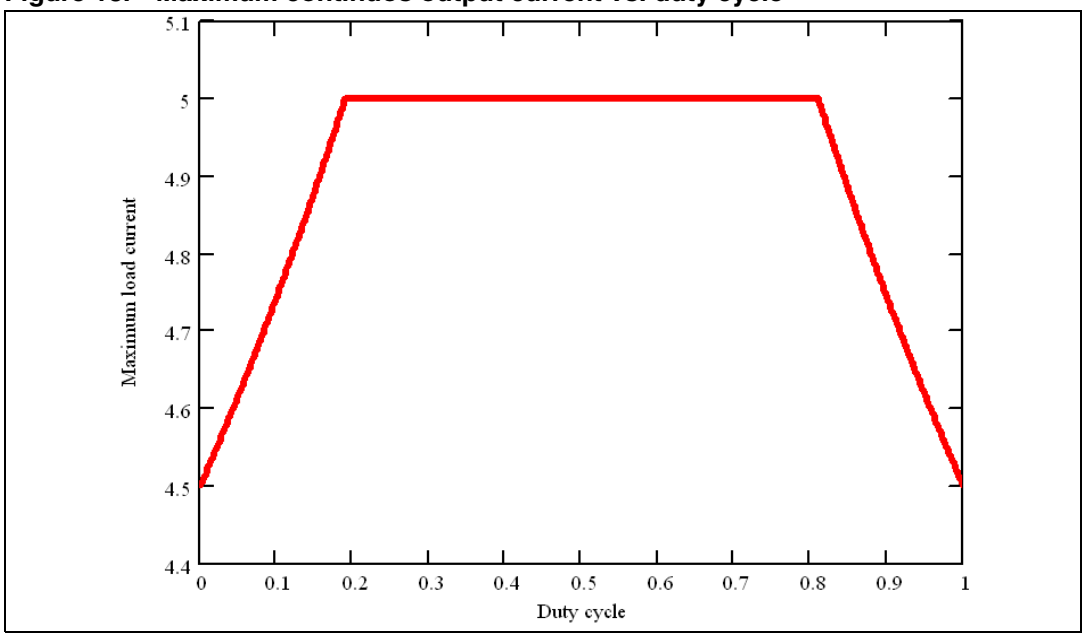
$$I_{RMS\ LS} = I_{LOAD} \cdot \sqrt{1 - D}$$

and the duty cycle D:

$$D = \frac{V_{OUT} + (R_{DS\ ON\ LS} + DCR) \cdot I_{LOAD}}{V_{IN} + (R_{DS\ ON\ LS} - R_{DS\ ON\ HS}) \cdot I_{LOAD}}$$

Fixing the limit of 4.5 A for $I_{RMS\ HS}$ and $I_{RMS\ LS}$ the maximum output current can be derived, as illustrated in *Figure 18*.

Figure 18. Maximum continuos output current vs. duty cycle



6.6 Thermal considerations

The thermal design is important to prevent the thermal shutdown of the device if the junction temperature goes above 150 °C. The three different sources of losses within the device are:

a) conduction losses due to the not negligible R_{DSON} of the power switch; these are equal to:

$$P_{ON} = R_{DSON\_HS} \cdot (I_{OUT})^2 \cdot D + R_{DSON\_LS} \cdot (I_{OUT})^2 \cdot (1 - D)$$

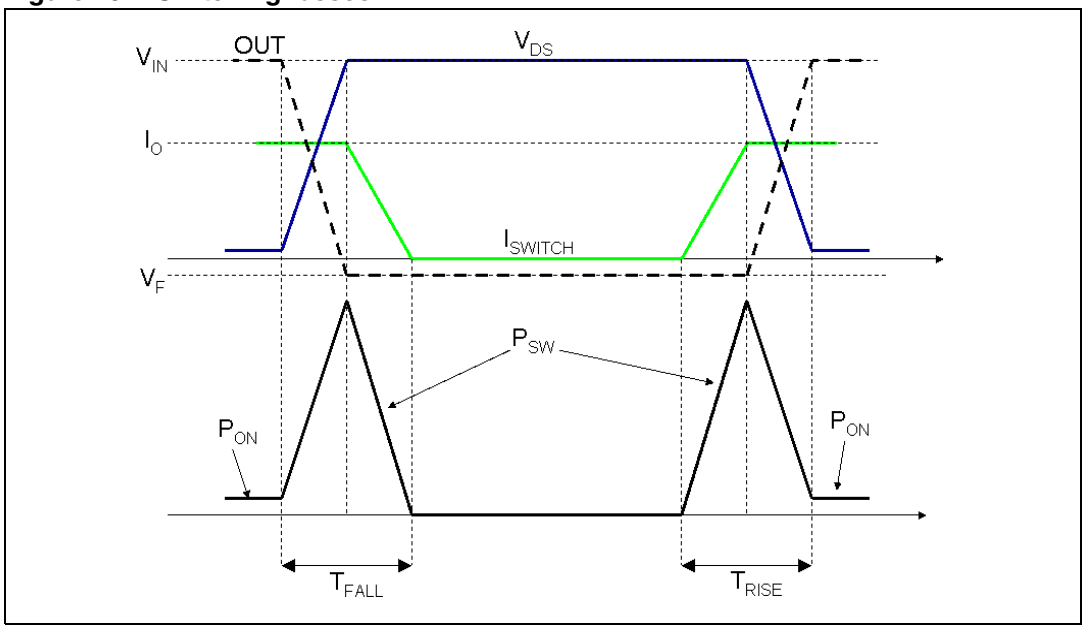
Where D is the duty cycle of the application. Note that the duty cycle is theoretically given by the ratio between V_{OUT} an V_{IN}, but actually it is quite higher to compensate the losses of the regulator. So the conduction losses increases compared with the ideal case.

b) switching losses due to power MOSFET turn ON and OFF; these can be calculated as:

$$P_{SW} = V_{IN} \cdot I_{OUT} \cdot \frac{(T_{RISE} + T_{FALL})}{2} \cdot Fsw = V_{IN} \cdot I_{OUT} \cdot T_{SW} \cdot F_{SW}$$

Where T_{RISE} and T_{FALL} represent the switching times of the power element that cause the switching losses when driving an inductive load (see *Figure 19*). T_{SW} is the equivalent switching time.

Figure 19. Switching losses



c) Quiescent current losses, calculated as:

$$P_Q = V_{IN} \cdot I_Q$$

where I_Q is the quiescent current.

The junction temperature T_J can be calculated as:

$$T_J = T_A + Rth_{JA} \cdot P_{TOT}$$

Where T_A is the ambient temperature and P_{TOT} is the sum of the power losses just seen.

R_{thJA} is the equivalent static thermal resistance junction to ambient of the device; it can be calculated as the parallel of many paths of heat conduction from the junction to the ambient. For this device the path through the exposed pad is the one conducting the largest amount of heat. The static Rth_{JA} measured on the application is about 40 °/W.

The thermal impedance of the system, considered as the device in HTSSOP16 package soldered on the application board, takes on an important rule when the maximum output power is limited by the static thermal performance and not by the electrical performance of the device. Therefore the embedded power elements could manage an higher current but the system is already taking away the maximum power generated by the internal losses.

In case the output power increases the thermal shutdown will be triggered because the junction temperature triggers the designed thermal shutdown threshold.

The R_{TH} is a static parameter of the package: it sets the maximum power loss which can be generated from the system given the operation conditions.

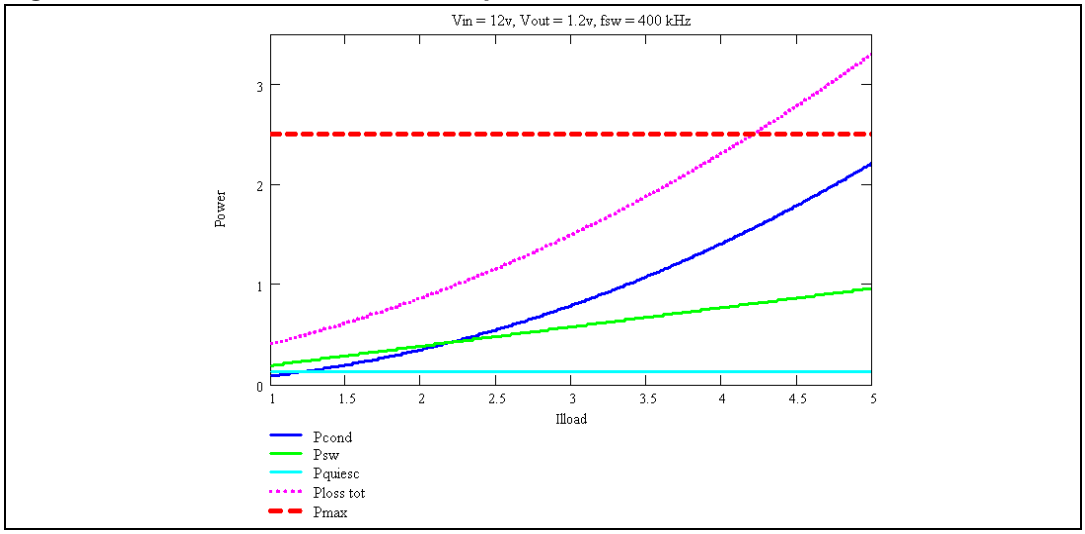
If we suppose, as an example, T_A = 40 °C, 140 °C is the maximum operating temperature before triggering the thermal shutdown and R_{TH} = 40 °C/W so the maximum power loss achievable with the thermal performance of the system will be:

$$P_{MAX\ DC} = \frac{\Delta T}{R_{TH}} = \frac{T_{J\ MAX} - T_{AMB}}{R_{TH}} = \frac{100}{40} = 2.5W$$

The switching, conduction and quiescent losses in case of V_{IN} = 12 V, V_{OUT} = 1.2 V, f_{SW} = 400 kHz are plotted in *Figure 20.* The calculations are performed considering the typical $R_{DS(on)}$ of the power element for a junction temperature of 125 °C ($R_{DS\_ON\ HS}$ = 120 mΩ, $R_{DS\_ON\ LS}$ = 83 mΩ; see *Maximum ratings on page 8* for details).

Conditions: V_{IN} = 12 V, V_{OUT} = 1.2 V, f_{SW} = 400 kHz

Figure 20. Estimation of the internal power losses



The red trace represents the maximum power which can be taken away as calculated above, whilst the purple trace is the total internal losses.

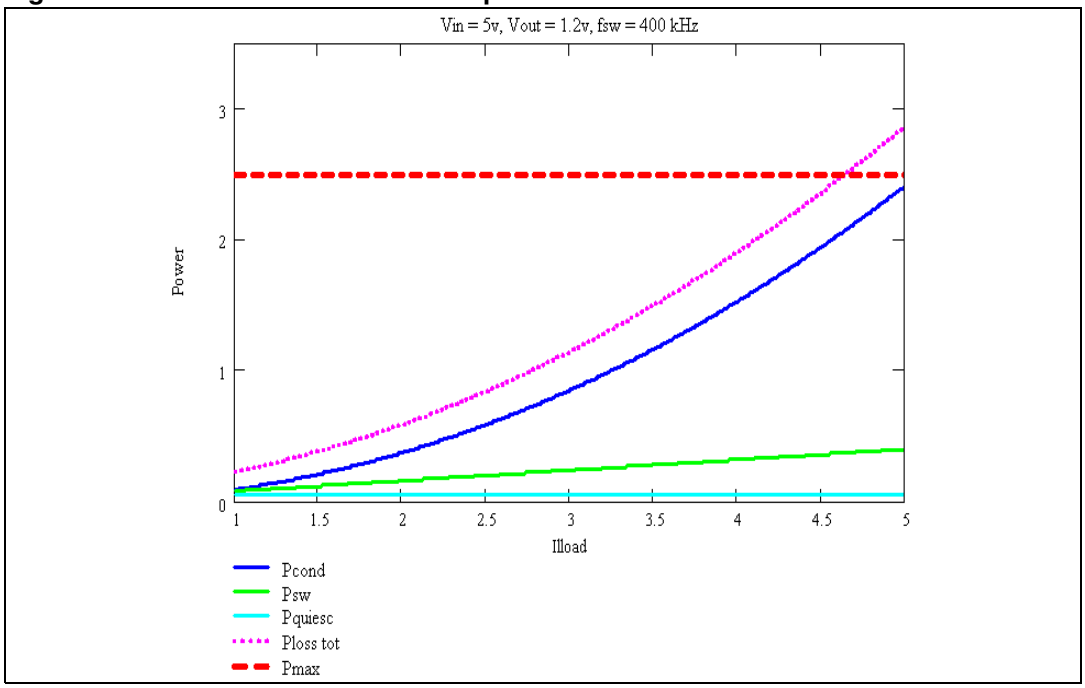
As a consequence, given these operating conditions, the system can manage a continuos output current up to 4.2 A. The device could deliver a continuos output current up to 5 A to the load (see *Chapter 6.5*), however the maximum power loss of 2.5 W is reached with an output current of 4.2 A, so the maximum output power is derated.

The calculation of the internal power losses must be done for each specific operating condition given by the final application.

For example, the result showed in *Figure 20.* is not valid in case the V_{IN} is equal to 5 V instead of 12 V: the lower contribution of the switching losses, which are proportional to the input voltage, increases the maximum output current from 4.2 A to 4.5 A (see *Figure 21*).

Conditions: V_{IN} = 5 V, V_{OUT} = 1.2 V, f_{SW} = 400 kHz

Figure 21. Estimation of the internal power losses



In applications where the current to the output is pulsed, the thermal impedance should be considered instead of the thermal resistance. Also, in these conditions, the current limitations described in *Chapter 6.5* are no more valid since they are related to continuos output current delivery.

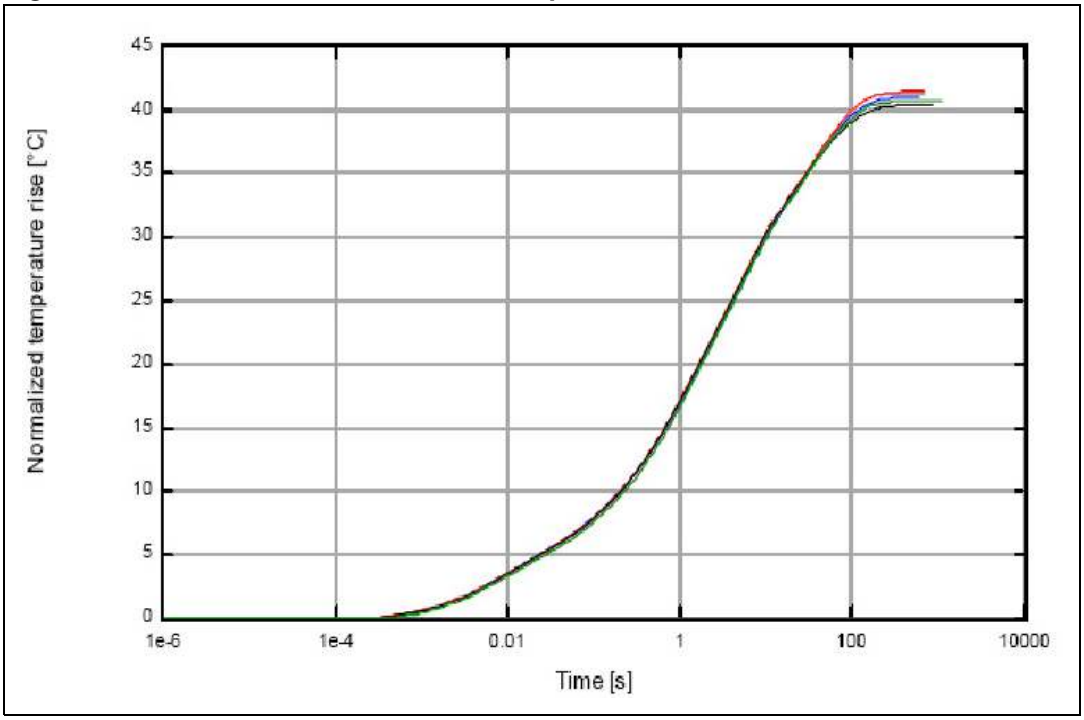
The thermal impedance of the system could be much lower than the thermal resistance, which is a static parameter. As a consequence the maximum power losses can be higher than 2.5 W if a pulsed output power is requested from the load:

$$P_{MAX}(t) = \frac{\Delta T}{Z_{TH}(t)} = \frac{T_{J\,MAX} - T_{AMB}}{Z_{TH}(t)}$$

So, depending on the pulse duration and its frequency, the maximum output current (even more than 5 A) can be delivered to the load.

The characterization of the thermal impedance is strictly dependent on the layout of the board. In *Figure 22.* the measurement of the thermal impedance of the evaluation board of the L5989D is provided.

Figure 22. Measurement of the thermal impedance of the evaluation board



As it can be see, for example, for load pulses with duration of 1 second, the actual thermal impedance is lower than 20 °C/W. This means that, for short pulses, a current higher that 5A (provided the current limitation is set correctly) can be managed.

6.7 Layout considerations

The PC board layout of switching DC/DC regulator is very important to minimize the noise injected in high impedance nodes and interferences generated by the high switching current loops. The L5989D is a monolithic device so most of the critical path are designed internally minimizing the potential issues introduced by the board layout.

In the operation of a step down converter two high current loops become evident and critical. The conduction of the high side switch highlight a current loop composed by the input capacitor, the inductor and the output capacitor whilst during the conduction of the low side switch the current flows from the power ground to the inductor and again the output capacitor.

The first consideration is to keep the trace of the switching node as short as possible to reduce radiated emission.

The bandwidth of the external power supply is limited if compared to the switching frequency of the device so the power supply delivers a certain RMS current in the switching period. As a consequence the input filter substains the input voltage during the conduction time of the

HS switch delivering an impulsive extra current equal to $I_{LOAD} + I_{RIPPLE} - I_{IN\ RMS}$ and it is recharged during the conduction time of the low side by the external power supply.

The golden rule is to reduce as much as possible the stray inductance of the path related to the capacitor and V_{IN} to reduce injected noise: the suggested layout (see *Figure 23* and *Figure 24*) solves this matter placing the input filter just above the package of the device to minimize noise. This placement offers the best filtering for the device and minimize the noise injected by the pulsing current path. The additional stray inductance introduced in the path from the switching node and the external inductor is not critical for the operation of the device.

The pin 4 of the L5989D supplies most of the analog circuitry and MOSFET drivers so an RMS current of few mA flows in its trace. A decoupling path between the power and signal input reduces the issues induced by the switching noise: an RC network is helpful to filter the signal supply from the noise generated by the switching activity and it becomes effective when its time constant is bigger than two or three switching cycles. The pin 4 supplies the drivers of the embedded MOSFET so the R value has to be kept limited to avoid voltage spikes during the operation of the embedded driver (the maximum value is in the order of few ohms).

The inductor current flows from power GND to the output capacitor during the conduction time of the LS switch: the power ground plane and the signal ground are kept partitioned in the PCB layout to minimize the injected noise on the signal ground. They are connected together below the ground of the output capacitor which is the less noisy power component.

The connection of the external resistor divider to the feedback pin (FB) is an high impedance node, so the interferences can be minimized placing the routing of feedback node as far as possible from the high current paths. To reduce the pick up noise the resistor divider has to be placed very close to the device.

Thanks to the exposed pad of the device, the ground plane helps to reduce the thermal resistance junction to ambient; so a large ground plane enhances the thermal performance of the converter allowing high power conversion.

Figure 23. Top board layout

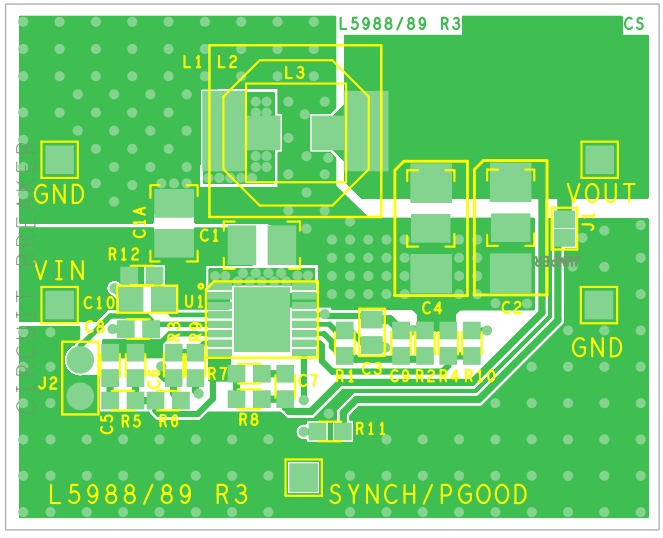
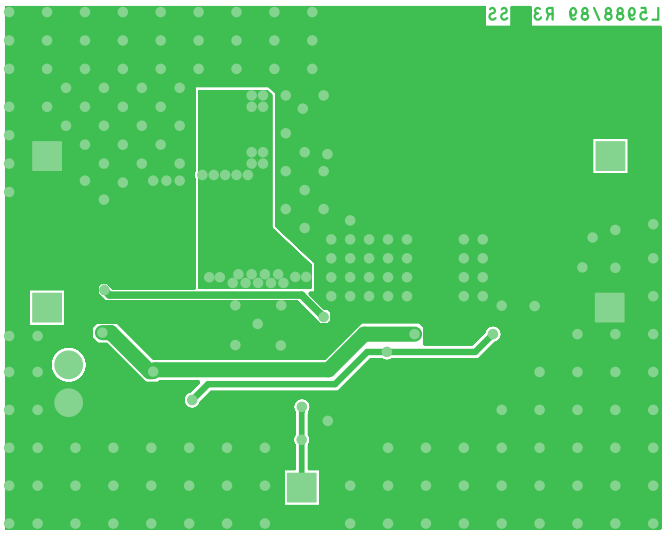


Figure 24. Bottom board layout



6.8 Application circuit

In *Figure 25* is shown the demonstration board application circuit working.

The operating switching frequency is 400 kHz. The designed system bandwidth is 68 kHz with a the phase margin of 50°. The peak current limitation is set 5.2 A, the valley current limitation 5.8 A in order to deliver up to 4 A DC to the load.

Figure 25. Demonstration board application circuit (f_{SW} = 400 kHz)

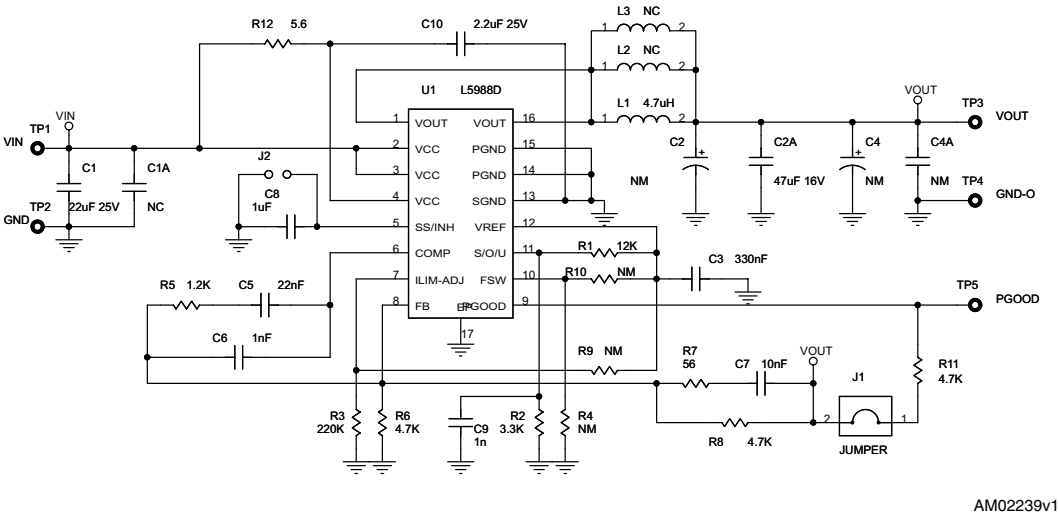


Table 13. Component list

Reference	Part number	Description	Manufacturer
C1	GRM32ER61E226KE15	Chip capacitor 22 µF 25V	Murata
C10	GRM188R71E105KA12	Chip capacitor 1µF 25V	Murata
C2A	GRM32ER61C476KE15	Chip capacitor 47 µF 16V	
C8		Chip capacitor 1 µF	
C3		Chip capacitor 330 nF	
C5		Chip capacitor 22 nF	
C6		Chip capacitor 1 nF	
C7		Chip capacitor 10 nF	
L1	744 311 470	Inductor 4.7 µH	Wurth elektronik
R1		Chip resistor 12 kΩ ± 1%	
R2		Chip resistor 3.3 kΩ ± 1%	
R3		Chip resistor 220 kΩ ± 1%	
R5		Chip resistor 1.2 kΩ ± 1%	
R6		Chip resistor 4.7 kΩ ± 1%	
R7		Chip resistor 56 Ω ± 1%	
R8		Chip resistor 4.7 kΩ ± 1%	
R11		Chip resistor 4.7 kΩ ±1%	
R12		Chip resistor 5.6 R ± 1%	
U1		I.C. L5989D	STMicroelectronics

In *Figure 26.* is shown an additional application example where the L5989D operates at a switching of 600 kHz. The designed system bandwidth is 73 kHz with a the phase margin of 51°. The peak current limitation is set 5.2 A, the valley current limitation 5.8 A in order to deliver up to 4 A DC to the load.

Figure 26. Demonstration board application circuit (f_{SW} = 600 kHz)

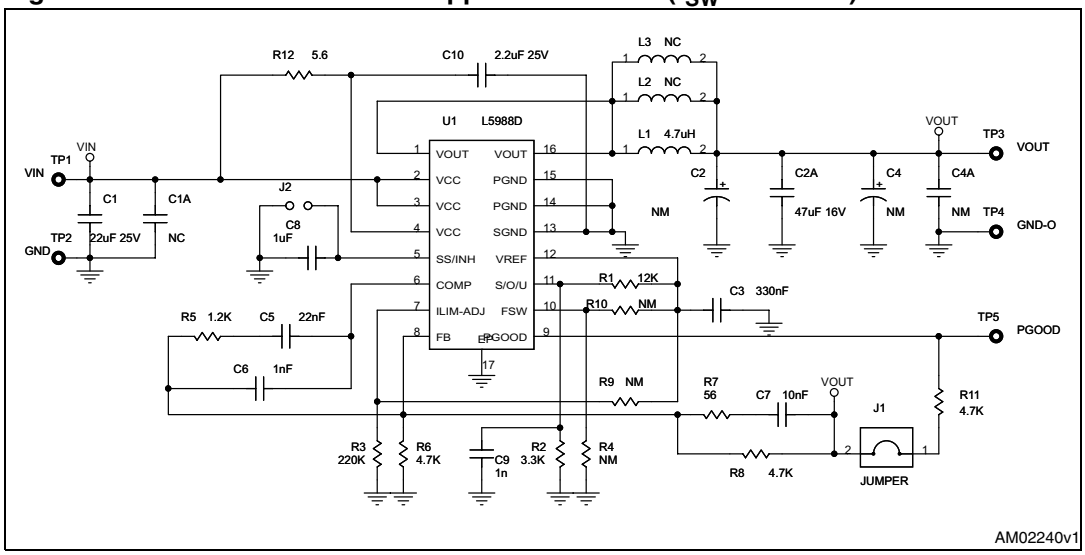


Table 14. Component list

Reference	Part number	Description	Manufacturer
C1	GRM32ER61E226KE15	Chip capacitor 22 µF 25 V	Murata
C10	GRM188R71E105KA12	Chip capacitor 1 µF 25 V	Murata
C2A	GRM32ER61C476KE15	Chip capacitor 47 µF 16 V	
C8		Chip capacitor 2.2 µF	
C3		Chip capacitor 330 nF	
C5		Chip capacitor 22 nF	
C6		Chip capacitor 1 nF	
C7		Chip capacitor 10 nF	
L1	744 311 330	Inductor 3.3 µH	Wurth elektronik
R1		Chip resistor 12 kΩ ±1%	
R2		Chip resistor 3.3 kΩ ±1%	
R3		Chip resistor 220 kΩ ±1%	
R4		Chip resistor 82 kΩ ±1%	
R5		Chip resistor 560 Ω ±1%	
R6		Chip resistor 1.1 kΩ±1%	
R7		Chip resistor 56 Ω ± 1%	
R8		Chip resistor 4.99 kΩ ±1%	
R11		Chip resistor 4.7 kΩ ±1%	
R12		Chip resistor 5.6 Ω ±1%	
U1		I.C. L5989D	STMicroelectronics

7 Typical characteristics

Figure 27. Junction temperature vs. f_{SW}

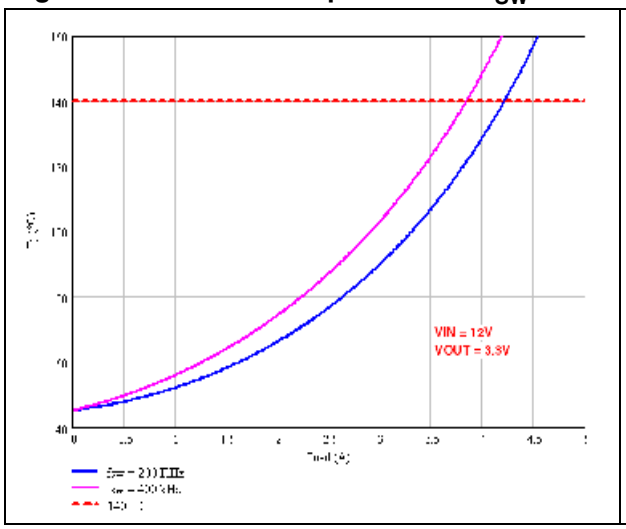


Figure 28. Junction temperature vs. f_{SW}

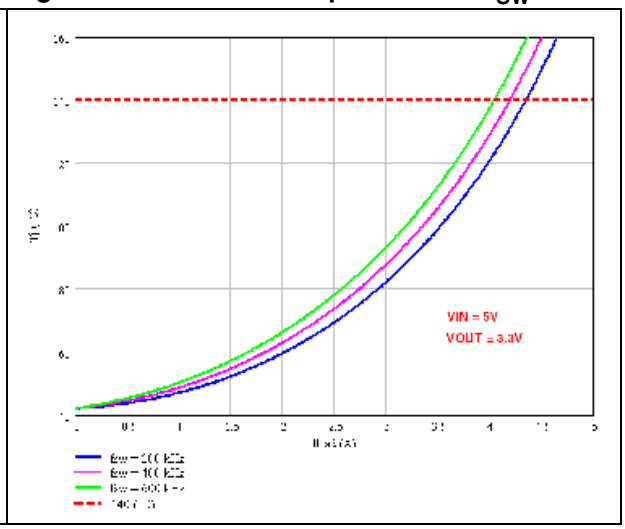


Figure 29. Junction temperature vs. f_{SW}

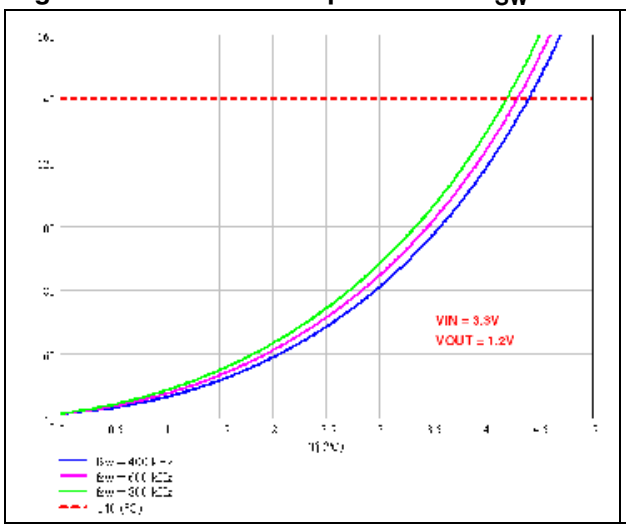


Figure 30. Junction temperature vs. V_{OUT}

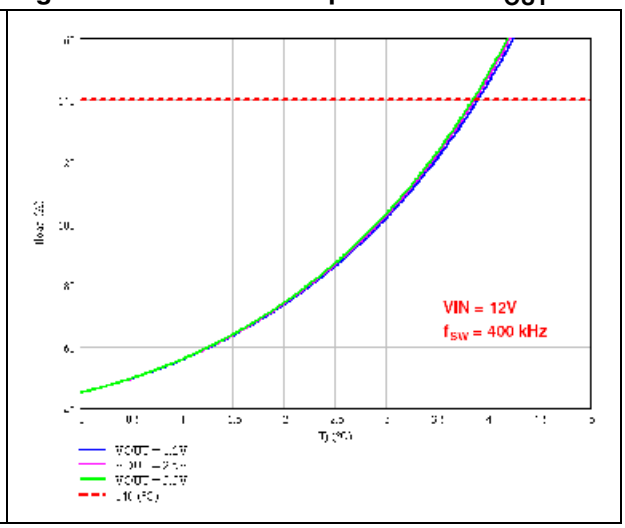


Figure 31. Junction temperature vs. V_{OUT}

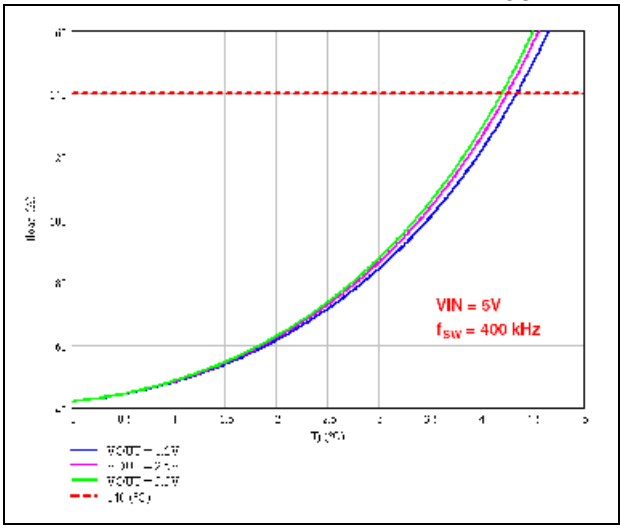


Figure 32. Junction temperature vs. V_{OUT}

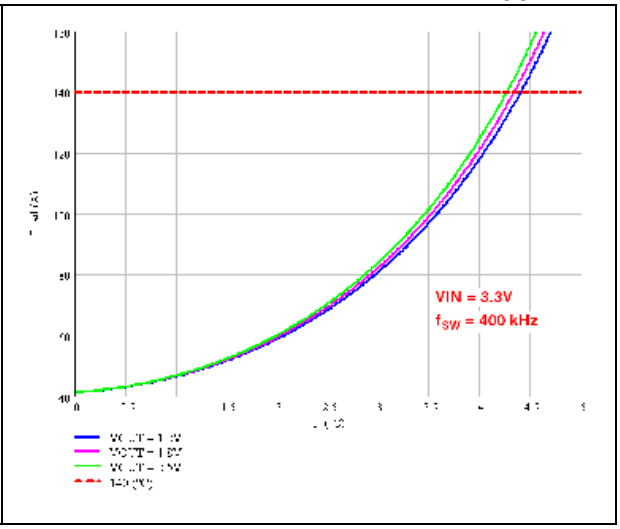


Figure 33. Efficiency vs. output current

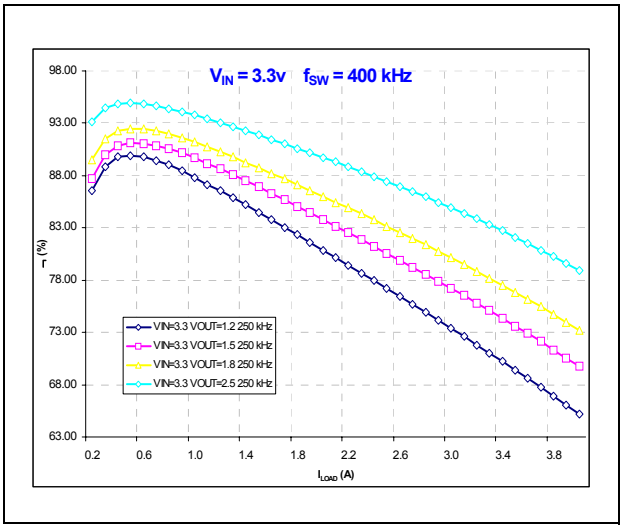


Figure 34. Efficiency vs. output current

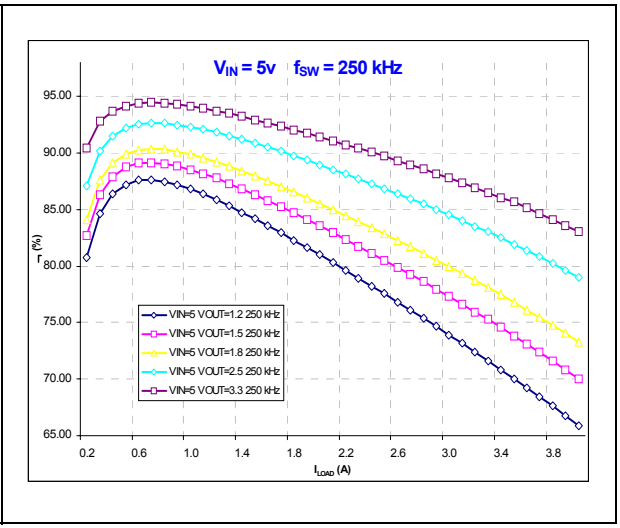


Figure 35. Efficiency vs. output current

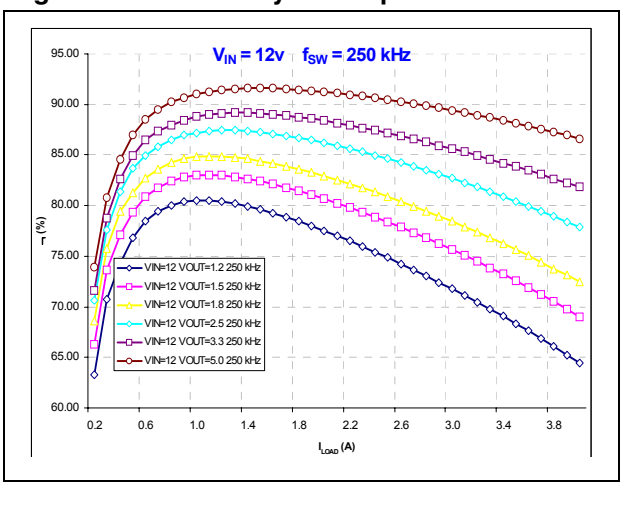


Figure 36. Load regulation

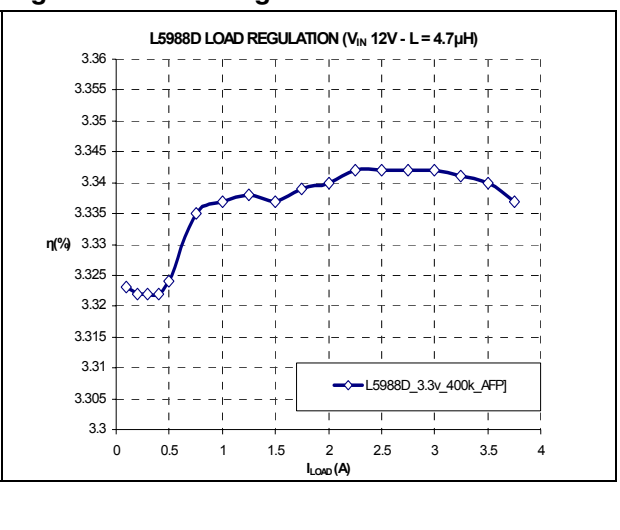


Figure 37. Line regulation

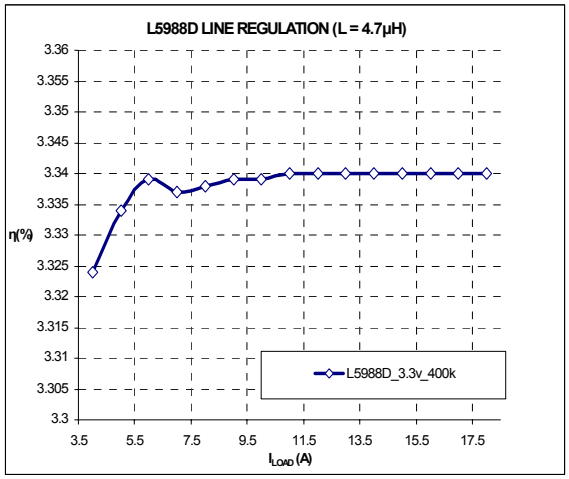


Figure 38. Load transient from 0 to 3 A

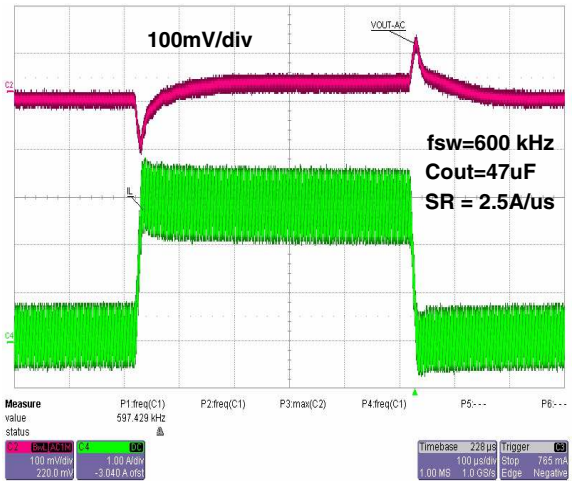
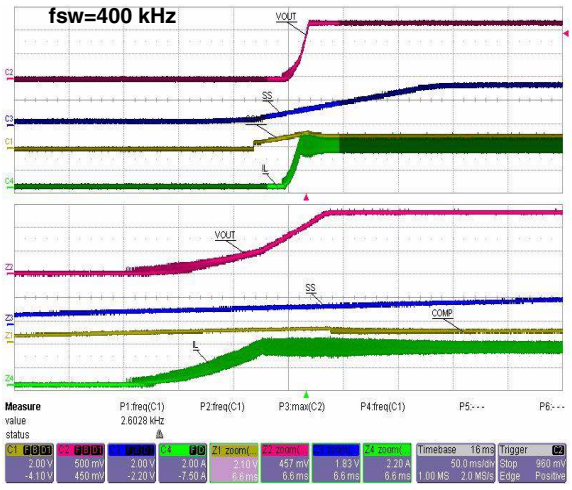


Figure 39. Soft-start



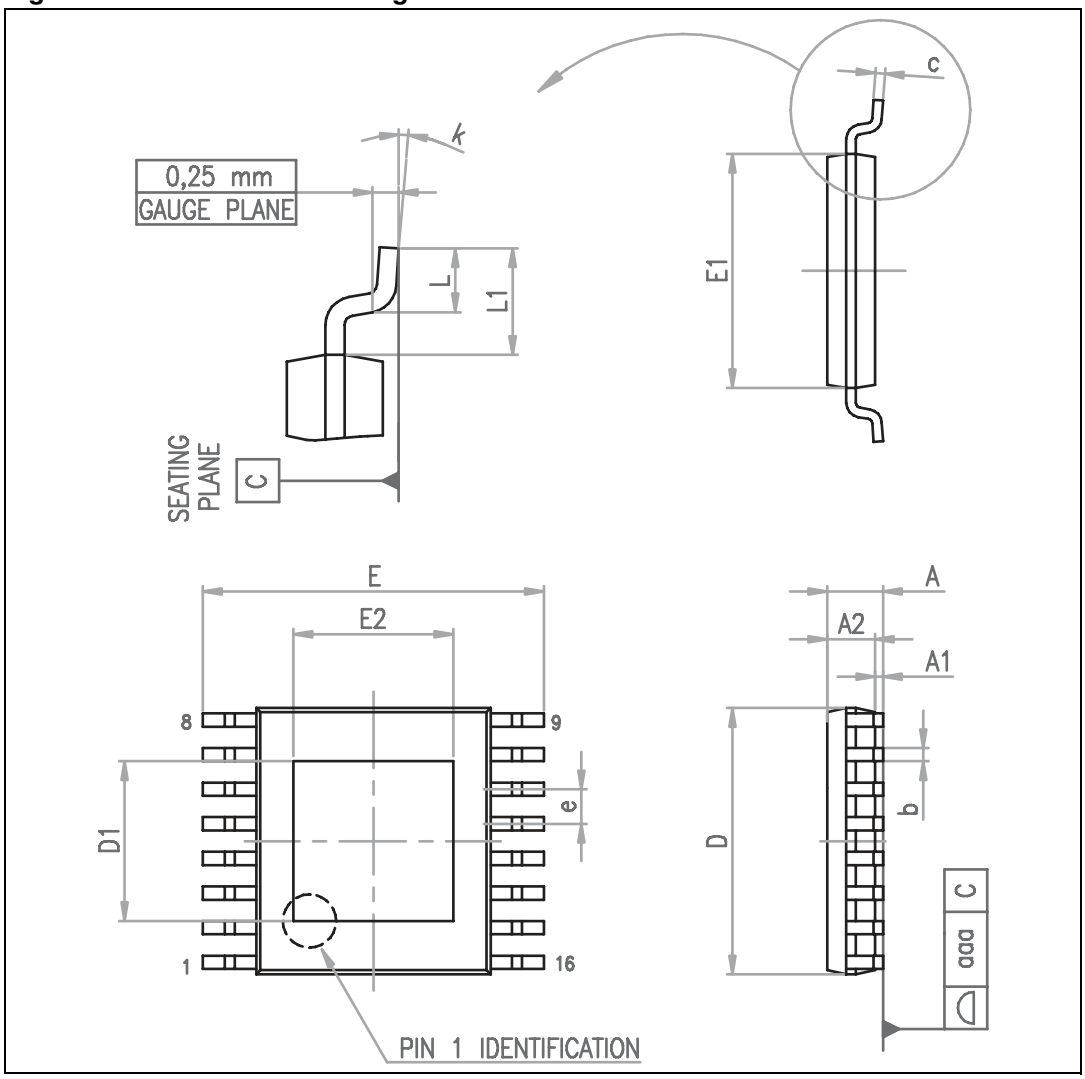
8 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Table 15. HTSSOP16 mechanical data

	(mm)		
Dim.	**Min.**	**Typ.**	**Max.**
A			1.20
A1			0.15
A2	0.80	1.00	1.05
b	0.19		0.30
c	0.09		0.20
D	4.90	5.00	5.10
D1	2.8	3	3.2
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
E2	2.8	3	3.2
e		0.65	
L	0.45	0.60	0.75
L1		1.00	
k	0.00		8.00
aaa			0.10

Figure 40. Mechanical drawing



9 Order codes

Table 16. Order codes

Order codes	Package	Packaging
L5989D	HTSSOP16	Tube
L5989DTR		Tape and reel

10 Revision history

Table 17. Document revision history

Date	Revision	Changes
04-Jun-2009	1	Initial release
24-Sep-2009	2	Updated: coverpage, *Table 4 on page 9*
18-Gen-2010	3	Updated: *Section 6.4 on page 27*, *Table 13 on page 42* and *Table 14 on page 43*

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