



# STB16N65M5 STD16N65M5

N-channel 650 V, 0.230  $\Omega$ , 12 A MDmesh™ V Power MOSFET  
in D<sup>2</sup>PAK, DPAK

## Features

Type	V <sub>DSS</sub> @ T <sub>Jmax</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>
STB16N65M5	710 V	< 0.279 $\Omega$	12 A
STD16N65M5			

- DPAK worldwide best R<sub>DS(on)</sub>
- Higher V<sub>DSS</sub> rating
- High dv/dt capability
- Excellent switching performance
- Easy to drive
- 100% avalanche tested

## Application

- Switching applications

## Description

These devices are N-channel MDmesh™ V Power MOSFETs based on an innovative proprietary vertical process technology, which is combined with STMicroelectronics' well-known PowerMESH™ horizontal layout structure. The resulting product has extremely low on-resistance, which is unmatched among silicon based Power MOSFETs, making it especially suitable for applications which require superior power density and outstanding efficiency.

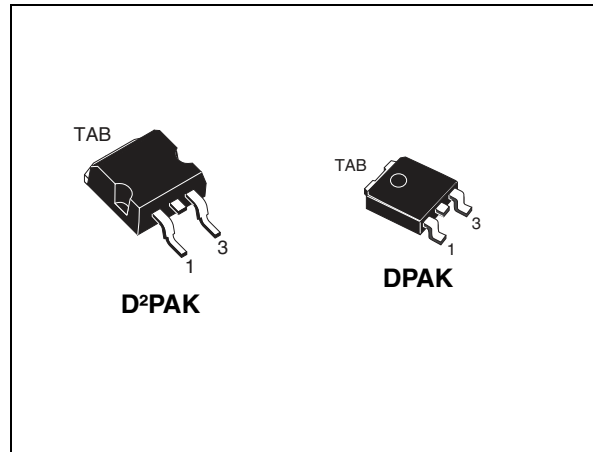


Figure 1. Internal schematic diagram

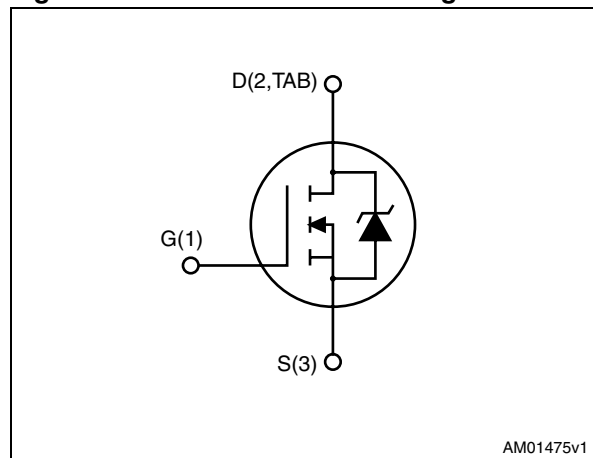


Table 1. Device summary

Order codes	Marking	Package	Packaging
STB16N65M5	16N65M5	D <sup>2</sup> PAK	Tape and reel
STD16N65M5		DPAK	

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	650	V
$V_{GS}$	Gate-source voltage	$\pm 25$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	12	A
$I_D$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	7.3	A
$I_{DM}^{(1)}$	Drain current (pulsed)	48	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	90	W
$I_{AR}$	Avalanche current, repetitive or not-repetitive (pulse width limited by $T_j$ max)	4	A
$E_{AS}$	Single pulse avalanche energy (starting $T_j = 25\text{ }^\circ\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ )	200	mJ
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
$T_{stg}$	Storage temperature	- 55 to 150	$^\circ\text{C}$
$T_j$	Max. operating junction temperature	150	$^\circ\text{C}$

1. Pulse width limited by safe operating area.

2.  $I_{SD} \leq 12\text{ A}$ ,  $di/dt \leq 400\text{ A}/\mu\text{s}$ ,  $V_{DD} = 400\text{ V}$ ,  $V_{Peak} < V_{(BR)DSS}$

**Table 3. Thermal data**

Symbol	Parameter	Value		Unit
		DPAK	D <sup>2</sup> PAK	
$R_{thj-case}$	Thermal resistance junction-case max	1.38		$^\circ\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb max	50	30	$^\circ\text{C}/\text{W}$

1. When mounted on 1inch<sup>2</sup> FR-4 board, 2 oz Cu

## 2 Electrical characteristics

( $T_C = 25\text{ °C}$  unless otherwise specified)

**Table 4. On /off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage ( $V_{GS} = 0$ )	$I_D = 1\text{ mA}$	650			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = 650\text{ V}$ $V_{DS} = 650\text{ V}, T_C = 125\text{ °C}$			1 100	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate-body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 25\text{ V}$			100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}, I_D = 6\text{ A}$		0.230	0.279	$\Omega$

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 100\text{ V}, f = 1\text{ MHz},$ $V_{GS} = 0$	-	1250	-	pF
$C_{oss}$	Output capacitance			30		pF
$C_{rss}$	Reverse transfer capacitance			3		pF
$C_{o(tr)}^{(1)}$	Equivalent capacitance time related	$V_{DS} = 0\text{ to }520\text{ V}, V_{GS} = 0$	-	100	-	pF
$C_{o(er)}^{(2)}$	Equivalent capacitance energy related			30		pF
$R_G$	Intrinsic gate resistance	$f = 1\text{ MHz open drain}$	-	2	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 520\text{ V}, I_D = 6\text{ A},$ $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 18</a> )	-	31	-	nC
$Q_{gs}$	Gate-source charge			8		nC
$Q_{gd}$	Gate-drain charge			12		nC

- $C_{oss\text{ eq}}$  time related is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$
- $C_{oss\text{ eq}}$  energy related is defined as a constant equivalent capacitance giving the same stored energy as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_d$ (v)	Voltage delay time	$V_{DD} = 400\text{ V}$ , $I_D = 8\text{ A}$ ,		25		ns
$t_r$ (v)	Voltage rise time	$R_G = 4.7\ \Omega$ , $V_{GS} = 10\text{ V}$		7		ns
$t_f$ (i)	Current fall time	(see <a href="#">Figure 19</a> )	-	6	-	ns
$t_c$ (off)	Crossing time	(see <a href="#">Figure 22</a> )		8		ns

**Table 7. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current				12	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		48	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 12\text{ A}$ , $V_{GS} = 0$	-		1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 12\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$		300		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 100\text{ V}$ (see <a href="#">Figure 22</a> )	-	3.5		nC
$I_{RRM}$	Reverse recovery current			23		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 12\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$		350		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 100\text{ V}$ , $T_j = 150\text{ }^\circ\text{C}$	-	4		nC
$I_{RRM}$	Reverse recovery current	(see <a href="#">Figure 22</a> )		24		A

1. Pulse width limited by safe operating area

2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for D<sup>2</sup>PAK

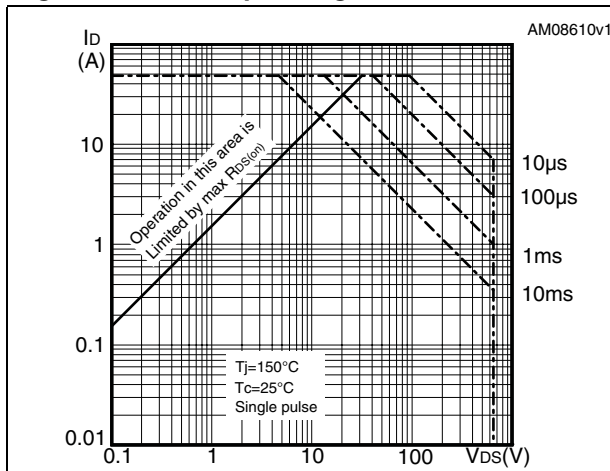


Figure 3. Thermal impedance for D<sup>2</sup>PAK

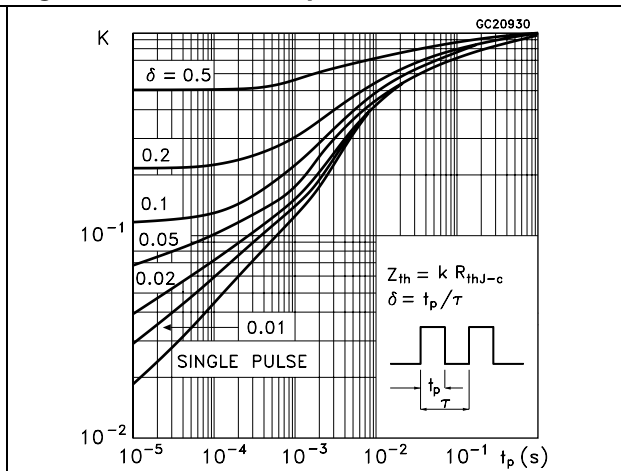


Figure 4. Safe operating area for DPAK

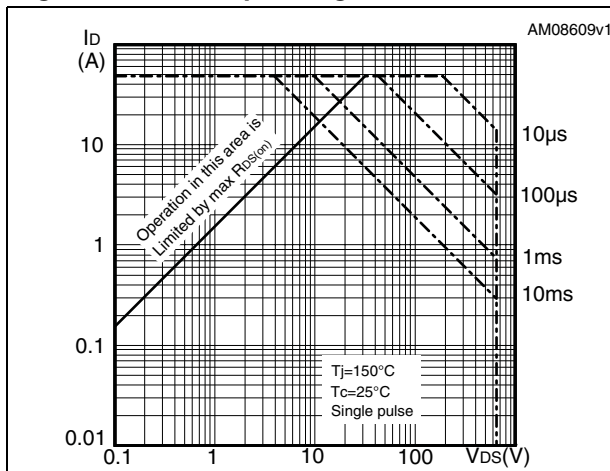


Figure 5. Thermal impedance for DPAK

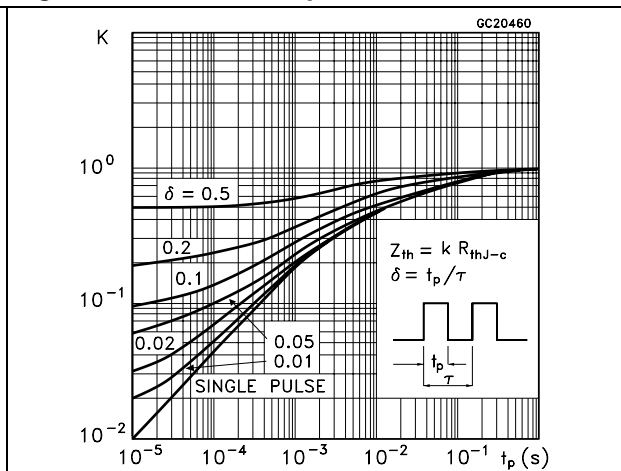


Figure 6. Output characteristics

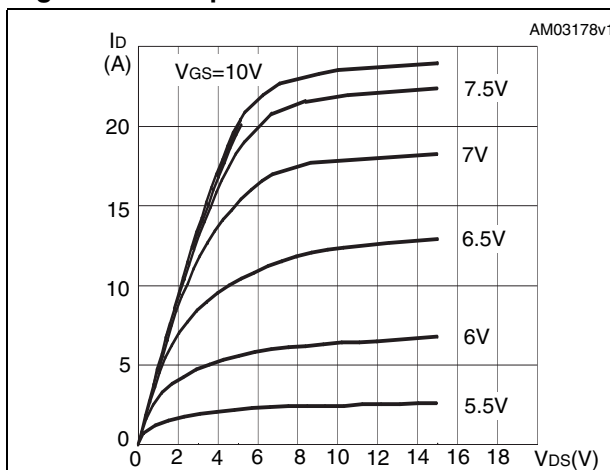


Figure 7. Transfer characteristics

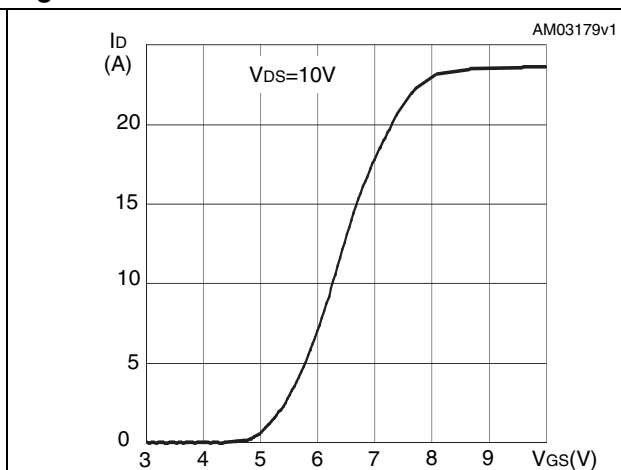


Figure 8. Normalized  $B_{V_{DSS}}$  vs. temperature

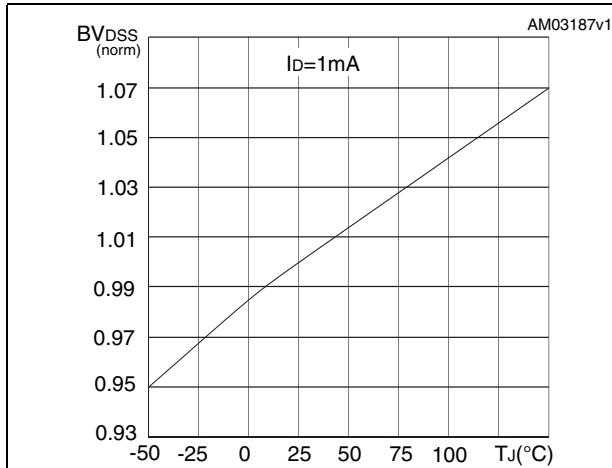


Figure 9. Static drain-source on resistance

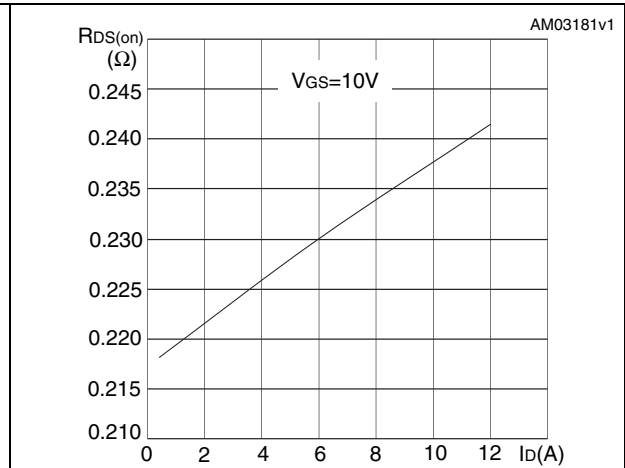


Figure 10. Output capacitance stored energy

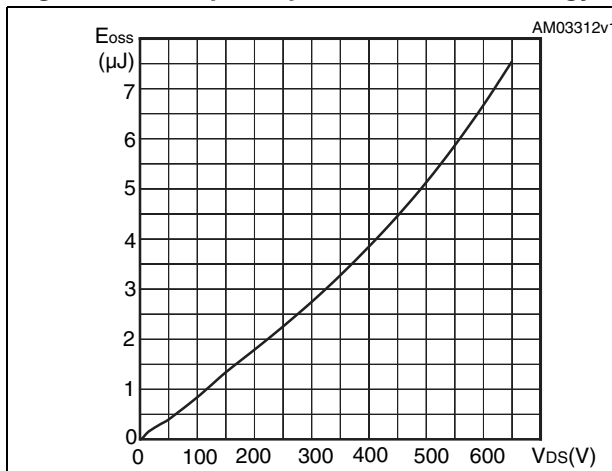


Figure 11. Capacitance variations

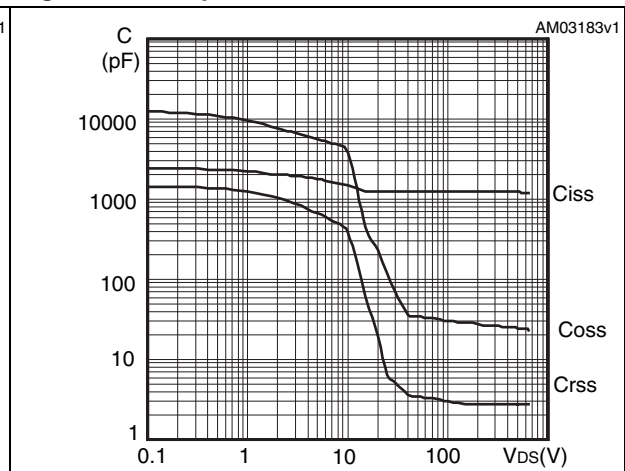


Figure 12. Gate charge vs. gate-source voltage

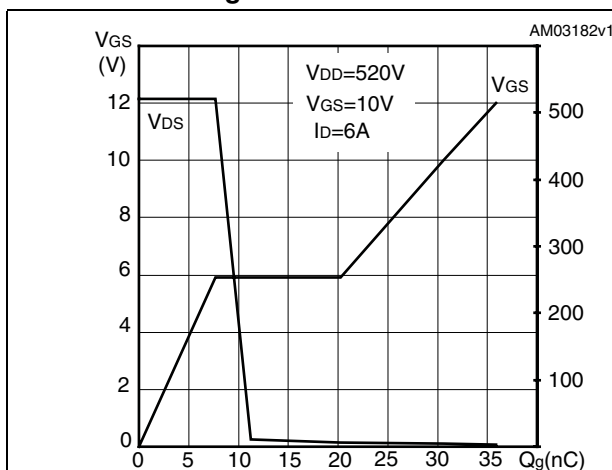


Figure 13. Normalized on resistance vs. temperature

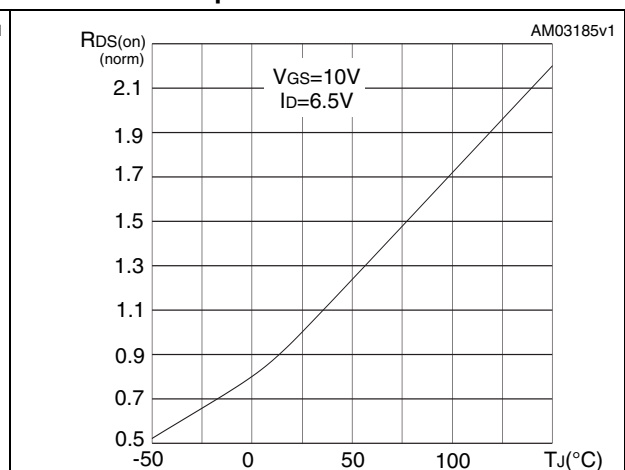


Figure 14. Normalized gate threshold voltage vs. temperature

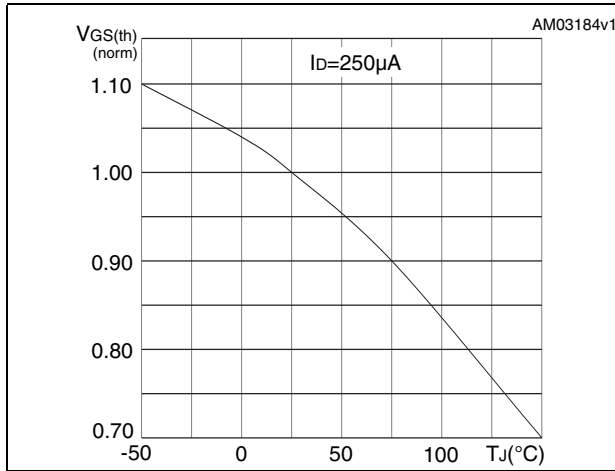


Figure 15. Source-drain diode forward characteristics

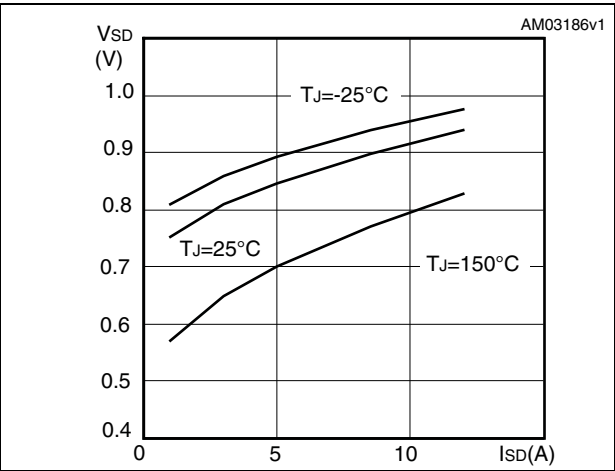
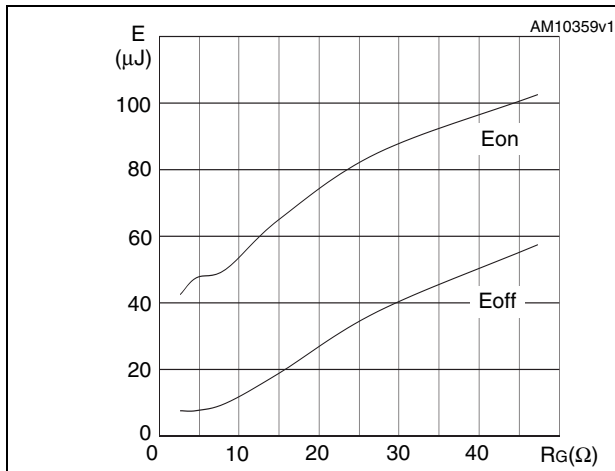


Figure 16. Switching losses vs. gate resistance<sup>(1)</sup>

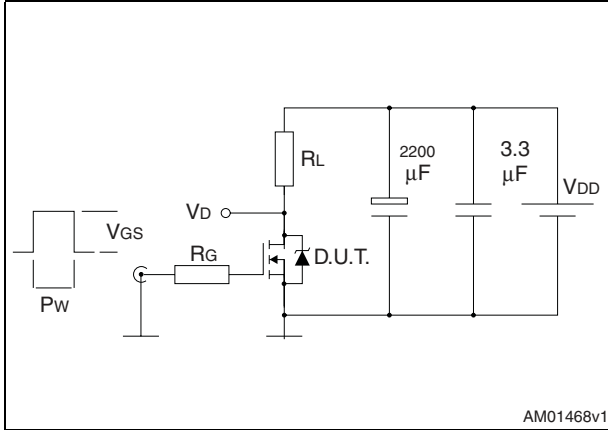


1. Eon including reverse recovery of a SiC diode.



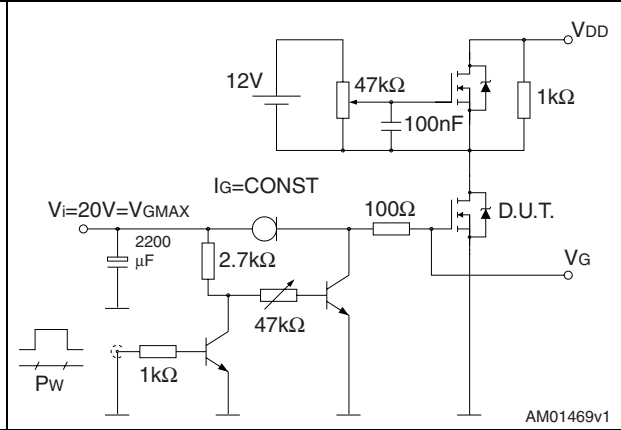
### 3 Test circuits

Figure 17. Switching times test circuit for resistive load



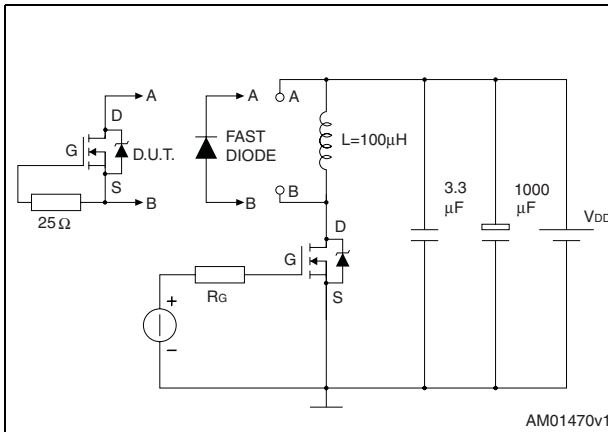
AM01468v1

Figure 18. Gate charge test circuit



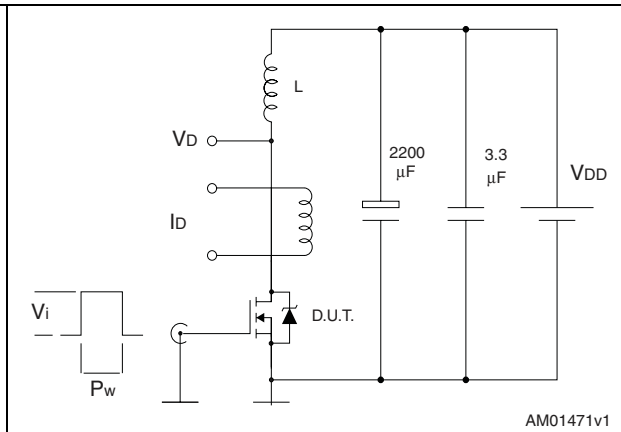
AM01469v1

Figure 19. Test circuit for inductive load switching and diode recovery times



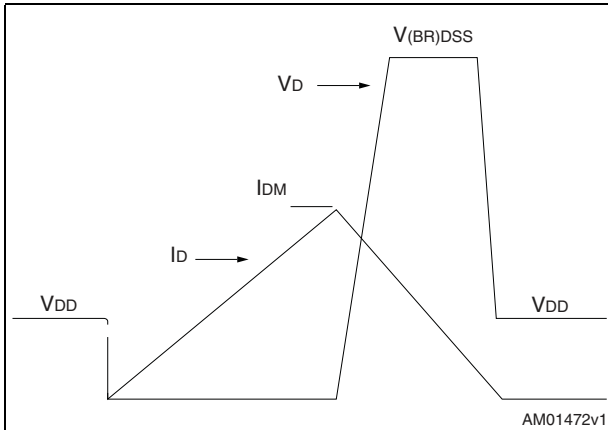
AM01470v1

Figure 20. Unclamped inductive load test circuit



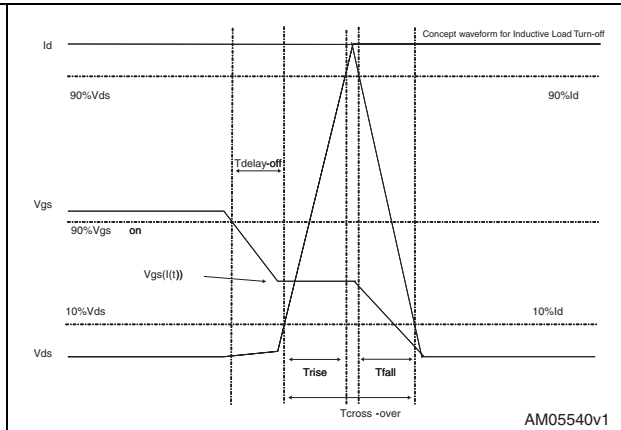
AM01471v1

Figure 21. Unclamped inductive waveform



AM01472v1

Figure 22. Switching time waveform



AM05540v1

## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

Table 8. D<sup>2</sup>PAK (TO-263) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50		
E	10		10.40
E1	8.50		
e		2.54	
e1	4.88		5.28
H	15		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.4	
V2	0°		8°

Figure 23. D<sup>2</sup>PAK (TO-263) drawing

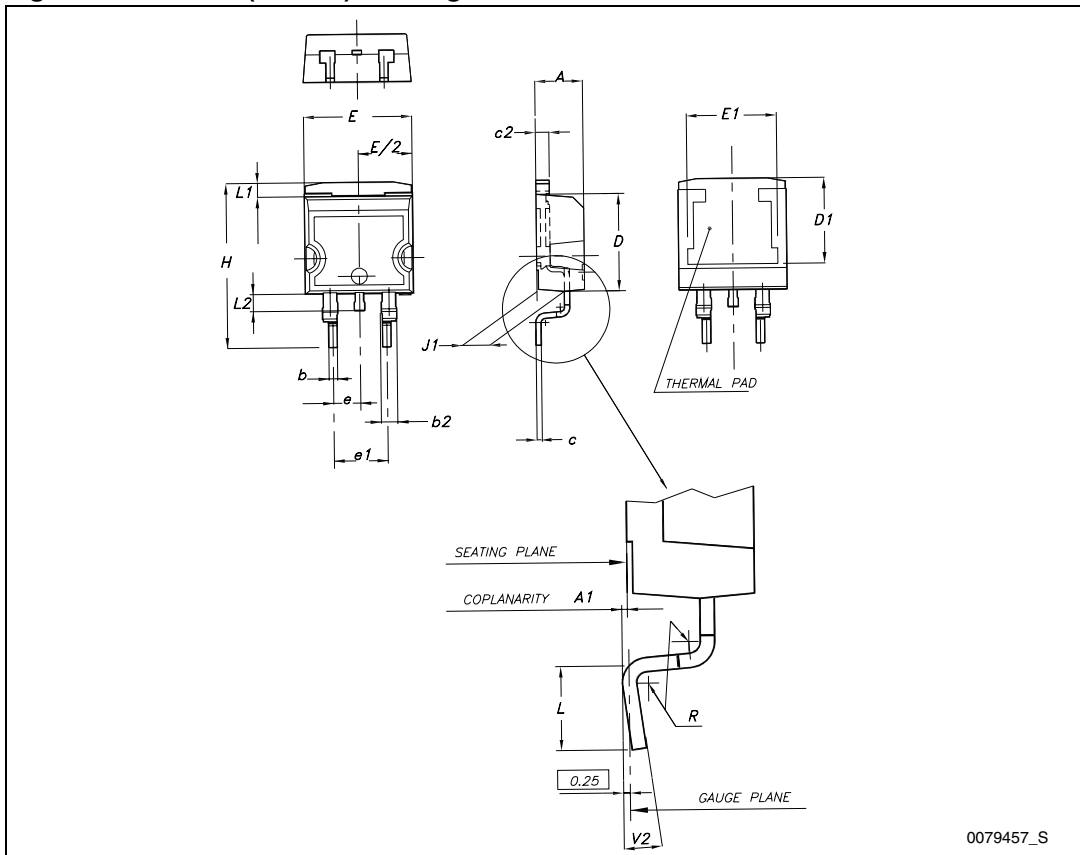
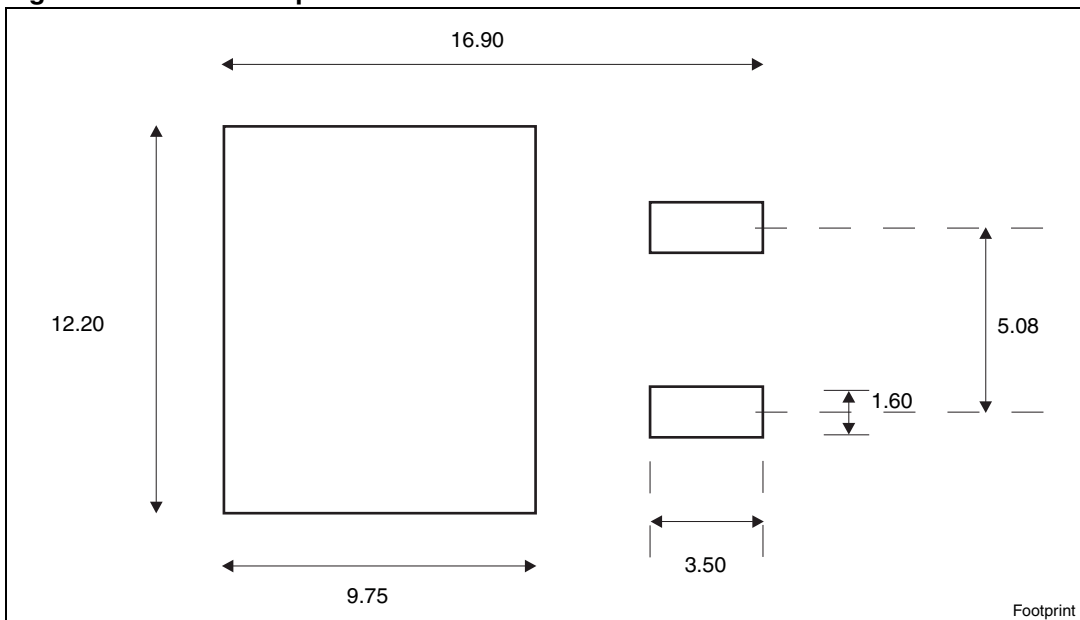


Figure 24. D<sup>2</sup>PAK footprint<sup>(a)</sup>



a. All dimensions are in millimeters

Table 9. DPAK (TO-252) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1		1.50
L1		2.80	
L2		0.80	
L4	0.60		1
R		0.20	
V2	0°		8°

Figure 25. DPAK (TO-252) drawing

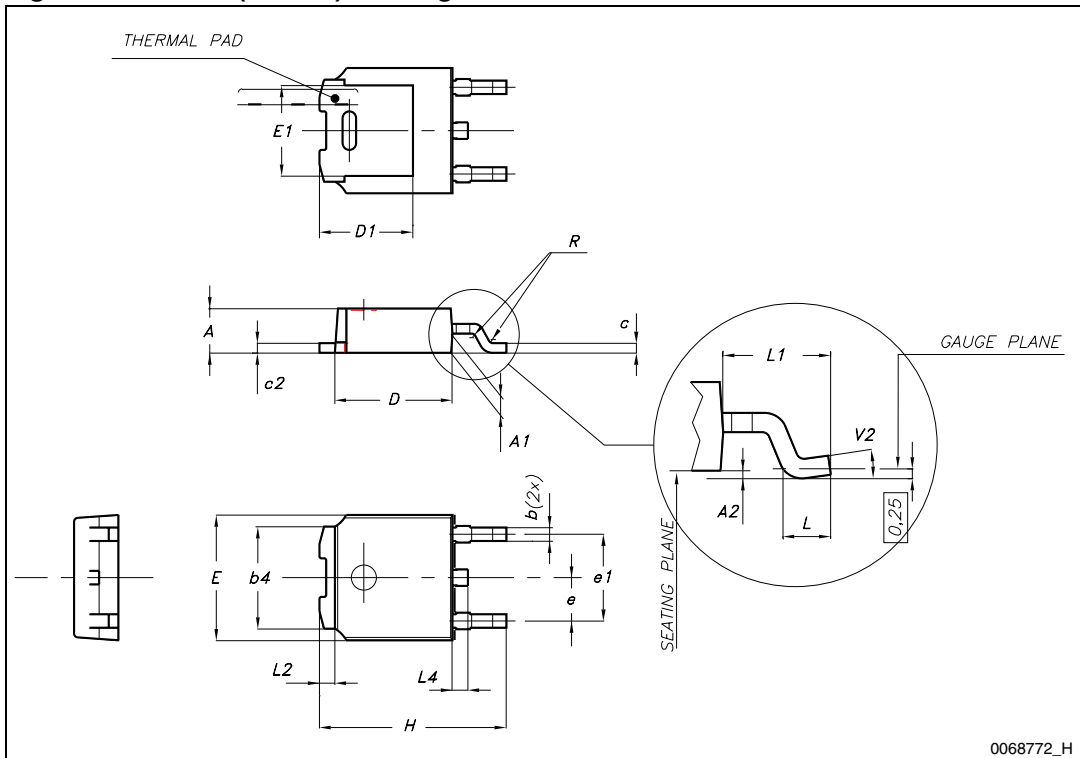
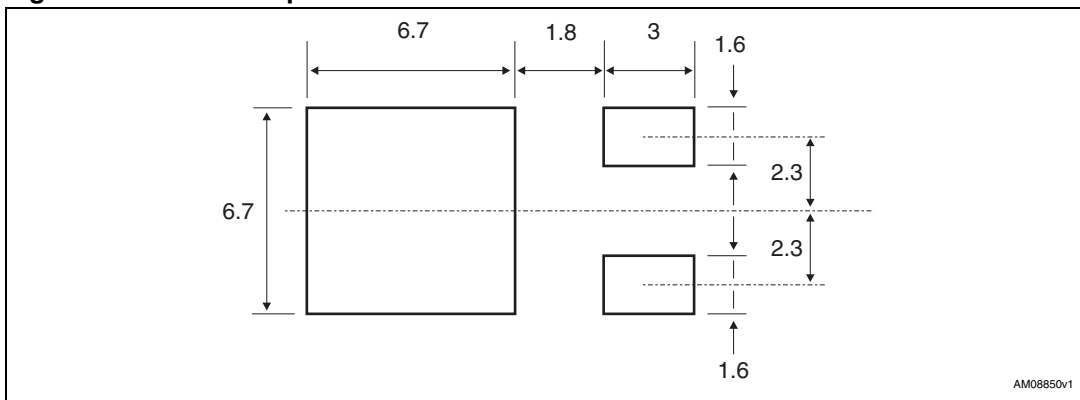


Figure 26. DPAK footprint<sup>(b)</sup>



b. All dimensions are in millimeters

## 5 Packaging mechanical data

Table 10. D<sup>2</sup>PAK (TO-263) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1		Base qty	1000
P2	1.9	2.1		Bulk qty	1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

Table 11. DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1		Base qty.	2500
P1	7.9	8.1		Bulk qty.	2500

Table 11. DPAK (TO-252) tape and reel mechanical data (continued)

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

Figure 27. Tape

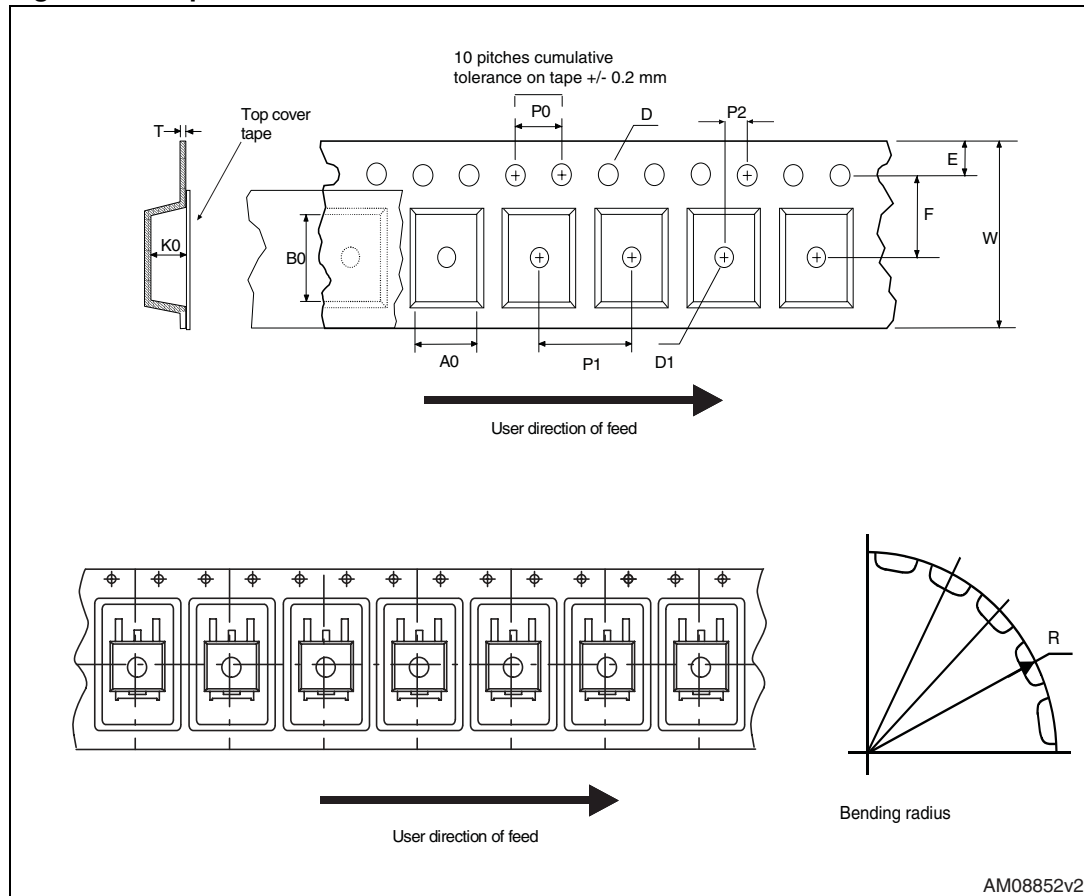
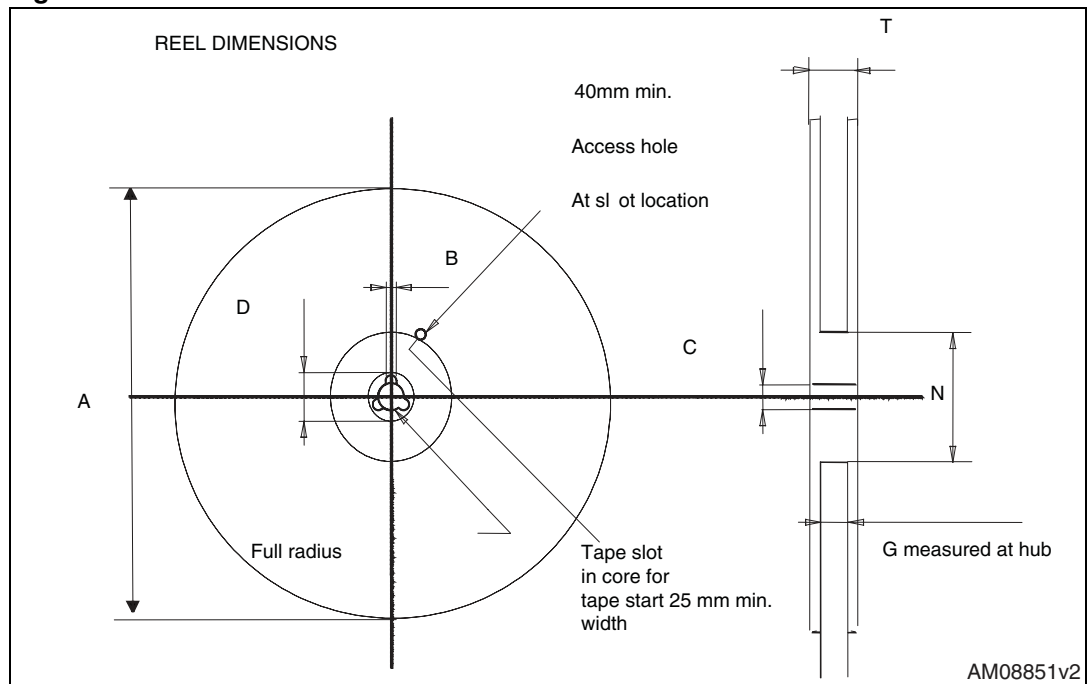




Figure 28. Reel



## 6 Revision history

Table 12. Document revision history

Date	Revision	Changes
09-Nov-2010	1	First release.
14-Oct-2011	2	Modified <a href="#">Section 2.1: Electrical characteristics (curves)</a> : – <a href="#">Figure 6</a> , <a href="#">Figure 7</a> , <a href="#">Figure 8</a> , <a href="#">Figure 9</a> , <a href="#">Figure 13</a> and <a href="#">Figure 14</a> – Added <a href="#">Figure 15</a> Updated $R_{DS(on)}$ value in coverpage and in <a href="#">Table 4</a> Updated values in <a href="#">Table 6</a> Updated <a href="#">Section 4: Package mechanical data</a> and <a href="#">Section 5: Packaging mechanical data</a> . Minor text changes.

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