Evaluating the ADN4624 5.7 kV RMS, Quad-Channel LVDS 2.5 Gigabit Isolator

FEATURES

- Isolated ground planes (logic side and bus side)
- High speed layout supports 2.5 Gigabit operation and precision jitter measurements (<1 ps rms for random jitter)
- Convenient connections through SMA terminals
  - 1.8 V power on Side 1 (V_{DD1}) and Side 2 (V_{DD2})
  - Ground on Side 1 (GND_1) and ground on Side 2 (GND_2)
  - LVDS input signals: D_{IN1+}, D_{IN1-}, D_{IN2+}, D_{IN2-}, D_{IN3+}, D_{IN3-}, D_{IN4+}, D_{IN4-}
  - LVDS output signals: D_{OUT1+}, D_{OUT1-}, D_{OUT2+}, D_{OUT2-}, D_{OUT3+}, D_{OUT3-}, D_{OUT4+}, D_{OUT4-}
- Jumper-selectable refresh mode
- Termination resistors on all LVDS receivers

EVALUATION KIT CONTENTS

- EVAL-ADN4624EB1Z

DOCUMENTS NEEDED

- ADN4624 data sheet

EQUIPMENT NEEDED

- Signal generator
- Oscilloscope
- Power supply

GENERAL DESCRIPTION

The EVAL-ADN4624EB1Z allows quick and easy evaluation of the ADN4624 low voltage differential signaling (LVDS) isolator without the need for external components. The ADN4624 employs Analog Devices, Inc., *i*Coupler® technology to combine a 4-channel isolator with LVDS receivers and drivers into a single, 28-lead wide body SOIC package with finer pitch. The device is capable of running at data rates of up to 2.5 Gbps with low jitter.

The evaluation board has a separate ground and power plane for each side of the isolator. This separation enables the evaluation of the ADN4624 with galvanic isolation between both sides of the device. 1.8 V power supplies are required on each side of the ADN4624 device.

For full details on the ADN4624, see the ADN4624 data sheet, which must be consulted in conjunction with this user guide when using the EVAL-ADN4624EB1Z.

EVALUATION BOARD PHOTOGRAPH

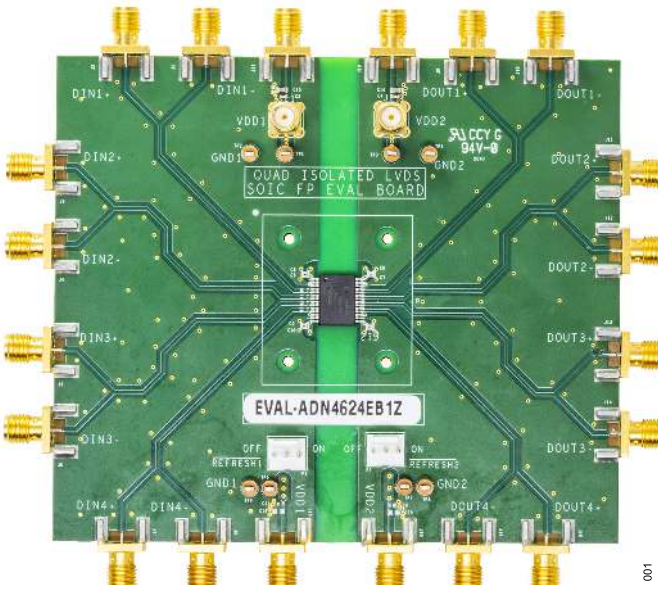

Figure 1.

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REVISION HISTORY

4/2021—Revision 0: Initial Version

EVALUATION BOARD CONFIGURATION

SETTING UP THE EVALUATION BOARD

On the EVAL-ADN4624EB1Z, connect 1.8 V power supplies to the J17, J18, or J21 subminiature Version A (SMA) connectors for Side 1 and the J19, J20, or J22 SMA connectors for Side 2 (see Table 2). At 1.25 GHz with a load resistance of 100 Ω, the maximum operating current from each power supply is 175 mA.

V_{DD1} (Pin 1 and Pin 14 on the ADN4624) is bypassed to GND_1 using 0.1 µF capacitors. V_{DD2} (Pin 15 and Pin 28 on the ADN4624) is bypassed to GND_2, also using 0.1 µF capacitors.

The ADN4624 integrates a refresh function to correct, if necessary, the output state in the absence of any input transitions. This function ensures the correct output state at power-up, for example. To reduce internal switching noise and provide even lower jitter, the refresh function can be disabled. This functionality is accessed on the EVAL-ADN4624EB1Z by changing the position of the P1 and P2 jumpers for Side 1 and Side 2, respectively, as described in Table 1.

Figure 3 shows an example operation of the EVAL-ADN4624EB1Z. The SMA connectors reveal all LVDS inputs and outputs for the EVAL-ADN4624EB1Z (see Table 3). To evaluate Channel 1 on the EVAL-ADN4624EB1Z, connect a signal generator to the board using the J1 connector and J2 connector and set up a 1.25 GHz square wave clock with an amplitude of 200 mV (400 mV peak-to-peak) and an offset of 1.2 V. Connect the oscilloscope to the J9 connector and J10 connector to perform timing measurements, including propagation delay, skew, and jitter. A differential probe with an SMA connector is recommended, terminating each output trace to 50 Ω connected to 1.24 V (providing 100 Ω differential termination and matching the ADN4624 driver offset voltage (V_{OS})). Refer to Table 3 for the connectors to use to evaluate Channel 2, Channel 3, and Channel 4 similarly on the EVAL-ADN4624EB1Z.

Figure 2 shows a plot of the oscilloscope connected via the J9 connector and J10 connector. The oscilloscope shows the differential voltage, that is, $D_{OUT1+} - D_{OUT1-}$.

Figure 2. D_{OUT1-} and D_{OUT1+} with a 1.25 GHz Clock, Differential

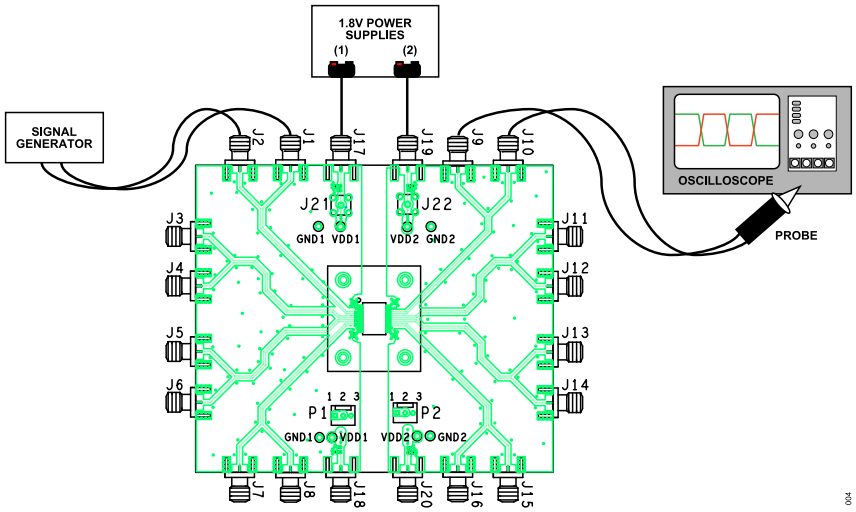

Figure 3. Basic LVDS Isolator Evaluation Board Operation for the EVAL-ADN4624EB1Z

Table 1. Jumper Configuration for EVAL-ADN4624EB1Z

Jumper	Position	Description
P1	1-2	Side 1 refresh disabled (quiet operation): $\overline{REFRESH_1}$ shorted to V_{DD1}.
	2-3	Side 1 refresh enabled (normal operation): $\overline{REFRESH_1}$ shorted to GND_1.
P2	1-2	Side 2 refresh disabled (quiet operation): $\overline{REFRESH_2}$ shorted to V_{DD2}.
	2-3	Side 2 refresh enabled (normal operation): $\overline{REFRESH_2}$ shorted to GND_2.

EVALUATION BOARD CONFIGURATION

Table 2. Connector Descriptions for EVAL-ADN4624EB1Z

Connector	Description
Side 1	
J17, J18, J21	Power supply, Side 1, connect 1.8 V to one connector option
Side 2	
J19, J20, J22	Power supply, Side 2, connect 1.8 V to one connector option

Table 3. Input and Output Connector Descriptions for EVAL-ADN4624EB1Z

Connector	EVAL-ADN4624EB1Z Description
J1	D_{IN1+}, noninverted LVDS input for Channel 1
J2	D_{IN1-}, inverted LVDS input for Channel 1
J3	D_{IN2+}, noninverted LVDS input for Channel 2
J4	D_{IN2-}, inverted LVDS input for Channel 2
J5	D_{IN3+}, noninverted LVDS input for Channel 3
J6	D_{IN3-}, inverted LVDS input for Channel 3
J7	D_{IN4+}, noninverted LVDS input for Channel 4
J8	D_{IN4-}, inverted LVDS input for Channel 4
J9	D_{OUT1+}, noninverted LVDS output for Channel 1
J10	D_{OUT1-}, inverted LVDS output for Channel 1
J11	D_{OUT2+}, noninverted LVDS output for Channel 2
J12	D_{OUT2-}, inverted LVDS output for Channel 2
J13	D_{OUT3+}, noninverted LVDS output for Channel 3
J14	D_{OUT3-}, inverted LVDS output for Channel 3
J15	D_{OUT4+}, noninverted LVDS output for Channel 4
J16	D_{OUT4-}, inverted LVDS output for Channel 4

EVALUATION BOARD SCHEMATICS AND ARTWORK

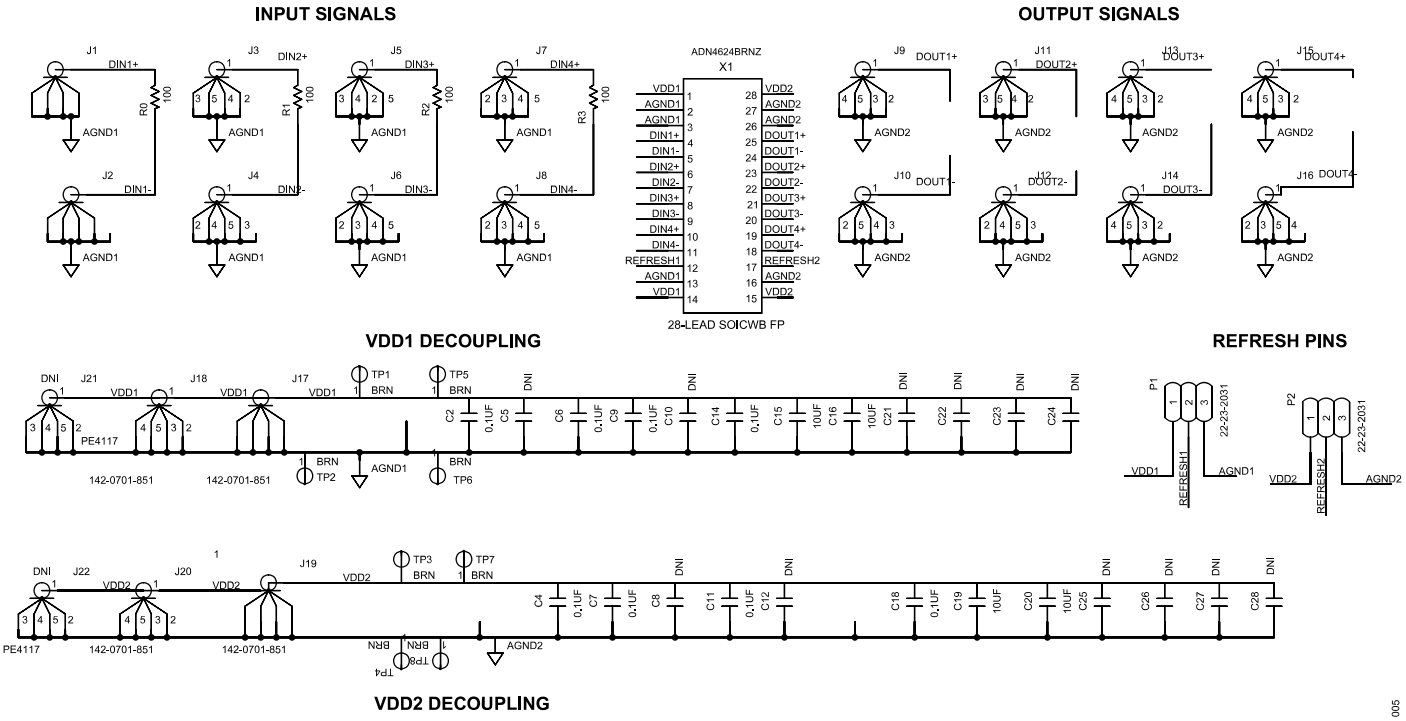

Figure 4. EVAL-ADN4624EB1Z Schematic

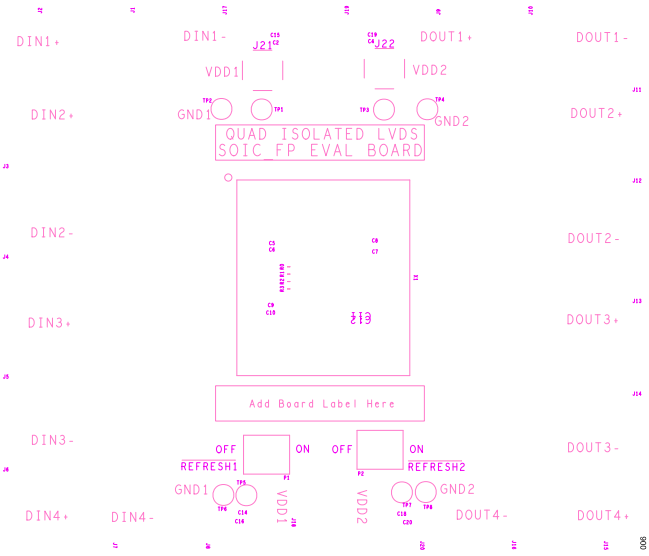

Figure 5. EVAL-ADN4624EB1Z Silkscreen

EVALUATION BOARD SCHEMATICS AND ARTWORK

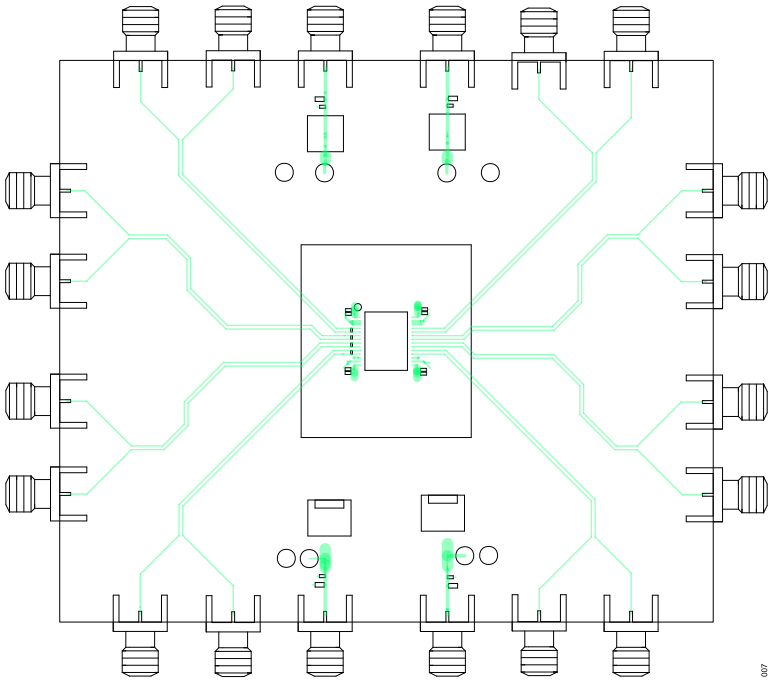

Figure 6. EVAL-ADN4624EB1Z Component Side

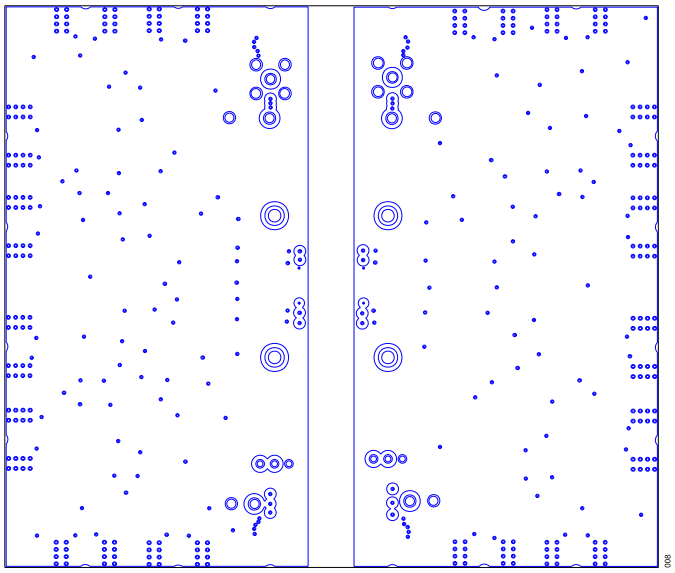

Figure 7. EVAL-ADN4624EB1Z Inner Layer 2, Ground

EVALUATION BOARD SCHEMATICS AND ARTWORK

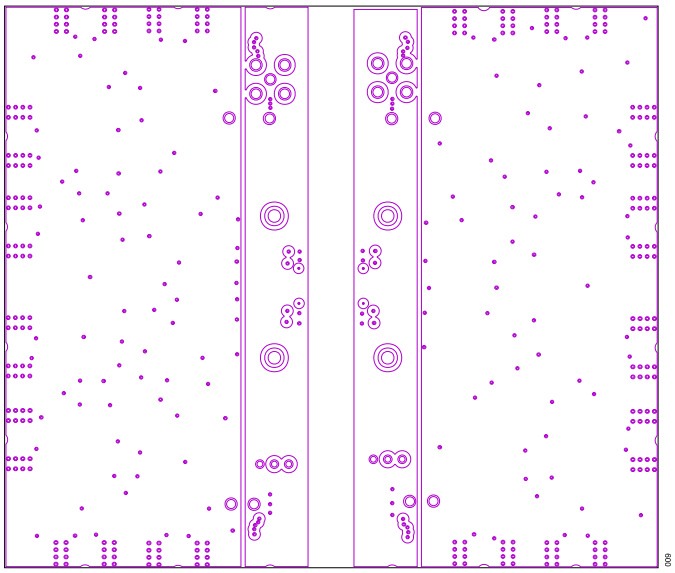

Figure 8. EVAL-ADN4624EB1Z Inner Layer 3, Power

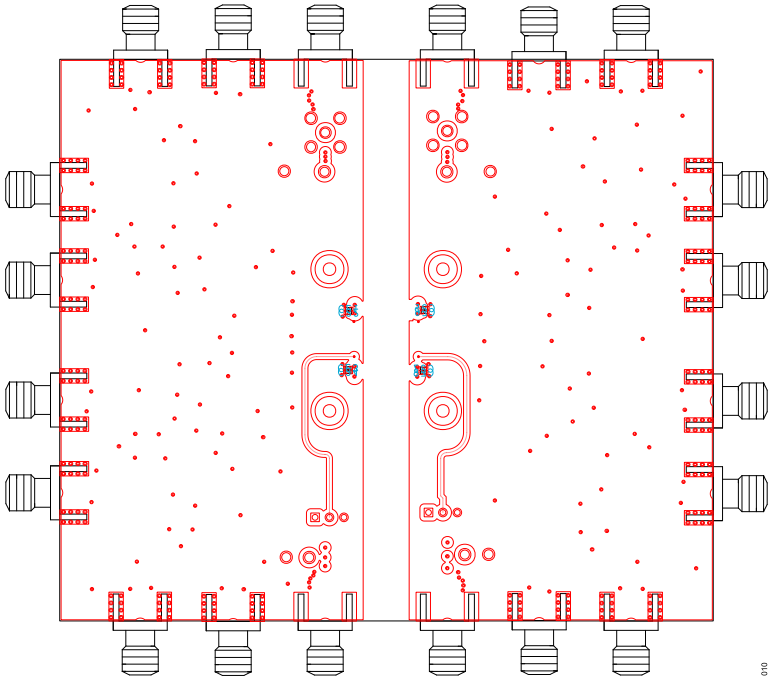

Figure 9. EVAL-ADN4624EB1Z Solder Side

ORDERING INFORMATION

BILL OF MATERIALS

Table 4. EVAL-ADN4624EB1Z Bill of Materials

Quantity	Reference Designator	Description	Manufacturer	Part Number
8	C2, C4, C6, C7, C9, C11, C14, C18	Capacitors, 100 nF, 0402	Kemet	C0402C104K4RACTU
4	C15, C16, C19, C20	Capacitors, 10 µF, 0603	Murata	GRM188R60J106ME47D
12	C5, C8, C10, C12, C21 to C28	Capacitors, 0402	Not fitted	Not applicable
20	J1 to J20	Connectors, SMA, edge	Johnson - Cinch	142-0701-851
2	J21, J22	Connectors, SMA (not fitted)	Pasternack Enterprises	PE4117 (not fitted)
2	P1, P2	3-pin, header (and jumper)	Molex (and Sullins)	22-23-2031 (and QPC02SXGN-RC)
4	R0, R1, R2, R3	Resistors, 100 Ω, 0201	Panasonic	ERJ-1GNF1000C
8	TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8	Test points	Components Corporation	TP104-01-01
1	X1	ADN4624 5.7 kV rms, quad-channel LVDS 2.5 Gigabit isolator	Analog Devices	ADN4624BRNZ

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.