User's Guide

TPS51513 Buck Controller Evaluation Module User's Guide

ABSTRACT

The TPS51513EVM-549 evaluation module (EVM) is a single-phase, D-CAP+™ synchronous buck converter providing 3-bit VID with 0.70-V to 1.05-V output range at up to 20 A from a 12-V input bus. The EVM uses the TPS51513 synchronous buck controller with selectable 250, 300, 350, or 500-kHz switching frequency.

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Trademarks

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1 Description

The TPS51513EVM-549 is designed to use a regulated 12-V (8-V to 14-V) bus to produce a high-current, regulated variable output at up to 20 A of the load current. The output voltage varies from 0.70 V to 1.05 V through a 3-bit VID digital-to-analog converter (DAC). The TPS51513EVM-549 is designed to demonstrate the TPS51513 in a typical low-voltage application while providing a number of test points to evaluate the performance of the TPS51513.

1.1 Typical Application

- General integrated circuit (IC) V_{CORE} application

1.2 Features

The TPS51513EVM-549 features:

- Output voltage variable from 0.70 V to 1.05 V through a 3-bit VID DAC or fixed 1.2-V option
- 20-A_{DC} steady-state current
- Selectable 250, 300, 350, or 500-kHz switching frequency
- Selectable current limit
- Selectable output overshoot reduction (OSR™)
- J6 for enable function
- Convenient test points for probing critical waveforms
- Six-layer PCB with 2-oz copper on the outside layer

2 Electrical Performance Specifications

Table 2-1. TPS51513EVM-549 Electrical Performance Specifications(1)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Characteristics					
Voltage range	V_{IN}	8	12	14	V
Maximum input current	V_{IN} = 8 V, 1.05 V/20 A at 300 kHz			3.0	A
No load input current	V_{IN} = 14 V, Io = 0 A			10	mA
Output Characteristics					
Output voltage, VOUT	VID0 = VID1 = VID2 = 0		1.05		V
Output voltage regulation	Line regulation		0.1%		
	Load regulation (Nondroop)		1.0%		
Output voltage ripple	V_{IN} = 12 V, I_O = 20 A at 300 kHz			30	mVpp
Output load current		0		20	A
Output over current			30		A
Systems Characteristics					
Switching frequency	Selectable	250	300	500	kHz
Peak efficiency	V_{IN} = 12 V, 1.05 V/10 A at 300 kHz		90.9%		
Full load efficiency	V_{IN} = 12 V, 1.05 V/20 A at 300 kHz		89.2%		
Operating temperature			25		°C

(1) Jumpers set to default locations; see Section 6.

3 Schematic

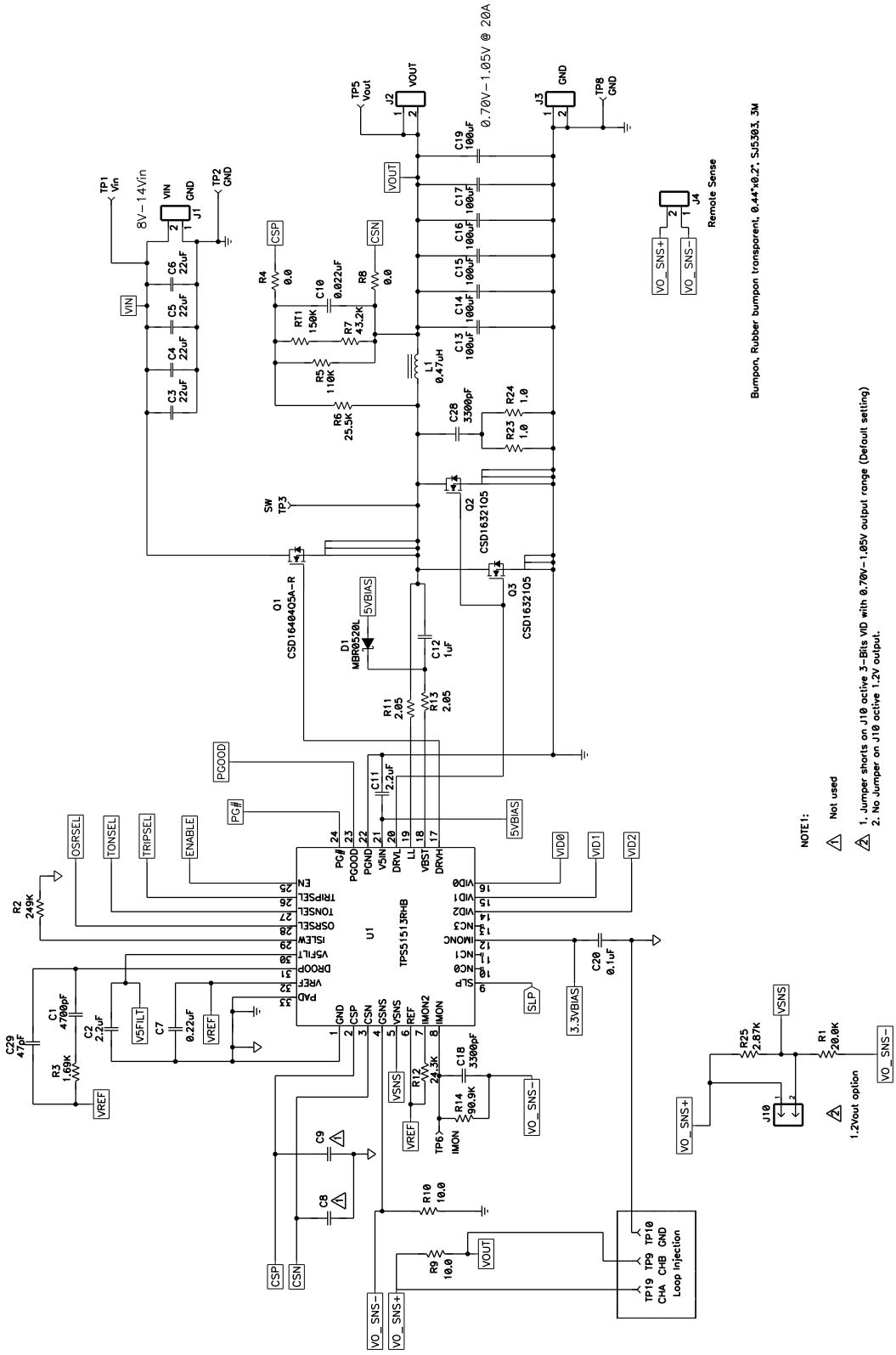

Figure 3-1. TPS51513EVM-549 Schematic, Sheet 1 of 2

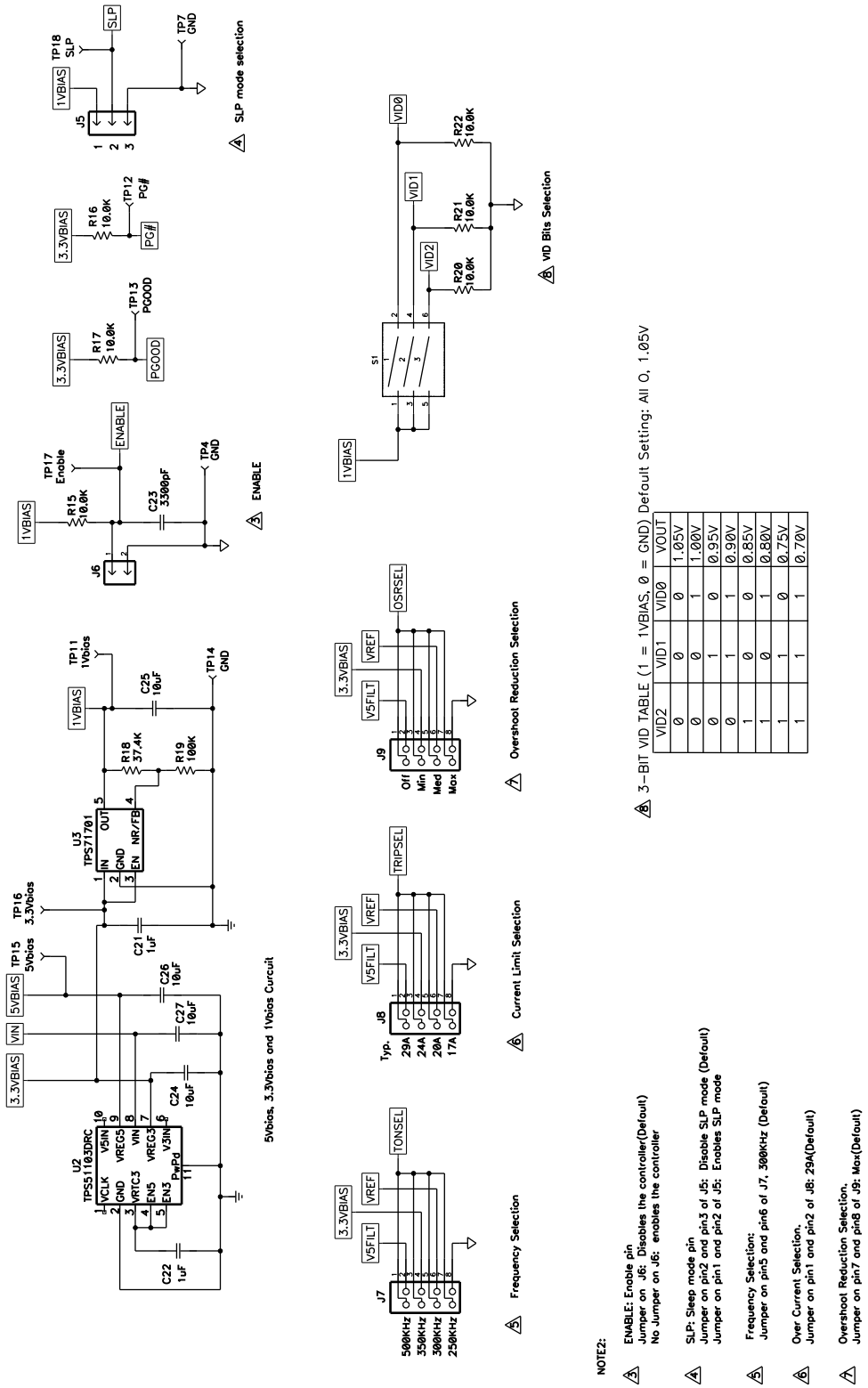

Figure 3-2. TPS51513EVM-549 Schematic, Sheet 2 of 2

4 Test Setup

4.1 Test Equipment

Voltage Source: The input voltage source, V_{IN}, must be a 0-V to 14-V variable DC source capable of supplying 10 A_{DC}. Connect V_{IN} to J1 as shown in Figure 4-2.

Multimeters: A 0-V to 14-V voltmeter (V1) must be used to measure V_{IN} at TP1 (VIN) and TP2 (GND). A 0-V to 5-V voltmeter (V2) is necessary for V_{OUT} measurement at TP5 (VOUT) and TP8 (GND). A 0-A to 10-A current meter (A1) as shown in Figure 4-2 is used for input current measurements.

Output Load: The output load must be an electronic constant resistance mode load capable of 0 A_{DC} to 30 A_{DC} at 1.05 V.

Oscilloscope: A digital or analog oscilloscope can be used to measure the output ripple. The oscilloscope must be set for the following:

- 1-MΩ impedance
- 20-MHz bandwidth
- AC coupling
- 2-µs/division horizontal resolution
- 20-mV/division vertical resolution

Test points TP5 and TP8 can be used to measure the output ripple voltage by placing the oscilloscope probe tip through TP5 and holding the ground barrel TP8 as shown in Figure 4-1. Do not use a leaded ground connection as this may induce additional noise due to the large ground loop.

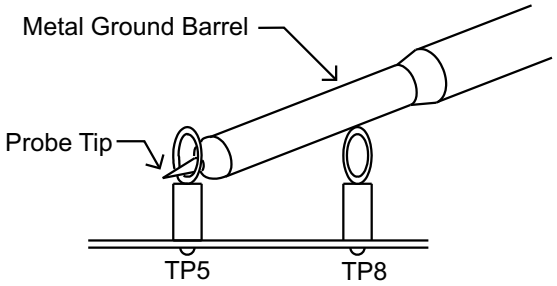

Figure 4-1. Tip and Barrel Measurement for V_{OUT} Ripple

Fan: Some of the components in this EVM may get hot and approach temperatures of 60°C during operation. A small fan capable of 200 LFM–400 LFM is recommended to reduce component temperatures while the EVM is operating. The EVM must not be probed if the fan is not running.

Recommended Wire Gauge: For VIN to J1 (12-V input) the recommended wire size is AWG 14 per input connection, with the total length of wire less than four feet (2-foot input, 2-foot return). For J2, J3 to LOAD, the minimum recommended wire size is 2× AWG 14, with the total length of wire less than four feet (2-foot output, 2-foot return)

4.2 Recommended Test Setup

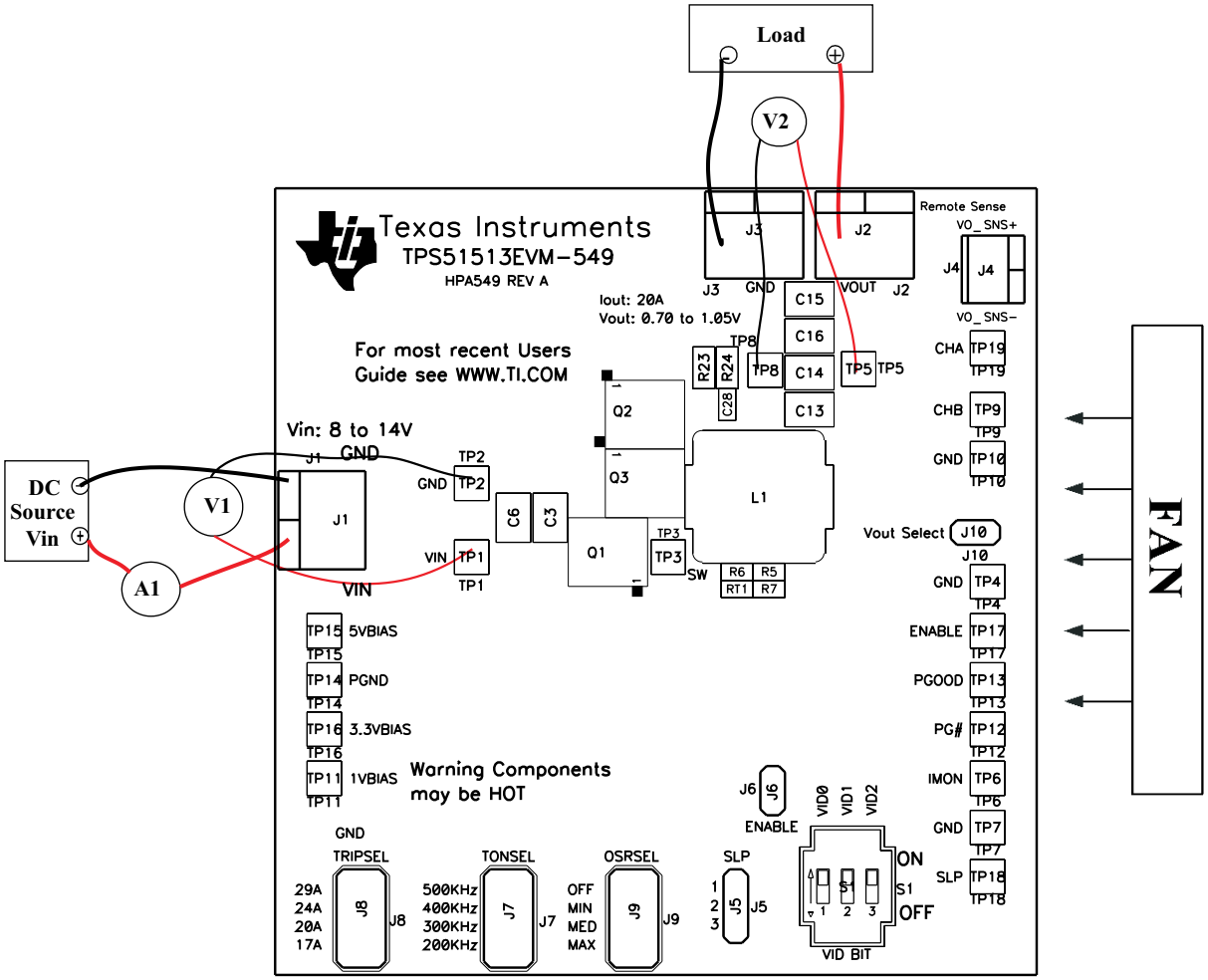

Figure 4-2. TPS51513EVM-549 Recommended Test Setup

Figure 4-2 is the recommended test setup to evaluate the TPS51513EVM-549. Working at an ESD workstation, ensure that any wrist straps, bootstraps, or mats are connected, referencing the user to earth ground before handling the EVM.

Input Connections:

1. Prior to connecting the dc input source, V_{IN}, it is advisable to limit the source current from V_{IN} to 10 A maximum. Ensure that V_{IN} is initially set to 0 V as shown in Figure 4-2.
2. Connect a voltmeter V1 at TP1 (VIN) and TP2 (GND) to measure the input voltage.
3. Connect a current meter A1 between V_{IN} DC source and J1.

Output Connections

1. Connect Load to J2, J3, and set Load to constant resistance mode to sink 0 A_{DC} before V_{IN} is applied.
2. Connect a voltmeter V2 at TP5 (VOUT) and TP8 (GND) to measure the output voltage.

Other Connections:

Place a fan as shown in Figure 4-2, and turn it on, ensuring that air is flowing across the EVM.

5 Configuration

All jumper selections must be made prior to applying power to the EVM. Users can configure this EVM with the following configurations.

5.1 Current Limit Trip Selection (J8: Trip Select)

The overcurrent protection (OCP) can be set by J8 Trip Select (TRIPSEL).

Default setting is 29 A.

Table 5-1. Current Limit Trip Selection

Jumper Set to	TRIPSEL	OCP Limit per Phase (Typ)
Top (1–2 pin shorted)	**5VFILT**	**29 A**
Second (3–4 pin shorted)	3.3VBIAS	24 A
Third (5–6 pin shorted)	VREF	20 A
Bottom (7–8 pin shorted)	GND	17 A

5.2 Frequency Selection (J7: TON Select)

The operating frequency can be set by J7 TON Select (TONSEL).

Default setting is 300 kHz.

Table 5-2. Frequency Selection

Jumper Set to	TONSEL	Frequency (kHz)
Top (1–2 pin shorted)	5VFILT	500
Second (3–4 pin shorted)	3.3VBIAS	350
Third (5–6 pin shorted)	**VREF**	**300**
Bottom (7–8 pin shorted)	GND	250

5.3 Overshoot Reduction Selection (J9: OSRTM Select)

The overshoot reduction can be set by J9 OSRTM Select (OSRSEL).

Default setting is Maximum.

Table 5-3. Overshoot Reduction Selection

Jumper set to	OSR	Overshoot Voltage Reduction
Top (1-2 pin shorted)	5VFILT	OFF
Second (3-4 pin shorted)	3.3VBIAS	Minimum
Third (5-6 pin shorted)	VREF	Medium
Bottom (7-8 pin shorted)	**GND**	**Maximum**

5.4 VID Bits Selection (S1)

The output voltage can be set by Switch S1 (VID Bits).

Default setting is 000.

Table 5-4. VID Bits Selection

3-Bit VID Table (1 = 1VBIAS, 0 = GND)			
VID2	**VID1**	**VID0**	**V_{OUT} (V)**
0	**0**	**0**	**1.05**
0	0	1	1.00
0	1	0	0.95
0	1	1	0.90
1	0	0	0.85
1	0	1	0.80

Table 5-4. VID Bits Selection (continued)

3-Bit VID Table (1 = 1VBIAS, 0 = GND)			
VID2	**VID1**	**VID0**	**V_{OUT} (V)**
1	1	0	0.75
1	1	1	0.70

5.5 Sleep Mode Selection (SLP)

The SLP can be set by J5 (SLP).

Default jumper setting on pin 2 and pin 3 of J5 to disable the SLP mode.

Table 5-5. SLP Mode Selection

Jumper set to	SLP Mode Selection
2-3 pin shorted	**Disable SLP mode**
1-2 pin shorted	Enable SLP mode

5.6 1.2-V Output Voltage Option (J10: V_{OUT} selection)

The 1.2-V output can be set by J10 (Vout Select).

Default setting: Jumper shorts on J10 to set 0.7-V to 1.05-V output.

Table 5-6. 1.2-V Output Option Selection

Jumper Set to	Output Range
No jumper	1.2-V output
Jumper shorted	**0.70 V to 1.05 V controlled by 3-bit VID**

6 Test Procedure

6.1 Line/Load Regulation and Efficiency Measurement Procedure

1. Ensure that Load is set to constant resistance mode and to sink 0 A_{DC}.
2. Ensure that the jumper provided with the EVM on J6 is present before V_{IN} is applied.
3. Increase V_{IN} from 0 V to 12 V. Use V1 to measure input voltage.
4. Remove the jumper on J6 to enable the controller.
5. Vary Load from 0 A_{DC} to 20 A_{DC}. V_{OUT} must remain in load regulation.
6. Vary V_{IN} from 8 V to 14 V. V_{OUT} must remain in line regulation.
7. Put the jumper on J6 to disable the controller.
8. Decrease Load to 0 A
9. Decrease V_{IN} to 0 V.

6.2 List of Test Points

Table 6-1. Functions of Each Test Points

Test Points	Name	Description
TP1	VIN	12 V_{IN}
TP2	GND	12 V_{IN} Ground
TP3	SW	Switching Node
TP4	GND	Ground
TP5	VOUT	$_{OUT}$
TP6	IMON	Current Monitor Output
TP7	GND	Ground
TP8	GND	V_{OUT} Ground
TP9	CHB	Input B for loop injection
TP10	GND	Ground
TP11	1Vbias	1-V bias
TP12	PG#	Negative Power Good, Active low
TP13	PGOOD	Power Good, Active high
TP14	GND	Ground
TP15	5Vbias	5-V bias
TP16	3.3Vbias	3.3-V bias
TP17	Enable	Enable, Active high
TP18	SLP	Sleep mode
TP19	CHA	Input A for loop injection

6.3 Equipment Shutdown

1. Shut down Load.
2. Shut down VIN.
3. Shut down FAN.

7 Performance Data and Typical Characteristic Curves

Figure 7-1 through Figure 7-10 present typical performance curves for TPS51513EVM-549. Jumpers are set to default locations; see Section 6 of this user's guide.

7.1 Efficiency

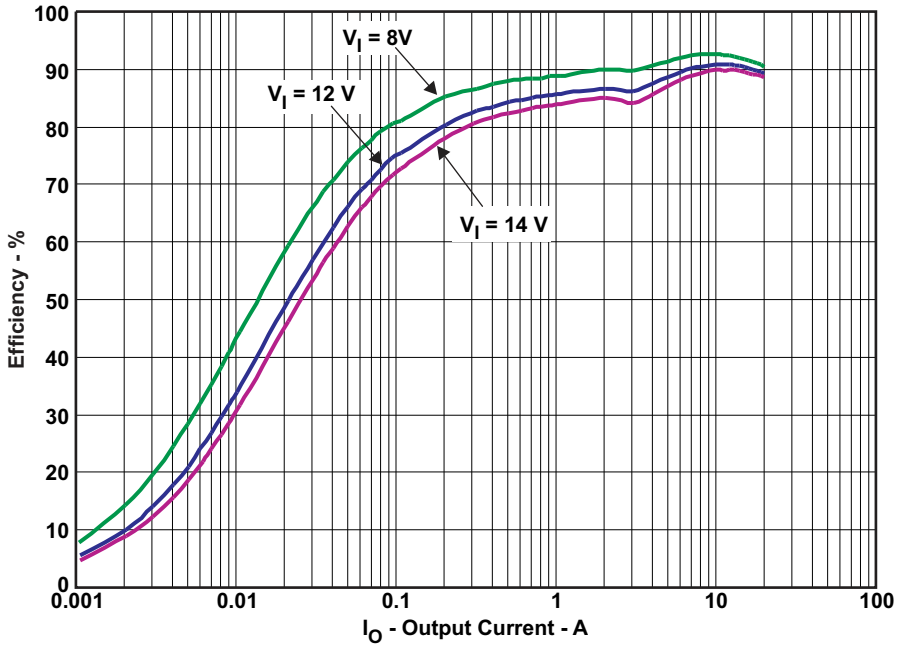

Figure 7-1. TPS51513EVM-549 Efficiency

7.2 Load Regulation

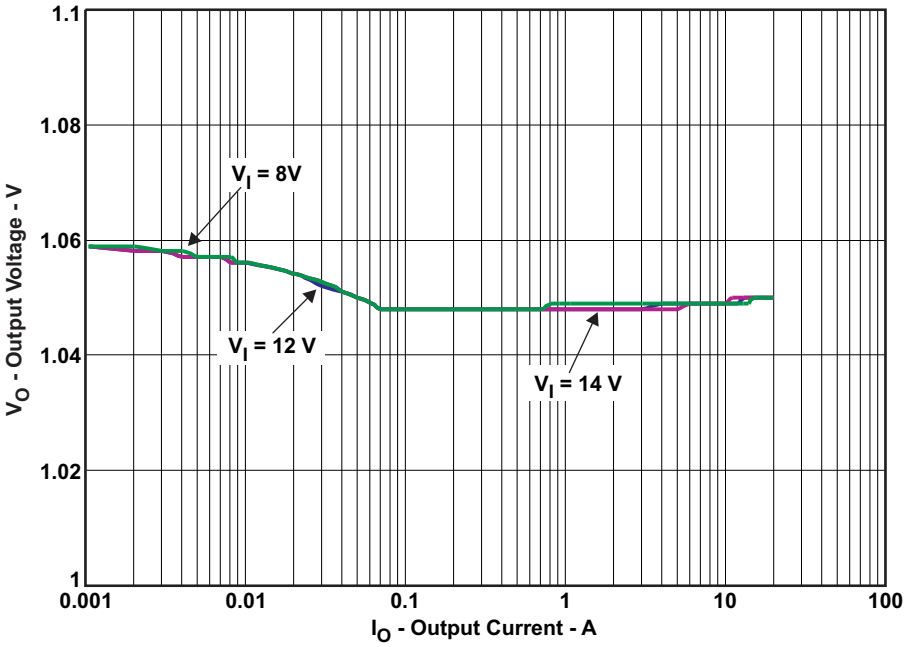

Figure 7-2. TPS51513EVM-549 Load Regulation

7.3 Line Regulation

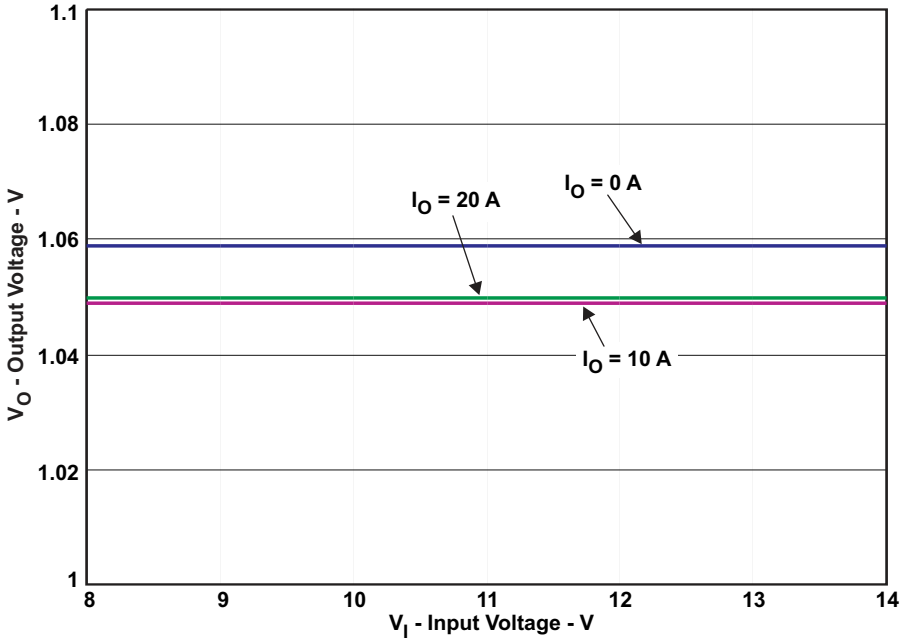

Figure 7-3. TPS51513EVM-549 Line Regulation

7.4 Current Monitor Voltage

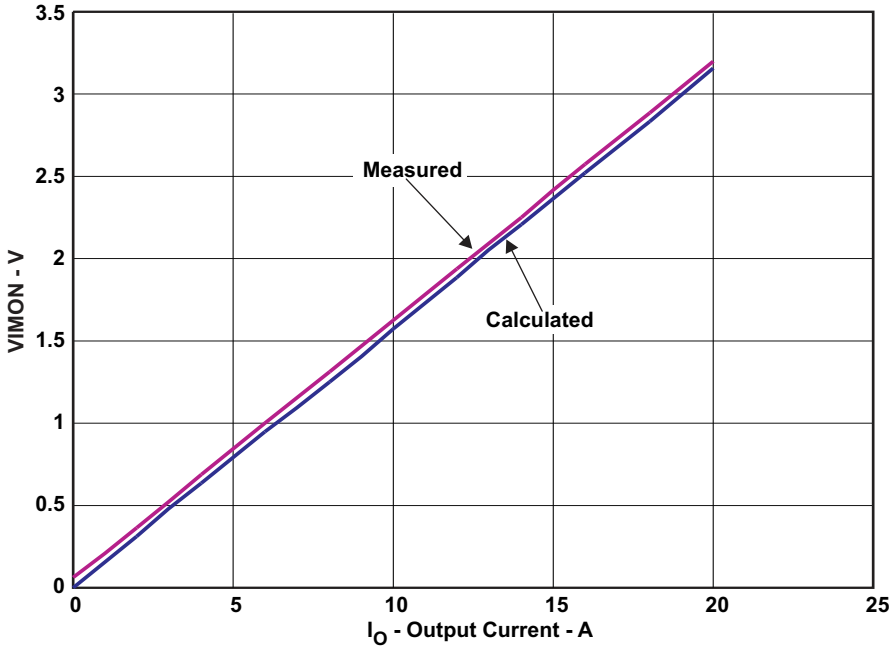

Figure 7-4. TPS51513EVM-549 IMON Voltage

7.5 Output Ripple

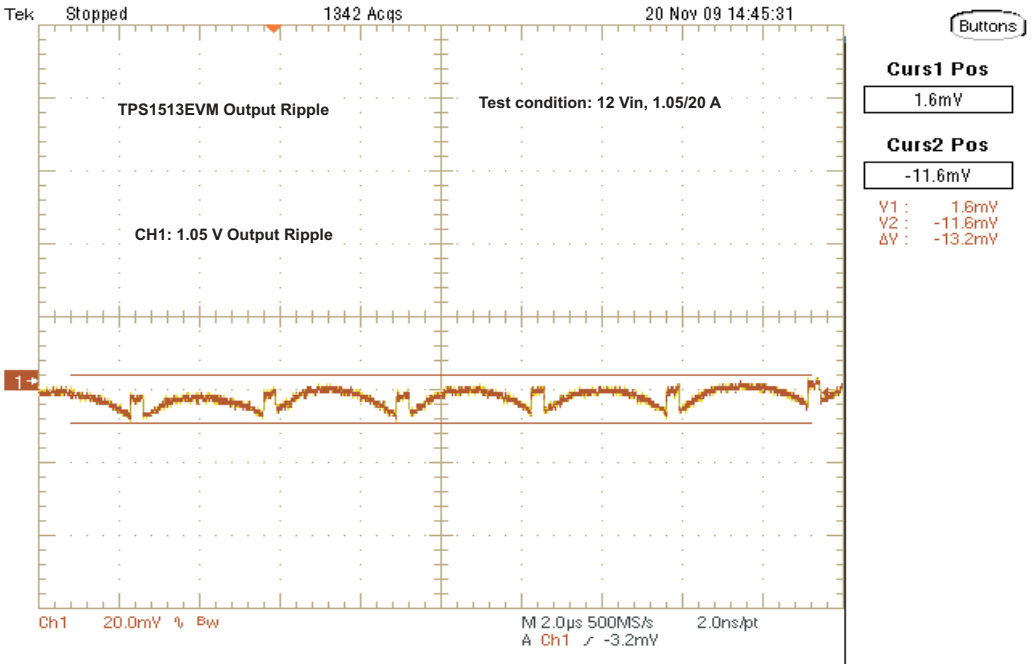

Figure 7-5. TPS51513EVM-549 Output Ripple (12 V_{IN}, 1.05 V/20 A)

7.6 Switching Node

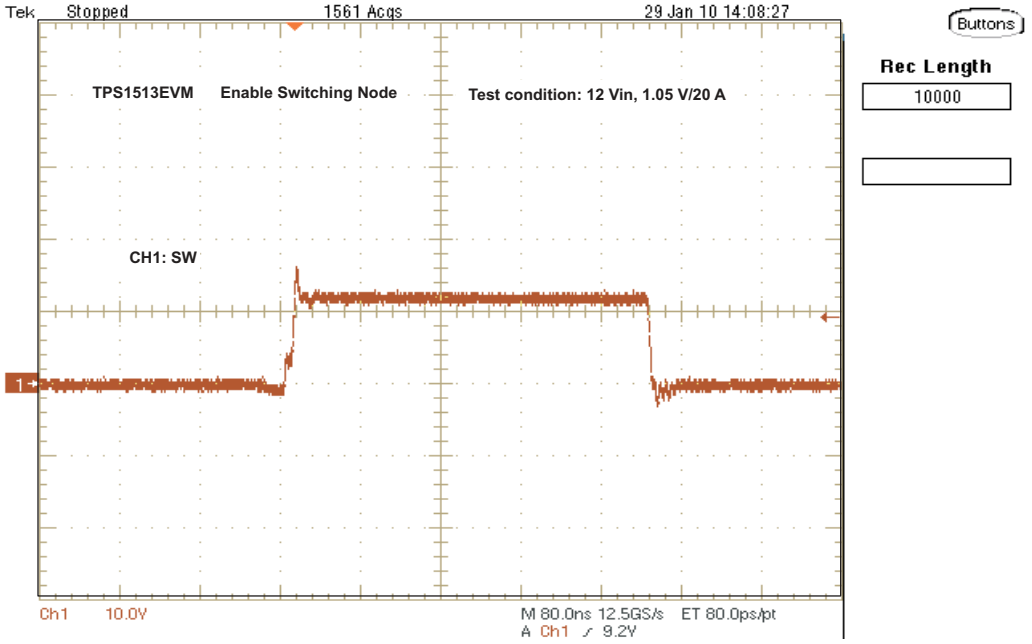

Figure 7-6. TPS51513EVM-549 Switching Node (12 V_{IN}, 1.05 V/20 A)

7.7 Output Transient

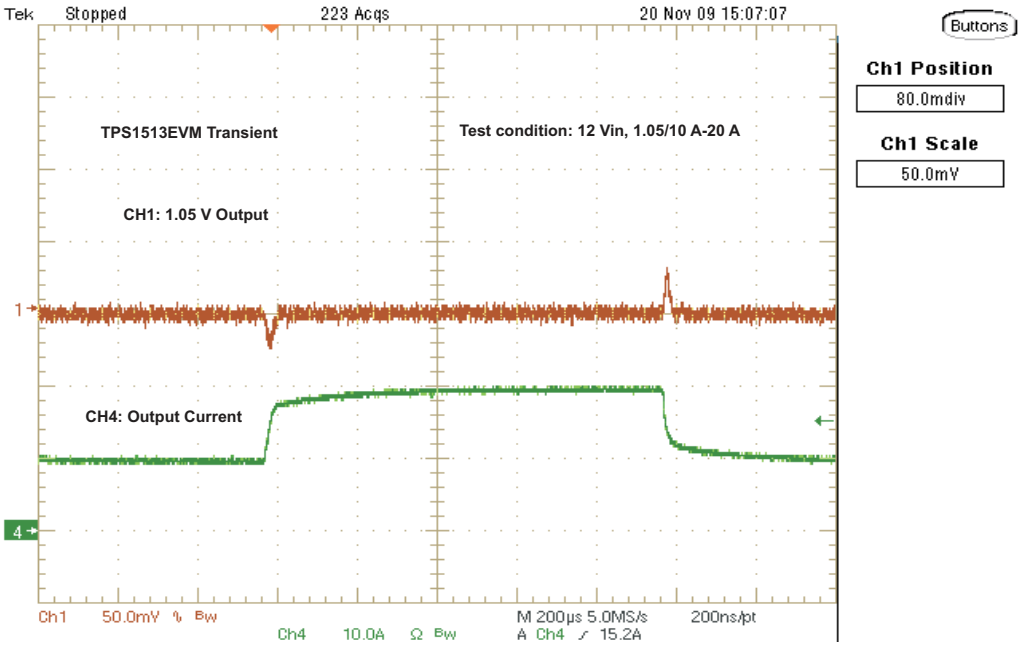

Figure 7-7. TPS51513EVM-549 Output Transient (12 V_I_, 1.05 V/10 A-20 A)

7.8 Turn-On Waveform

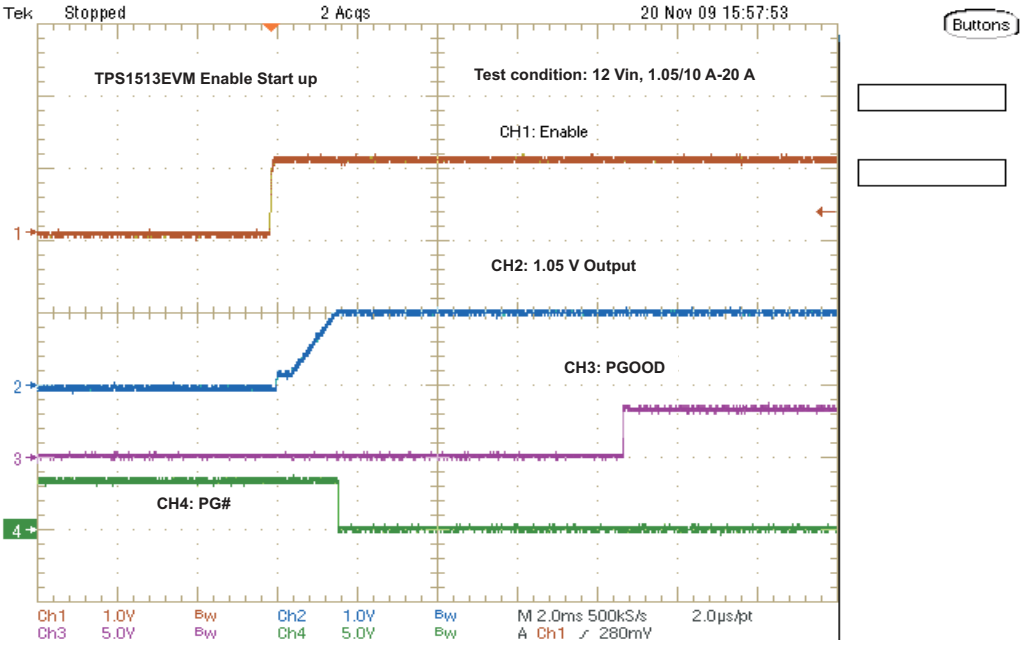

Figure 7-8. TPS51513EVM-549 Enable Turn-On Waveform (12 V_{IN}, 1.05 V/20 A)

7.9 Turn-Off Waveform

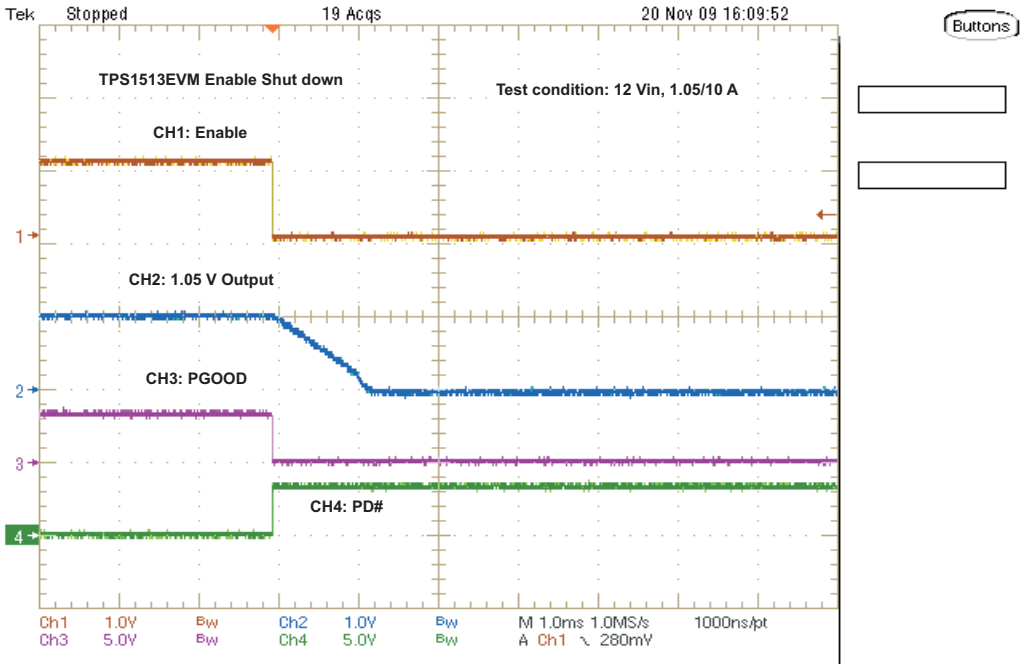

Figure 7-9. TPS51513EVM-549 Enable Turn-Off Waveform (12 V_{IN}, 1.05 V/10 A)

7.10 Bode Plot

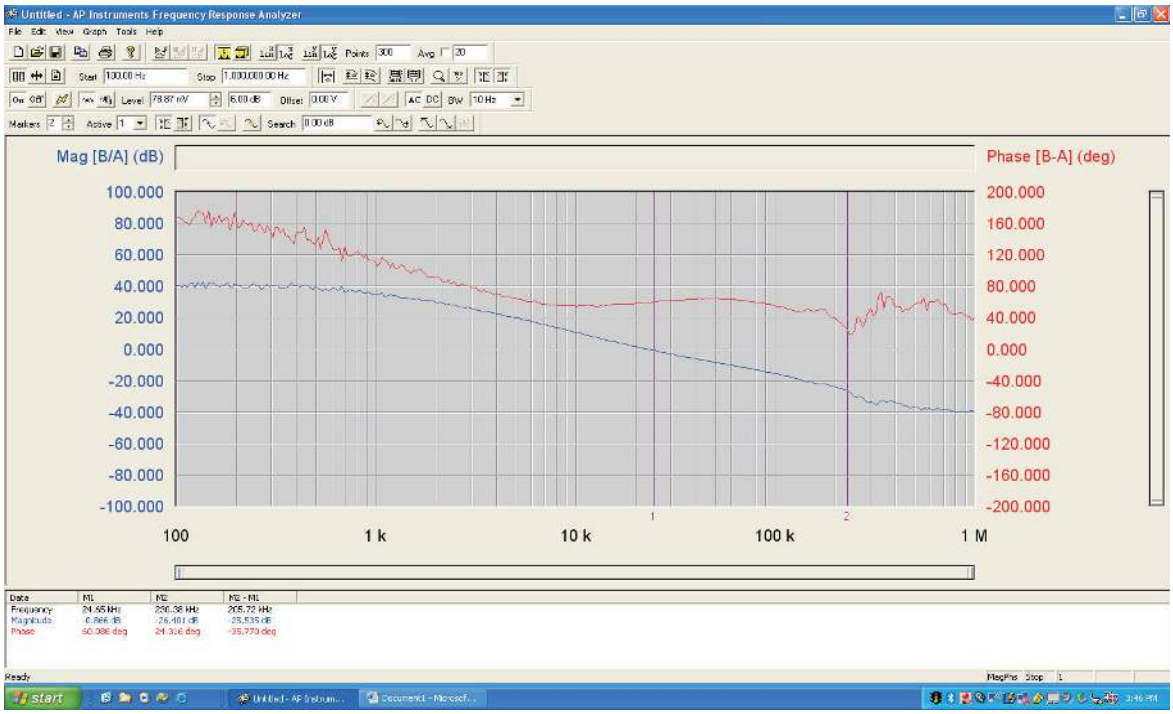

Figure 7-10. TPS51513EVM-549 Bode Plot (12 V_{IN}, 1.05 V/17 A)

8 EVM Assembly Drawing and PCB Layout

Figure 8-1 through Figure 8-8 show the design of the TPS51513EVM-549 printed-circuit board. The EVM has been designed using a six-layer circuit board with 2-oz copper on outside layers.

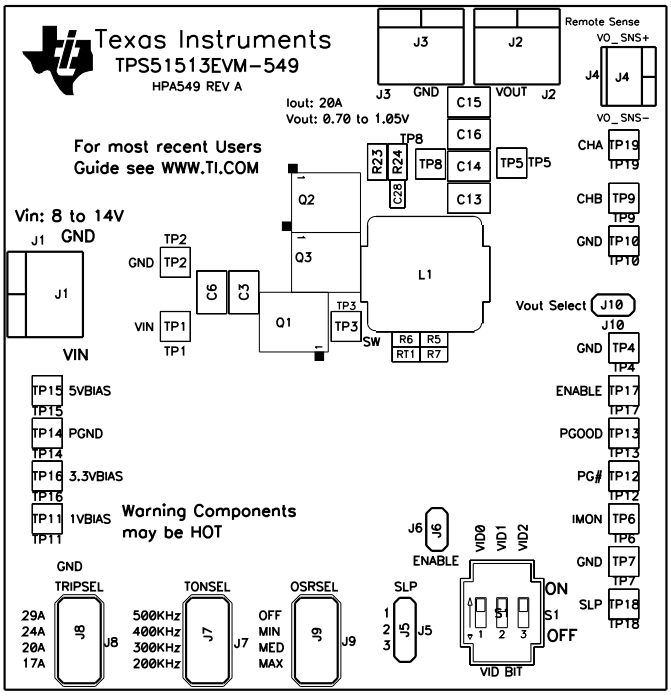

Figure 8-1. TPS51513EVM-549 Top Layer Assembly Drawing (Top View)

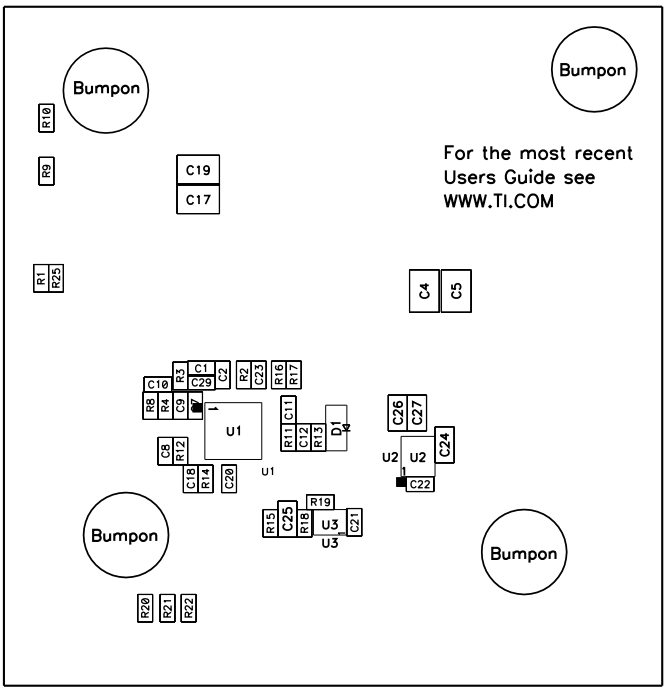

Figure 8-2. TPS51513EVM-549 Bottom Assembly Drawing (Bottom View)

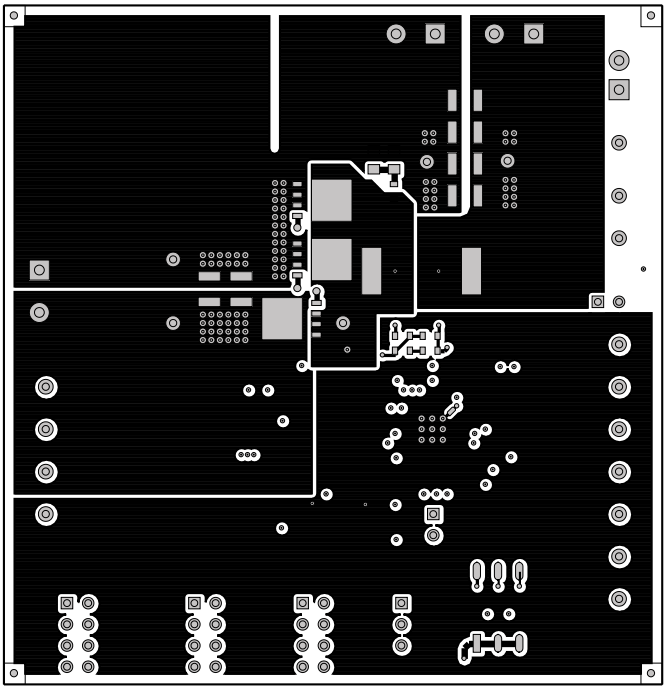

Figure 8-3. TPS51513EVM-549 Top Copper (Top View)

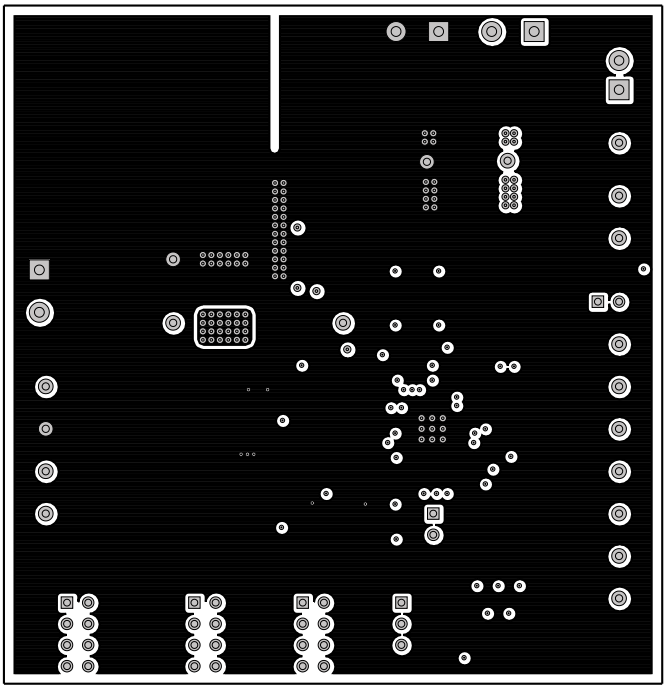

Figure 8-4. TPS51513EVM-549 Internal Layer 2 (Top View)

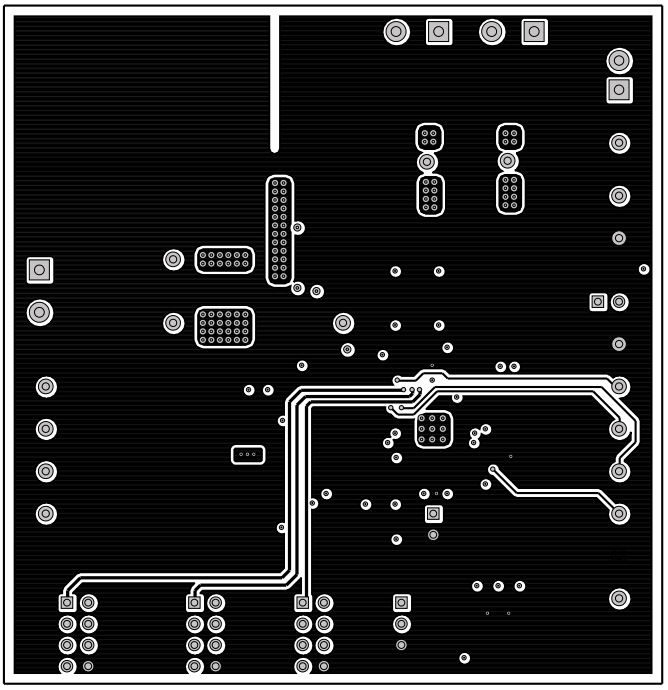

Figure 8-5. TPS51513EVM-549 Internal Layer 3 (Top View)

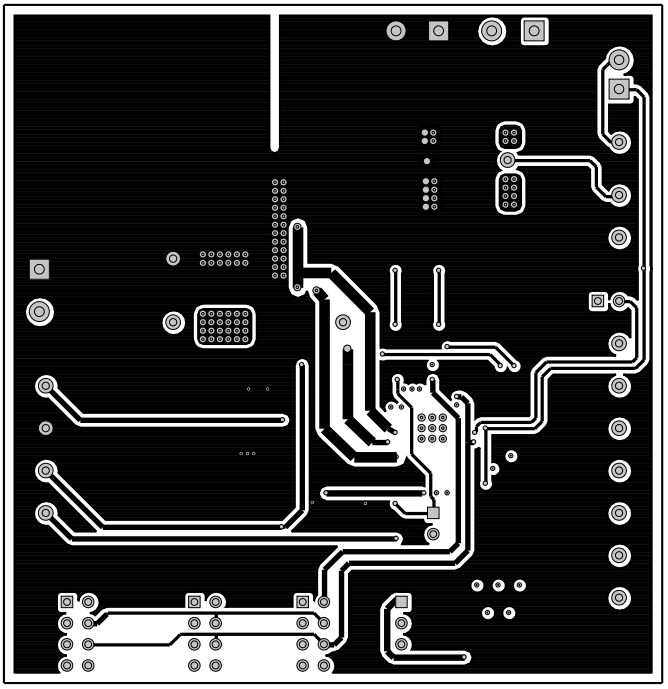

Figure 8-6. TPS51513EVM-549 Internal Layer 4 (Top View)

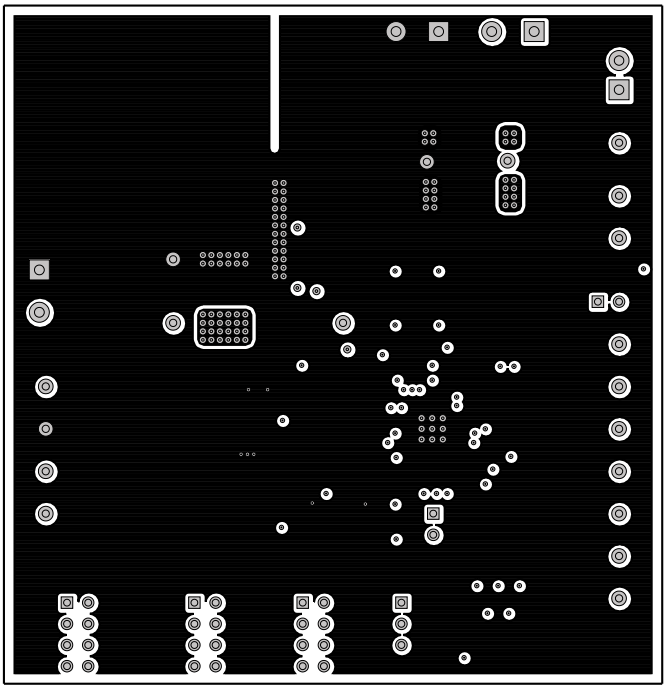

Figure 8-7. TPS51513EVM-549 Internal Layer 5 (Top View)

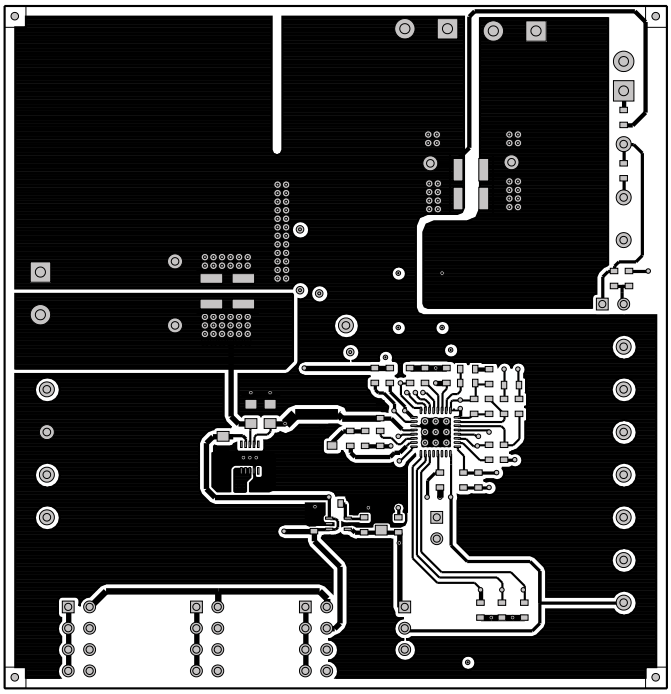

Figure 8-8. TPS51513EVM-549 Bottom Copper (Top View)

9 Bill of Materials

Table 9-1. The EVM Components List According to the Schematic Shown in Figure 3-1 and Figure 3-2

QTY	RefDes	Description	MFR	Part Number
1	C1	Capacitor, Ceramic, 4700 pF, 25 V, X7R, 10%, 0603	STD	STD
1	C10	Capacitor, Ceramic, 0.022 µF, 25 V, X7R, 10%, 0603	STD	STD
1	C12	Capacitor, Ceramic, 1 µF, 50 V, X5R, 10%, 0603	STD	STD
6	C13–C19	Capacitor, Ceramic, 100 µF, 6.3 V, X5R, 20%, 1210	Murata	GRM32ER60J107ME20L
2	C18, C23	Capacitor, Ceramic, 3300 pF, 10 V, X7R, 10%, 0603	STD	STD
1	C29	Capacitor, Ceramic, 47 pF, 25 V, C0G&NPO, 10%, 0603	STD	STD
2	C2, C11	Capacitor, Ceramic, 2.2 µF, 10 V, X5R, 10%, 0603	STD	STD
1	C20	Capacitor, Ceramic, 0.1 µF, 16 V, X7R, 10%, 0603	STD	STD
2	C21, C22	Capacitor, Ceramic, 1 µF, 10 V, X7R, 10%, 0603	STD	STD
1	C28	Capacitor, Ceramic, 3300 pF, 50 V, X7R, 10%, 0603	STD	STD
4	C24–C27	Capacitor, Ceramic, 10 µF, 16 V, X5R, 10%, 0805	STD	STD
4	C3, C4, C5, C6	Capacitor, Ceramic, 22 µF, 16 V, X5R, 10%, 1210	Murata	GRM32ER61C226KE20L
1	C7	Capacitor, Ceramic, 0.22 µF, 6.3 V, X7R, 10%, 0603	STD	STD
1	D1	Diode, Schottky, 0.5 A, 30 V, SOD-123	On Semi	MBR0520L
1	L1	Inductor, SMT, 0.47 µH, 41 A, 0.001 Ω, 20%	Vishay	IHLP5050FDERR47M01
2	R11, R13	Resistor, Chip, 2.05, 1/16W, 1%, 0603	STD	STD
1	R12	Resistor, Chip, 24.3 K, 1/16W, 1%, 0603	STD	STD
1	R14	Resistor, Chip, 90.9 K, 1/16W, 1%, 0603	STD	STD
6	R15–R17, R20–R22	Resistor, Chip, 10 K, 1/16W, 1%, 0603	STD	STD
1	R18	Resistor, Chip, 37.4 K, 1/16W, 1%, 0603	STD	STD
1	R19	Resistor, Chip, 100 K, 1/16W, 1%, 0603	STD	STD
1	R2	Resistor, Chip, 249 K, 1/16W, 1%, 0603	STD	STD
2	R23, R24	Resistor, Chip, 1.0, 1/10W, 5%, 0805	STD	STD
2	R4, R8	Resistor, Chip, 0, 1/16W, 1%, 0603	STD	STD
1	R3	Resistor, Chip, 1.69 K, 1/16W, 1%, 0603	STD	STD
1	R25	Resistor, Chip, 2.87 K, 1/16W, 1%, 0603	STD	STD
1	R1	Resistor, Chip, 20.0 K, 1/16W, 1%, 0603	STD	STD
1	R5	Resistor, Chip, 110 K, 1/16W, 1%, 0603	STD	STD
1	R6	Resistor, Chip, 25.5 K, 1/16W, 1%, 0603	STD	STD
1	R7	Resistor, Chip, 43.2 K, 1/16W, 1%, 0603	STD	STD
1	RT1	NTC, Chip, Thermistor, 150 K, 5%, 0603	Panasonic-ECG	ERT-J1VV154J
2	R9, R10	Resistor, Chip, 10, 1/16W, 1%, 0603	STD	STD
1	Q1	MOSFET, Nch, 25 V, 21 A, 5.7 mΩ, QFN5X6mm	TI(Ciclon)	CSD16404Q5A
2	Q2, Q3	MOSFET, Nch, 25 V, 31 A, 2.1 mΩ, QFN5X6mm	TI(Ciclon)	CSD16321Q5
1	U1	IC, Single-phase, D-CAP+, Synchronous Buck Controller, QFN-32	TI	TPS51513RHB
1	U2	IC, Integrated LDO with switch-over circuit, DGS10	TI	TPS51103DRC
1	U3	IC, 150-mA, LDO Linear Regulator, SC70	TI	TPS71701DCK

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (February 2010) to Revision A (January 2022) **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document. 2

- Updated user's guide title..... 2

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265