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Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

FAIRCHILD SEMICONDUCTOR

February 1990
Revised May 2005

MM74HCT573 • MM74HCT574
Octal D-Type Latch • 3-STATE Octal D-Type Flip-Flop

General Description

The MM74HCT573 octal D-type latches and MM74HCT574 octal D-type flip-flop advanced silicon-gate CMOS technology, which provides the inherent benefits of low power consumption and wide power supply range, but are LS-TTL input and output characteristic and pin-out compatible. The 3-STATE outputs are capable of driving 15 LS-TTL loads. All inputs are protected from damage due to static discharge by internal diodes to V_{CC} and ground.

When the MM74HCT573 Latch Enable input is HIGH, the Q outputs will follow the D inputs. When the Latch Enable goes LOW, data at the D inputs will be retained at the outputs until Latch Enable returns HIGH again. When a high logic level is applied to the Output Control input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

The MM74HCT574 are positive edge triggered flip-flops. Data at the D inputs, meeting the setup and hold time requirements, are transferred to the Q outputs on positive going transitions of the Clock (CK) input. When a high logic level is applied to the Output Control (OC) input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

The MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

Features

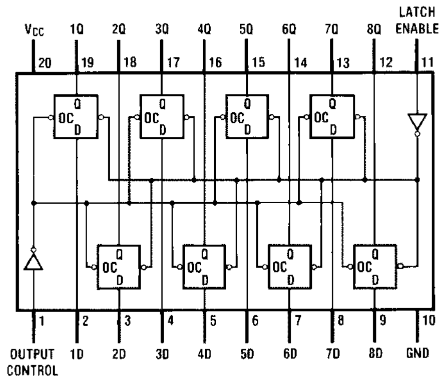
- TTL input characteristic compatible
- Typical propagation delay: 18 ns
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA maximum
- Compatible with bus-oriented systems
- Output drive capability: 15 LS-TTL loads

Ordering Codes:

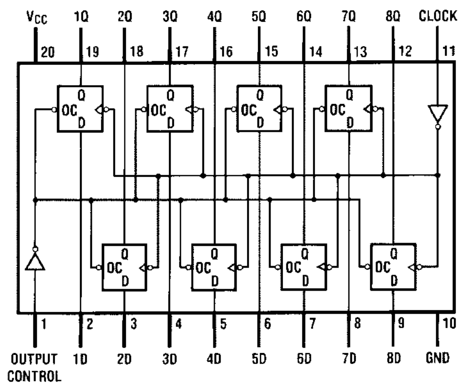
Order Number	Package Number	Package Description
MM74HCT573WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
MM74HCT573SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HCT573MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HCT573N	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
MM74HCT574WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
MM74HCT574SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HCT574MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HCT574N	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending suffix letter “X” to the ordering code.

Connection Diagrams



Top View
MM74HCT573



Top View
MM74HCT574

Truth Tables

MM74HCT573

Output Control	LE	Data	Output
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

H = HIGH Level
L = LOW Level
Q_0 = Level of output before steady-state input conditions were established.
Z = High Impedance State

MM74HCT574

Output Control	LE	Data	Output
L	$\uparrow$	H	H
L	$\uparrow$	L	L
L	L	X	Q_0
H	X	X	Z

H = HIGH Level
L = LOW Level
Q_0 = Level of output before steady-state input conditions were established.
X = Don't Care
Z = High Impedance State
$\uparrow$ = Transition from LOW-to-HIGH

Absolute Maximum Ratings(Note 1)

(Note 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+ 1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+ 0.5V
Clamp Diode Current (I_{IK}, I_{OK})	± 20 mA
DC Output Current, per pin (I_{OUT})	± 35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	± 70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S. O. Package only	500 mW
Lead Temperature (T_L)	
(Soldering 10 seconds)	260°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage			
(V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)	−40	+85	°C
Input Rise or Fall Times			
t_r, t_f		500	ns

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C.

DC Electrical Characteristics

V_{CC} = 5V ± 10% (unless otherwise specified)

Symbol	Parameter	Conditions	T_A = 25°C	T_A = −40 to 85°C	T_A = −55 to 125°C		Units
			Typ	Guaranteed Limits			
V_{IH}	Minimum HIGH Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum LOW Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum HIGH Level Output Voltage	V_{IN} = V_{IH} or V_{IL}					V
		$\|I_{OUT}\|$ = 20 μA	V_{CC}	V_{CC} − 0.1	V_{CC} − 0.1	V_{CC} − 0.1	
		$\|I_{OUT}\|$ = 6.0 mA, V_{CC} = 4.5V	4.2	3.98	3.84	3.7	
		$\|I_{OUT}\|$ = 7.2 mA, V_{CC} = 5.5V	5.7	4.98	4.84	4.7	
V_{OL}	Maximum LOW Level Voltage	V_{IN} = V_{IH} or V_{IL}					V
		$\|I_{OUT}\|$ = 20 μA	0	0.1	0.1	0.1	
		$\|I_{OUT}\|$ = 6.0 mA, V_{CC} = 4.5V	0.2	0.26	0.33	0.4	
		$\|I_{OUT}\|$ = 7.2 mA, V_{CC} = 5.5V	0.2	0.26	0.33	0.4	
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND, V_{IH} or V_{IL}		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum 3-STATE Output Leakage Current	V_{OUT} = V_{CC} or GND Enable = V_{IH} or V_{IL}		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA		8.0	80	160	μA
		V_{IN} = 2.4V or 0.5V (Note 4)		1.5	1.8	2.0	mA

Note 4: Measured per pin. All others tied to V_{CC} or ground.

AC Electrical Characteristics MM74HCT573

V_{CC} = 5.0V, $t_r = t_f$ = 6 ns, T_A = 25°C (unless otherwise specified)

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL} t_{PLH}	Maximum Propagation Delay Data to Output	C_L = 45 pF	17	27	ns
t_{PHL} t_{PLH}	Maximum Propagation Delay Latch Enable to Output	C_L = 45 pF	16	27	ns
t_{PZH} t_{PZL}	Maximum Enable Propagation Delay Control to Output	C_L = 45 pF R_L = 1 kΩ	21	30	ns
t_{PHZ} t_{PLZ}	Maximum Disable Propagation Delay Control to Output	C_L = 5 pF R_L = 1 kΩ	14	23	ns
t_W	Minimum Clock Pulse Width			15	ns
t_S	Minimum Setup Time Data to Clock			5	ns
t_H	Minimum Hold Time Clock to Data			12	ns

AC Electrical Characteristics MM74HCT573

V_{CC}= 5.0V ± 10%, $t_r = t_f$ = 6 ns (unless otherwise specified)

Symbol	Parameter	Conditions	T_A = 25°		T_A = −40 to 85°C	T_A = −55 to 125°C	Units
			Typ	Guaranteed Limits			
t_{PHL} t_{PLH}	Maximum Propagation Delay Data to Output	C_L = 50 pF	18	30	38	45	ns
t_{PHL} t_{PLH}	Maximum Propagation Delay Latch Enable to Output	C_L = 50 pF	17	30	44	53	ns
t_{PZH} t_{PZL}	Maximum Enable Propagation Delay Control to Output	C_L = 50 pF R_L = 1 kΩ	22	30	38	45	ns
t_{PHZ} t_{PLZ}	Maximum Disable Propagation Delay Control to Output	C_L = 50 pF R_L = 1 kΩ	15	30	38	45	ns
t_{THL} t_{TLH}	Maximum Output Rise and Fall Time	C_L = 50 pF	6	12	15	18	ns
t_W	Minimum Clock Pulse Width			15	20	24	ns
t_S	Minimum Setup Time Data to Clock		−3	5	6	8	ns
t_H	Minimum Hold Time Clock to Data		4	12	15	18	ns
C_{IN}	Maximum Input Capacitance			10	10	10	pF
C_{OUT}	Maximum Output Capacitance			20	20	20	pF
C_{PD}	Power Dissipation Capacitance (Note 5)	OC = V_{CC} OC = GND		5 52			pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}2 f{+}I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f{+}I_{CC}$.

AC Electrical Characteristics MM74HCT574

V_{CC} = 5.0V, $t_r = t_f$ = 6 ns, T_A = 25°C

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Clock Frequency		60	33	MHz
t_{PHL} t_{PLH}	Maximum Propagation Delay to Output	C_L = 45 pF	17	27	ns
t_{PZH} t_{PZL}	Maximum Enable Propagation Delay Control to Output	C_L = 45 pF R_L = 1 kΩ	19	28	ns
t_{PHZ} t_{PLZ}	Maximum Disable Propagation Delay Control to Output	C_L = 45 pF R_L = 1 kΩ	14	25	ns
t_W	Minimum Clock Pulse Width			15	ns
t_S	Minimum Setup Time Data to Clock			12	ns
t_H	Minimum Hold Time Clock to Data			5	ns

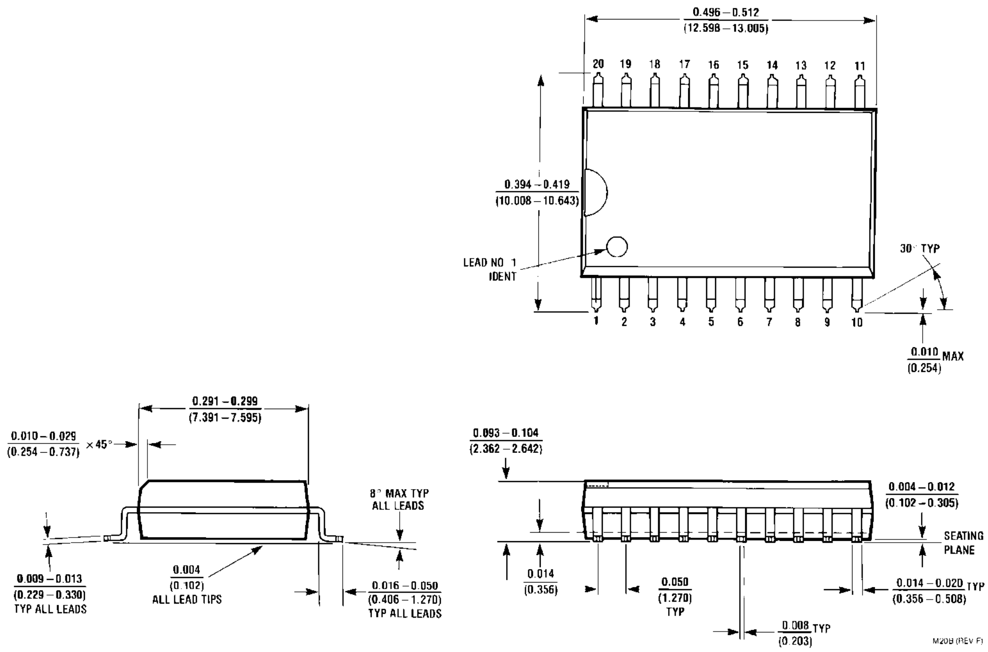
AC Electrical Characteristics MM74HCT574

V_{CC} = 5.0V ± 10%, $t_r = t_f$ = 6 ns (unless otherwise specified)

Symbol	Parameter	Conditions	T_A = 25°C		T_A = −40 to 85°C	T_A = −55 to 125°C	Units
			Typ	Guaranteed Limits			
f_{MAX}	Maximum Clock Frequency			33	28	23	MHz
t_{PHL} t_{PLH}	Maximum Propagation Delay Clock to Output	C_L = 50 pF	18	30	38	45	ns
t_{PZH} t_{PZL}	Maximum Enable Propagation Delay Control to Output	C_L = 50 pF R_L = 1 kΩ	22	30	38	45	ns
t_{PHZ} t_{PLZ}	Maximum Disable Propagation Delay Control to Output	C_L = 50 pF R_L = 1 kΩ	15	30	38	45	ns
t_{THL} t_{TLH}	Maximum Output Rise and Fall Time	C_L = 50 pF	6	12	15	18	ns
t_W	Minimum Clock Pulse Width			15	20	24	ns
t_S	Minimum Setup Time Data to Clock		6	12	15	18	ns
t_H	Minimum Hold Time Clock to Data		−1	5	6	8	ns
C_{IN}	Maximum Input Capacitance			10	10	10	pF
C_{OUT}	Maximum Output Capacitance			20	20	20	pF
C_{PD}	Power Dissipation Capacitance (Note 6)	OC = V_{CC} OC = GND	5 58				pF

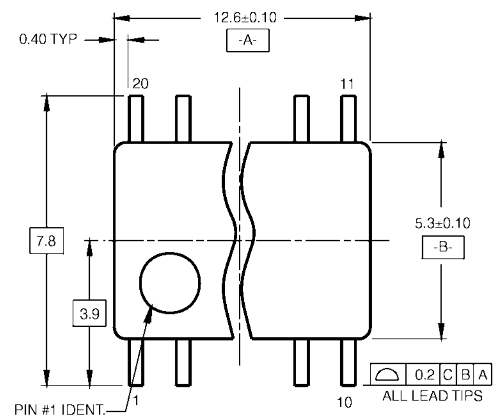
Note 6: C_{PD} determines the no load power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

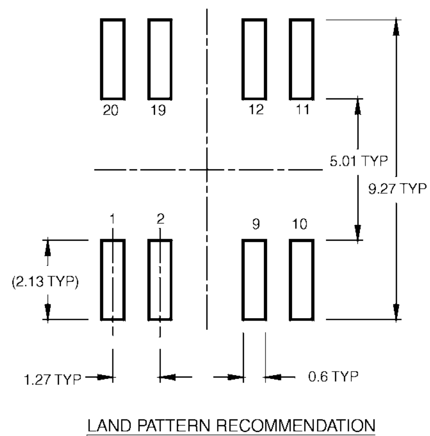
Physical Dimensions inches (millimeters) unless otherwise noted

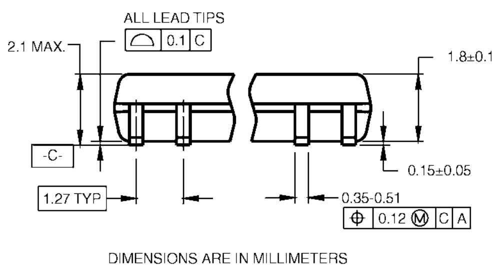


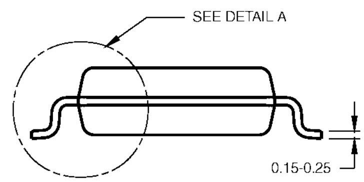
20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
Package Number M20B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)









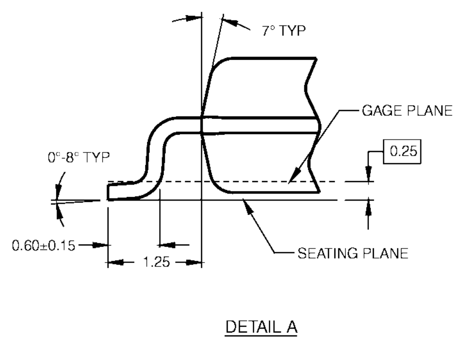
NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.

B. DIMENSIONS ARE IN MILLIMETERS.

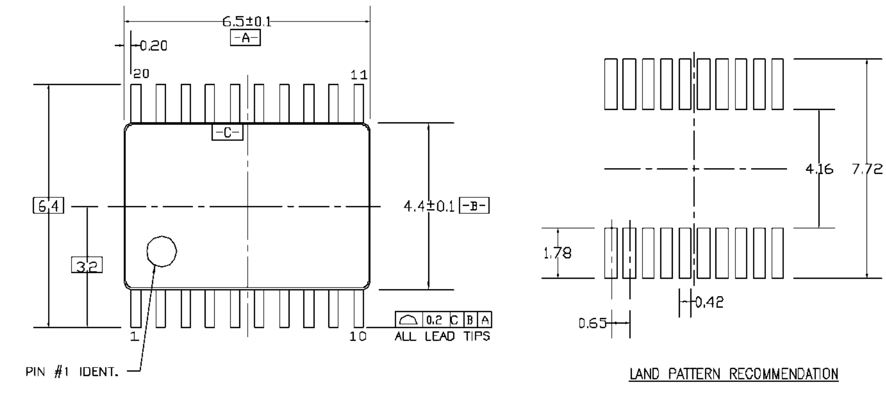
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

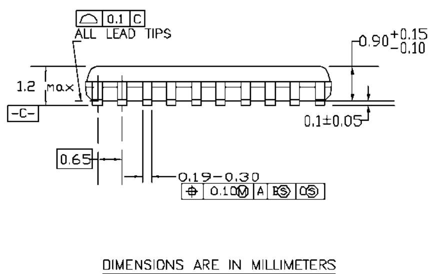
M20DRevB1

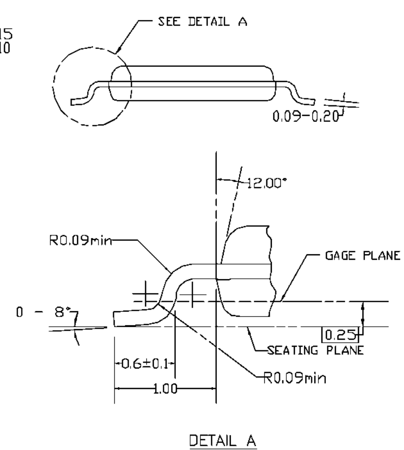


20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M20D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)







NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.

B. DIMENSIONS ARE IN MILLIMETERS.

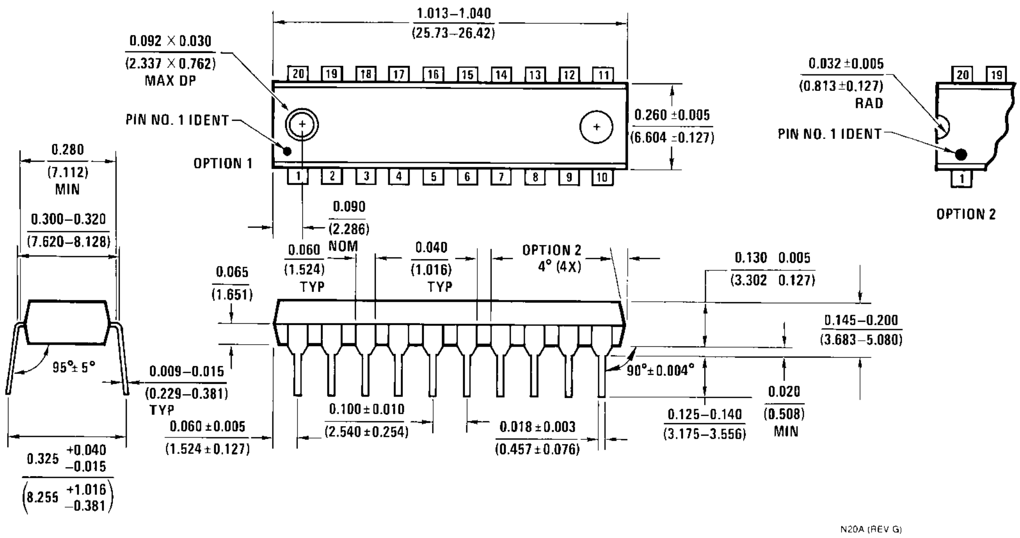
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH, AND TIE BAR EXTRUSIONS.

D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC20REVD1

20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC20

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N20A

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