

Product Summary

$V_{(BR)DSS}$	$R_{DS(ON)}$ max	I_D max $T_A = +25^\circ\text{C}$
-20V	45m Ω @ $V_{GS} = -4.5\text{V}$	-4.5A
	65m Ω @ $V_{GS} = -2.5\text{V}$	-3.8A

Description

This new generation MOSFET is designed to minimize the on-state resistance ($R_{DS(on)}$), and yet maintain superior switching performance, making it ideal for high-efficiency power management applications.

Applications

- General Purpose Interfacing Switch
- Power Management Functions

Features and Benefits

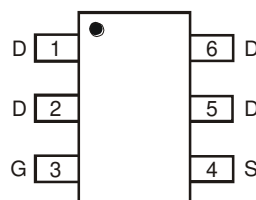
- Low On-Resistance
- Low Gate Threshold Voltage
- Low Input Capacitance
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **Qualified to AEC-Q101 Standards for High Reliability**

Mechanical Data

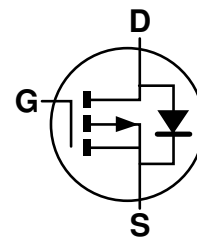
- Case: SOT26
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections: See Diagram
- Terminals: Finish — Matte Tin Annealed over Copper Leadframe. Solderable per MIL-STD-202, Method 208 (63)
- Weight: 0.015 grams (Approximate)



Top View



Top View
Pin-Out



Equivalent Circuit

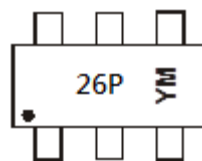
Ordering Information (Note 4)

Part Number	Case	Packaging
DMP2066LVT-7	SOT26	3,000/Tape & Reel
DMP2066LVT-13	SOT26	10,000/Tape & Reel

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
 2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds. For packaging details, go to our website at <http://www.diodes.com>.
 4. For packaging details, go to our website at <http://www.diodes.com/products/packages.html>.

Marking Information

SOT26



Shanghai A/T Site

26P = Product Type Marking Code
 YM = Date Code Marking for SAT (Shanghai Assembly/ Test site)
 Y or Y = Year (ex: A = 2013)
 M = Month (ex: 9 = September)

Date Code Key

Year	2011	2012	2013	2014	2015	2016	2017
Code	Y	Z	A	B	C	D	E

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

Maximum Ratings (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic	Symbol	Value	Unit	
Drain-Source Voltage	V_{DSS}	-20	V	
Gate-Source Voltage	V_{GSS}	± 8	V	
Drain Current (Note 5) Continuous	I_D	$T_A = +25^\circ\text{C}$	-4.5	A
		$T_A = +70^\circ\text{C}$	-3.7	
Pulsed Drain Current (10 μs pulse, duty cycle = 1%)	I_{DM}	-20	A	
Body-Diode Continuous Current (Note 5)	I_S	-2.0	A	

Thermal Characteristics (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic	Symbol	Value	Units
Total Power Dissipation (Note 5)	P_D	1.2	W
Thermal Resistance, Junction to Ambient (Note 5)	Steady State	100	$^\circ\text{C/W}$
	$t < 10\text{s}$	74	
Total Power Dissipation (Note 6)	P_D	1.8	W
Thermal Resistance, Junction to Ambient (Note 6)	Steady State	70	$^\circ\text{C/W}$
	$t < 10\text{s}$	46	
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to +150	$^\circ\text{C}$

Electrical Characteristics (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
STATIC PARAMETERS (Note 7)						
Drain-Source Breakdown Voltage	BV_{DSS}	-20	—	—	V	$I_D = -250\mu\text{A}, V_{GS} = 0\text{V}$
Zero Gate Voltage Drain Current	I_{DSS}	—	—	-1	μA	$V_{DS} = -16\text{V}, V_{GS} = 0\text{V}$
@ $T_J = +55^\circ\text{C}$ (Note 8)				-10		$V_{DS} = -16\text{V}, V_{GS} = 0\text{V}$
Zero Gate Voltage Drain Current	I_{DSS}	—	—	-100	μA	@ $T_J = +150^\circ\text{C}$ (Note 8) $V_{DS} = -16\text{V}, V_{GS} = 0\text{V}$
Gate-Body Leakage Current	I_{GSS}	—	—	± 100	nA	$V_{DS} = 0\text{V}, V_{GS} = \pm 8\text{V}$
Gate Threshold Voltage	$V_{GS(th)}$	-0.4	—	-1.5	V	$V_{DS} = V_{GS}, I_D = -250\mu\text{A}$
Static Drain-Source On-Resistance	$R_{DS(on)}$	—	25 33	45 65	m Ω	$V_{GS} = -4.5\text{V}, I_D = -4.5\text{A}$ $V_{GS} = -2.5\text{V}, I_D = -3.8\text{A}$
Static Drain-Source On-Resistance @ $T_J = +125^\circ\text{C}$ (Note 8)	$R_{DS(on)}$	—	—	72	m Ω	$V_{GS} = -4.5\text{V}, I_D = -4.5\text{A}$
Diode Forward Voltage	V_{SD}	-0.5	-0.72	-1.4	V	$I_S = -2.1\text{A}, V_{GS} = 0\text{V}$
On State Drain Current (Note 8)	$I_{D(on)}$	10	—	—	A	$V_{DS} \leq 5\text{V}, V_{GS} = 4.5\text{V}$
DYNAMIC PARAMETERS (Note 8)						
Input Capacitance	C_{iss}	—	1,496	2,990	pF	$V_{DS} = -15\text{V}, V_{GS} = 0\text{V}$ $f = 1.0\text{MHz}$
Output Capacitance	C_{oss}	—	130	260	pF	
Reverse Transfer Capacitance	C_{rss}	—	116	230	pF	
Total Gate Charge	Q_G	—	14.4	25	nC	$V_{DS} = -10\text{V}, V_{GS} = -4.5\text{V},$ $I_D = -4.5\text{A}$
Gate-Source Charge	Q_{GS}	—	2.6	5		
Gate-Drain Charge	Q_{GD}	—	2.7	5.5		
Turn-On Delay Time	$t_{d(on)}$	—	8.5	30	ns	$V_{DS} = -5\text{V}, V_{GS} = -4.5\text{V},$ $I_D = -1\text{A}, R_G = 6.0\Omega$
Rise Time	t_r	—	11	60		
Turn-Off Delay Time	$t_{d(off)}$	—	61	130		
Fall Time	t_f	—	25	100		

- Notes: 5. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
6. Device mounted on FR-4 substrate PC board, 2oz copper, with 1 inch square copper plate.
7. Short duration pulse test used to minimize self-heating effect.
8. Guaranteed by design. Not subject to product testing.

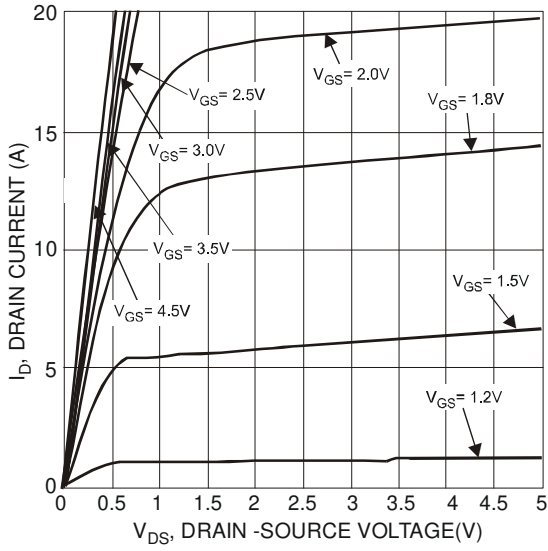


Figure 1 Typical Output Characteristics

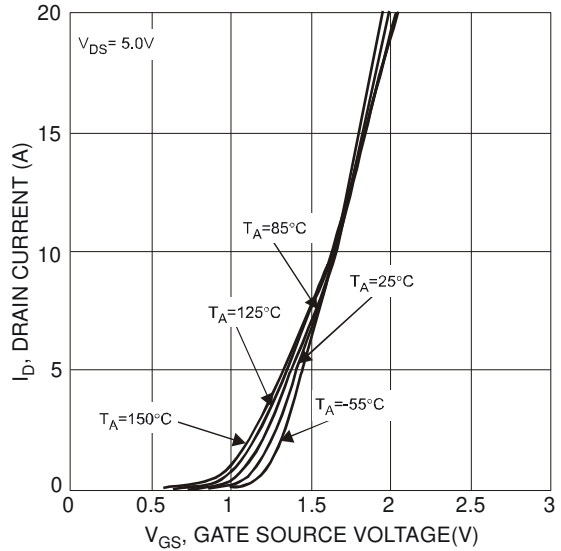


Figure 2 Typical Transfer Characteristics

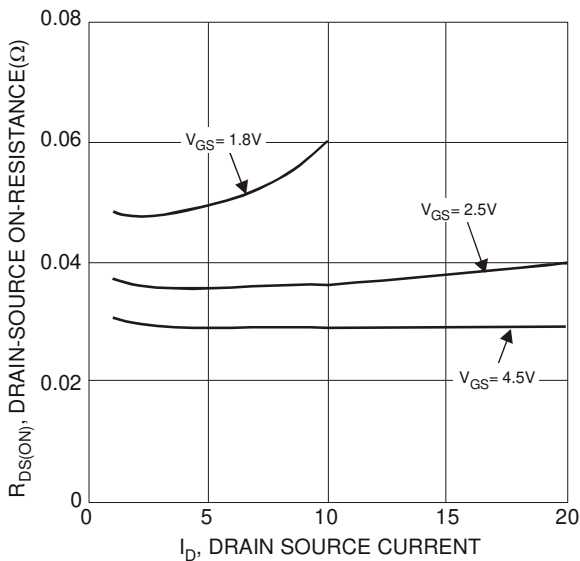


Figure 3 Typical On-Resistance vs. Drain Current and Gate Voltage

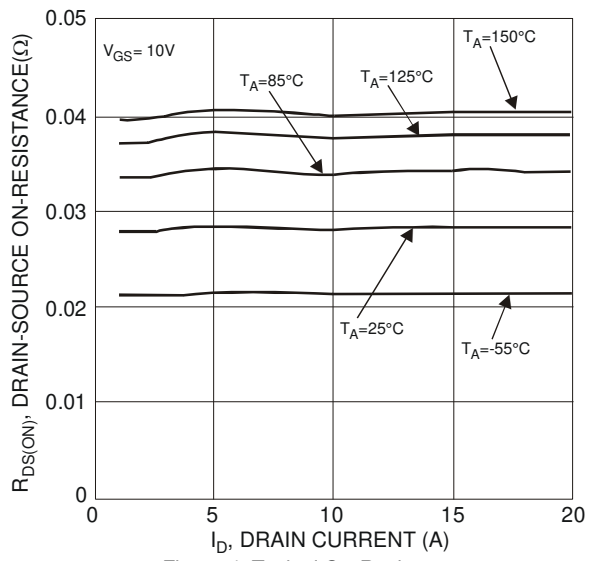


Figure 4 Typical On-Resistance vs. Drain Current and Temperature

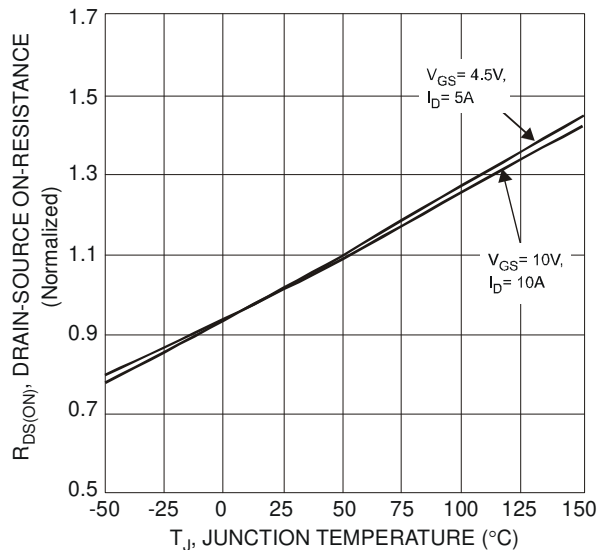


Figure 5 On-Resistance Variation with Temperature

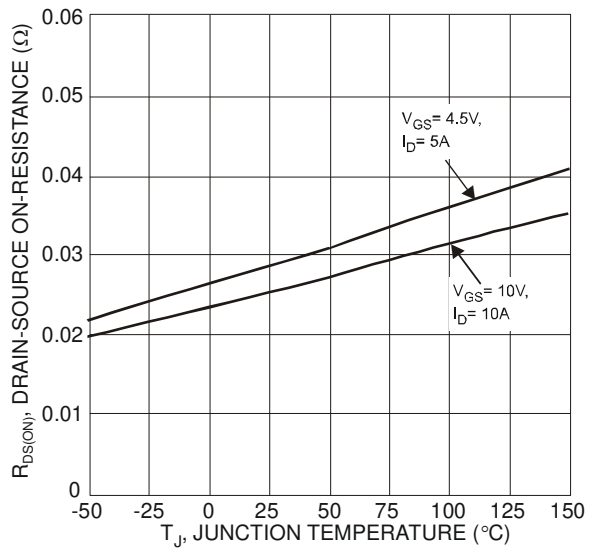


Figure 6 On-Resistance Variation with Temperature

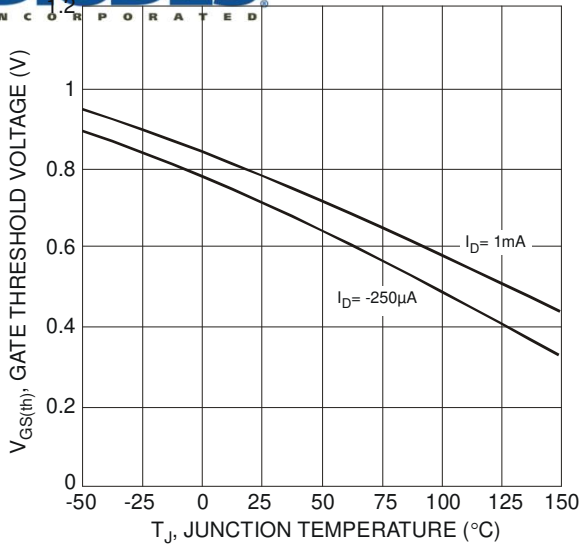


Figure 7 Gate Threshold Variation vs. Ambient Temperature

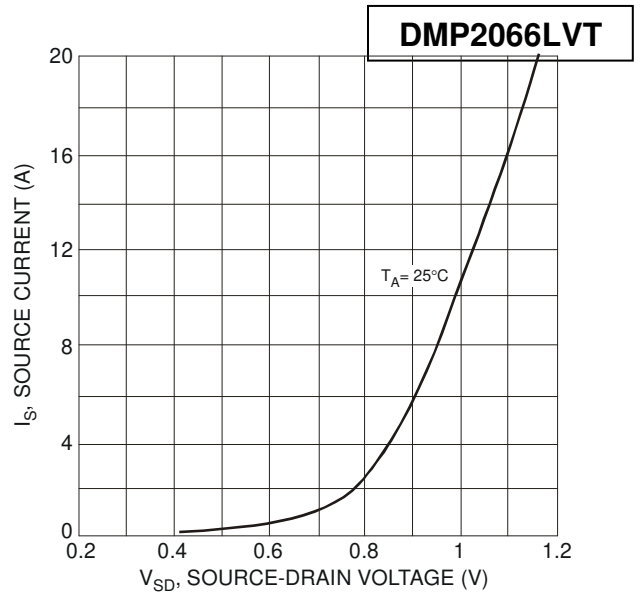


Figure 8 Diode Forward Voltage vs. Current

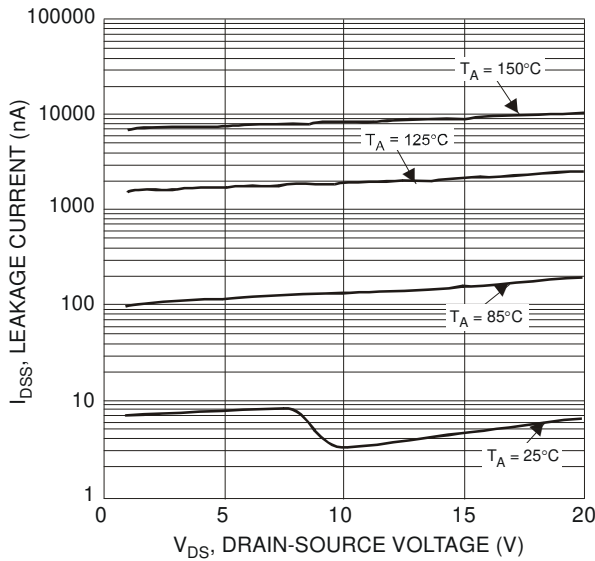


Figure 9 Typical Drain-Source Leakage Current vs. Voltage

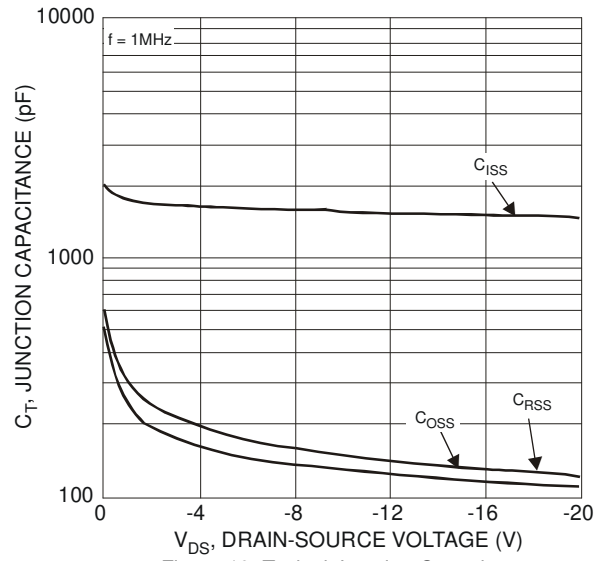


Figure 10 Typical Junction Capacitance

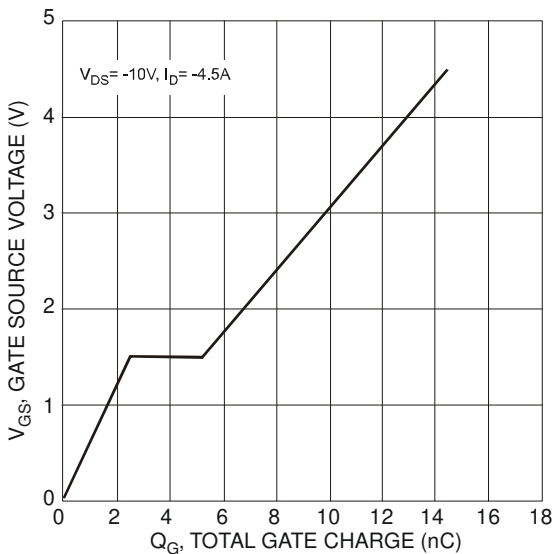
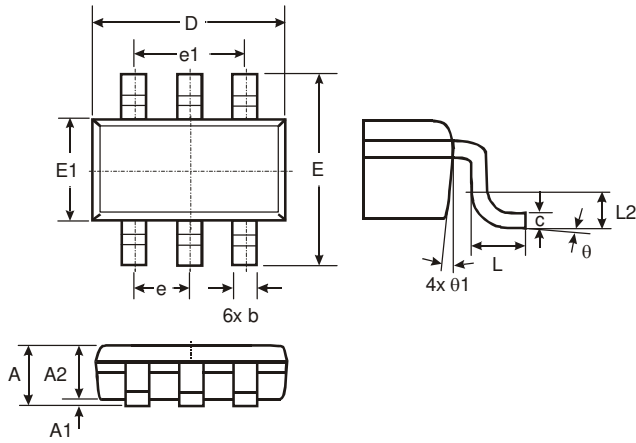


Figure 11 Gate Charge Characteristics

Package Outline Dimensions

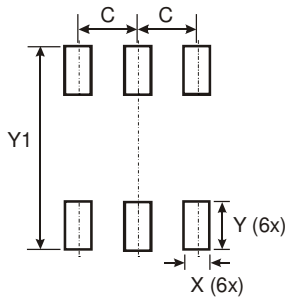
TSOT26



TSOT26			
Dim	Min	Max	Typ
A	–	1.00	–
A1	0.01	0.10	–
A2	0.84	0.90	–
D	–	–	2.90
E	–	–	2.80
E1	–	–	1.60
b	0.30	0.45	–
c	0.12	0.20	–
e	–	–	0.95
e1	–	–	1.90
L	0.30	0.50	–
L2	–	–	0.25
theta	0°	8°	4°
theta1	4°	12°	–
All Dimensions in mm			

Suggested Pad Layout

TSOT26



Dimensions	Value (in mm)
C	0.950
X	0.700
Y	1.000
Y1	3.199

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