

High Speed 12-Bit Monolithic D/A Converters

AD566A

FEATURES

Single Chip Construction

Very High Speed Settling to 1/2 LSB

AD565A: 250 ns max AD566A: 350 ns max

Full-Scale Switching Time: 30 ns

Guaranteed for Operation with $\pm 12 \text{ V}$ (565A) Supplies,

with -12 V Supply (AD566A)

Linearity Guaranteed Overtemperature

1/2 LSB max (K, T Grades)

Monotonicity Guaranteed Overtemperature

Low Power: AD566A = 180 mW max;

AD565A = 225 mW max

Use with On-Board High Stability Reference (AD565A)

or with External Reference (AD566A)

Low Cost

MIL-STD-883-Compliant Versions Available

PRODUCT DESCRIPTION

The AD565A and AD566A are fast 12-bit digital-to-analog converters that incorporate the latest advances in analog circuit design to achieve high speeds at low cost.

The AD565A and AD566A use 12 precision, high speed bipolar current-steering switches, a control amplifier, and a laser-trimmed thin-film resistor network to produce a very fast, high accuracy analog output current. The AD565A also includes a buried Zener reference that features low noise, long-term stability, and temperature drift characteristics comparable to the best discrete reference diodes.

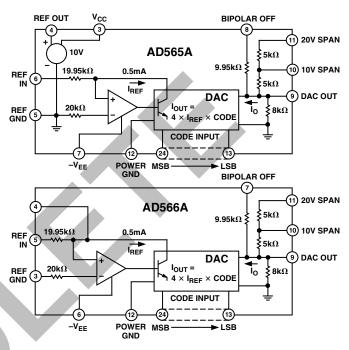
The combination of performance and flexibility in the AD565A and AD566A has resulted from major innovations in circuit design, an important new high speed bipolar process, and continuing advances in laser-wafer-trimming techniques (LWT). The AD565A and AD566A have a 10%–90% full-scale transition time less than 35 ns and settle to within $\pm 1/2$ LSB in 250 ns max (350 ns for AD566A). Both are laser-trimmed at the wafer level to $\pm 1/8$ LSB typical linearity and are specified to $\pm 1/4$ LSB max error (K and T grades) at $\pm 25^{\circ}$ C. High speed and accuracy make the AD565A and AD566A the ideal choice for high speed display drivers as well as for fast analog-to-digital converters.

The laser trimming process that provides the excellent linearity is also used to trim both the absolute value and the temperature coefficient of the reference of the AD565A, resulting in a typical full-scale gain TC of 10 ppm/°C. When tighter TC performance is required or when a system reference is available, the AD566A may be used with an external reference.

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FUNCTIONAL BLOCK DIAGRAMS



AD565A and AD566A are available in four performance grades. The J and K grades are specified for use over the 0°C to +70°C temperature range while the S and T grades are specified for the -55°C to +125°C range. The D grades are all packaged in a 24-lead, hermetically sealed, ceramic, dual-in-line package. The JR grade is packaged in a 28-lead plastic SOIC.

PRODUCT HIGHLIGHTS

- 1. The wide output compliance range of the AD565A and AD566A are ideally suited for fast, low noise, accurate voltage output configurations without an output amplifier.
- 2. The devices incorporate a newly developed, fully differential, nonsaturating precision current switching cell structure that combines the dc accuracy and stability first developed in the AD562/AD563 with very fast switching times and an optimally damped settling characteristic.
- 3. The devices also contain SiCr thin-film application resistors that can be used with an external op amp to provide a precision voltage output or as input resistors for a successive-approximation A/D converter. The resistors are matched to the internal ladder network to guarantee a low gain temperature coefficient and are laser-trimmed for minimum full-scale and bipolar offset errors.
- 4. The AD565A and AD566A are available in versions compliant with MIL-STD-883. Refer to the Analog Devices *Military Products Databook* or current /883B data sheet for detailed specifications.

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$\label{eq:AD565A-SPECIFICATIONS} \textbf{AD565A-SPECIFICATIONS} \ \, (\textbf{T}_{A} = 25^{\circ}\text{C}, \, \textbf{V}_{CC} = 15 \, \text{V}, \, \textbf{V}_{EE} = 15 \, \text{V}, \, \text{unless otherwise noted.})$

TTL or 5 V CMOS Input Voltage Bit ON Logic "1" Bit ON Logic "1" 0.8 0.8 V	Parameter	Min	AD565AJ Typ	Max	Min	AD565AK Typ	Max	Unit
Input Voltage Bit ON Logic *1" 2.0 5.5 2.0 5.5 V	DATA INPUTS ¹ (Pins 13 to 24)							
DEFORMENTIAL NONLINEARITY 1.20 5.5 2.0 5.5 V								
Dogic Current (Each Bit) Bit ON Logic "1" 35 100 120 300 µA µA Bit ON Logic "1" 35 100 35 100 µA µA Bit OFF Logic "0" 35 100 µA µA µA µA µA µA µA	Bit ON Logic "1"	2.0		5.5	2.0		5.5	V
Bit ON Logic "1" 120 300 120 300 120 300 120 300 120 300 120 300 120 300 120 300 120 300 120 300 120 300 120 300 120 300 120 300 120 300 120 300 120 300 120 300 120 300 120 120 300 12				0.8			0.8	V
RESOLUTION 12 12 13 100 14			120	300		120	300	пА
OUTPUT Current Curr								
Current Unipolar (All Bits On or Off) Bipolar (All Bits On or Off) ±0.8	RESOLUTION			12			12	Bits
Unipolar (All Bits On) Elos 2-2.0 2-2.4 2-1.6 2-2.0 2-2.4 2-1.8 2-0.8 2-1.0 2-1.2 2-0.8 2-0.8 2-1.0 2-1.2 2-0.8 2-1.0 2-1.2 2-0.8 2-1.0 2-1.2 2-0.8 2-1.0 2-1.2 2-0.8 2-1.0 2-1.2 2-0.8 2-1.0 2-								
Bijolar (All Bits On or Off) \$\phi 0.5 \phi 1.0 \phi 1.2 \phi 0.5 \pm 1.0 \phi 1.2 \pm 1.0 \pm 1.2 \pm 1.2 \pm 1.0 \pm 1.		_1.6	2.0	_2 1	_1 6	2.0	_2 4	m Δ
Offset Unipolar Bipolar (Figure 3, R2 = 50 Ω Fixed) 0.01 0.05 0.15 0.05 0.1 0.05 0.15 0.05 0.15 0.05 0.15 0.05 0.15 0.15 0.05 0.15		1						
Unipolar Signate Si		6	8	10	6	8	10	kΩ
Bipolar (Figure 3, R2 = 50 Ω Fixed) Capacitance Cap			0.01	0.05		0.01	0.05	% of F.S. Range
Compilance Voltage Time to Time t								
Time to Times			25			25		pF
ACCURACY (Error Relative to Full Scale) 25°C 1.14 ±112 (0.006) (0.012) (0.003) (0.0084) (0.0084) 1.12 ±1.12 ±3.14 ±112 ±1.14 ±112 ±1.14 ±112 ±1.14 ±1.14 ±1.12 ±1.14		-1.5		+10	-1.5		+10	V
TMIN to TMAX								
TMIN to TMAX	Full Scale) 25°C							
DIFFERENTIAL NONLINEARITY 25% 21/4 21/4 21/4 21/2 23/4 21/4	Typy to Typy							
25°C	1 MIN to 1 MAX							
Temperature Coefficients With Internal Reference Unipolar Zero 1 2 1 2 ppm/°C ppm/°								
TEMPERATURE COEFICIENTS With Internal Reference Unipolar Zero Bipolar Zero Gain (Full Scale) Jipolar Zero Bipolar Zero Bi		MONOT			MONOT			LSB
With Internal Reference		MONOI	UNICITY GU	AKANTEED	MONOI	UNICITY GUA	KANTEED	
Bipolar Zero Sample Sam								
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$						1		
Differential Nonlinearity 2								ppm/°C
All Bits ON-to-OFF or OFF-to-ON				30			20	ppm/°C
10% to 90% Delay plus Rise Time 15 30 30 50 30 50 ns			250	400		250	400	ns
90% to 10% Delay plus Fall Time 30 50 30 50 50 TEMPERATURE RANGE Operating Storage	FULL-SCALE TRANSITION							
TEMPERATURE RANGE Operating $0 - 65$ $0 + 70 - 65$ $0 - 70 - 70$ $0 - 70$ 0								
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$			30	30		30	30	118
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$		0		+70	0		+70	°C
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$		-65		+150	-65		+150	°C
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	POWER REQUIREMENTS			,		2	_	
POWER SUPPLY GAIN SENSITIVITY2 $V_{CC} = +11.4 \text{ to } +16.5 \text{ V dc}$ $V_{EE} = -10.5 \text{ to } +10.5 \text{ V dc}$ $V_{EE} = -10.5 \text{ to } +10.5 \text{ V dc}$ $V_{EE} = -10.5 \text{ to } +10.5 \text{ V dc}$ $V_{EE} = -10.5 \text{ to } +10.5 \text{ V dc}$ $V_{EE} = -10.5 \text{ to } +10.5 \text{ V dc}$ $V_{EE} = -10.5 \text{ to } +10.5 \text{ V dc}$ $V_{EE} = -10.5 \text{ to } +10.5 \text{ V dc}$ $V_{EE} = -10.5 \text{ to } +10.5 \text{ V dc}$ $V_{EE} = -10.5 \text{ to } +10.5 \text{ V dc}$ $V_{EE} = -10.5 \text{ to } +10.5 \text{ V dc}$ $V_{EE} = -10.5 \text{ to } +10.5 \text{ to } +10.5 \text{ V dc}$ $V_{EE} = -10.5 \text{ to } +10.5 \text$								
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$			12					
PROGRAMMABLE OUTPUT RANGES (See Figures 2, 3, 4) 0 to +5 -2.5 to +2.5 0 to +10 -5 to +5 -10 to +10 EXTERNAL ADJUSTMENTS Gain Error with Fixed 50 Ω Resistor for R2 (Figure 2) Bipolar Zero Error with Fixed 50 Ω Resistor for R1 (Figure 3) Gain Adjustment Range (Figure 2) Bipolar Zero Adjustment Range EXPERENCE INPUT Input Impedance 15 20 25 15 20 25 10.00 10.00 10.10	V_{CC} = +11.4 to +16.5 V dc							
$ (See \ Figures \ 2, \ 3, \ 4) \\ (See \ Figures \ 2, \ 3, \ 4) \\ (See \ Figures \ 2, \ 3, \ 4) \\ (See \ Figures \ 2, \ 3, \ 4) \\ (See \ Figures \ 2, \ 3, \ 4) \\ (See \ Figures \ 2, \ 3, \ 4) \\ (See \ Figures \ 2, \ 3, \ 4) \\ (See \ Figures \ 2, \ 3, \ 4) \\ (See \ Figures \ 2, \ 3, \ 4) \\ (See \ Figures \ 2, \ 3, \ 4) \\ (See \ Figures \ 2, \ 5, \ 4.0) \\ (See \ Figures \ 2, \ 5, \ 4.0) \\ (See \ Figures \ 2, \ 5, \ 4.0) \\ (See \ Figures \ 2, \ 4.0) \\ (See \ Figures \ 2, \ 5, \ 4.0) \\ (See \ Figures \ 2, \ 4.0) \\ (See \ Figures \ 4.0) \\ (See $		1	15	25		15	25	ppm of F.S./%
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$			0 to +5			0 to +5		V
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	(See Figures 2, 3, 4)			5			5	
		1						
EXTERNAL ADJUSTMENTS Gain Error with Fixed 50Ω Resistor for R2 (Figure 2) Bipolar Zero Error with Fixed 50Ω Resistor for R1 (Figure 3) Gain Adjustment Range (Figure 2) Bipolar Zero Adjustment Range ± 0.05 ± 0.15 ± 0.05 ± 0.15 ± 0.05 ± 0.10 % of F.S. Range % of F.S. R								
Gain Error with Fixed 50 Ω Resistor for R2 (Figure 2) Bipolar Zero Error with Fixed 50 Ω Resistor for R1 (Figure 3) Gain Adjustment Range (Figure 2) Bipolar Zero Adjustment Range EFFERENCE INPUT Input Impedance 15 20 25 10.10 25 40.11 20.25 40.05 40.11 20.05 40.11 20.05 40.15 20.05 40.15 40.05 40.11 20.05 40.15 20.05 40.10 20.05 40.10 20.05 40.10 20.05 40.10 20.05 40.10 20.05 40.10 20.05 20.05 20.05 40.10 20.05 20.05 20.05 40.10 20.05 40.10 20.05 20.05 20.05 40.10 20.05 20.	EXTERNAL ADJUSTMENTS		10.10 110			10 10 110		,
Bipolar Zero Error with Fixed 50 Ω Resistor for R1 (Figure 3) ± 0.05 ± 0.15 ± 0.05 ± 0.15 ± 0.05 ± 0.16 ± 0.05 ± 0.17 % of F.S. Range Gain Adjustment Range (Figure 2) ± 0.15 ± 0.15 ± 0.15 ± 0.15 % of F.S. Range	Gain Error with Fixed 50 Ω							
50Ω Resistor for R1 (Figure 3) ± 0.05 ± 0.15 ± 0.05 ± 0.15 ± 0.05 ± 0.1 % of F.S. Range Gain Adjustment Range (Figure 2) ± 0.25 ± 0.15 ± 0.15 ± 0.25 ± 0.15 ± 0.15 % of F.S. Range % of F.S. Rang			± 0.1	±0.25		± 0.1	±0.25	% of F.S. Range
Gain Adjustment Range (Figure 2) ± 0.25 ± 0.25 ± 0.15 % of F.S. Range REFERENCE INPUT Input Impedance 15 20 25 15 20 25 ± 0.15 REFERENCE OUTPUT Voltage Current (Available for External Loads) ³ 9.90 10.00 10.10 9.90 10.00 10.10 V List 2.5 2.5 mA			±0.05	±0.15		±0.05	± 0.1	% of F.S. Range
REFERENCE INPUT Input Impedance 15 20 25 15 20 25 $kΩ$ REFERENCE OUTPUT Voltage Current (Available for External Loads) ³ 1.5 2.5 10.10 9.90 10.00 10.10 V mA	Gain Adjustment Range (Figure 2)							% of F.S. Range
Input Impedance 15 20 25 15 20 25 kΩ REFERENCE OUTPUT Voltage 9.90 10.00 10.10 9.90 10.00 10.10 V Current (Available for External Loads) ³ 1.5 2.5 1.5 2.5 mA	, ,	±0.15			±0.15			% of F.S. Range
REFERENCE OUTPUT 9.90 10.00 10.10 9.90 10.00 10.10 V Current (Available for External Loads)³ 1.5 2.5 1.5 2.5 mA		15	20	25	15	20	25	kO
Voltage Current (Available for External Loads) ³ 9.90 1.5 10.00 2.5 10.10 1.5 9.90 2.5 10.00 1.5 10.10 2.5 V mA		13	20	<u> </u>	1.7	20		Na E
	Voltage	1		10.10			10.10	
POWER DISSIPATION 225 345 mW		1.5			1.5			
	POWER DISSIPATION NOTES		225	345		225	345	mW

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NOTES

1 The digital inputs are guaranteed but not tested over the operating temperature range.

2 The power supply gain sensitivity is tested in reference to a V_{CC} , V_{EE} of \pm 15 V dc.

3 For operation at elevated temperatures, the reference cannot supply current for external loads. It, therefore, should be buffered if additional loads are to be supplied. Specifications subject to change without notice.

Parameter	Min	AD565AS Typ	Max	Min	AD565AT Typ	Max	Unit
DATA INPUTS ¹ (Pins 13 to 24) TTL or 5 V CMOS							
Input Voltage							**
Bit ON Logic "1" Bit OFF Logic "0"	2.0		5.5 0.8	2.0		5.5 0.8	V V
Logic Current (Each Bit)							
Bit ON Logic "1" Bit OFF Logic "0"		120 35	300 100		120 35	300 100	μA μA
RESOLUTION			12			12	Bits
OUTPUT							
Current Unipolar (All Bits On)	-1.6	-2.0	-2.4	-1.6	-2.0	-2.4	mA
Bipolar (All Bits On or Off)	±0.8	± 1.0	±1.2	±0.8	±1.0	±1.2	mA
Resistance (Exclusive of Span Resistors) Offset	6	8	10	6	8	10	kΩ
Unipolar		0.01	0.05		0.01	0.05	% of F.S. Range
Bipolar (Figure 3, R2 = 50 Ω Fixed)		0.05 25	0.15		0.05 25	0.1	% of F.S. Range
Capacitance Compliance Voltage		23			25		pF
T_{MIN} to T_{MAX}	-1.5		+10	-1.5		+10	V
ACCURACY (Error Relative to Full Scale) 25°C		±1/4	±1/2		±1/8	±0.35	LSB
I'uli Scale) 25 G		(0.006)	(0.012)		(0.003)	(0.0084)	% of F.S. Range
$\mathrm{T_{MIN}}$ to $\mathrm{T_{MAX}}$		$\pm 1/2$ (0.012)	±3/4 (0.018)		$\pm 1/4$ (0.006)	±1/2 (0.012)	LSB % of F.S. Range
DIFFERENTIAL NONLINEARITY		(0.012)	(0.018)		(0.000)	(0.012)	70 Of F.S. Kange
25°C		±1/2	±3/4		±1/4	±1/2	LSB
T _{MIN} to T _{MAX} TEMPERATURE COEFFICIENTS	MONO	TONICITY G	UARANTEED	MONO	FONICITY GU	ARANTEED	
With Internal Reference							
Unipolar Zero		1	2		1	2	ppm/°C
Bipolar Zero Gain (Full Scale)		5 15	10 30		5 10	10 15	ppm/°C ppm/°C
Differential Nonlinearity		2			2		ppm/°C
SETTLING TIME TO 1/2 LSB All Bits ON-to-OFF or OFF-to-ON		250	400		250	400	ns
FULL-SCALE TRANSITION		15	20		1.5	20	
10% to 90% Delay plus Rise Time 90% to 10% Delay plus Fall Time		15 30	30 50		15 30	30 50	ns ns
TEMPERATURE RANGE							
Operating Storage	-55 -65		+125 +150	-55 -65		+125 +150	°C °C
POWER REQUIREMENTS	-03		+150	-03		T130	C
V _{CC} , +11.4 to +16.5 V dc		3	5		3	5	mA
V _{EE} , -11.4 to -16.5 V dc		-12	-18		-12	-18	mA
POWER SUPPLY GAIN SENSITIVITY ² $V_{CC} = +11.4 \text{ to } +16.5 \text{ V dc}$		3	10		3	10	ppm of F.S./%
$V_{EE} = -11.4 \text{ to } -16.5 \text{ V dc}$		15	25		15	25	ppm of F.S./%
PROGRAMMABLE OUTPUT RANGES		0			0		**
(See Figures 2, 3, 4)		0 to +5 -2.5 to +2	.5		0 to +5 -2.5 to +2.5	5	V V
		0 to +10			0 to +10		V
		−5 to +5 −10 to +10)		−5 to +5 −10 to +10		V V
EXTERNAL ADJUSTMENTS			<u> </u>				·
Gain Error with Fixed 50 Ω		101	. 0. 2.5		101		0/ CE C P
Resistor for R2 (Figure 2) Bipolar Zero Error with Fixed		±0.1	±0.25		± 0.1	±0.25	% of F.S. Range
50Ω Resistor for R1 (Figure 3)	10.05	± 0.05	± 0.15	10.05	± 0.05	±0.1	% of F.S. Range
Gain Adjustment Range (Figure 2) Bipolar Zero Adjustment Range	±0.25 ±0.15			±0.25 ±0.15			% of F.S. Range % of F.S. Range
REFERENCE INPUT							
Input Impedance	15	20	25	15	20	25	kΩ
REFERENCE OUTPUT Voltage	9.90	10.00	10.10	9.90	10.00	10.10	V
Current (Available for External Loads) ³	1.5	2.5	10.10	1.5	2.5	10.10	mA
POWER DISSIPATION		225	345		225	345	mW

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in **boldface** are tested on all production units.

Specification subject to change without notice.

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$\label{eq:AD566A-SPECIFICATIONS} \textbf{(} \textbf{T}_{A} = 25^{\circ} \textbf{C} \textbf{, } \textbf{V}_{EE} = -15 \textbf{ V} \textbf{, unless otherwise noted)}$

	Τ	ADSCCAL			ADSCCAR		
Parameter	Min	AD566AJ Typ	Max	Min	AD566AK Typ	Max	Unit
DATA INPUTS ¹ (Pins 13 to 24)							
TTL or 5 V CMOS Input Voltage							
Bit ON Logic "1"	2.0		5.5	2.0		5.5	V
Bit OFF Logic "0"	0		0.8	0		0.8	V
Logic Current (Each Bit) Bit ON Logic "1"		120	300		120	300	μΑ
Bit OFF Logic "0"		35	100		35	100	μA
RESOLUTION			12			12	Bits
OUTPUT Current							
Unipolar (All Bits On)	-1.6	-2.0	-2.4	-1.6	-2.0	-2.4	mA
Bipolar (All Bits On or Off) Resistance (Exclusive of Span Resistors)	±0.8	±1.0 8	±1.2	±0.8	±1.0 8	±1.2	mA kΩ
Offset							
Unipolar (Adjustable to Zero per Figure 3) Bipolar (Figure 4, R1 and R2 = 50 Ω Fixed)		0.01 0.05	0.05 0.15		0.01 0.05	0.05	% of F.S. Range % of F.S. Range
Capacitance		25	0.13		25	VII	pF
Compliance Voltage T_{MIN} to T_{MAX}	-1.5		+10	-1.5		+10	v
ACCURACY (Error Relative to	1.5		. 10	1.5		110	,
Full Scale) 25°C		±1/4	±1/2		±1/8	±0.35	LSB
T_{MIN} to T_{MAX}		(0.006) $\pm 1/2$	(0.012) $\pm 3/4$		(0.003) $\pm 1/4$	(0.0084) $\pm 1/2$	% of F.S. Range LSB
- MIN MAX		(0.012)	(0.018)		(0.006)	(0.012)	% of F.S. Range
DIFFERENTIAL NONLINEARITY		1.1/0	. 244		1.1/4	. 1/2	100
25°C T_{MIN} to T_{MAX}	MONO	±1/2 PTONICITY G	±3/4 UARANTEED	молото	±1/4 NICITY GUA	±1/2 RANTEED	LSB
TEMPERATURE COEFFICIENTS							
Unipolar Zero		1 5	2 10		1 5	2	ppm/°C
Bipolar Zero Gain (Full Scale)		7	10		3	10 5	ppm/°C ppm/°C
Differential Nonlinearity		2			2		ppm/°C
SETTLING TIME TO 1/2 LSB All Bits ON-to-OFF or OFF-to-ON		250	350		250	350	ns
FULL-SCALE TRANSITION 10% to 90% Delay plus Rise Time		15	30		15	30	ns
90% to 10% Delay plus Fall Time		30	50		30	50	ns
POWER REQUIREMENTS							
V _{EE} , -11.4 to -16.5 V dc POWER SUPPLY GAIN SENSITIVITY ²		-12	-18		-12	-18	mA
$V_{EE} = -11.4 \text{ to } -16.5 \text{ V dc}$		15	25		15	25	ppm of F.S./%
PROGRAMMABLE OUTPUT RANGES							
(see Figures 3, 4, 5)		0 to +5 -2.5 to +2	5		0 to +5 -2.5 to +2	5	V V
		0 to +10	.5		0 to +10		V
		-5 to +5 -10 to +10)		−5 to +5 −10 to +10)	V V
EXTERNAL ADJUSTMENTS		-10 to 110	,		-10 to 110	,	V
Gain Error with Fixed 50 Ω							
Resistor for R2 (Figure 3) Bipolar Zero Error with Fixed		±0.1	± 0.25		±0.1	± 0.25	% of F.S. Range
50 Ω Resistor for R1 (Figure 4)		± 0.05	± 0.15		±0.05	± 0.1	% of F.S. Range
Gain Adjustment Range (Figure 3) Bipolar Zero Adjustment Range	±0.25 ±0.15			±0.25 ±0.15			% of F.S. Range % of F.S. Range
REFERENCE INPUT							70 0111011tanige
Input Impedance	15	20	25	15	20	25	kΩ
POWER DISSIPATION	-	180	300		180	300	mW
MULTIPLYING MODE PERFORMANCE (All Models) Quadrants		Two (2): I	Bipolar Operatio	 n at Digital In	nut Only		
Reference Voltage		1 V to 10	V, Unipolar	J			
Accuracy Reference Feedthrough (Unipolar Mode,		10 Bits (±	0.05% of Reduc	ed F.S.) for 1	V dc Reference	Voltage	
All Bits OFF, and 1 V to 10 V [p-p], Sine Wave							
Frequency for 1/2 LSB [p-p] Feedthrough) Output Slew Rate 10%–90%		40 5					kHz typ mA/µs
90%-10%		1					mA/μs mA/μs
Output Settling Time (All Bits ON and a 0 V-10 V Step Change in Reference Voltage)		1 5 110 +0 0	01% F S				
CONTROL AMPLIFIER	+	1.5 μs to 0	.0170 Г.З.				
Full Power Bandwidth		300					kHz
Small-Signal Closed-Loop Bandwidth		1.8					MHz

Specifications subject to change without notice.

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NOTES 1 The digital input levels are guaranteed but not tested over the temperature range. 2 The power supply gain sensitivity is tested in reference to a V_{EE} of -1.5 V dc.

Parameter	Min	AD566AS Typ	Max	Min	AD566AT Typ	Max	Unit
DATA INPUTS¹ (Pins 13 to 24)							
TTL or 5 V CMOS Input Voltage							
Bit ON Logic "1"	2.0		5.5	2.0		5.5	V
Bit OFF Logic "0" Logic Current (Each Bit)	0		0.8	0		0.8	V
Bit ON Logic "1"		120	300		+120	300	μΑ
Bit OFF Logic "0" RESOLUTION		35	100		+35	100	μA Bits
OUTPUT			12			12	Dits
Current							
Unipolar (All Bits On) Bipolar (All Bits On or Off)	-1.6 ±0.8	-2.0 ± 1.0	-2.4 ±1.2	-1.6 ±0.8	-2.0 ±1.0	-2.4 ±1.2	mA mA
Resistance (Exclusive of Span Resistors)	6	8	10	6	8	10	kΩ
Offset Unipolar (Adjustable to Zero per Figure 3)		0.01	0.05		0.01	0.05	% of F.S. Range
Bipolar (Figure 4, R1 and R2 = 50Ω Fixed)		0.05	0.15		0.05	0.1	% of F.S. Range
Capacitance Compliance Voltage		25			25		pF
T _{MIN} to T _{MAX}	-1.5		+10	-1.5		+10	V
ACCURACY (Error Relative to		1.1/4	. 1/2		1.1/0	10.05	LOD
Full Scale) 25°C		$\pm 1/4$ (0.006)	$\pm 1/2$ (0.012)		±1/8 (0.003)	±0.35 (0.0084)	LSB % of F.S. Range
T_{MIN} to T_{MAX}		±1/2	±3/4		±1/4	±1/2	LSB
DIEGEDENTHAL MONHING ABITM		(0.012)	(0.018)		(0.006)	(0.012)	% of F.S. Range
DIFFERENTIAL NONLINEARITY 25°C		±1/2	±3/4		±1/4	±1/2	LSB
T_{MIN} to T_{MAX}	MONOT	ONICITY G	JARANTEED	MONOT	ONICITY GUA	ARANTEED	
TEMPERATURE COEFFICIENTS		1	,		1	2	/0C
Unipolar Zero Bipolar Zero		1 5	2 10		1 5	2 10	ppm/°C ppm/°C
Gain (Full Scale)		7 2	10		3 2	5	ppm/°C
Differential Nonlinearity SETTLING TIME TO 1/2 LSB		2					ppm/°C
All Bits ON-to-OFF or OFF-to-ON		250	350		250	350	ns
FULL-SCALE TRANSITION							
10% to 90% Delay plus Rise Time 90% to 10% Delay plus Fall Time		15 30	30 50		15 30	30 50	ns ns
POWER REQUIREMENTS		30	7		30		
V _{EE} , -11.4 to -16.5 V dc		-12	-18		-12	-18	mA
POWER SUPPLY GAIN SENSITIVITY ² V _{EE} = -11.4 to -16.5 V dc		15	25		15	25	ppm of F.S./%
PROGRAMMABLE OUTPUT RANGES		15	23		13	23	ppiii 01 1 .3./ /0
(see Figures 3, 4, 5)		0 to +5			0 to +5		V
		-2.5 to + 0 to +10	2.5		-2.5 to +2 0 to +10	.5	V
		−5 to +5			−5 to +5		V
EXPERIENCE A PARTICULAR PROPERTY.		-10 to +1	0		-10 to +10)	V
EXTERNAL ADJUSTMENTS Gain Error with Fixed 50 Ω							
Resistor for R2 (Figure 3)		± 0.1	± 0.25		± 0.1	± 0.25	% of F.S. Range
Bipolar Zero Error with Fixed 50 Ω Resistor for R1 (Figure 4)		±0.05	±0.15		±0.05	±0.1	% of F.S. Range
Gain Adjustment Range (Figure 3)	±0.25			±0.25			% of F.S. Range
Bipolar Zero Adjustment Range REFERENCE INPUT	±0.15			±0.15			% of F.S. Range
Input Impedance	15	20	25	15	20	25	kΩ
POWER DISSIPATION		180	300		180	300	mW
MULTIPLYING MODE PERFORMANCE (All Models)							
Quadrants Reference Voltage			Bipolar Operation V, Unipolar	n at Digital	Input Only		
Accuracy			0.05% of Reduc	ed F.S.) for	1 V dc Referenc	e Voltage	
Reference Feedthrough (Unipolar Mode, All Bits OFF, and 1 V to 10 V [p-p], Sine Wave							
Frequency for 1/2 LSB [p-p] Feedthrough)		40					kHz typ
Output Slew Rate 10%–90% 90%–10%		5 1					mA/μs mA/μs
Output Settling Time (All Bits ON and a 0 V-10 V							11111/405
Step Change in Reference Voltage)		1.5 μs to	0.01% F.S.				
CONTROL AMPLIFIER Full Power Bandwidth		300					kHz
Small-Signal Closed-Loop Bandwidth		1.8					MHz

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in **boldface** are tested on all production units.

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Specification subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

V_{CC} to Power Ground 0 V to +18 V
V_{EE} to Power Ground (AD565A) 0 V to –18 V
Voltage on DAC Output (Pin 9)3 V to +12 V
Digital Inputs (Pins 13 to 24) to
Power Ground1.0 V to +7.0 V
REF IN to Reference Ground $\pm 12 \text{ V}$
Bipolar Offset to Reference Ground ±12 V
10 V Span R to Reference Ground ±12 V
20 V Span R to Reference Ground ±24 V
REF OUT (AD565A) Indefinite Short to Power Ground
Momentary Short to V _{CC}
Power Dissipation

GROUNDING RULES

The AD565A and AD566A use separate reference and power grounds to allow optimum connections for low noise and high speed performance. These grounds should be tied together at one point, usually the device power ground. The separate ground returns minimize current flow in low level signal paths. In this way, logic return currents are not summed into the same return path with analog signals.

AD565A ORDERING GUIDE

Model ¹	Max Gain T.C. (ppm of F.S./°C)	Temperature Range	Linearity Error Max @ +25°C	Package Options ²
AD565AJD	50	0°C to +70°C	±1/2 LSB	Ceramic (D-24)
AD565AJR	50	0°C to +70°C	±1/2 LSB	SOIC (RW-28)
AD565AKD	20	0°C to +70°C	±1/4 LSB	Ceramic (D-24)
AD565ASD	30	−55°C to +125°C	±1/2 LSB	Ceramic (D-24)
AD565ATD	15	−55°C to +125°C	±1/4 LSB	Ceramic (D-24)

NOTES

AD566A ORDERING GUIDE

Model ¹	Max Gain T.C. (ppm of F.S./°C)	Linearity Temperature Range	Error Max @ +25°C	Package Option ²	
AD566AJD	10	0°C to +70°C	±1/2 LSB	Ceramic (D-24	
AD566AKD	3	0°C to +70°C	±1/4 LSB	Ceramic (D-24)	
AD566ASD	10	−55°C to +125°C	±1/2 LSB	Ceramic (D-24)	
AD566ATD	3	−55°C to +125°C	±1/4 LSB	Ceramic (D-24)	

NOTES

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CAUTION _

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD565A/AD566A features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

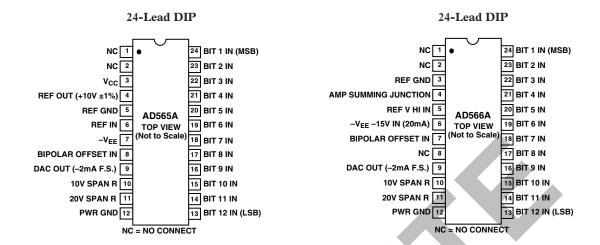


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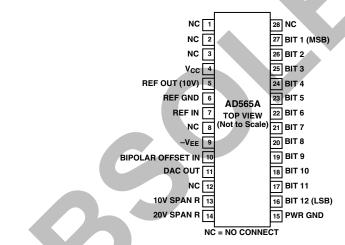
¹For details on grade and package offerings screened in accordance with MIL-STD-883, refer to the Analog Devices *Military Products Databook* or current/883B data sheet. ²D = Ceramic DIP, R = SOIC.

¹For details on grade and package offerings screened in accordance with MIL-STD-883, refer to the Analog Devices *Military Products Databook* or current/883B data sheet. ²D = Ceramic DIP.

PIN CONFIGURATIONS



28-Lead SOIC



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CONNECTING THE AD565A FOR BUFFERED VOLTAGE OUTPUT

The standard current-to-voltage conversion connections using an operational amplifier are shown in Figures 1, 2, and 3 with the preferred trimming techniques. If a low offset operational amplifier (OP77, AD741L, OP07) is used, excellent performance can be obtained in many situations without trimming (an op amp with less than 0.5 mV max offset voltage should be used to keep offset errors below 1/2 LSB). If a 50 Ω fixed resistor is substituted for the 100 Ω trimmer, unipolar zero is typically within $\pm 1/2$ LSB (plus op amp offset) and full-scale accuracy is within 0.1% (0.25% max). Substituting a 50 Ω resistor for the 100 Ω bipolar offset trimmer gives a bipolar zero error typically within ± 2 LSB (0.05%).

The AD509 is recommended for buffered voltage-output applications that require a settling time to $\pm 1/2$ LSB of 1 μs . The feedback capacitor is shown with the optimum value for each application; this capacitor is required to compensate for the 25 pF DAC output capacitance.

FIGURE 1. UNIPOLAR CONFIGURATION

This configuration provides a unipolar 0 V to 10 V output range. In this mode, the bipolar terminal, Pin 8, should be grounded if not used for trimming.

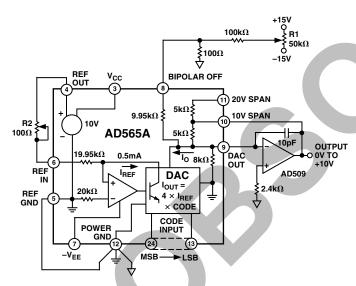


Figure 1. 0 V to 10 V Unipolar Voltage Output

STEP I . . . ZERO ADJUST

Turn all bits OFF and adjust zero trimmer R1 until the output reads 0.000 V (1 LSB = 2.44 mV). In most cases, this trim is not needed, but Pin 8 should then be connected to Pin 12.

STEP II . . . GAIN ADJUST

Turn all bits ON and adjust $100\,\Omega$ gain trimmer R2 until the output is 9.9976 V. (Full scale is adjusted to 1 LSB less than nominal full scale of 10.000 V.) If a 10.2375 V full scale is desired (exactly 2.5 mV/bit), insert a $120\,\Omega$ resistor in series with the gain resistor at Pin 10 to the op amp output.

FIGURE 2. BIPOLAR CONFIGURATION

This configuration provides a bipolar output voltage from -5.000 V to +4.9976 V, with positive full scale occurring with all bits ON (all 1s).

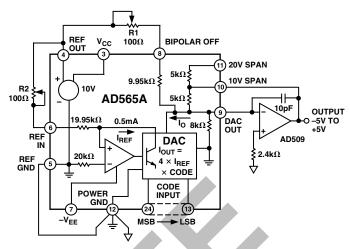


Figure 2. ±5 V Bipolar Voltage Output

STEP I . . . OFFSET ADJUST

Turn OFF all bits. Adjust $100\,\Omega$ trimmer R1 to give –5.000 V output.

STEP II . . . GAIN ADJUST

Turn ON all bits. Adjust 100 Ω gain trimmer R2 to give a reading of +4.9976 V.

Please note that it is not necessary to trim the op amp to obtain full accuracy at room temperature. In most bipolar situations, an op amp trim is unnecessary unless the untrimmed offset drift of the op amp is excessive.

FIGURE 3. OTHER VOLTAGE RANGES

The AD565A can also be easily configured for a unipolar 0 V to +5 V range or ± 2.5 V and ± 10 V bipolar ranges by using the additional 5 k Ω application resistor provided at the 20 V span R terminal, Pin 11. For a 5 V span (0 V to +5 V, or ± 2.5 V), the two 5 k Ω resistors are used in parallel by shorting Pin 11 to Pin 9 and connecting Pin 10 to the op amp output and the bipolar offset either to ground for unipolar or to REF OUT for the bipolar offset either to ground for unipolar or to REF OUT for the bipolar range. For the ± 10 V range (20 V span) use the 5 k Ω resistors in series by connecting only Pin 11 to the op amp output and the bipolar offset connected as shown. The ± 10 V option is shown in Figure 3.

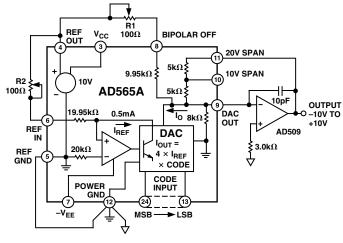


Figure 3. ±10 V Voltage Output

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CONNECTING THE AD566A FOR BUFFERED VOLTAGE OUTPUT

The standard current-to-voltage conversion connections using an operational amplifier are shown in Figures 4, 5, and 6 with the preferred trimming techniques. If a low offset operational amplifier (OP77, AD741L, OP07) is used, excellent performance can be obtained in many situations without trimming (an op amp with less than 0.5 mV max offset voltage should be used to keep offset errors below 1/2 LSB). If a 50 Ω fixed resistor is substituted for the 100 Ω trimmer, unipolar zero typically is within $\pm 1/2$ LSB (plus op amp offset), and full-scale accuracy is within 0.1% (0.25% max). Substituting a 50 Ω resistor for the 100 Ω bipolar offset trimmer gives a bipolar zero error typically within ± 2 LSB (0.05%).

The AD509 is recommended for buffered voltage-output applications that require a settling time to $\pm 1/2$ LSB of 1 μ s. The feedback capacitor is shown with the optimum value for each application; this capacitor is required to compensate for the 25 pF DAC output capacitance.

FIGURE 4. UNIPOLAR CONFIGURATION

This configuration provides a unipolar 0 V to 10 V output range. In this mode, the bipolar terminal, Pin 7, should be grounded if not used for trimming.

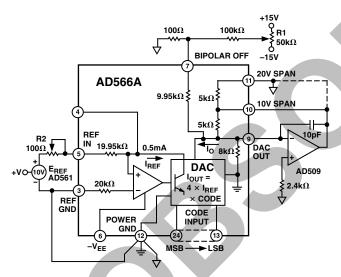


Figure 4. 0 V to 10 V Unipolar Voltage Output

STEP I . . . ZERO ADJUST

Turn all bits OFF and adjust zero trimmer, R1, until the output reads 0.000 V (1 LSB = 2.44 mV). In most cases, this trim is not needed, but Pin 7 should then be connected to Pin 12.

STEP II . . . GAIN ADJUST

Turn all bits ON and adjust $100~\Omega$ gain trimmer, R2, until the output is 9.9976 V. (Full scale is adjusted to 1 LSB less than nominal full scale of 10.000 V.) If a 10.2375 V full scale is desired (exactly 2.5 mV/bit), insert a $120~\Omega$ resistor in series with the gain resistor at Pin 10 to the op amp output.

FIGURE 5. BIPOLAR CONFIGURATION

This configuration provides a bipolar output voltage from -5.000 V to +4.9976 V, with positive full scale occurring with all bits ON (all 1s).

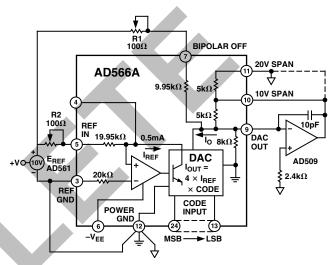


Figure 5. ±5 V Bipolar Voltage Output

STEP I . . . OFFSET ADJUST

Turn OFF all bits. Adjust $100\,\Omega$ trimmer R1 to give –5.000 output V.

STEP II . . . GAIN ADJUST

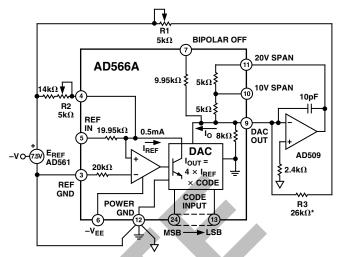
Turn ON all bits. Adjust $100\,\Omega$ gain trimmer R2 to give a reading of +4.9976 V.

Please note that it is not necessary to trim the op amp to obtain full accuracy at room temperature. In most bipolar situations, an op amp trim is unnecessary unless the untrimmed offset drift of the op amp is excessive.

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FIGURE 6. OTHER VOLTAGE RANGES

The AD566A can also be easily configured for a unipolar 0 V to +5 V range or ± 2.5 V and ± 10 V bipolar ranges by using the additional 5 k Ω application resistor provided at the 20 V span R terminal, Pin 11. For a 5 V span (0 V to +5 V or ± 2.5 V), the two 5 k Ω resistors are used in parallel by shorting Pin 11 to Pin 9 and connecting Pin 10 to the op amp output and the bipolar offset resistor either to ground for unipolar or to V_{REF} for the bipolar range. For the ± 10 V range (20 V span), use the 5 k Ω resistors in series by connecting only Pin 11 to the op amp output and the bipolar offset connected as shown. The ± 10 V option is shown in Figure 6.



^{*} THE PARALLEL COMBINATION OF THE BIPOLAR OFFSET RESISTOR AND R3 ESTABLISHES A CURRENT TO BALANCE THE MSB CURRENT. THE EFFECT OF TEMPERATURE COEFFICIENT MISMATCH BETWEEN THE BIPOLAR RESISTOR COMBINATION AND DAC RESISTORS IS EXPANDED ON PREVIOUS PAGE.

Figure 6. ±10 V Voltage Output

Table I. Digital Input Codes

DIGITAL INPUT MSB LSB	Straight Binary	ANALOG OUTPUT Offset Binary	Twos Complement*
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Zero	-FS	Zero
	Mid Scale – 1 LSB	Zero – 1 LSB	+FS – 1 LSB
	+1/2 FS	Zero	-FS
	+FS – 1 LSB	+FS – 1 LSB	Zero – 1 LSB

^{*}Inverts the MSB of the offset binary code with an external inverter to obtain twos complement.

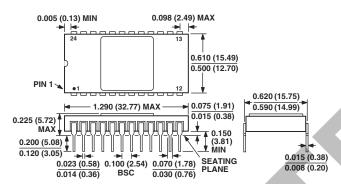


OUTLINE DIMENSIONS

24-Lead Side-Brazed Solder Lid Ceramic DIP [DIP/SB]

(D-24)

Dimensions shown in inches and (millimeters)

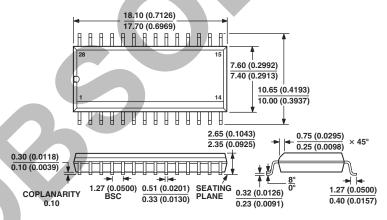


CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

28-Lead Standard Small Outline Package [SOIC] Wide Body

(RW-28)

Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MS-013AE
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Revision History

Location	Page
10/02—Data Sheet changed from REV. D to REV. E.	
Edits to SPECIFICATIONS	2
OUTLINE DIMENSIONS updated	11

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