PRODUCT DISCONTINUATION NOTICE - LAST TIME BUY EXPIRES MAY 6, 2017

General Description

The 87946I is a low skew, ÷1, ÷2 LVCMOS Fanout Buffer. The 87946I has two selectable single ended clock inputs. The 87946I has two selectable single ended clock inputs. The single ended clock inputs accept LVCMOS or LVTTL input levels. The low impedance LVCMOS outputs are designed to drive 50Ω series or parallel terminated transmission lines. The effective fanout can be increased from 10 to 20 by utilizing the ability of the outputs to drive two series terminated lines.

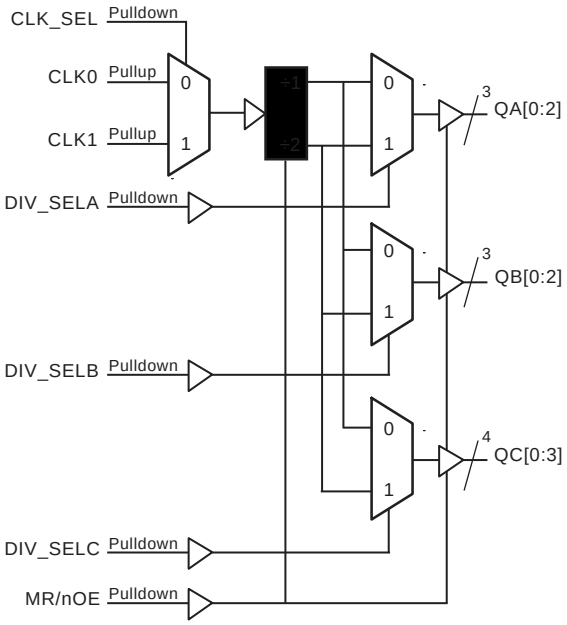
The divide select inputs, DIV_SELx, control the output frequency of each bank. The outputs can be utilized in the ÷1, ÷2 or a combination of ÷1 and ÷2 modes. The master reset input, MR/nOE, resets the internal frequency dividers and also controls the active and high impedance states of all outputs.

The 87946I is characterized at 3.3V core/3.3V output. Guaranteed output and part-to-part skew characteristics make the 87946I ideal for those clock distribution applications demanding well defined performance and repeatability.

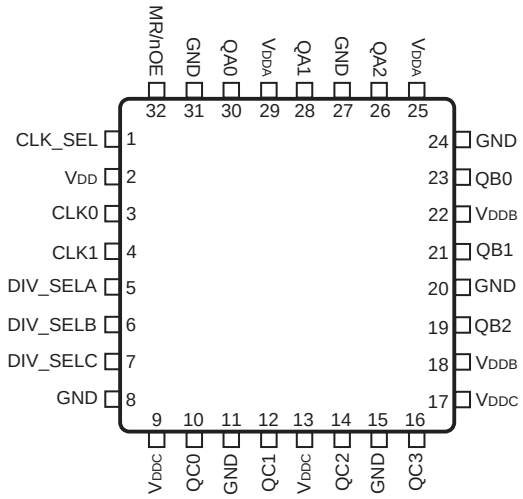
Features

- Ten single-ended LVCMOS outputs, 7Ω typical output impedance
- Selectable CLK0 and CLK1 LVCMOS clock inputs
- CLK0 and CLK1 can accept the following input levels: LVCMOS and LVTTL
- Maximum input/output frequency: 150MHz
- Output skew: 350ps (maximum)
- 3.3V input, 3.3V outputs
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package
- For drop-in replacement use 87946i-147

Block Diagram



Pin Assignment



87946I

32-Lead LQFP
7mm x 7mm x 1.4mm package body
Y Package
Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1	CLK_SEL	Input	Pulldown	Clock select input. When HIGH, selects CLK1. When LOW, selects CLK0. LVCMOS / LVTTL interface levels.
2	V_{DD}	Power		Positive supply pin.
3, 4	CLK0, CLK1	Input	Pullup	LVCMOS/LVTTL clock inputs.
5	DIV_SELA	Input	Pulldown	Controls frequency division for Bank A outputs. LVCMOS/LVTTL interface levels.
6	DIV_SELB	Input	Pulldown	Controls frequency division for Bank B outputs. LVCMOS/LVTTL interface levels.
7	DIV_SELC	Input	Pulldown	Controls frequency division for Bank C outputs. LVCMOS/LVTTL interface levels.
8, 11, 15, 20, 24, 27, 31	GND	Power		Power supply ground.
9, 13, 17	V_{DDC}	Power		Positive supply pins for Bank C outputs.
10, 12, 14, 16	QC0, QC1, QC2, QC3	Output		Bank C clock outputs. LVCMOS/LVTTL interface levels. 7Ω typical output impedance.
18, 22	V_{DDB}	Power		Positive supply pins for Bank B outputs.
19, 21, 23	QB2, QB1, QB0	Output		Bank B clock outputs. LVCMOS/LVTTL interface levels. 7Ω typical output impedance.
25, 29	V_{DDA}	Power		Positive supply pins for Bank A outputs.
26, 28, 30	QA2, QA1, QA0	Output		Bank A clock outputs. LVCMOS/LVTTL interface levels. 7Ω typical output impedance.
32	MR/nOE	Input	Pulldown	Master reset and output enable. When LOW, output drivers are enabled. When HIGH, output drivers are in High-Impedance and dividers are reset. LVCMOS / LVTTL interface levels.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance				4	pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
C_{PD}	Power Dissipation Capacitance (per output); NOTE 1	V_{DD}, V_{DDX} = 3.6V		25		pF
R_{OUT}	Output Impedance			7		Ω

NOTE 1: V_{DDx} denotes V_{DDA}, V_{DDB}, V_{DDC}.

Table 3. Function Table

Inputs				Outputs		
MR/nOE	**DIV_SELA**	**DIV_SELB**	**DIV_SELC**	**QA0:QA2**	**QB0:QB2**	**QC0:QC3**
1	X	X	X	High-Impedance	High-Impedance	High-Impedance
0	0	X	X	$f_{IN}/1$	Active	Active
0	1	X	X	$f_{IN}/2$	Active	Active
0	X	0	X	Active	$f_{IN}/1$	Active
0	X	1	X	Active	$f_{IN}/2$	Active
0	X	X	0	Active	Active	$f_{IN}/1$
0	X	X	1	Active	Active	$f_{IN}/2$

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	**Rating**
Supply Voltage, V_{DD}	4.6V
Inputs, V_{DD}	-0.5V to V_{DD} + 0.5V
Outputs, V_{DD}	-0.5V to V_{DDX}+ 0.5V
Package Thermal Impedance, θ_{JA}	47.9°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, $V_{DD} = V_{DDX} = 3.3V \pm 0.3V$, T_A = -40°C to 85°C

Symbol	**Parameter**	**Test Conditions**	**Minimum**	**Typical**	**Maximum**	**Units**
V_{DD}	Positive Supply Voltage		3.0	3.3	3.6	V
V_{DDX}	Output Supply Voltage; NOTE 1		3.0	3.3	3.6	V
I_{DD}	Power Supply Current				85	mA

NOTE 1: V_{DDX} denotes V_{DDA}, V_{DDB}, V_{DDC}.

Table 4B. LVCMOS/LVTTL DC Characteristics, $V_{DD} = V_{DDX} = 3.3V \pm 0.3V$, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	DIV_SELA, DIV_SELB, DIV_SELC, CLK_SEL, MR/nOE		2		V_{DD} + 0.3	V
		CLK0, CLK1		2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	DIV_SELA, DIV_SELB, DIV_SELC, CLK_SEL, MR/nOE		-0.3		0.8	V
		CLK0, CLK1		-0.3		1.3	V
I_{IH}	Input High Current	DIV_SELA, DIV_SELB, DIV_SELC, CLK_SEL, MR/nOE	$V_{DD} = V_{IN} = 3.6V$			120	µA
		CLK0, CLK1	$V_{DD} = V_{IN} = 3.6V$			5	µA
I_{IL}	Input Low Current	DIV_SELA, DIV_SELB, DIV_SELC, CLK_SEL, MR/nOE	$V_{DD} = 3.6V$, $V_{IN} = 0V$	-5			µA
		CLK0, CLK1	$V_{DD} = 3.6V$, $V_{IN} = 0V$	-120			µA
V_{OH}	Output High Voltage		I_{OH} = -20mA	2.5			V
V_{OL}	Output Low Voltage		I_{OH} = 20mA			0.4	V

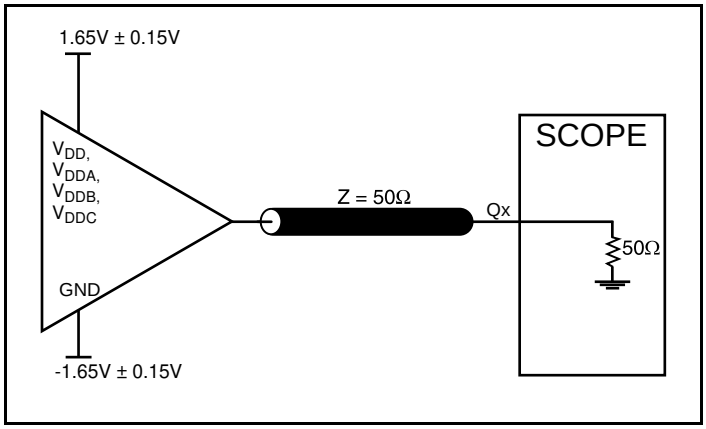
AC Electrical Characteristics

Table 5. AC Characteristics, $V_{DD} = V_{DDX} = 3.3V \pm 0.3V$, $T_A = -40°C$ to $85°C$

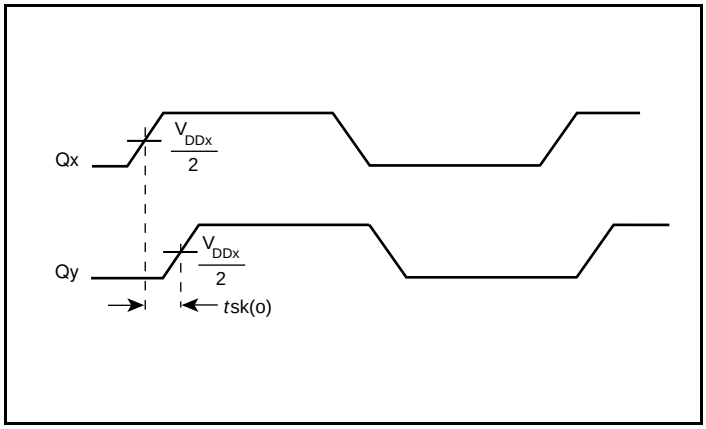
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{IN}	Input Frequency				150	MHz
tp_{LH}	Propagation Delay Low to High; NOTE 1		2		12	ns
tp_{HL}	Propagation Delay High to Low; NOTE 1		2.0		11.5	ns
*t*sk(o)	Output Skew; NOTE 2, 6				350	ps
*t*sk(w)	Multiple Frequency Skew; NOTE 3, 6	$f_{MAX} < 100MHz$			350	ps
		$f_{MAX} > 100MHz$			450	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 4, 6				4.5	ns
t_R / t_F	Output Rise/Fall Time; NOTE 5	0.8V to 2.0V	0.1		1.0	ns
t_{EN}	Output Enable Time; NOTE 5				11	ns
t_{DIS}	Output Disable Time; NOTE 5				11	ns

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: V_{DDX} denotes V_{DDA}, V_{DDB}, V_{DDC}.
NOTE 1: Measured from $V_{DD}/2$ of the input to $V_{DDX}/2$ of the output.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDX}/2$.
NOTE 3: Defined as skew across banks of outputs operating at different frequencies with the same supply voltage and equal load conditions.
NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltage, same frequency and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at $V_{DDX}/2$.
NOTE 5: These parameters are guaranteed by characterization. Not tested in production.
NOTE 6: This parameter is defined in accordance with JEDEC Standard 65.

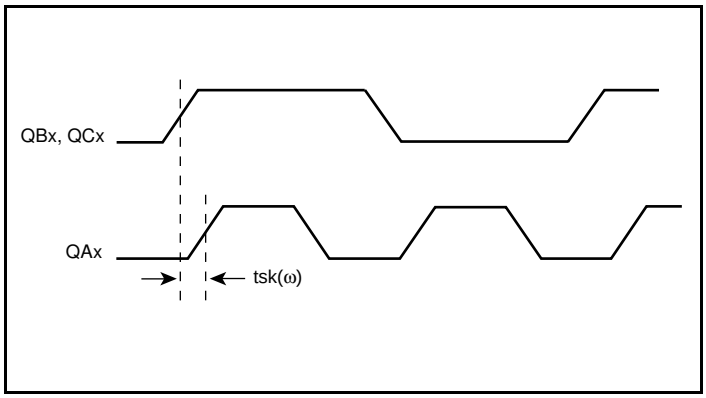
Parameter Measurement Information



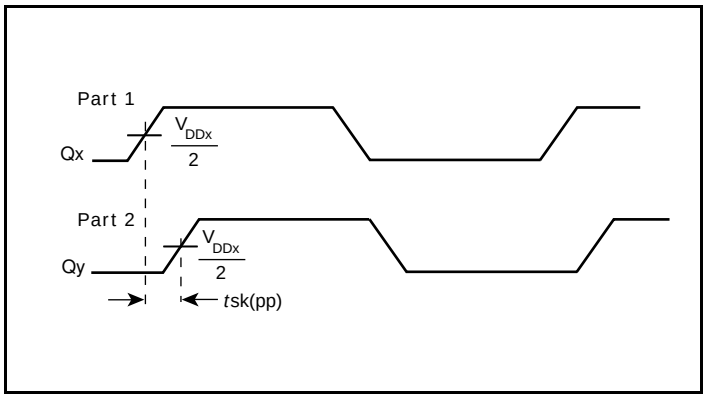
3.3V Output Load AC Test Circuit



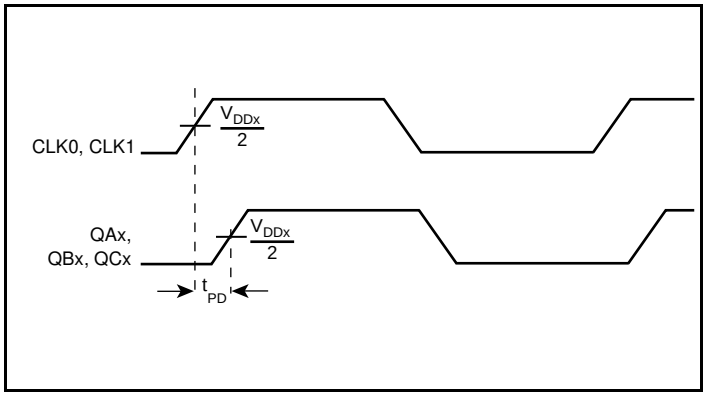
Output Skew



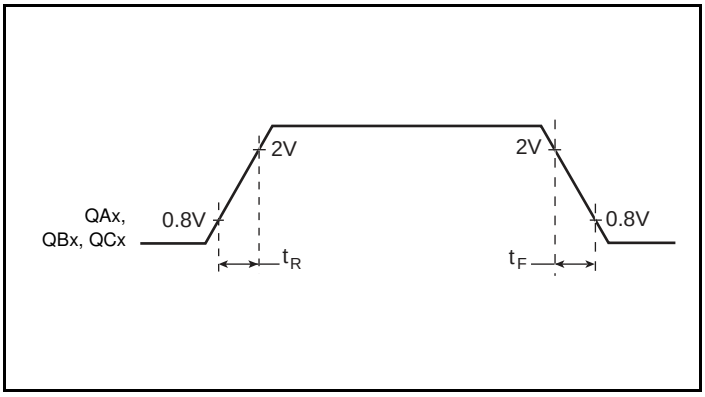
Multiple Frequency Skew



Part-to-Part Skew



Propagation Delay



Output Rise/Fall Time

Application Information

Recommendations for Unused Input and Output Pins

Inputs:

CLK Inputs

For applications not requiring the use of a clock input, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the CLK input to ground.

LVCMOS Control Inputs

All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVCMOS Outputs

All unused LVCMOS output can be left floating. There should be no trace attached.

Reliability Information

Table 6. θ_{JA} vs. Air Flow Table

θ_{JA} vs. Air Flow (Linear Feet per Minute)			
Linear Feet per Minute	**0**	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W
NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.			

Transistor Count

The transistor count for 87946I is: 1204

Package Outline and Package Dimensions

Package Outline - Y Suffix for 32 Lead LQFP

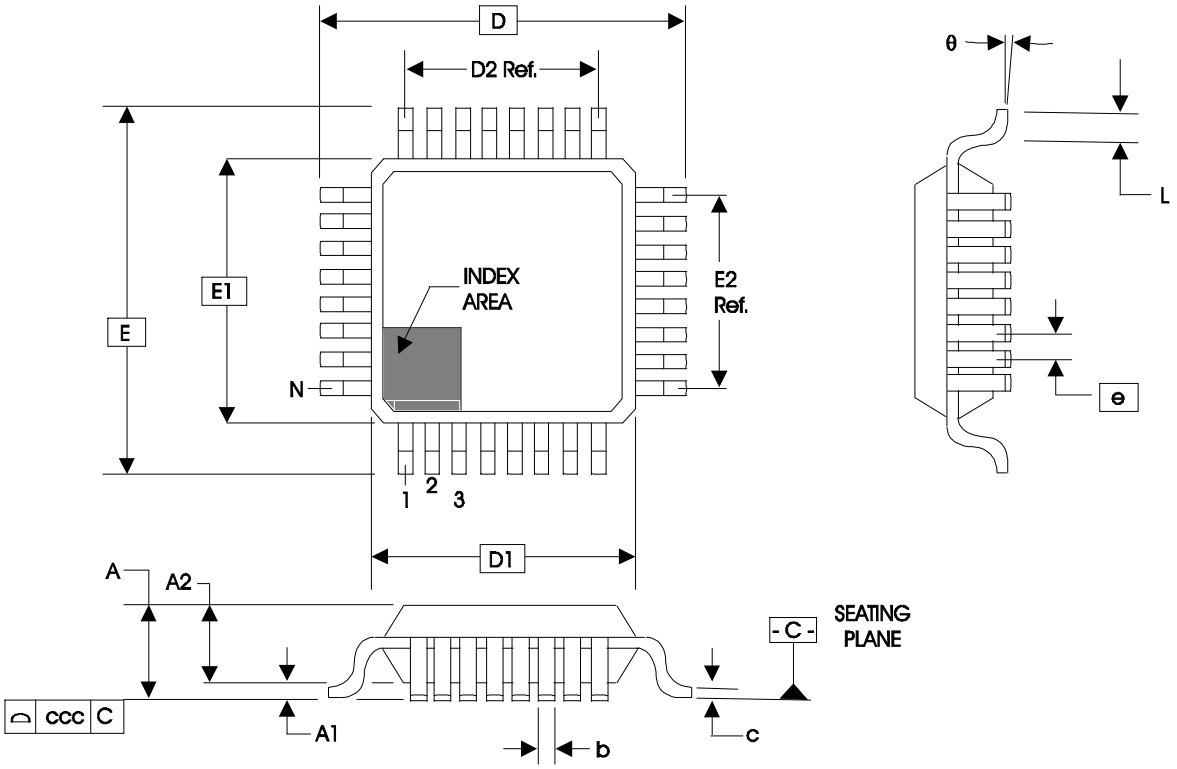


Table 7. Package Dimensions for 32 Lead LQFP

JEDEC Variation: All Dimensions in Millimeters			
Symbol	**Minimum**	**Nominal**	**Maximum**
N		32	
A			1.60
A1	0.05		0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
c	0.09		0.20
D & E		9.00 Basic	
D1 & E1		7.00 Basic	
D2 & E2		5.60 Ref.	
e		0.80 Basic	
L	0.45	0.60	0.75
θ	0°		7°
ccc			0.10

Reference Document: JEDEC Publication 95, MS-026

Ordering Information

Table 8. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
87946AYILF	ICS87946AYIL	“Lead-Free” 32 Lead LQFP	Tray	-40°C to 85°C
87946AYILFT	ICS87946AYIL	“Lead-Free” 32 Lead LQFP	Tape & Reel	-40°C to 85°C

Revision History Sheet

Rev	Table	Page	Description of Change	Date
A	T1	1 2 6	Features section added *Max Input/Output frequency* bullet. Revised MR/nOE description. Revised Output Rise & Fall time diagram	8/14/02
B	T5	4	AC Characteristics Table changed: (CLK0, CLK1) TP_{LH} from 6.0ns max. to 12.0ns max, deleted typical value (CLK0, CLK1) TP_{HL} from 6.0ns max. to 11.5ns max, deleted typical value	10/22/02
B	T5 T8	5 6 7 8 9	AC Characteristics Table - changed symbol f_{OUT} to f_{IN}. Moved 150MHz min. to max. column. Added Thermal Note. Corrected NOTE 2. Updated parameter Measurement Information section. Added Recommendations for Unused Input and Output Pins section. Updated Package Outline drawing. Ordering Information Table - deleted ICS prefix from Part/Order Number column. Added lead-free marking.	3/17/10
B		1	Deleted HiperClocks logo from General Description. Update Header / Footer of the datasheet.	6/22/12
B	T8	9	Ordering Information - removed leaded devices, PDN CQ-13-02. Updated data sheet format.	2/18/15
B	T8	9	Ordering Information - Deleted LF note below table. Product Discontinuation Notice - Last time buy expires May 6, 2017. PDN CQ-16-01 Updated header and footer.	6/28/16
C		1	Corrected datasheet title. Corrected *General Description*, first sentence from *Clock Generator* to *Fanout Buffer*.	9/20/16

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