Low Skew, Low Additive Jitter 2 x10 LVPECL Fanout Buffer

Features

- Two inputs accept any differential (LVPECL, HCSL, LVDS, SSTL, CML) or single ended LVCMOS signal
- Ten 2.5V/3.3V LVPECL outputs
- Ultra-low additive jitter: 53fs for 125 MHz clock measured in 12KHz to 20MHz band
- Supports clock frequencies from 0 to 1.6GHz
- Supports 2.5V or 3.3V power supplies
- Embedded Low Drop Out (LDO) Voltage regulator provides superior Power Supply Noise Rejection
- Maximum output to output skew of 50ps
- Maximum input to output delay of 1.2ns
- Small input to output delay variation over voltage, temperature and process of 0.34ns
- Fast rise and fall times of 168ps
- Phase noise floor below -160dB/Hz for 125MHz clock

Ordering Information

ZL40260LDG1	32 Pin QFN	Trays
ZL40260LDF1	32 pin QFN	Tape and Reel
ZL40260QGG1	32 pin eTQFP	Trays
ZL40260QGF1	32 pin eTQFP	Tape and Reel

Package size: 5 x 5 mm QFN and 7 x 7 mm eTQFP

-40°C to +85°C

Applications

- General purpose clock distribution
- Low jitter clock trees
- Logic translation
- Clock and data signal restoration
- Wired communications: OTN, SONET/SDH, GE, 10 GE, FC and 10G FC
- PCI Express generation 1/2/3/4 clock distribution
- Wireless communications
- High performance microprocessor clock distribution
- Test equipment

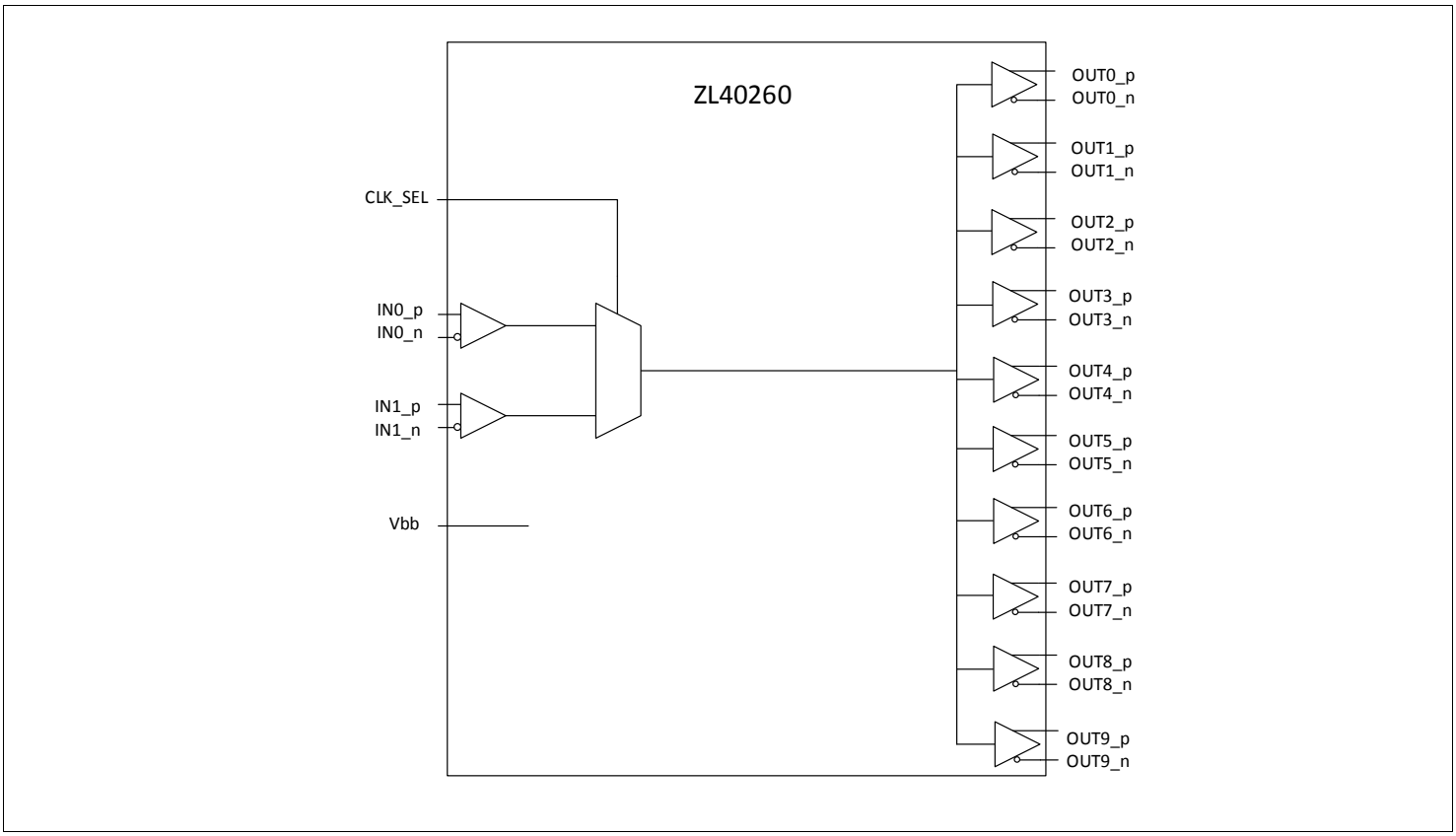


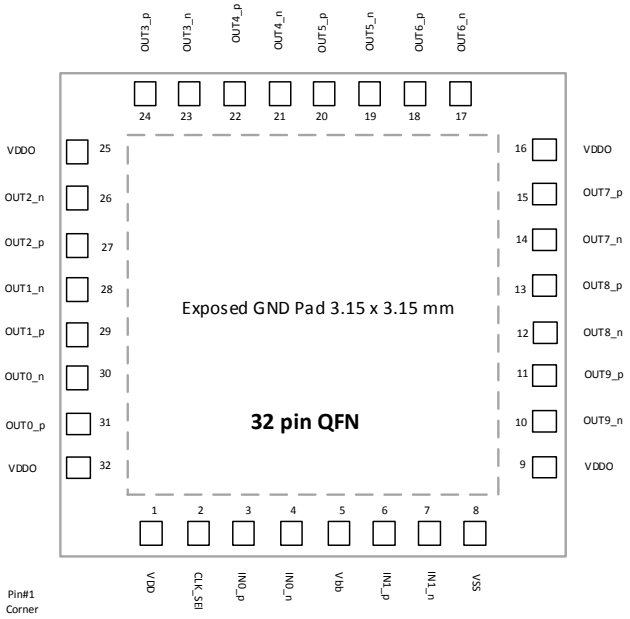
Figure 1. Functional Block Diagram

Table of Contents

List of Figures

Pin Diagram

The device is packaged in a 5x5mm 32-pin QFN and 7x7mm 32-pin eTQFP.



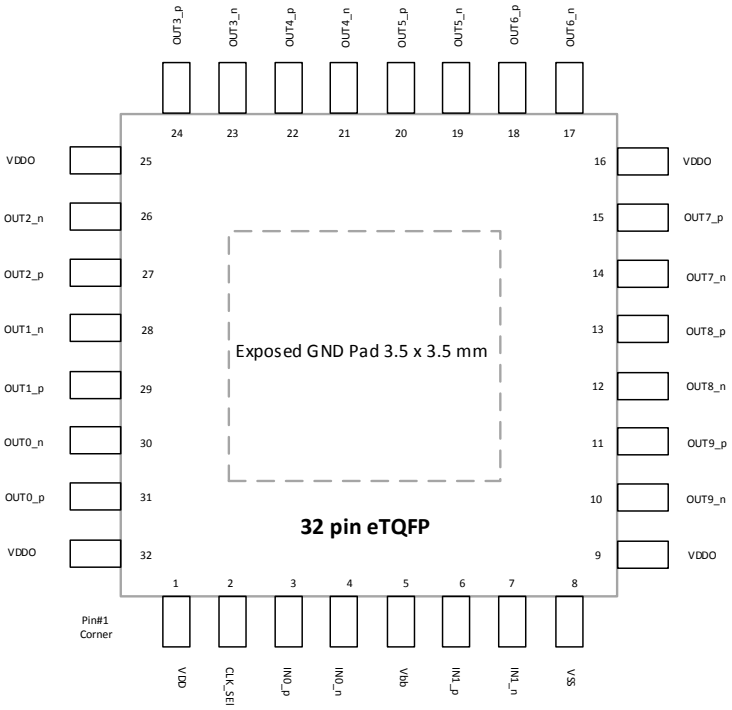


Figure 2. Pin Diagram (not to scale)

Pin Descriptions

All device inputs and outputs are LVPECL unless described otherwise. The I/O column uses the following symbols: I – input, I_{PU} – input with 31kΩ internal pull-up resistor, I_{PD} – input with 30kΩ internal pull-down resistor, $I_{PU/PD}$ – input biased to VDD/2 with 60kΩ internal pull-up and pull-down resistors (30 kΩ equivalent), O – output, P – power supply pin.

Table 1 Pin Descriptions

#	Name	I/O	Description
Input Reference			
3 4 6 7	IN0_p IN0_n IN1_p IN1_n	I_{PD} $I_{PU/PD}$ I_{PD} $I_{PU/PD}$	**Differential/Single Ended References 0 and 1** Input frequency range 0Hz to 1.6GHz. Non inverting inputs (_p) are pulled down with internal 30kΩ pull-down resistors. Inverting inputs (_n) are pulled up and pulled down with 60kΩ internal resistors (30kΩ equivalent) to keep inverting input voltages at VDD/2 when inverting inputs are left floating (device fed with a single ended reference).
Output Clocks			
31 30 29 28 27 26 24 23 22 21 20 19 18 17 15 14 13 12 11 10	OUT0_p OUT0_n OUT1_p OUT1_n OUT2_p OUT2_n OUT3_p OUT3_n OUT4_p OUT4_n OUT5_p OUT5_n OUT6_p OUT6_n OUT7_p OUT7_n OUT8_p OUT8_n OUT9_p OUT9_n	O	**Ultra Low Additive Jitter Differential LVPECL Outputs 0 to 9** Output frequency range 0 to 1.6GHz
Control			
2	CLK_SEL	I_{PD}	**Clock select input.** Logic level at this pin selects one of input references. When low selects IN0_p/IN0_n. When high selects IN1_p/IN1_n Accepts LVPECL and LVCMOS logic levels. This pin is pulled down with 30kΩ resistor.

Input Biasing			
5	Vbb	O	**Bias Output Voltage** Provides power output to bias IN0_n and/or IN1_n when input are fed by a single ended LVPECL inputs or if differential inputs signal is AC coupled (see application section).
Power and Ground			
1	VDD	P	**Positive Supply Voltage.** Connect to 3.3V or 2.5V supply. VDD does not have to be connected to the same voltage level as VDDO pins.
9 16 25 32	VDDO	P	**Positive Supply Voltage for LVPECL Outputs** Connect 3.3V or 2.5V. VDDO pins do not have to be connected to the same voltage level as VDD pin.
8	VSS	P	**Ground** Connect to the ground
E-Pad	VSS	P	**Ground** Connect to the ground

Functional Description

The ZL40260 is a 2x10 LVPECL clock fan out buffer shown in Figure 1with ten identical output clock drivers capable of operating at frequencies up to 1600MHz.

The ZL40260 has two inputs. Each input can accept differential (LVPECL, SSTL, LVDS, HSTL, CML) or a single ended LVPECL input or a CMOS input. The voltage level at CLK_SEL pin selects which input will be passed to the output drivers. LVPECL input must be externally biased and terminated with resistors. The device provides biasing voltage at the output pin Vbb which can minimize number of external resistors.

The ZL40260 is designed to fan out low-jitter reference clocks for wired or optical communications applications while adding minimal jitter to the clock signal. An internal linear power supply regulator and bulk capacitors minimize additive jitter due to power supply noise. The device operates from 2.5V+/-5% or 3.3V+/-5% supply. Its operation is guaranteed over the industrial temperature range -40°C to +85°C.

Clock Inputs

The following blocks diagram shows how to terminate different signals fed to the ZL40260 inputs. Please note that value of AC coupling capacitors needs to be increased for frequencies below 10MHz to reduce voltage drop. When driven from an AC coupled driver, the input voltage biasing is provided from Vbb output.

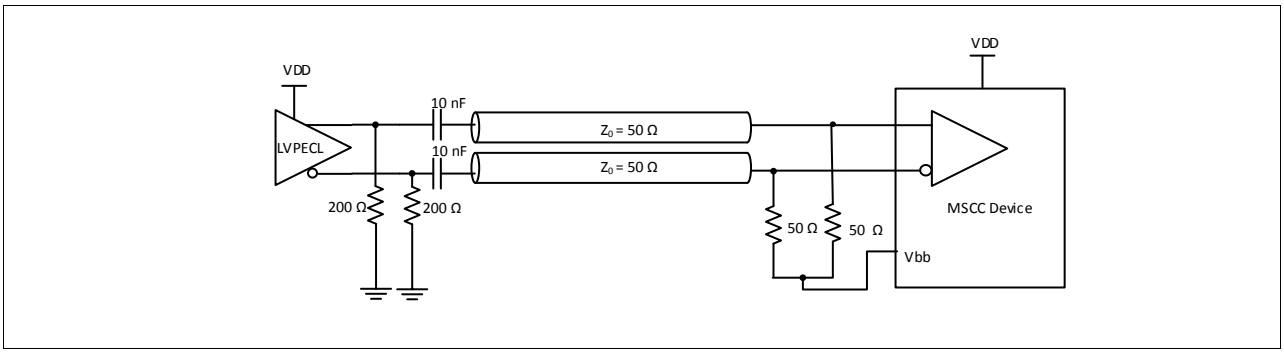


Figure 3. Input driven by a AC coupled LVPECL output

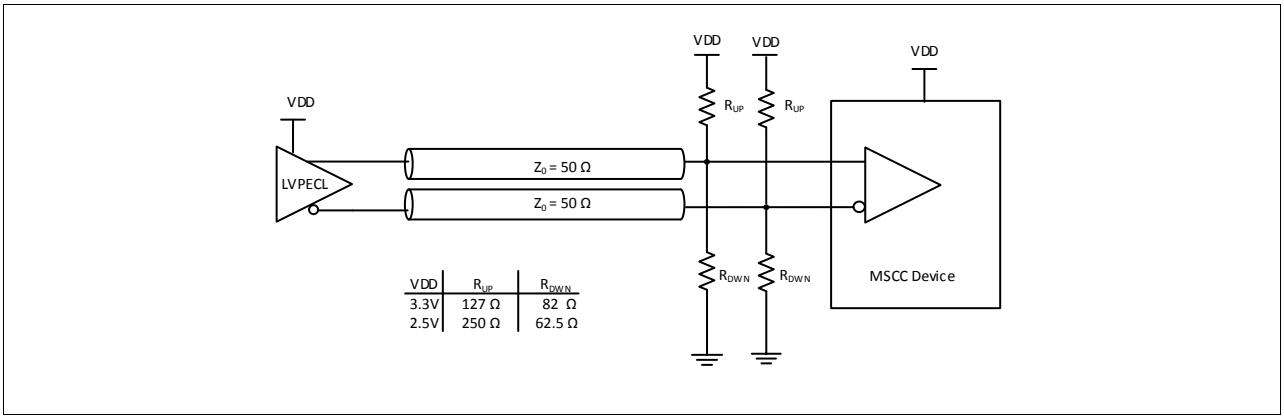


Figure 4. Input driven by a DC coupled LVPEVCL output

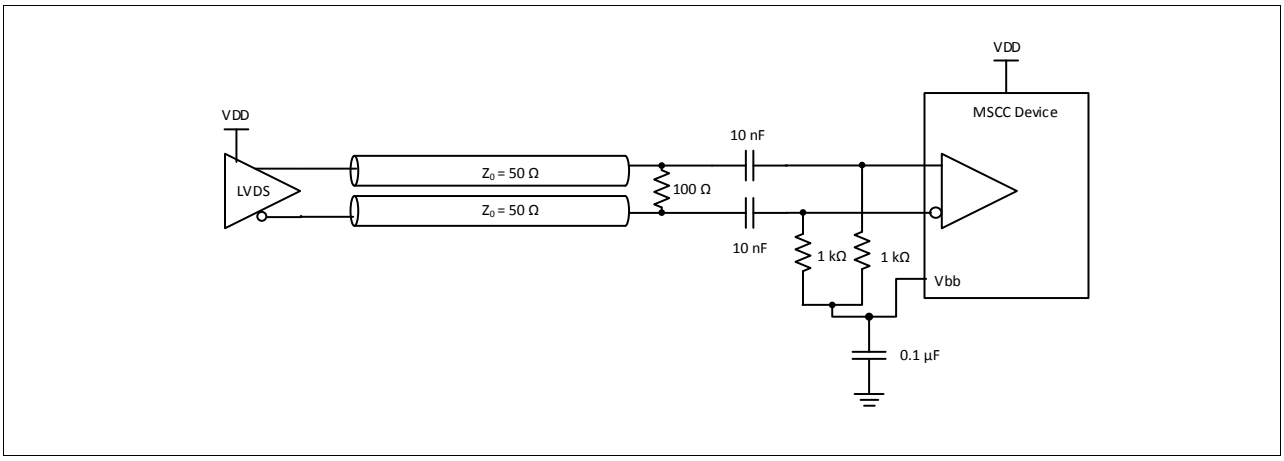


Figure 5. Input driven by AC coupled LVDS output

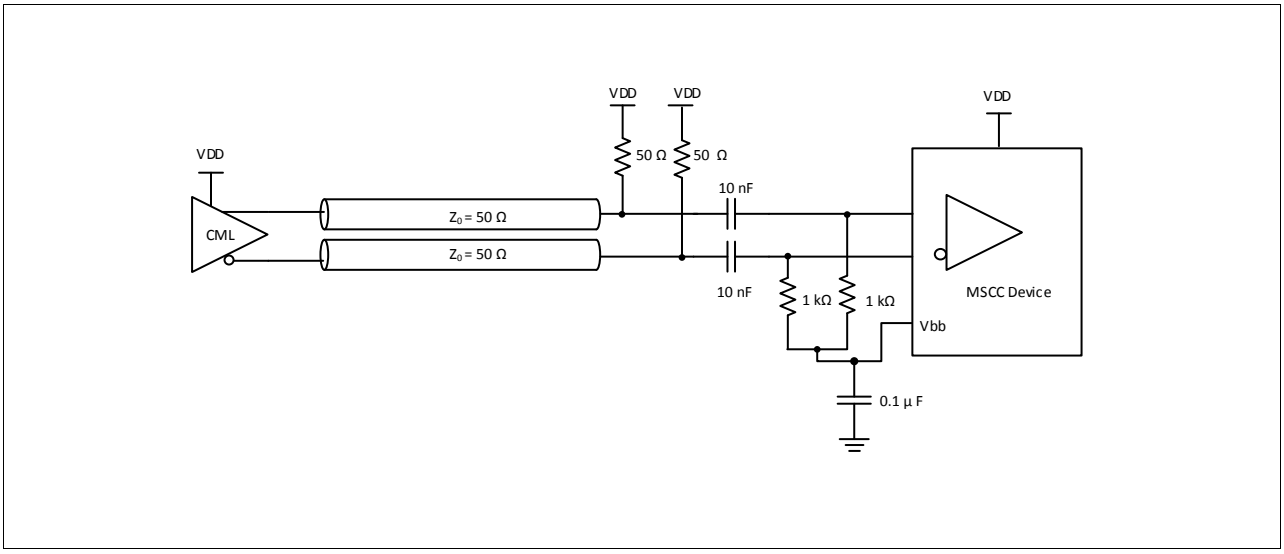


Figure 6. Input driven by 3.3V CML output

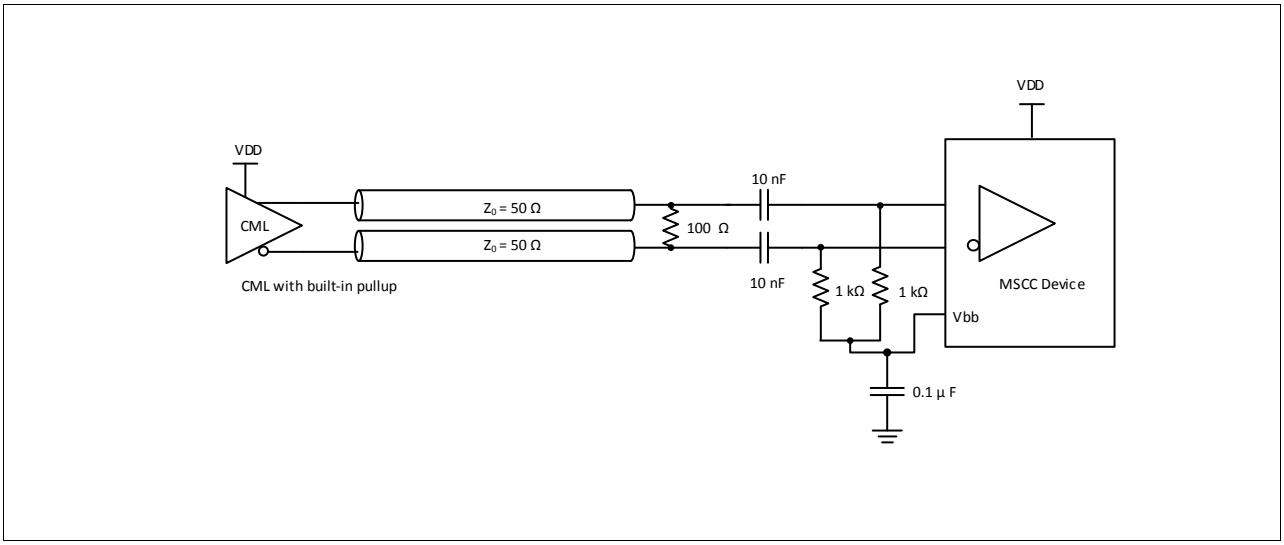


Figure 7. Input driven by 3.3V CML output with internal pull-ups

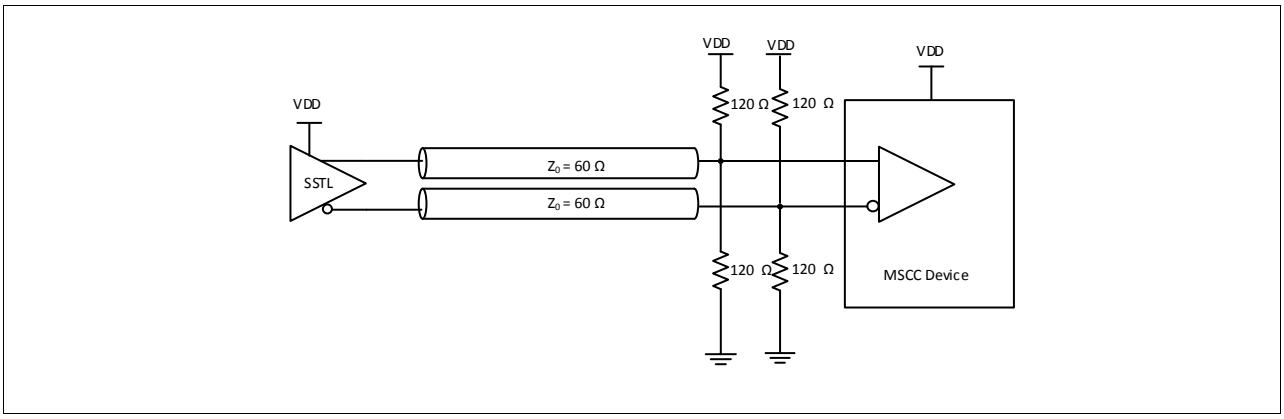


Figure 8. Input driven by SSTL output

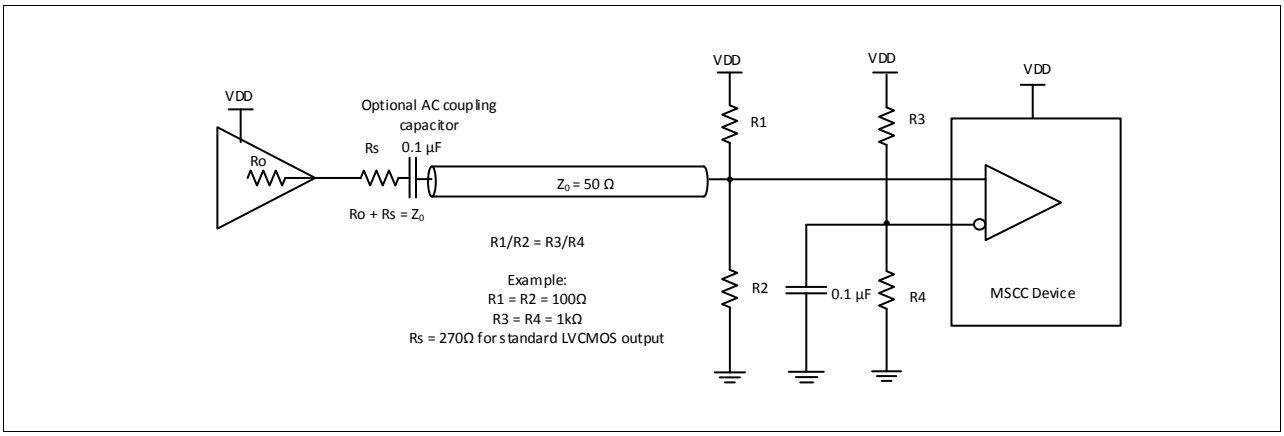


Figure 9. Input driven by single-ended output

Figure 9 shows how to terminate a single ended output such as LVCMOS. Ideally, resistors R1 and R2 should be 100Ω each and Ro + Rs should be 50Ω so that the transmission line is terminated at both ends with characteristic impedance. If the driving strength of the output driver is not sufficient to drive low impedance, the value of series resistor R_S should be increased. This will reduce the voltage swing at the input but this should be fine as long as the input voltage swing requirement is not violated (Table 4). The source resistors of Rs = 270Ω could be used for standard LVCMOS driver. This will provide 516mV of voltage swing for 3.3V LVCMOS driver with load current of (3.3V/2) *(1/(270Ω + 50Ω)) = 5.16mA.

For optimum performance both differential input pins (_p and _n) need to be DC biased to the same voltage. Hence, the ratio R1/R2 should be equal to the ratio R3/R4.

Clock Outputs

Termination for 3.3V LVPECL outputs is shown in following figures:

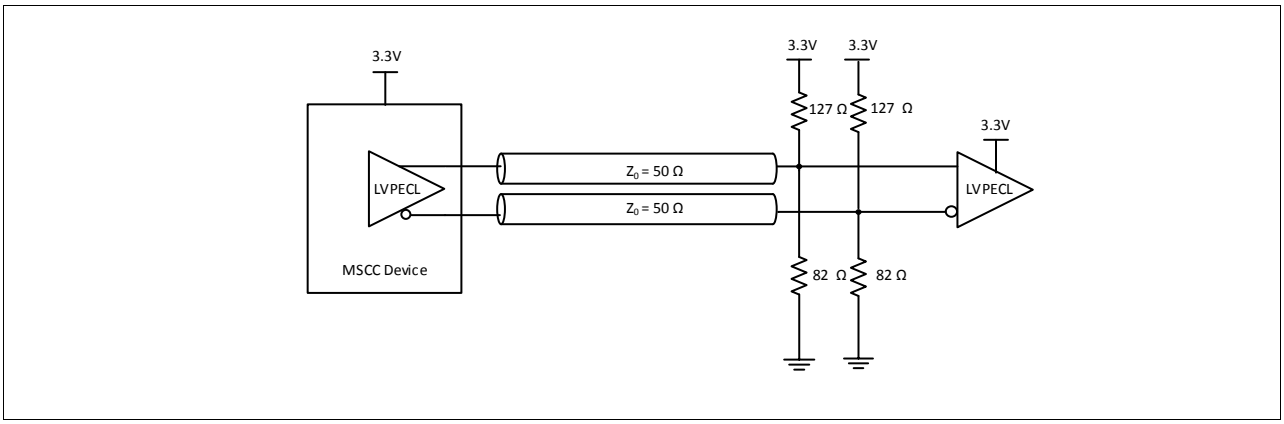


Figure 10. Termination for 3.3V LVPECL outputs

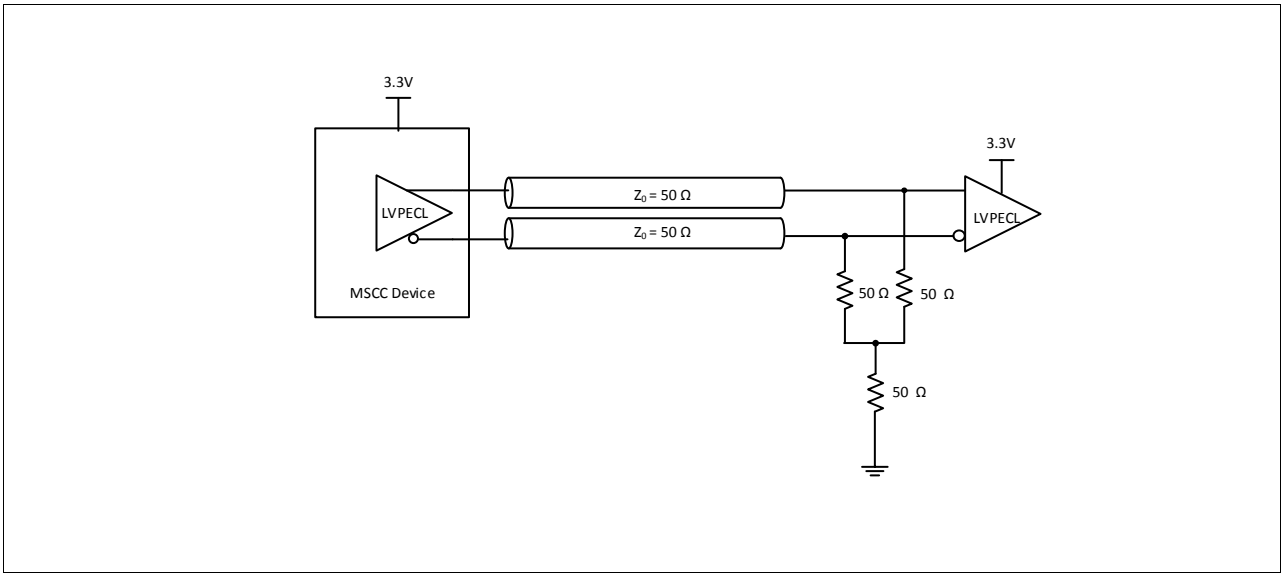


Figure 11. Alternative termination for 3.3V LVPECL outputs

Termination for 2.5V LVPECL outputs is shown in following figures:

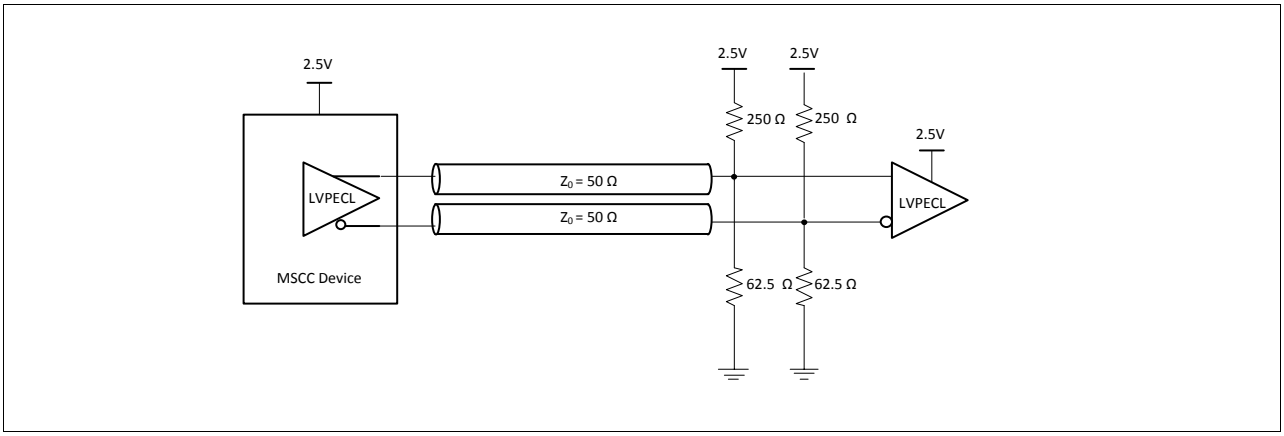


Figure 12. Termination for 2.5V LVPECL output

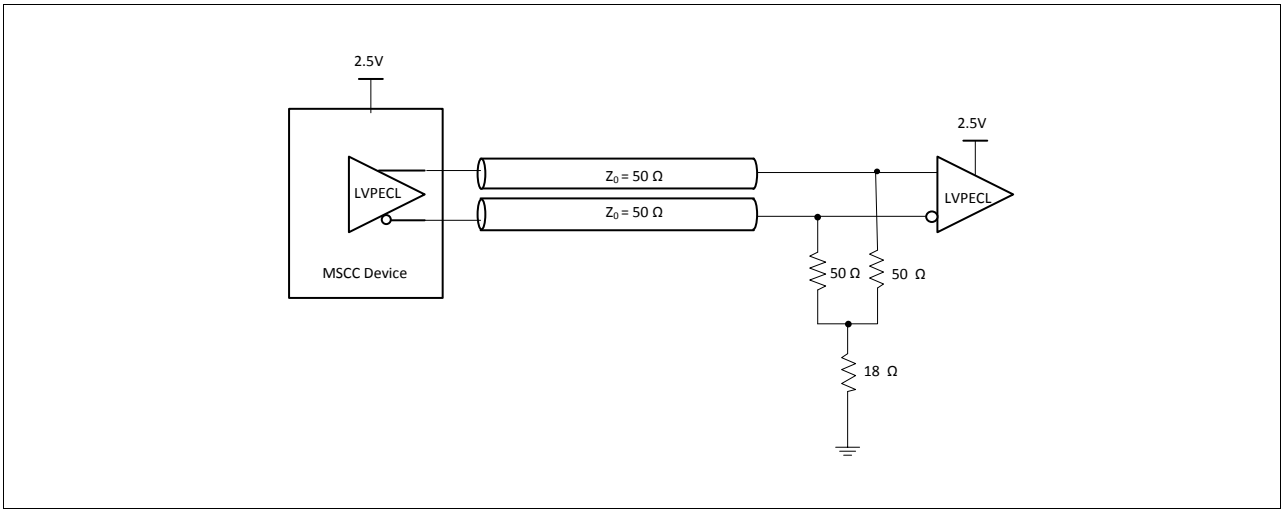


Figure 13. Alternative termination for 2.5V LVPECL output

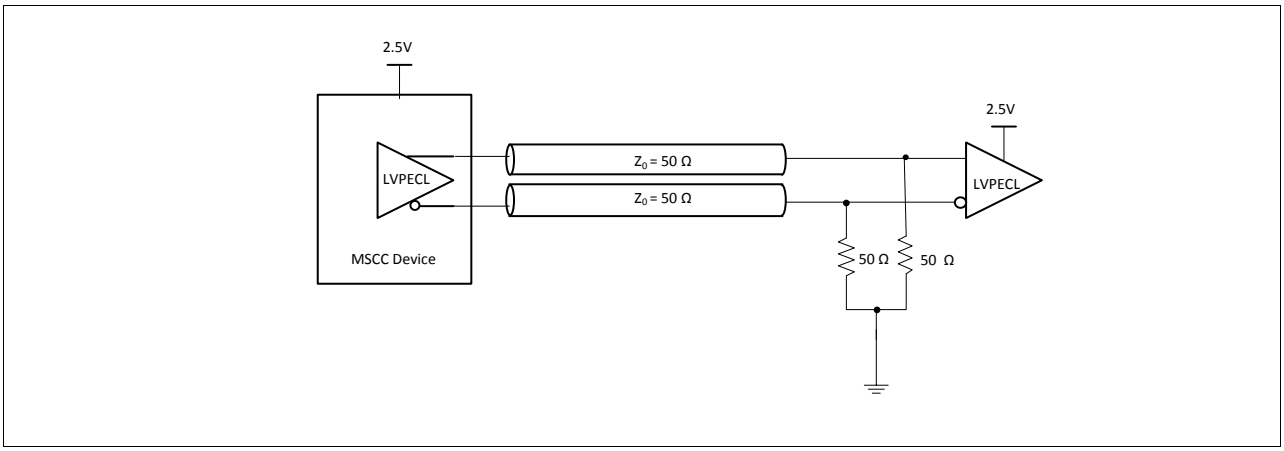


Figure 14. Alternative termination for 2.5V LVPECL output

The device is designed to drive differential input of semiconductor devices. In applications that use a transformer to convert from the differential to the single ended output (for example driving an oscilloscope 50Ω input), a resistor larger than 10Ω should be added at the center tap of the primary winding to achieve optimum jitter performance as shown in Figure 15. This is to provide a nominal common mode impedance of 10 Ω or higher which is typical for differential terminations.

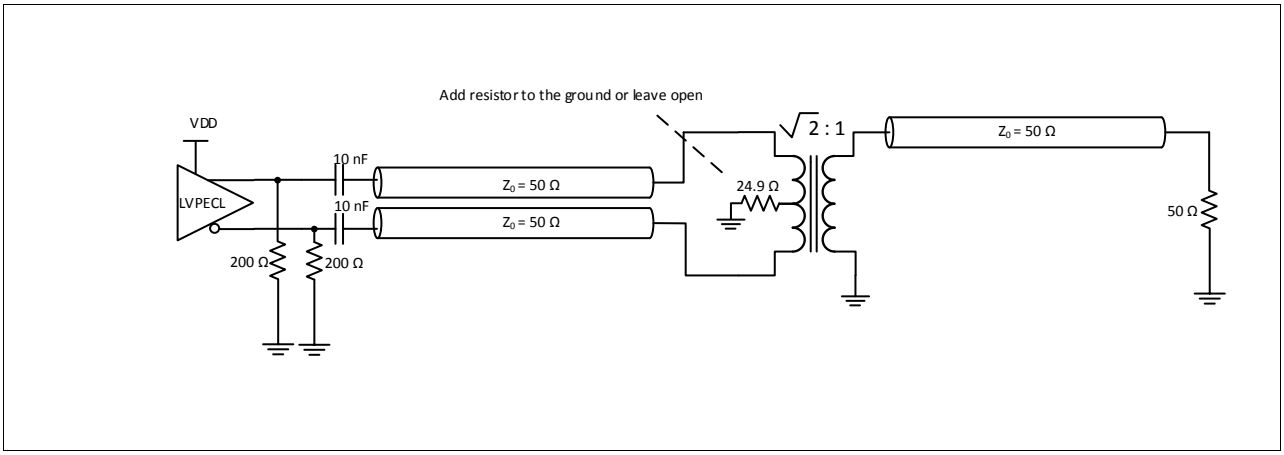


Figure 15. Driving a load via transformer

Termination of unused inputs and outputs

Unused inputs can be left unconnected or alternatively IN_0/1 can be pulled-down by 1KΩ resistor. Unused outputs should be left unconnected.

Power Consumption

The device total power consumption can be calculated as:

$$P_T = P_C + P_O$$

Where:

$P_C = V_{DD} \times I_{CORE}$ — The core power. The current is specified in Table 3.

$P_O = V_{DDO} \times I_{OUT} \times 10$ — Output power where the per output current is specified in Table 3.

Power dissipated inside the device can be calculated by subtracting power dissipated in termination/biasing resistors from the power consumption.

$$P_D = P_T - 10 \times P_{LVPECL}$$

$$P_{LVPECL} = (V_{OH} - V_B)^2 / 50\Omega + (V_{OL} - V_B)^2 / 50\Omega + (V_{OH} - V_B) \times V_B / 50\Omega + (V_{OL} - V_B) \times V_B / 50\Omega$$

V_{OH} and V_{OL} are the output high and low voltages respectively for LVPECL output

V_B is LVPECL bias voltage equal to V_{DD} – 2V

Power Supply Filtering

Each power pin (VDD and VDDO) should be decoupled with 0.1µF capacitor with minimum equivalent series resistance (ESR) and minimum series inductance (ESL). For example 0402 X5R Ceramic Capacitors with 6.3V minimum rating could be used. These capacitors should be placed as close as possible to the power pins. To reduce the power noise from adjacent digital components on the board each power supply could be further insulated with low resistance ferrite bead with two capacitors. The ferrite bead will also insulate adjacent component from the noise generated from the device. Following figure shows recommended decoupling for each power pin.

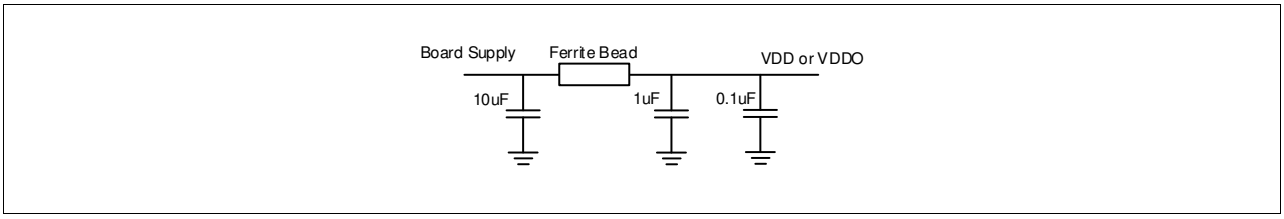


Figure 16. Power Supply Filtering

Power Supplies and Power-up Sequence

The device has two different power supplies: VDD and VDDO which are mutually independent.

The device is not sensitive to the power-up sequence. For example commonly used sequence where higher voltage comes up before or at the same time as the lower voltages can be used (or any other sequence).

AC and DC Electrical Characteristics

Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings*

	Parameter	Sym.	Min.	Typ.	Max.	Units	Notes
1	Supply voltage (3.3V)	V_{DD}	-0.5		4.6	V	
2	Supply voltage (2.5V)	V_{DD}	-0.5		4.6	V	
3	Storage temperature	T_{ST}	-55		125	°C	

* Exceeding these values may cause permanent damage
* Functional operation under these conditions is not implied
* Voltages are with respect to ground (GND) unless otherwise stated
*

Recommended Operating Conditions

Table 3 Recommended Operating Conditions*

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	Supply voltage 3.3V	V_{DD}/ V_{DDO}	3.135	3.30	3.465	V	
2	Supply voltage 2.5V	V_{DD}/ V_{DDO}	2.375	2.50	2.625	V	
3	Operating temperature	T_A	-40	25	85	°C	
4	Input voltage	V_{IN}	-0.3		V_{DD} + 0.3	V	
5	Core current	I_{CORE}		140	185	mA	
6	Current per output	I_{OUT}		22	28	mA	

* Voltages are with respect to ground (GND) unless otherwise stated
* The device supports two power supply modes (3.3V and 2.5V)

DC Electrical Characteristics

Table 4 DC Electrical Characteristics V_{DD}=V_{DDO}=3.3V

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	Output voltage reference (V_{BB})	V_{BB}	1.6	1.9	2.2	V	
2	Output high voltage	V_{OH}	1.9	2.08	2.4	V	
3	Output low voltage	V_{OL}	1.2	1.36	1.7	V	
4	Output differential swing**	V_{SW}	0.6	0.72	0.9	V	
5	Differential input common mode voltage for IN0_p/n and IN1_p/n	V_{CM}	1		2	V	
6	Differential input voltage difference for IN0_p/n and IN1_p/n f ≤ 800MHz	V_{ID}	0.17		1.3	V	
7	Differential input voltage difference for IN0_p/n and IN1_p/n 800MHz < f ≤ 1GHz	V_{ID}	0.22		1.3	V	
8	Differential input voltage difference for IN0_p/n and IN1_p/n for 1GHz < f ≤ 1.2GHz	V_{ID}	0.29		1.3	V	
9	Differential input voltage difference for IN0_p/n and IN1_p/n for 1.2GHz < f ≤ 1.4GHz	V_{ID}	0.39		1.3	V	
10	Differential input voltage difference for IN0_p/n and IN1_p/n for 1.4GHz < f ≤ 1.6GHz	V_{ID}	0.5		1.3	V	
11	Differential input leakage current for IN0_p/n and IN1_p/n (includes current due to pull-up and pull-down resistors)	I_{IL}	-150		150	µA	V_I = 2V or 0V
12	Single ended input voltage for IN0_p and IN1_p	V_{SI}	-0.3		2.7	V	
13	Single ended input common mode voltage (IN0_p/n and IN1_p/n)	V_{SIC}	1		2	V	
14	Single ended input voltage swing for IN0_p and IN1_p	V_{SID}	0.35		1.3	V	
15	Input pull-up/ pull-down resistance for INx_n	R_{PU}/R_{PD}		60		kΩ	
16	Input pull-down resistance for INx_p	R_{PD}		30		kΩ	

**Output differential swing is calculated as V_{SW} = V_{OH}-V_{OL}. It should not be confused with V_{SW} = 2 * (V_{OH}-V_{OL}) used in some datasheets.

Table 5 LVPECL DC characteristics; V_{DD}=V_{DDO}=2.5V

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	Output voltage reference (V_{BB})	V_{BB}	1	1.25	1.50	V	
2	Output high voltage	V_{OH}	1.1	1.28	1.7	V	
3	Output low voltage	V_{OL}	0.4	0.57	0.9	V	
4	Output differential swing**	V_{SW}	0.6	0.71	0.9	V	
5	Differential input common mode voltage for IN0_p/n and IN1_p/n	V_{CM}	1		2	V	
6	Differential input voltage difference for IN0_p/n and IN1_p/n f ≤ 800MHz	V_{ID}	0.18		1.3	V	
7	Differential input voltage difference for IN0_p/n and IN1_p/n 800MHz < f ≤ 1GHz	V_{ID}	0.25		1.3	V	
8	Differential input voltage difference for IN0_p/n and IN1_p/n for 1GHz < f ≤ 1.2GHz	V_{ID}	0.39		1.3	V	
9	Differential input voltage difference for IN0_p/n and IN1_p/n for 1.2GHz < f ≤ 1.4GHz	V_{ID}	0.7		1.3	V	
10	Differential input voltage difference for IN0_p/n and IN1_p/n for 1.4GHz < f ≤ 1.6GHz	V_{ID}	0.94		1.3	V	
11	Differential input leakage current for IN0_p/n and IN1_p/n (includes current due to pull-up and pull-down resistors)	I_{IL}	-150		150	µA	V_I = 2V or 0V
12	Single ended input voltage for IN0_p and IN1_p	V_{SI}	-0.3		2.7	V	
13	Single ended input common mode voltage (IN0_p/n and IN1_p/n)	V_{SIC}	1		2	V	
14	Single ended input voltage swing for IN0_p and IN1_p	V_{SID}	0.35		1.3	V	
15	Input pull-up/ pull-down resistance for INx_n	R_{PU}/R_{PD}		60		kΩ	
16	Input pull-down resistance for INx_p	R_{PD}		30		kΩ	

**Output differential swing is calculated as V_{SW} = V_{OH}-V_{OL}. It should not be confused with V_{SW} = 2 * (V_{OH}-V_{OL}) used in some datasheets.

Table 6 AC Electrical Characteristics – 3.3V LVPECL Outputs

Item	Symbol	Parameter	-40°C			25°C			85°C			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
1	f_{OUT}	Output Frequency	0		1.6	0		1.6	0		1.6	GHz
2	t_{PD}	Propagation Delay (from IN0_p/n)	860	968	1100	877	1004	1136	918	1052	1186	ps
3	$t_{sk(o)}$	Output Skew		28	50		28	50		28	50	ps
4	$t_{sk(pp)}$	Part-to-Part Skew		110	150		110	150		110	150	ps
5	P_{n1K}	Phase noise at 125MHz, Offset=1KHz		-127.4	-123.7		-127.4	-123.8		-127.4	-123.2	dBc/Hz
6	P_{n10K}	Phase noise at 125MHz, Offset=10KHz		-145.6	-142.8		-145.1	-139.9		-144.9	-140.8	dBc/Hz
7	P_{n100K}	Phase noise at 125MHz, Offset=100KHz		-154.6	-151.2		-155.1	-150.6		-155.0	-150.4	dBc/Hz
8	P_{n1M}	Phase noise at 125MHz, Offset=1MHz		-159.7	-158.3		-159.4	-157.7		-158.5	-156.1	dBc/Hz
9	P_{n10M}	Phase noise at 125MHz, Offset=10MHz		-162.0	-160.8		-161.4	-160.6		-160.8	-160.0	dBc/Hz
10	P_{n20M}	Phase noise at 125MHz, Offset=20MHz		-162.0	-160.9		-161.6	-160.8		-161.0	-160.5	dBc/Hz
11	t_{jit}	Buffer Additive Phase Jitter, RMS Carrier=125MHz		49	57		53	62		60	68	fs 12KHz-20MHz
12	t_R /t_F	Output Rise/Fall Time (125MHz) 20% to 80%, zero track, CL=1pF		152	165		168	178		177	187	ps
13	Duty-Cycle	Output differential duty cycle		50.5	51.5		50.5	51.8		50.5	51.6	%

Table 7 AC Electrical Characteristics – 2.5V LVPECL Output

Item	Symbol	Parameter	-40°C			25°C			85°C			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
1	f_{OUT}	Output Frequency	0		1.6	0		1.6	0		1.6	GHz
2	t_{PD}	Propagation Delay (from IN0_p/n)	820	954	1050	851	969	1093	893	1012	1139	ps
3	$t_{sk(o)}$	Output Skew		28	50		28	50		28	50	ps
4	$t_{sk(pp)}$	Part-to-Part Skew		110	150		110	150		110	150	ps
5	P_{n1K}	Phase noise at 125MHz; Offset=1KHz		-125.1	-121.0		-125.2	-120.8		-125.3	-120.9	dBc/Hz
6	P_{n10K}	Phase noise at 125MHz; Offset=10KHz		-143.7	-139.2		-143.5	-138.2		-143.9	-139.6	dBc/Hz
7	P_{n100K}	Phase noise at 125MHz; Offset=100KHz		-152.2	-149.3		-152.2	-148.9		-152.6	-149.1	dBc/Hz
8	P_{n1M}	Phase noise at 125MHz; Offset=1MHz		-158.6	-156.4		-158.5	-156.6		-157.9	-155.7	dBc/Hz
9	P_{n10M}	Phase noise at 125MHz; Offset=10MHz		-161.2	-159.4		-160.6	-159.3		-159.8	-158.3	dBc/Hz
10	P_{n20M}	Phase noise at 125MHz; Offset=20MHz		-161.3	-159.4		-160.8	-159.4		-160.0	-158.4	dBc/Hz
11	t_{jit}	Buffer Additive Phase Jitter, RMS Carrier=125MHz		52	69		58	74		67	79	fs 12KHz-20MHz
12	t_R /t_F	Output Rise/Fall Time (125MHz) 20% to 80%, zero track, CL=1pF		102	105		108	154		130	173	ps
13	Duty-Cycle	Output differential duty cycle		50.3	51.5		50.4	51.4		50.3	51.3	%

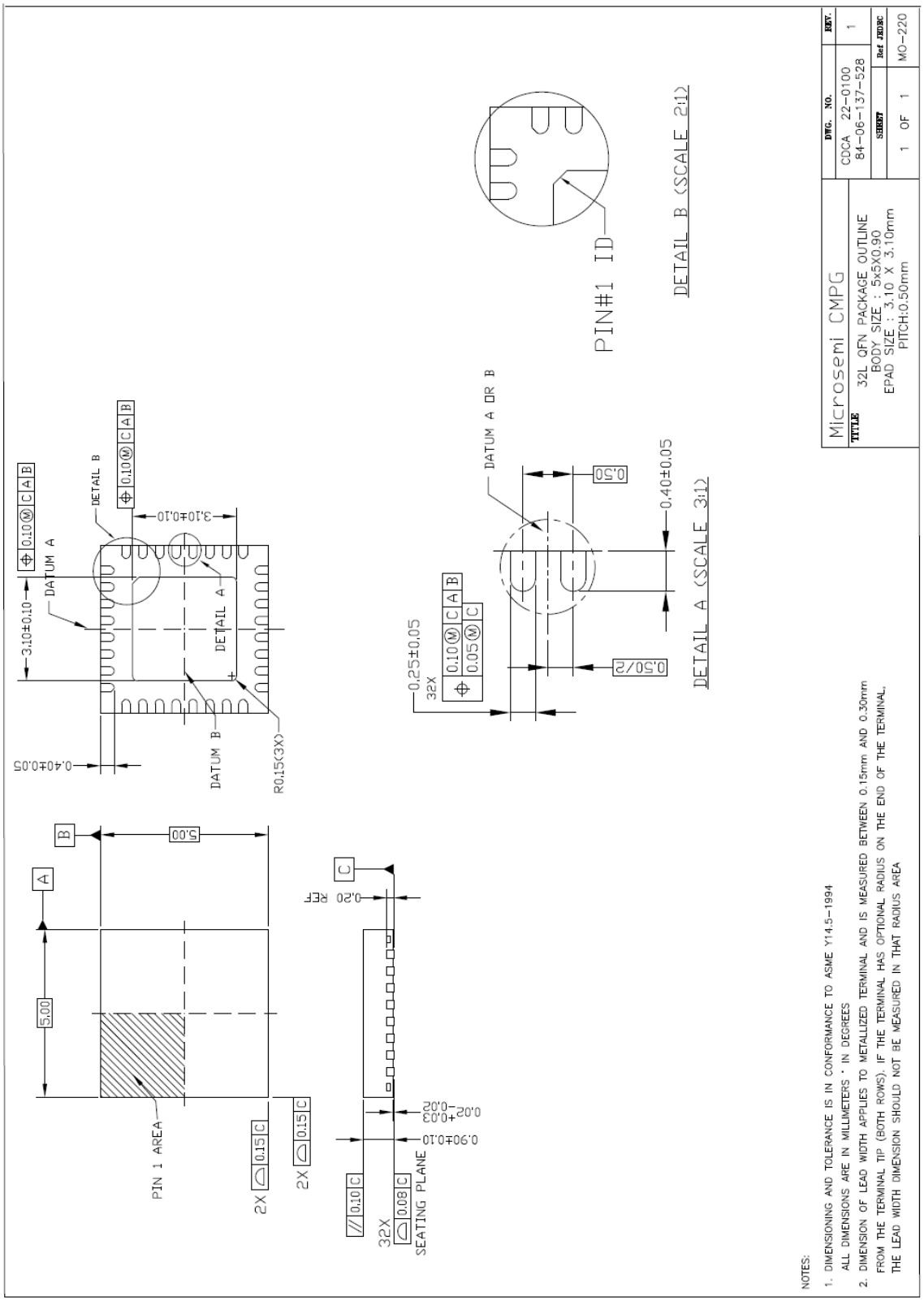
Table 8 5x5mm QFN Package Thermal Properties

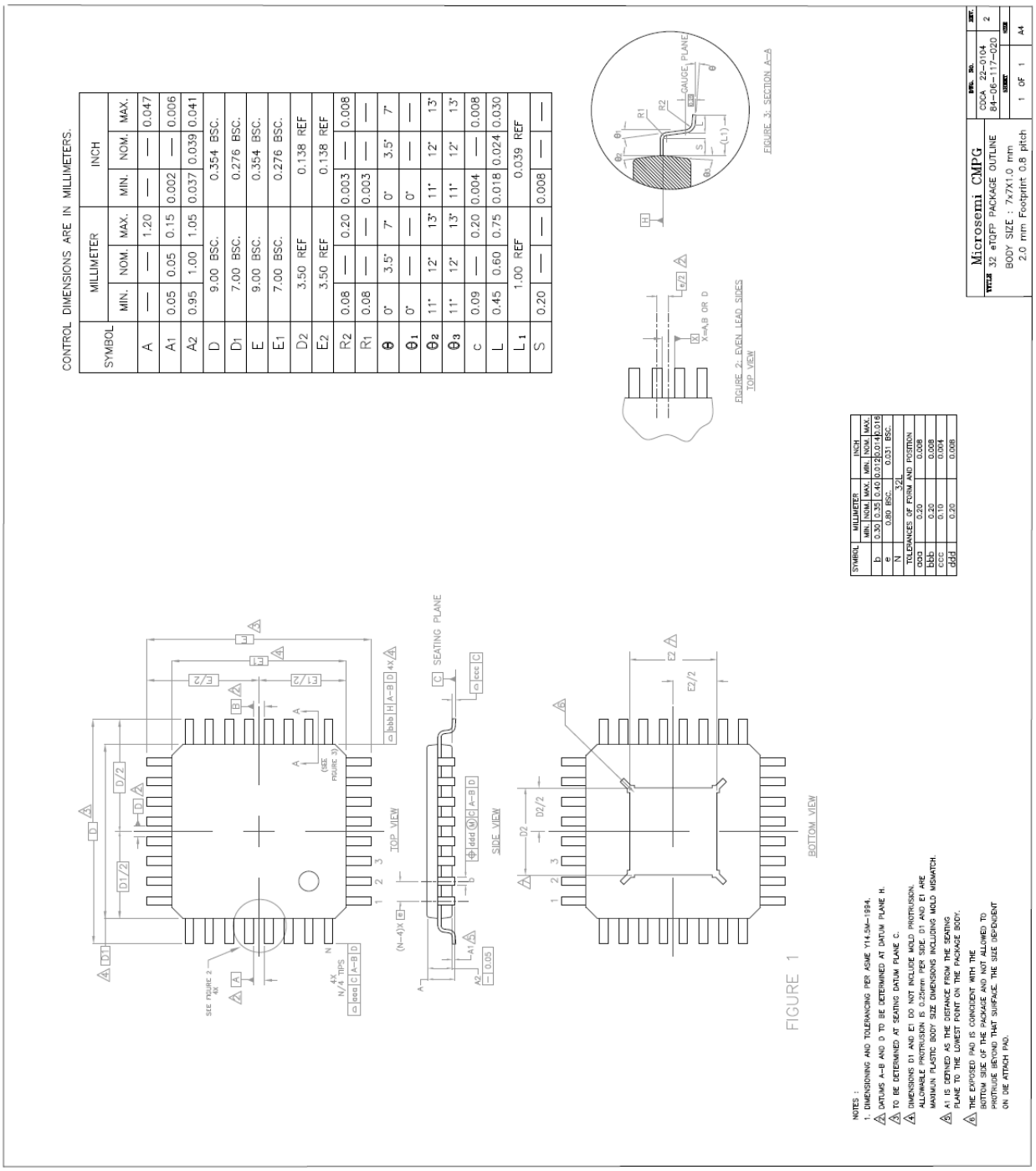
Parameter	Symbol	Conditions	Value	Units
Maximum Ambient Temperature	T_A		85	°C
Maximum Junction Temperature	T_{JMAX}		125	°C
Junction to Ambient Thermal Resistance	θ_{JA}	still air	25.2	°C/W
		1m/s airflow	20.6	
		2.5m/s airflow	18.8	
Junction to Board Thermal Resistance	θ_{JB}		10.9	°C/W
Junction to Case Thermal Resistance	θ_{JC}		18.9	°C/W
Junction to Pad Thermal Resistance	θ_{JP}	Still air	6.5	°C/W
Junction to Top-Center Thermal Characterization Parameter	Ψ_{JT}	Still air	0.6	°C/W

Table 9 7x7mm eTQFP Package Thermal Properties

Parameter	Symbol	Conditions	Value	Units
Maximum Ambient Temperature	T_A		85	°C
Maximum Junction Temperature	T_{JMAX}		125	°C
Junction to Ambient Thermal Resistance	θ_{JA}	still air	17.6	°C/W
		1m/s airflow	11.6	
		2.5m/s airflow	10.2	
Junction to Board Thermal Resistance	θ_{JB}		6.9	°C/W
Junction to Case Thermal Resistance	θ_{JC}		13.6	°C/W
Junction to Pad Thermal Resistance	θ_{JP}	Still air	4.5	°C/W
Junction to Top-Center Thermal Characterization Parameter	Ψ_{JT}	Still air	0.6	°C/W

QFN and eTQFP Package Outline




CONTROL DIMENSIONS ARE IN MILLIMETERS.
SYMBOL | MILLIMETER MIN. NOM. MAX. | INCH MIN. NOM. MAX.
A — — 1.20 — — 0.047
A1 0.05 0.05 0.15 0.002 — 0.006
A2 0.95 1.00 1.05 0.037 0.039 0.041
D 9.00 BSC. 0.354 BSC.
D1 7.00 BSC. 0.276 BSC.
E 9.00 BSC. 0.354 BSC.
E1 7.00 BSC. 0.276 BSC.
D2 3.50 REF 0.138 REF
E2 3.50 REF 0.138 REF
R2 0.08 — 0.20 0.003 — 0.008
R1 0.08 — — 0.003 — —
θ 0° 3.5° 7° 0° 3.5° 7°
θ1 0° — — 0° — —
θ2 11° 12° 13° 11° 12° 13°
θ3 11° 12° 13° 11° 12° 13°
c 0.09 — 0.20 0.004 — 0.008
L 0.45 0.60 0.75 0.018 0.024 0.030
L1 1.00 REF 0.039 REF
S 0.20 — — 0.008 — —
FIGURE 1
FIGURE 2: EVEN LEAD SIDES
FIGURE 3: SECTION A–A
SYMBOL | MILLIMETER MIN. NOM. MAX. | INCH MIN. NOM. MAX.
b 0.30 0.35 0.40 0.012 0.014 0.016
e 0.80 BSC. 0.031 BSC.
N 32L
TOLERANCES OF FORM AND POSITION
aaa 0.20 0.008
bbb 0.20 0.008
ccc 0.10 0.004
ddd 0.20 0.008
NOTES :
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
2 DATUMS A–B AND D TO BE DETERMINED AT DATUM PLANE H.
3 TO BE DETERMINED AT SEATING DATUM PLANE C.
4 DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
5 A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
6 THE EXPOSED PAD IS CONCIDENT WITH THE BOTTOM SIDE OF THE PACKAGE AND NOT ALLOWED TO PROTRUDE BEYOND THAT SURFACE. THE SIZE DEPENDENT ON DIE ATTACH PAD.
Microsemi CMPG
32 eTQFP PACKAGE OUTLINE
BODY SIZE : 7x7X1.0 mm
2.0 mm Footprint 0.8 pitch
CDCA 22-0104
84-06-117-020
1 OF 1
A4

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