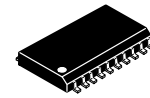


Inverting Octal 3-STATE Buffer, Octal 3-STATE Buffer

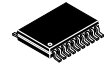
MM74HCT240, MM74HCT244



SOIC-20 WB
CASE 751D-05



TSSOP-20 WB
CASE 948E



TSSOP-20
CASE 948AQ

General Description

The MM74HCT240 and MM74HCT244 3-STATE buffers utilize advanced silicon-gate CMOS technology and are general purpose high speed inverting and non-inverting buffers. They possess high drive current outputs which enable high speed operation even when driving large bus capacitances. These circuits achieve speeds comparable to low power Schottky devices, while retaining the low power consumption of CMOS. All three devices are TTL input compatible and have a fanout of 15 LS-TTL equivalent inputs.

MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug-in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

The MM74HCT240 is an inverting buffer and the MM74HCT244 is a non-inverting buffer. Each device has two active low enables (1G and 2G), and each enable independently controls 4 buffers.

All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- TTL Input Compatible
- Typical Propagation Delay: 14 ns
- 3-STATE Outputs for Connection to System Buses
- Low Quiescent Supply Current: 160 μA
- High Output Drive Current: 6 mA (min)
- These are Pb-Free Devices

TRUTH TABLES

MM74HCT240

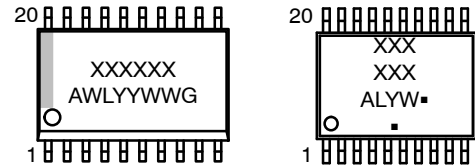
1G	1A	1Y	2G	2A	2Y
L	L	H	L	L	H
L	H	L	L	H	L
H	L	Z	H	L	Z
H	H	Z	H	H	Z

MM74HCT244

1G	1A	1Y	2G	2A	2Y
L	L	L	L	L	L
L	H	H	L	H	H
H	L	Z	H	L	Z
H	H	Z	H	H	Z

NOTES: H = HIGH Level
L = LOW Level
Z = High Impedance

MARKING DIAGRAMS

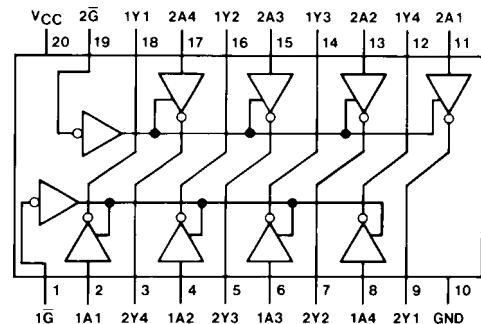


- XXXXXX = Specific Device Code
- A = Assembly Location
- L/WL = Wafer Lot
- Y/YY = Year
- W/WW = Work Week
- or G = Pb-Free Package

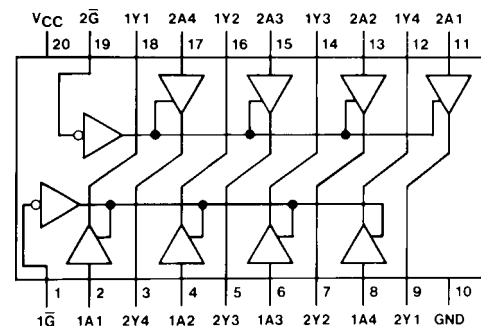
(Note: Microdot may be in either location)

CONNECTION DIAGRAMS

Pin Assignment for SOIC and TSSOP



MM74HCT240 (Top View)



MM74HCT244 (Top View)

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

MM74HCT240, MM74HCT244

Logic Diagrams

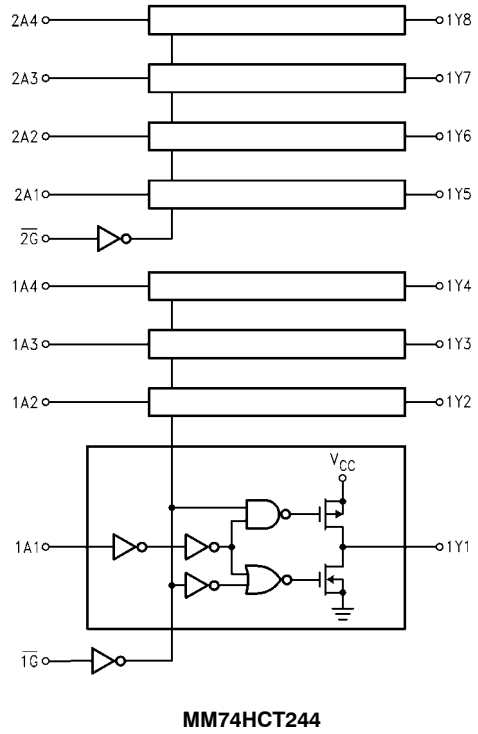
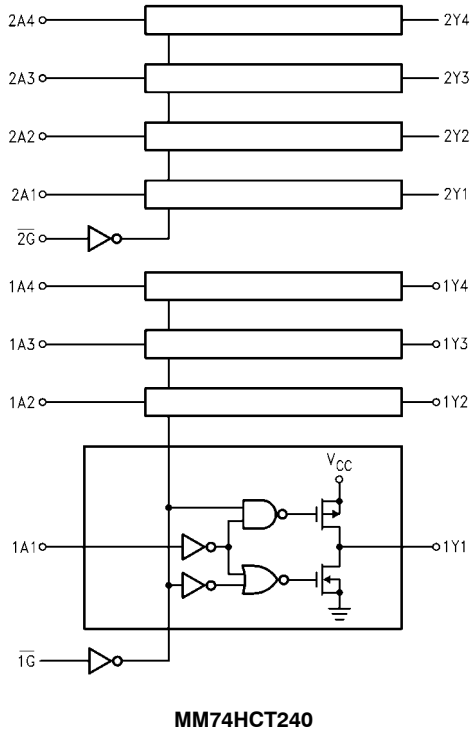


Figure 1. Logic Diagrams

MM74HCT240, MM74HCT244

ABSOLUTE MAXIMUM RATINGS (Note 1)

Symbol	Parameter	Value	Unit
V _{CC}	Supply Voltage	-0.5 to +7.0	V
V _{IN}	DC Input Voltage	-0.5 to V _{CC} + 0.5	V
V _{OUT}	DC Output Voltage	-0.5 to V _{CC} + 0.5	V
I _{IK} , I _{OK}	Clamp Diode Current	±20	mA
I _{OUT}	DC Output Current, per Pin	±35	mA
I _{CC}	DC V _{CC} or GND Current, per Pin	±70	mA
T _{STG}	Storage Temperature Range	-65 to +150	°C
P _D	Power Dissipation S. O. Package Only	500	mW
T _L	Lead Temperature (Soldering 10 seconds)	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Unless otherwise specified all voltages are referenced to ground.

RECOMMENDED OPERATING CONDITIONS (Note 1)

Symbol	Parameter	Min	Max	Unit
V _{CC}	Supply Voltage	4.5	5.5	V
V _{IN} , V _{OUT}	DC Input or Output Voltage	0	V _{CC}	V
T _A	Operating Temperature Range	-55	+125	°C
t _r , t _f	Input Rise or Fall Times	-	500	ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V ±10% unless otherwise specified)

Symbol	Parameter	Conditions	T _A = 25°C		T _A = -40°C to 85°C	T _A = -55°C to 125°C	Unit
			Typ	Guaranteed Limits			
V _{IH}	Minimum HIGH Level Input Voltage		-	2.0	2.0	2.0	V
V _{IL}	Maximum LOW Level Input Voltage		-	0.8	0.8	0.8	V
V _{OH}	Minimum HIGH Level Output Voltage	V _{IN-EE} = V _{IH} or V _{IL} I _{OUT} = 20 μA I _{OUT} = 6.0 mA, V _{CC} = 4.5 V I _{OUT} = 7.2 mA, V _{CC} = 5.5 V	V _{CC} 4.2 5.2	V _{CC} -0.1 3.98 4.98	V _{CC} -0.1 3.84 4.84	V _{CC} -0.1 3.7 4.7	V
V _{OL}	Maximum LOW Level Output Voltage	V _{IN} = V _{IH} or V _{IL} I _{OUT} = 20 μA I _{OUT} = 6.0 mA, V _{CC} = 4.5 V I _{OUT} = 7.2 mA, V _{CC} = 5.5 V	0 0.2 0.2	0.1 0.26 0.26	0.1 0.33 0.33	0.1 0.4 0.4	V
I _{IN}	Maximum Input Current	V _{IN} = V _{CC} or GND, V _{IH} or V _{IL}	-	±0.05	±0.5	±1.0	μA
I _{OZ}	Maximum 3-STATE Output Leakage Current	V _{OUT} = V _{CC} or GND G = V _{IH} G = V _{IL}	-	±0.25	±2.5	±10	μA
I _{CC}	Maximum Quiescent Supply Current	V _{IN} = V _{CC} or GND I _{OUT} = 0 μA	-	4.0	40	160	μA
		V _{IN} = 2.4 V or 0.5 V (Note 2)	0.6	1.0	1.3	1.5	mA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Measured per input. All other inputs at V_{CC} or GND.

MM74HCT240, MM74HCT244

AC ELECTRICAL CHARACTERISTICS

(MM74HCT240, MM74HCT244 $V_{CC} = 5.0\text{ V}$, $t_r = t_f = 6\text{ ns}$, $T_A = 25^\circ\text{C}$, unless otherwise specified)

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Unit
t_{PHL} , t_{PLH}	Maximum Output Propagation Delay	$C_L = 45\text{ pF}$	14	18	ns
t_{PZL} , t_{PZH}	Maximum Output Enable Time	$C_L = 45\text{ pF}$, $R_L = 1\text{ k}\Omega$	20	30	ns
t_{PLZ} , t_{PHZ}	Maximum Output Disable Time	$C_L = 5\text{ pF}$, $R_L = 1\text{ k}\Omega$	16	25	ns

AC ELECTRICAL CHARACTERISTICS

(MM74HCT240, MM74HCT244 $V_{CC} = 5.0\text{ V} \pm 10\%$, $t_r = t_f = 6\text{ ns}$, unless otherwise specified)

Symbol	Parameter	Conditions	$T_A = 25^\circ\text{C}$		$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	$T_A = -55^\circ\text{C to } 125^\circ\text{C}$	Unit
			Typ	Guaranteed Limits			
t_{PHL} , t_{PLH}	Maximum Output Propagation Delay	$C_L = 50\text{ pF}$	14	20	25	30	ns
		$C_L = 150\text{ pF}$	20	28	35	42	
t_{PZH} , t_{PZL}	Maximum Output Enable Time	$R_L = 1\text{ k}\Omega$, $C_L = 50\text{ pF}$	21	30	38	45	ns
		$R_L = 1\text{ k}\Omega$, $C_L = 150\text{ pF}$	26	42	53	63	ns
t_{PHZ} , t_{PLZ}	Maximum Output Disable Time	$R_L = 1\text{ k}\Omega$ $C_L = 50\text{ pF}$	16	25	32	38	ns
t_{THL} , t_{TLH}	Maximum Output Rise and Fall Time	$C_L = 50\text{ pF}$	6	12	15	18	ns
C_{IN}	Maximum Input Capacitance		10	15	15	15	pF
C_{OUT}	Maximum Output Capacitance		15	20	20	20	pF
C_{PD}	Power Dissipation Capacitance (Note 3)	(per buffer) $\bar{G} = V_{CC}$, $G = \text{GND}$	5	-	-	-	pF
		$\bar{G} = \text{GND}$, $G = V_{CC}$	90	-	-	-	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} \cdot V_{CC}^2 \cdot f + I_{CC} \cdot V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} \cdot V_{CC} \cdot f + I_{CC}$.

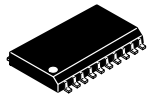
MM74HCT240, MM74HCT244

ORDERING INFORMATION

Device	Package	Shipping [†]
MM74HCT240MTCX	TSSOP-20, case 948AQ (Pb-Free)	2500 Units / Tape & Reel
MM74HCT244MTC	TSSOP-20 WB, case 948E (Pb-Free)	75 Units / Tube
MM74HCT244MTCX	TSSOP-20, case 948AQ (Pb-Free)	2500 Units / Tape & Reel
MM74HCT244WM	SOIC-20 WB, case 751D-05 (Pb-Free)	38 Units / Tube
MM74HCT244WMX	SOIC-20 WB, case 751D-05 (Pb-Free)	1000 Units / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

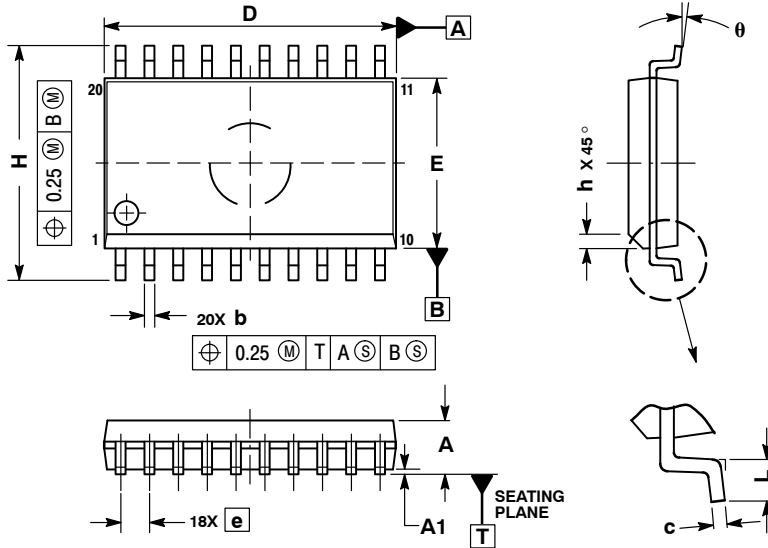
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-20 WB
CASE 751D-05
ISSUE H

DATE 22 APR 2015

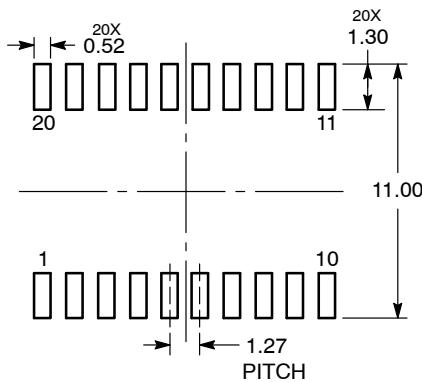


NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
b	0.35	0.49
c	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

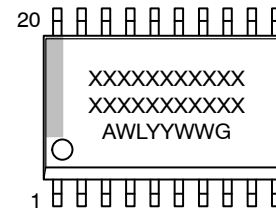
RECOMMENDED
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*



- XXXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- YY = Year
- WW = Work Week
- G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

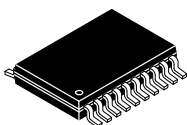
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MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

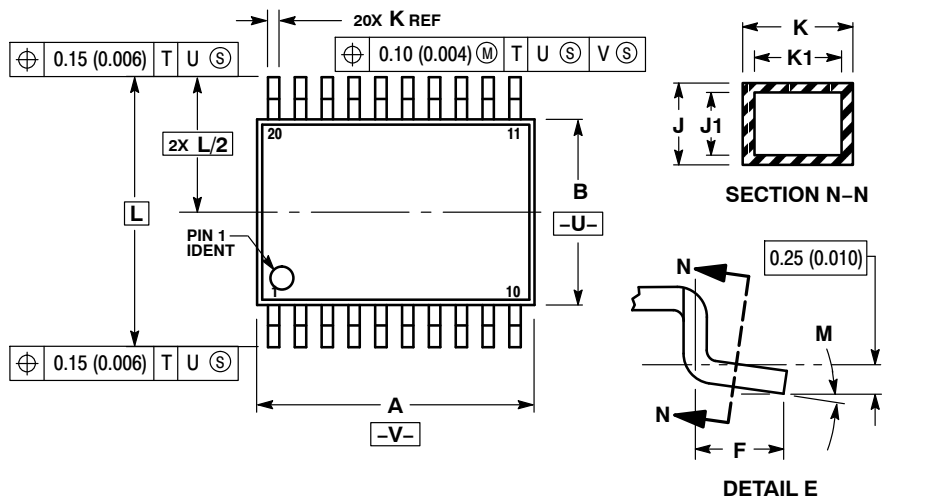
ON Semiconductor®



TSSOP-20 WB
CASE 948E
ISSUE D

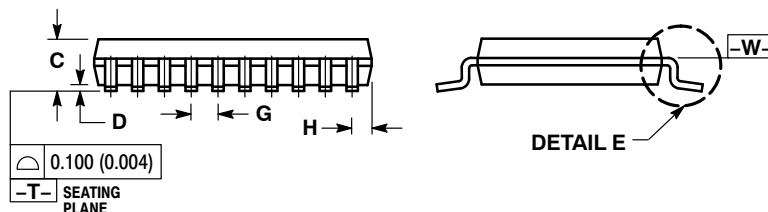
DATE 17 FEB 2016

SCALE 2:1

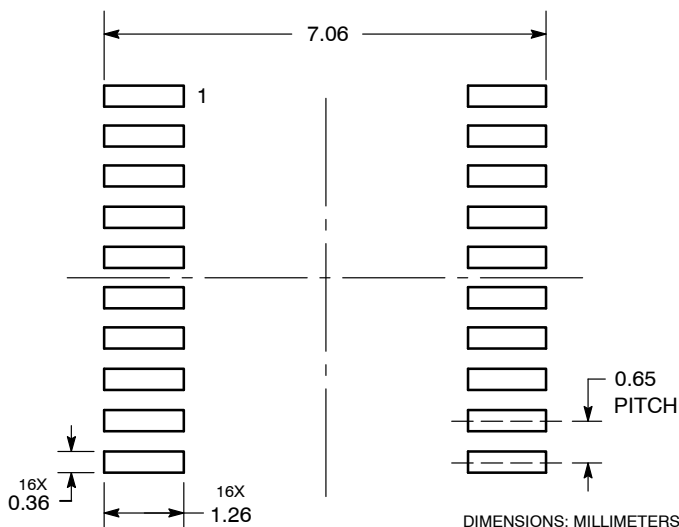


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
 4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
 5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
 6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
 7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

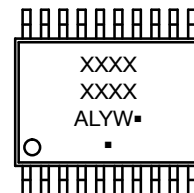
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°



SOLDERING FOOTPRINT



GENERIC MARKING DIAGRAM*



- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

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MECHANICAL CASE OUTLINE

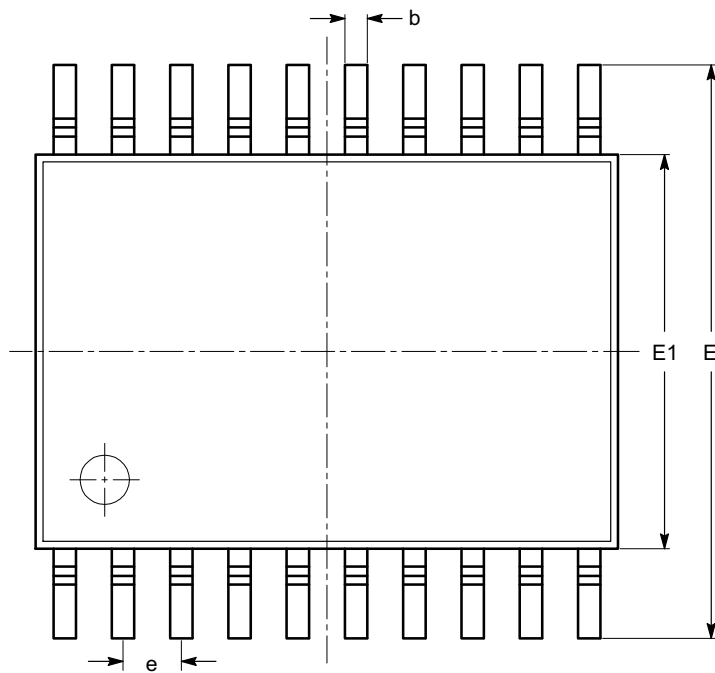
PACKAGE DIMENSIONS

ON Semiconductor®



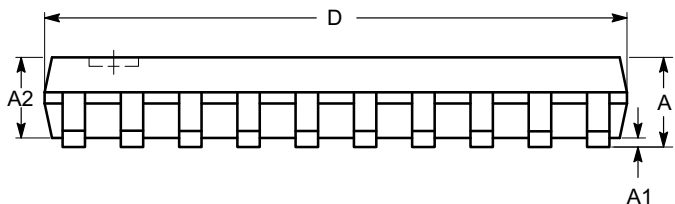
TSSOP20, 4.4x6.5
CASE 948AQ-01
ISSUE A

DATE 19 MAR 2009

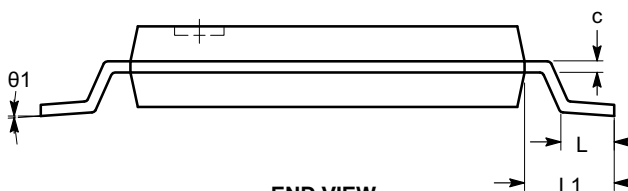


SYMBOL	MIN	NOM	MAX
A			1.20
A1	0.05		0.15
A2	0.80		1.05
b	0.19		0.30
c	0.09		0.20
D	6.40	6.50	6.60
E	6.30	6.40	6.50
E1	4.30	4.40	4.50
e	0.65 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°		8°

TOP VIEW



SIDE VIEW



END VIEW

Notes:

- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC MO-153.

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