ACS8526 LC/P LITE

Line Card Protection Switch for PDH, SONET or SDH Systems

ADVANCED COMMUNICATIONS **FINAL** **DATASHEET**

Description

The ACS8526 is a highly integrated single-chip solution for protection switching between two SECs (SDH/SONET Equipment Clocks) from Master and Slave SETS clock cards, for line cards in a PDH, SONET or SDH Network Element. The ACS8526 has fast activity monitors on the inputs and will raise a flag on a pin if there is a loss of activity on the currently selected input. The protection switching between the input reference clock sources is controlled by an external pin.

The ACS8526 has two SEC reference clock input ports, configured for expected frequency by setting hardware pins or by writing to registers via the serial interface.

The ACS8526 can perform frequency translation, converting, for example, an 8 kHz SEC input clock from a backplane into a 155.52 MHz clock for local line cards.

The ACS8526 generates two independent SEC clock outputs, one on a PECL/LVDS port and one on a TTL/CMOS port, at spot frequencies configured by hardware pins, or by writing to registers via the serial interface. The hardware selectable spot frequencies range from 1.544 MHz up to 155.52 MHz, with further options for N x E1/DS1 and 311.04 MHz via register selection. The ACS8526 also provides an 8 kHz Frame Sync output and 2 kHz Multi-Frame Sync output, both with programmable pulse width and polarity.

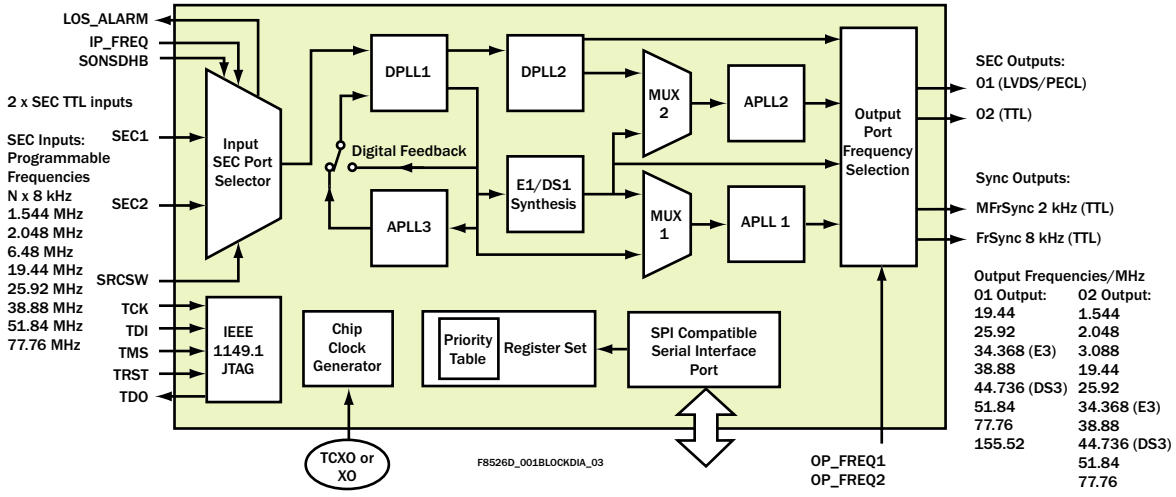
Advanced configuration possibilities are available via the serial port (which can be SPI compatible), however the basic configuration of I/O frequencies and SONET/SDH selection by hardware make the device suitable for standalone operation, i.e., no need for a microprocessor.

Features

- Line card protection switch - partners Semtech SETS devices for Stratum 3E/3/4E/4 PDH, SONET or SDH applications
- High performance DPLL/APLL solution
- Output jitter compliant to STM-1
- Two independent SEC inputs ports (TTL)
- Four independent output ports:
  - Two clock ports: one PECL/LVDS, one TTL
  - Two Syncs (TTL): 8 kHz FrSync & 2 KHz MFrSync
- TTL I/O ports: spot frequencies 2 kHz to 77.76 MHz
- PECL/LVDS port: spot frequencies 2 kHz to 311 MHz
- N x E1/DS1 mode
- Programmable pulse width and polarity on Syncs
- SONET/SDH frequency translation
- Digital Holdover mode on input failure
- Separate activity monitors and register alarms on each input.
- “Loss of activity” on selected input flagged on dedicated pin
- Source switch under external hardware control
- PLL “Locked” and “Acquisition” bandwidth selectable from 18, 35 or 70 Hz
- Configurable via serial interface or hardware pins
- Output clock phase continuity to GR-1244-CORE[13]
- Single 3.3 V operation, 5 V I/O compatible
- IEEE 1149.1 JTAG Boundary Scan is supported
- Operating temperature (ambient) of -40 to +85 °C
- Available in LQFP 64 package
- Lead (Pb)-free version available (ACS8526T), RoHS and WEEE compliant.

Block Diagram

Figure 1 Block Diagram of the ACS8526 LC/P LITE



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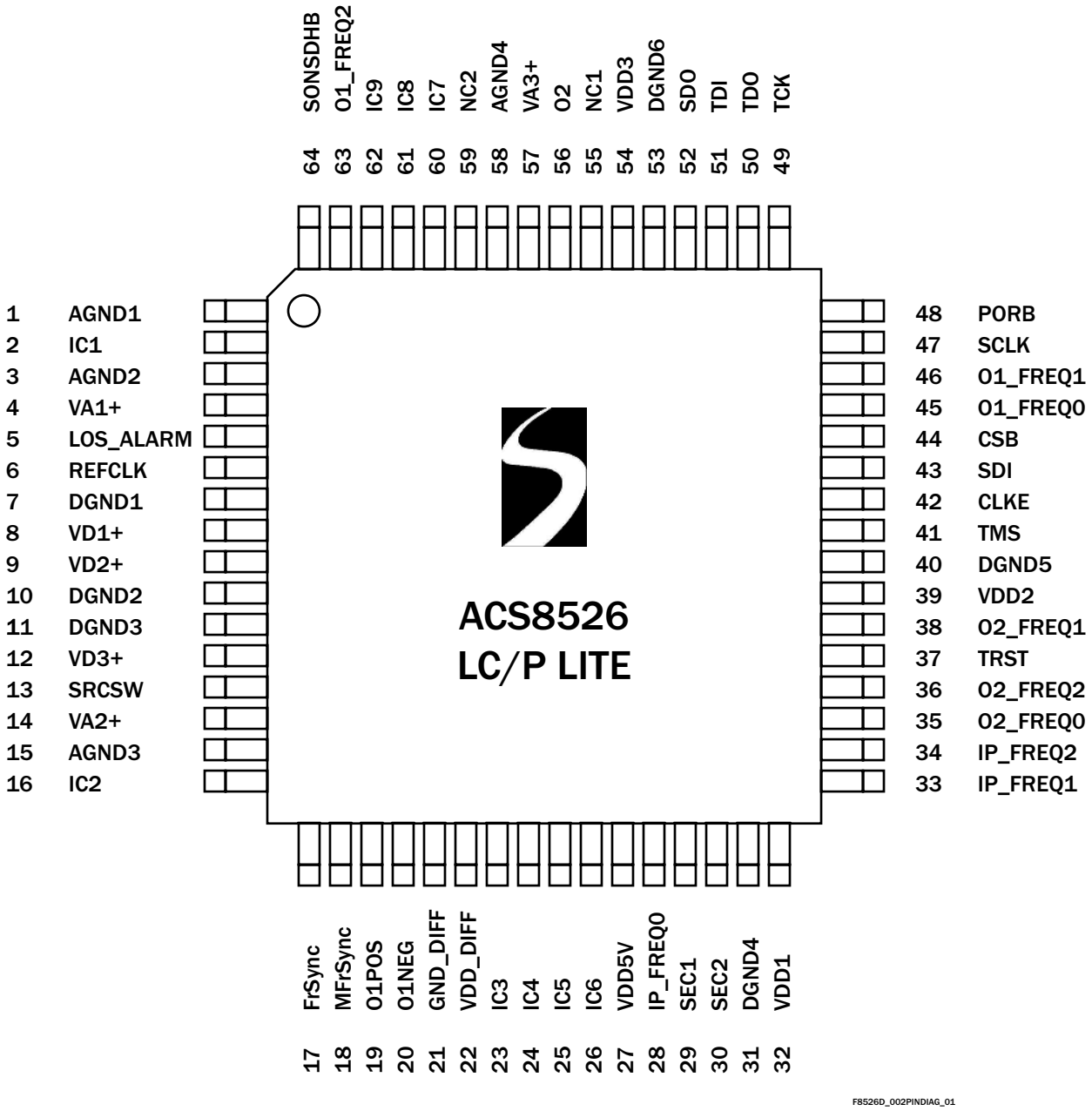


Pin Description

Table 1 Power Pins

Pin Number	Symbol	I/O	Type	Description
8, 9, 12	VD1+, VD2+, VD3+	P	-	Supply Voltage: Digital supply to gates in analog section, +3.3 Volts ±10%.
22	VDD_DIFF	P	-	Supply Voltage: Digital supply for differential output pins 19 and 20, +3.3 Volts ±10%.
27	VDD5V	P	-	Digital Supply for +5 Volts tolerance to input pins. Connect to +5 Volts (±10%) for clamping to +5 Volts. Connect to VDD for clamping to +3.3 Volts. Leave floating for no clamping, input pins tolerant up to +5.5 Volts.
32, 39, 54	VDD1, VDD2, VDD3,	P	-	Supply Voltage: Digital supply to logic, +3.3 Volts ±10%.
4	VA1+	P	-	Supply Voltage: Analog supply to clock multiplying PLL, +3.3 Volts ±10%.
14, 57	VA2+, VA3+	P	-	Supply Voltage: Analog supply to output PLLs APLL2 and APLL1, +3.3 Volts ±10%.
15, 58	AGND3, AGND4		-	Supply Ground: Analog ground for output PLLs APLL2 and APLL1.
7, 10, 11	DGND1, DGND2, DGND3	P	-	Supply Ground: Digital ground for components in PLLs.
31, 40, 53	DGND4, DGND5, DGND6	P	-	Supply Ground: Digital ground for logic.
21	GND_DIFF	P	-	Supply Ground: Digital ground for differential output pins 19 and 20.
1, 3	AGND1, AGND2	P	-	Supply Ground: Analog grounds.

Note...I = Input, O = Output, P = Power, TTL^U = TTL input with pull-up resistor, TTL_D = TTL input with pull-down resistor.

Table 2 Internally Connected

Pin Number	Symbol	I/O	Type	Description
2, 16, 23, 24, 25, 26, 60, 61, 62	IC1, IC2, IC3, IC4, IC5, IC6, IC7, IC8 IC9	-	-	Internally Connected: Leave to float.
55, 59	NC1, NC2	-	-	Not Connected: Leave to float.

Table 3 Other Pins

Pin Number	Symbol	I/O	Type	Description
5	LOS_ALARM	O	TTL/CMOS	LOS_Alarm: Flag to indicate loss of activity of currently selected reference source.
6	REFCLK	I	TTL	Reference Clock: 12.800 MHz (refer to section headed Local Oscillator Clock).
13	SRCSW	I	TTL_D	Source Switching: Controls switchover between SEC1 and SEC2 inputs as the selected reference. SRCSW must be held *High* on power-up or reset, and for a further 251 ms after PORB has gone *High*. See “Initialization” on page 8.
17	FrSync	O	TTL/CMOS	Output Reference: 8 kHz Frame Sync output.

Table 3 Other Pins (cont...)

Pin Number	Symbol	I/O	Type	Description
18	MFrSync	O	TTL/CMOS	Output Reference: 2 kHz Multi-Frame Sync output.
19, 20	O1POS, O1NEG	O	LVDS/PECL	Output Reference 1: Differential output., default LVDS.
28	IP_FREQ0	I	TTL_D	Input Reference Frequency Select: Frequency select for input SEC1 and SEC2.
29	SEC1	I	TTL_D	Input Reference 1: Primary input.
30	SEC2	I	TTL_D	Input Reference 2: Secondary input.
33	IP_FREQ1	I	TTL_D	Input Reference Frequency Select: Frequency select for input SEC1 and SEC2.
34	IP_FREQ2	I	TTL_D	Input Reference Frequency Select: Frequency select for input SEC1 and SEC2.
35	O2_FREQ0	I	TTL_D	Output O2 Frequency Select: Frequency select for output O2.
36	O2_FREQ2	I	TTL_D	Output O2 Frequency Select: Frequency select for output O2.
37	TRST	I	TTL_D	JTAG Control Reset Input: TRST = 1 to enable JTAG Boundary Scan mode. TRST = 0 for normal device operation (JTAG logic transparent). NC if not used.
38	O2_FREQ1	I	TTL_D	Output O2 Frequency Select: Frequency select for output O2.
41	TMS	I	TTL_D	JTAG Test Mode Select: Boundary Scan enable. Sampled on rising edge of TCK. NC if not used.
42	CLKE	I	TTL_D	SCLK Edge Select: SCLK active edge select, CLKE = 1, selects falling edge of SCLK to be active.
43	SDI	I	TTL_D	Interface Address: SPI compatible Serial Data Input.
44	CSB	I	TTL^U	Chip Select (Active *Low*): This pin is asserted *Low* by the external device (microprocessor) to enable the Serial interface.
45	O1_FREQ0	I	TTL^U	Output O1 Frequency Select: Frequency select for output O1.
46	O1_FREQ1	I	TTL^U	Output O1 Frequency Select: Frequency select for output O1.
47	SCLK	I	TTL_D	Serial Data Clock: The *Low* to *High* transition on this input latches the data on the SDI input into the internal registers. The active clock edge (defined by CLKE) latches the data out of the internal registers onto the SDO output.
48	PORB	I	TTL^U	Power-On Reset: Master reset. If PORB is forced *Low*, all internal states are reset back to default values.
49	TCK	I	TTL_D	JTAG Clock: Boundary Scan clock input.
50	TDO	O	TTL/CMOS	JTAG Output: Serial test data output. Updated on falling edge of TCK.
51	TDI	I	TTL_D	JTAG Input: Serial test data Input. Sampled on rising edge of TCK. NC if not used.
52	SDO	O	TTL_D	Interface Address: SPI compatible Serial Data Output.
56	O2	O	TTL/CMOS	Output Reference: Programmable, default 19.44 MHz.
63	O1_FREQ2	I	TTL^U	Output O1 Frequency Select: Frequency select for output O1.
64	SONSDHB	I	TTL_D	SONET or SDH frequency select: Sets the initial power-up state (or state after a PORB) of the SONET/SDH frequency selection registers, Reg. 34, Bit 2 and Reg. 38, Bit 5, Bit 6 and Reg. 64 Bit 4. The register states can be changed after power-up by software. When set *Low*, SDH rates are selected (2.048 MHz etc.) and when set *High*, SONET rates are selected (1.544 MHz etc.) The register states can be changed after power-up by software.

Introduction

The ACS8526 is a highly integrated, single-chip solution for protection switching of two SEC inputs from, for example, Master and Slave SETS clock cards sources, for Line Cards in a SONET or SDH Network Element. The ACS8526 has fast activity monitors on the SEC clock inputs.

The ACS8526 can be used as a standalone part without the serial interface where all input and output frequencies are set by external control using the IP_FREQ and OP_FREQ pins. These pins determine the default power-up or reset state of internal registers, that in turn determine the I/O frequencies.

If more detailed control is required, then the registers within the device can be re-configured, after an initialization period, by writes through the serial interface. The SRCSW pin is used to select one of the two SEC inputs to lock to. The SRCSW pin must remain *High* for at least 251 ms following power-up or reset (251 ms after the PORB signal has gone *High*). SRCSW *Low* following a power-up or reset is not supported.

The ACS8526 has two SEC inputs from which it can generate independent clocks on outputs 01 and 02 with a total of 53 possible output frequencies. In addition, there are two Sync outputs; 8 kHz Frame Synchronization (FrSync) signal and a 2 kHz Multi-Frame Synchronization (MFrSync) signal.

Initially the ACS8526 generates a stable, low-noise clock signal at a frequency to the same accuracy as the external oscillator, or it can be made more accurate via software calibration to within ±0.02 ppm. The device always attempts to lock to one of its inputs (according to the value on the SRCSW pin). Once locked to a reference the accuracy of the output clock is determined directly by the accuracy of the input reference. In the absence of any input references the device simply maintains its most recent frequency in a Digital Holdover mode. However, as soon as the DPLL detects an input presence, it will attempt to lock to it and will not “qualify” it first. As soon as the DPLL detects a failure on the input, the DPLL freezes its operating frequency and raises the LOS alarm on device pin LOS_ALARM.

The overall PLL loop bandwidth, damping, pull-in range and frequency accuracy are all determined by digital parameters that provide a consistent level of performance. An Analog PLL (APLL) takes the signal from the DPLL output and provides a lower jitter output. The APLL bandwidth is set four orders of magnitude higher than the DPLL bandwidth. This ensures that the overall system performance still maintains the advantage of consistent behavior provided by the digital approach. The DPLLs are clocked by the external oscillator module (TCXO or XO) so that prior to initial lock (with no input reference) or in Digital Holdover, the frequency stability is only determined by the stability of the external oscillator module. This gives the key advantage of confining all temperature critical components to one well defined and pre-calibrated oscillator module, whose performance can be chosen to match the application. All performance parameters of the DPLLs are programmable without the need to understand detailed PLL equations. Bandwidth, damping factor and lock range can all be configured under software control.

The hardware set-up configures a subset of the registers in the register block, with the remainder adopting their default settings. If hardware set-up alone is insufficient for configuring, controlling and monitoring the device for a particular application, then access to the full set of registers for these purposes is provided by an SPI compatible serial interface port.

Each register (8-bit wide data field) is identified by and referred to by its hexadecimal address and name, e.g. Reg. 7D *cnfg_LOS_alarm*. The “Register Map” on page 30 summarizes the content of all of the registers, and each register is individually described in the subsequent Register Tables, organized in order of ascending Address (hexadecimal), in the “Register Descriptions” from page 32 onwards.

An Evaluation board and intuitive GUI-based software package is available for device introduction. This has its own documentation “ACS8526-EVB”.

General Description

The following description refers to the Block Diagram (Figure 1 on page 1).

Inputs

The ACS8526 SETS device has two TTL/CMOS compatible SEC input ports. They are 3 V and 5 V compatible (with clamping if required by connecting the VDD5V pin). Refer to the “Electrical Specifications” on page 61 for more information on electrical compatibility.

Input frequencies supported range from 2 kHz to 155.52 MHz. Common E1, DS1, OC-3 and sub-divisions are supported as spot frequencies that the DPLLs will directly lock to. Any input frequency, up to 100 MHz, that is a multiple of 8 kHz can also be locked to via an inbuilt programmable divider.

In addition to the SEC inputs, there are four configuration pins IP_FREQ [2:0] and SONSDHB used to configure the input to expect a particular input frequency (same value applies to both inputs), and a control pin SRCSW for switching between SEC1 and SEC2 as the selected input reference to which the device tries to lock.

Preconfiguring Inputs - Expected Input Frequency

The inputs SEC1 and SEC2 must be preconfigured to expect a particular input frequency.

The expected input frequencies can be selected from a range of spot frequencies by either:

- Hardware selection: configuring the hardware pins IP_FREQ [2:0] and SONSDHB, which are read on reset
- Register programming: writing to the *cnfg_ref_source_frequency* and *cnfg_input_mode* registers.

Hardware Selection of Expected I/P Frequency

The combined pin states of IP_FREQ [2:0] and SONSDHB represent a 4-bit word which addresses a particular frequency value as given in Table 4.

The frequency selected by the hardware configuration is always applied to both inputs on Power-up or Reset, so both will be preconfigured to expect the same frequency. If SEC1 and SEC2 are required to expect different frequencies, then these inputs must be subsequently reconfigured by programming the appropriate registers.

Register Programming of Expected I/P Frequency

The expected input frequencies can be programmed by writing to the *cnfg_ref_source_frequency* registers (Reg. 22 and 23) and *ip_sonsdhb* (Bit 2 of *cnfg_input_mode*,Reg. 34), via the serial interface. This must not be done until after the end of the initialization period (see “Initialization” on page 8).

Note...Any subsequent reset will cause these registers to be overwritten by values that equate to the single hardware selected frequency on the pins at the time of reset, i.e both inputs will be configured to expect the same input frequency. After a reset and initialization period, any change of state on IP_FREQ [2:0] or SONSDHB will have no effect on the device configuration, as these are only read during the reset period.

The register programming approach provides a greater range of frequencies than the hardware selection method: more spot frequencies, plus frequencies derived using DivN Mode up to 100 MHz (TTL technology limit).

Table 4 Hardware Configuration for Selecting Expected Input Frequency on SEC1 and SEC2

IP_FREQ Pins			SONSDHB Pin	Input frequency
2	1	0		
0	0	0	X	8 kHz
0	0	1	0	2.048 MHz
			1	1.544 MHz
0	1	0	X	6.48 MHz
0	1	1	X	19.44 MHz
1	0	0	X	25.92 MHz
1	0	1	X	38.88 MHz
1	1	0	X	51.84 MHz
1	1	1	X	77.76 MHz

Preconfiguring Inputs- SONET/SDH

The *cnfg_input_mode* register bit *ip_sonsdhb* is used to select SDH or SONET mode for the entire device and its setting affects parameters other than just the expected input frequency selection, e.g. output frequency. To set the device for use in a SONET network, set *ip_sonsdhb* = 1. For SDH, set *ip_sonsdhb* = 0.

Input Locking Frequency Modes

Each input port has to be configured to receive the expected input frequency. To achieve this, three input locking frequency modes are provided: Direct Lock, Lock8K and DivN.

Direct Lock Mode

In Direct Lock mode, DPLL1 can lock to the selected input at the spot frequency of the input, for example 19.44 MHz performs the DPLL phase comparisons at 19.44 MHz.

In Lock8K and DivN modes an internal divider is used prior to DPLL1 to divide the input frequency before it is used for phase comparisons.

Lock8K Mode

Lock8K mode automatically sets the divider parameters to divide the input frequency down to 8 kHz. Lock8K can only be used on the supported spot frequencies. See *divn_SEC1* and *2* descriptions (Bit 7 of Reg. 22 and 23, *cnfg_ref_source_frequency*). Lock8k mode is enabled by setting the *Lock8k* bit (Bit 6) in the appropriate *cnfg_ref_source_frequency* register. Using lower frequencies for phase comparisons in the DPLL results in a greater tolerance to input jitter. It is possible to choose which edge of the input reference clock to lock to, by setting *8K Edge Polarity*, (Bit 2 of Reg. 03, *test_register1*).

DivN Mode

In DivN mode, the divider parameters are set manually by configuration (Bit 7 of the *cnfg_ref_source_frequency* register), but must be set so that the frequency after division is exactly 8 kHz.

The DivN function is defined as:

DivN = "Divide by N+ 1", i.e. it is the dividing factor used for the division of the input frequency, and has a value of (N+1) where N is an integer from 1 to 12499 inclusive.

Therefore, in DivN mode the input frequency can be divided by any integer value between 2 to 12499. Consequently, any input frequency which is a multiple of 8 kHz, between 8 kHz to 125 MHz, can be supported by using DivN mode.

Note...Both reference inputs can be set to use DivN independently of the frequency and configuration of the other input. However only one value of N is allowed, so if both inputs have DivN selected, they must be running at the same frequency.

DivN Examples

(a) To lock to 2.000 MHz:

(i) Set the *cnfg_ref_source_frequency* register to 10XX0000 (binary) to enable DivN, and set the frequency to 8 kHz - the frequency required after division. (XX = "Leaky Bucket" ID for this input).

(ii) To achieve 8 kHz, the 2 MHz input must be divided by 250. So, if DivN = 250 = (N + 1) then N must be set to 249. This is done by writing F9 hex (249 decimal) to the DivN register pair Reg. 46/47.

(b) To lock to 10.000 MHz:

(i) The *cnfg_ref_source_frequency* register is set to 10XX0000 (binary) to set the DivN and the frequency to 8 kHz, the post-division frequency. (XX = "Leaky Bucket" ID for this input).

(ii) To achieve 8 kHz, the 10 MHz input must be divided by 1,250. So, if DivN, = 250 = (N+1) then N must be set to 1,249. This is done by writing 4E1 hex (1,249 decimal) to the DivN register pair Reg. 46/47.

Selection of Input SECs

Initialization

Switching between inputs SEC1 and SEC2 is triggered directly from a dedicated pin (SRCSW), though for the device to operate properly, the device must first be initialized by holding the pin *High* during reset and for at least a further 251 ms after PORB has gone *High* (250 ms allowance for the internal reset to be removed plus 1 ms allowance for APLLs to start-up and become stable). A simple external circuit to set SCRSW high for the required period is shown in the "Simplified Application Schematic" on page 70. If SCRSW is held *Low* at any time during the 251 ms initialization period, this will result in incorrect device operation.

SEC Selection - SRCSW pin

After the ACS8526 has been initialized (see previous "Initialization" section), then the value of SRCSW pin directly selects either SEC1 (SRCSW *High*) or SEC2 (SRCSW *Low*). The default frequency tolerance of SEC1 and SEC2 is ±80 ppm (Reg. 41 and Reg. 42) with respect to the local (calibrated) oscillator clock. These registers can be subsequently set by external software, if required.

After initialization, the output clocks are stable and the device will operate as a simple switch, with the DPLL trying to lock on to the selected reference source.

Output Clock Phase Continuity on Source Switchover

A phase offset between SEC inputs will be seen as a phase shift on the output on source switchover equal to the input phase offset.

Note...The ACS8526 has no Phase Build-out function to accommodate this. If this function is required, it is available on the AS8525 LC/P device.

The rate of change of phase on the output, during the time between input switchover and the output settling to a steady state, is dependent on factors of: input frequency,

input phase change, DPLL bandwidth, DPLL frequency limit, and phase detector capture range. The ACS8526 always complies with GR-1244-CORE[13] spec for Stratum 3 (max rate of phase change of 81 ns/1.326 ms), for input frequencies at 6.48 MHz or higher, with the default 1UI phase detector capture range.

For inputs at a lower frequency than 6.48 MHz (e.g. 8 kHz) with the DPLL frequency limit set to greater than ±30 ppm (note default is ±80 ppm), then to ensure compliance with GR-1244-CORE[13] at DPLL bandwidth settings of 18, 35 or 70 Hz, the input phase difference between the Master and Slave inputs to the line card PLL should be limited to less than 600, 330 ns or 190 ns respectively. Alternatively, the DPLL frequency range should be set <±30 ppm. A well designed system would have Master and Slave clock from the clock sync cards aligned to within a few nanoseconds. In which case a complete system using the Semtech SETS clock card parts (ACS8530, ACS8520 or ACS8510) and this line card part would be fully compliant to GR-1244-CORE[13] specifications under all conditions due to the lower frequency range and bandwidth set at the clock card end.

Activity Monitors

Two types of Activity monitors are incorporated in the ACS8526:

- SEC Activity Monitors, which raise flags in Reg. 11, *sts_reference_sources* for each SEC in event of no input activity, as defined by the configuration of Leaky Bucket accumulator.
- Fast Activity Monitor (part of DPLL), which raises LOS alarm on pin LOS_ALARM in event of two missing cycles of input activity on the selected source.

SEC Activity Monitors

There is a SEC activity monitor assigned to each SEC input. Each has a programmable Leaky Bucket Accumulator which is used to determine at what point the period of inactivity is deemed sufficient to raise or clear an alarm. Each SEC has its own no activity alarm bit in Reg. 11, *sts_reference_sources,*. The monitors operate continuously such that at all times the activity status of each SEC input is known.

Leaky Bucket Accumulator

Anomalies detected by the Activity Monitor are integrated in a Leaky Bucket Accumulator. There is one Leaky Bucket Accumulator per SEC input. The accumulators share a set of configuration parameters which can be programmed via Reg. 50 to Reg. 53. They are:

- Bucket size
- Alarm trigger (set threshold)
- Alarm clear (reset threshold)
- Leak rate (decay rate)

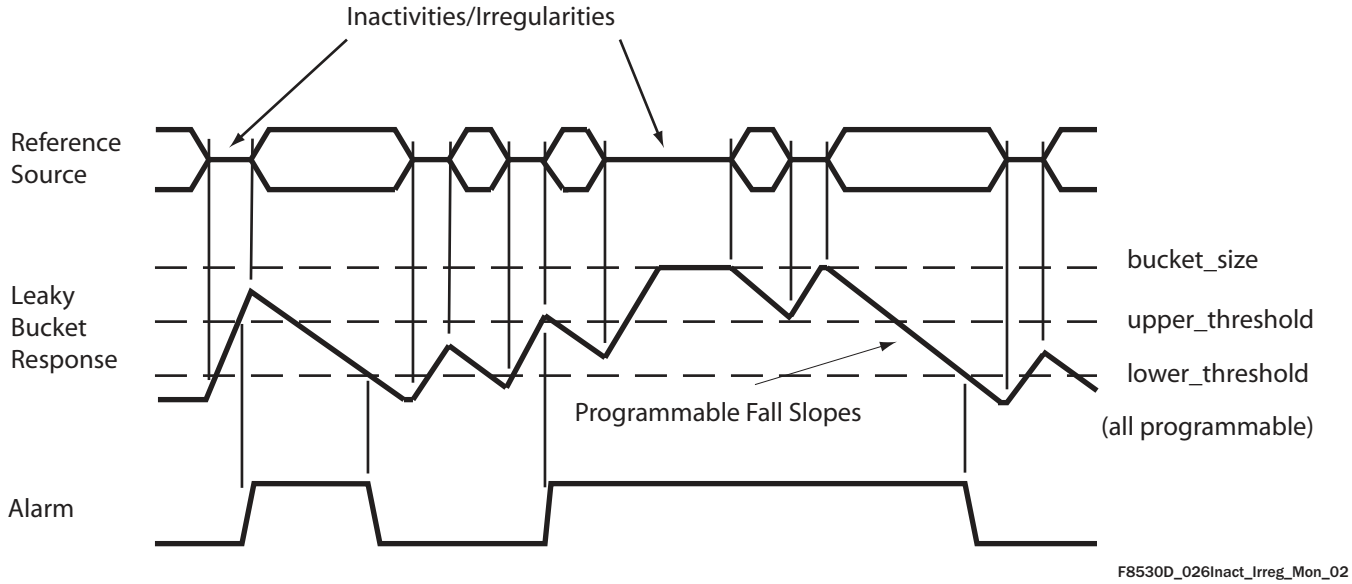
There are occasional anomalies that do not cause the Accumulator to cross the alarm setting threshold, but if the Bucket fills faster than it leaks it will eventually cross the alarm setting threshold and the associated *SEC Input Activity Alarm* bit in Reg. 11, *sts_reference_sources*, will change to 1 (Alarm active).

Each Leaky Bucket Accumulator is a digital circuit which mimics the operation of an analog integrator. If several events occur close together, each event adds to the amplitude and the alarm will be triggered quickly; if events occur over a greater time period but still sufficiently close together to overcome the decay, the alarm will be triggered eventually. If events occur at a rate which is not sufficient to overcome the decay, the alarm will not be triggered. Similarly, if no defect events occur for a sufficient time, the amplitude will decay gradually and the alarm will be cleared when the amplitude falls below the alarm clearing threshold. The ability to decay the amplitude over time allows the importance of defect events to be reduced as time passes by. This means that, in the case of isolated events, the alarm will not be set, whereas, once the alarm becomes set, it will be held on until normal operation has persisted for a suitable time (but if the operation is still erratic, the alarm will remain set). Figure 3 illustrates the behavior of the Leaky Bucket Accumulator.

Each SEC input is monitored over a 128 ms period. If, within a 128 ms period, an irregularity occurs that is not deemed to be due to allowable jitter/wander, then the Accumulator is incremented.

The Accumulator continues to increment up to the point that it reaches the programmed Bucket size. The “fill rate” of the Leaky Bucket is, therefore, 8 units/second. The “leak rate” of the Leaky Bucket is programmable to be in multiples of the fill rate (x 1, x 0.5, x 0.25 and x 0.125) to give a programmable leak rate from 8 units/sec down to 1 unit/sec. A conflict between trying to “leak” at the same time as a “fill” is avoided by preventing a leak when a fill event occurs.

Figure 3 Inactivity and Irregularity Monitoring



Leaky Bucket Timing

The time taken (in seconds) to raise an inactivity alarm on an SEC that has previously been fully active (Leaky Bucket empty) will be:

(cnfg_upper_threshold) / 8

If an input is intermittently inactive then this time can be longer. The default setting of *cnfg_upper_threshold* is 6, therefore the default time is 0.75 s.

The time taken (in seconds) to cancel the activity alarm on a previously completely inactive SEC is calculated, for a particular Leaky Bucket, as:

$[2^{(a)} \times (b - c)]/ 8$

where:

a = cnfg_decay_rate
b = cnfg_bucket_size
c = cnfg_lower_threshold
The default setting is shown in the following:

$[2^1 \times (8 - 4)] /8 = 1.0$ *secs*

Fast Activity Monitor

Anomalies on the selected clock have to be detected as they occur and the PLL must be temporarily isolated until the clock is once again pure. The SEC activity monitor cannot be used for this because the high degree of accuracy required dictates that the process be slow. To achieve the immediacy required, the PLL uses an alternative mechanism. The phase locked loop itself contains an additional fast activity monitor such that within approximately two missing input clock cycles, a no-activity flag is raised and the DPLL is frozen in Digital Holdover mode. This flag generates LOS (Loss of Signal) alarm on pin LOS_ALARM.

With the DPLL in Digital Holdover mode it is isolated from further disturbances. If the input becomes active again then the DPLL will continue to lock to the input, with little disturbance.

Phase Locked Loops (PLLs)

This section is in four parts;

- Overview description of the PLLs
- Architectural description, introducing the sub-blocks and their interconnection options for different frequency selection and jitter filtering
- Description of PLL controls- phase error detector options, Loop bandwidth and damping selection
- DPLL summary feature list.

PLL Overview

The PLL circuitry comprises the following blocks shown in Figure 1: Two Digital PLLs (DPLL1 and DPLL2), two output multiplying and filtering Analog PLLs (APLL1 and APLL2), output frequency dividers in an Output Port Frequency Selection block, a synthesis block, multiplexers MUX1 and MUX2, and a feedback Analog PLL (APLL3).

These functional blocks, and their interconnections, are highly configurable, via register control, which provides a

range of output frequencies and levels of jitter performance. However if the device is configured by hardware alone, then the PLLs are configured as shown in Table 7 and 8.

Digital Synthesis is used to generate all required SONET/SDH output frequencies. The digital logic operates at 204.8 MHz that is multiplied up from the external 12.800 MHz oscillator module. Hence the best resolution of the output signals from the DPLLs is one 204.8 MHz cycle or 4.9 ns.

Additional resolution and lower final output jitter is provided by a de-jittering APLL that reduces the 4.9 ns p-p jitter from the digital down to 500 ps p-p and 60 ps RMS as typical final outputs measured broadband (from 10 Hz to 1 GHz). This arrangement combines the advantages of the flexibility and repeatability of a DPLL with the low jitter of an APLL.

The DPLLs in the ACS8526 are programmable for parameters of bandwidth (18, 35 and 70 Hz) and damping factor (from 1.2 to 20). See Sections “DPLL1 Jitter Transfer Characteristic, (Freq. = 1.544 MHz, Jitter = 0.2 UI p-p, Damping Factor = 5)” on page 14, and “Damping Factor Programmability” on page 15.

DPLL1 input frequency is programmable with 12 common SONET/SDH spot frequencies. See *cnfg_nominal_frequency* Reg. 3C and Reg. 3D

The DPLL has programmable frequency acceptance and output range (from 0 to 80 ppm) set by the allowable offset between the expected input frequency and the calibrated external frequency, Reg. 41 and Reg. 42).

There is no requirement to understand the loop filter equations or detailed gain parameters since all high level factors such as overall bandwidth can be set directly in registers via the microprocessor interface. No external critical components are required for either the internal DPLLs or APLLs, providing another key advantage over traditional discrete designs.

DPLL1 always produces an output at 77.76 MHz to feed the APLL, regardless of the frequency selected at the output pins or the locking frequency (frequency at the input of the Phase and Frequency Detector- PFD).

DPLL2 can be operated at a number of frequencies. This is to enable the generation of extra output frequencies, which cannot be easily related to 77.76 MHz. If DPLL2 is enabled, it locks to the 8 kHz from DPLL1. This is because all of the frequencies of operation of DPLL2 can be divided to 8 kHz and this will ensure synchronization of frequencies, from 8kHz upwards, within the two DPLLs.

Both of the DPLLs’ outputs can be connected to multiplying and filtering APLLs. The outputs of these APLLs are divided making a number of frequencies simultaneously available for selection at the output clock ports. The various combinations of DPLL, APLL and divider configurations allow for generation of a comprehensive set of frequencies, as listed in Table 9, “Output Frequency Selection,” on page 19.

A function is provided to synchronize the lower output frequencies when DPLL1 is locked to a high frequency reference input. The dividers that generate the 2 kHz and 8 kHz outputs are reset such that the output 2/8 kHz clocks are lined up with the input 2 kHz.

The PLL configurations required for particular output frequencies are described in “Output Frequency Selection by Hardware” on page 17, and “Output Frequency Selection by Register Programming” on page 17.

An advanced feature of the device is its ability to control the amount of jitter and wander that is tolerated on the input. This is achieved by the configuration of the Phase and Frequency detectors within the DPLLs, which determines the phase error input to the Digital Loop Filter. For basic operation, the configuration should not be changed from the default settings.

PLL Architecture

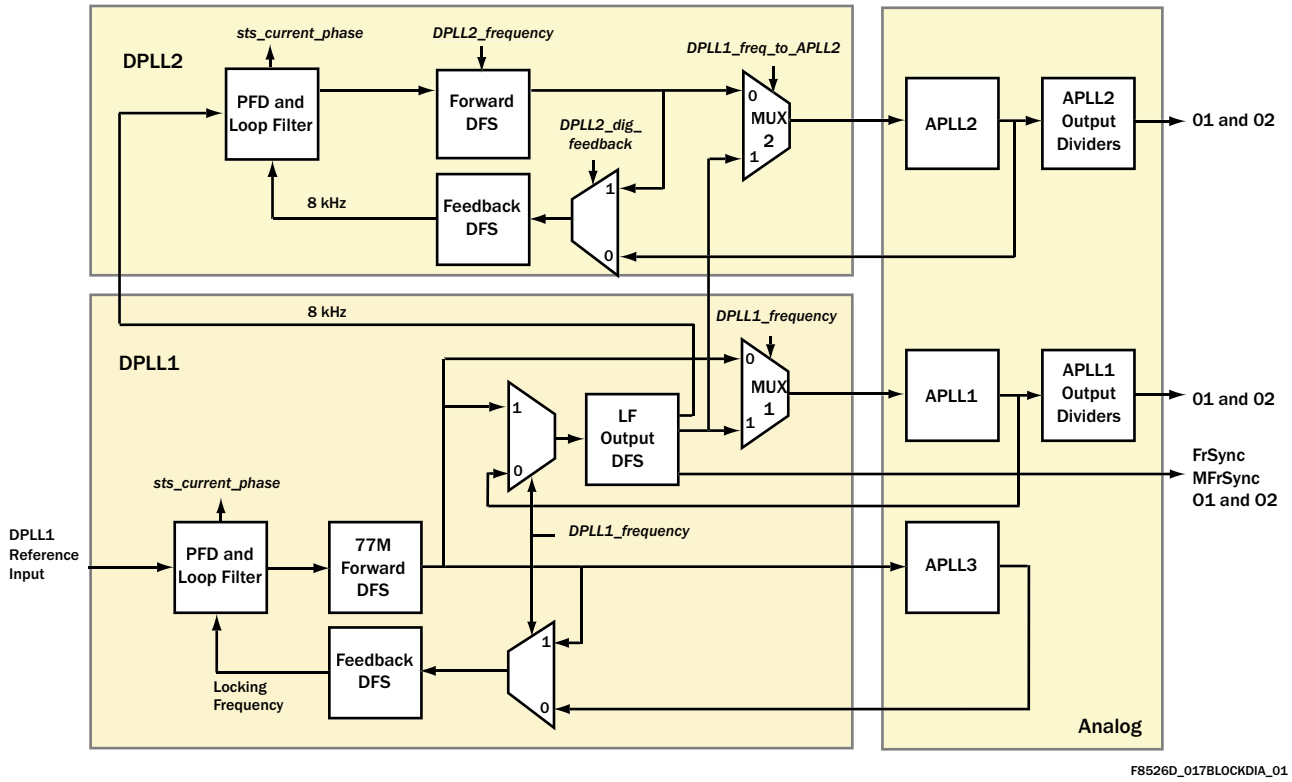
Figure 4 shows the PLL arrangement in more detail. Each DPLL comprises a generic Phase and Frequency Detector (PFD) with a Digital Loop filter, together with Forward, Feedback, and Low Frequency (LF) (DPLL1 only) Digital Frequency Synthesis (DFS) blocks. The Forward DFS block represents a Digital Timed Oscillator (DTO).

The DPLL architecture for DPLL1 is more complex than that of DPLL2. See “DPLL Feature Summary” on page 16..

The selected SEC input is always supplied to DPLL1. DPLL1 may use either digital feedback or analog feedback (via APLL3).

DPLL2 always takes its feed from DPLL1 and cannot be used to select a different input to that of DPLL1.

Figure 4 PLL Block Diagram



DFS is a technique for generating an output frequency using a higher frequency system clock (204.8 MHz in the case of the 77.76 MHz synthesis). However, the edges of the output clock are not ideally placed in time, since all edges of the output clock will be aligned to the active edge of the system clock. This means that the generated clock will inherently have jitter on it equivalent to one period of the system clock.

DPLL1 and APLLs

DPLL1 always produces 77.76 MHz. The input reference is either passed directly to the PFD or via a pre-divider (not shown) to produce the reference input. The feedback 77.76 MHz is either divided or synthesized to generate the locking frequency.

The DPLL1 77M Forward DFS block uses DFS clocked by the 204.8 MHz system clock to synthesize the 77.76 MHz and, therefore, has an inherent 4.9 ns of p-p jitter. There is an option to use a feedback APLL (APLL3) to filter out this jitter before the 77.76 MHz is used to generate the feedback locking frequency in the DPLL1 feedback DFS block. This analog feedback option allows a lower jitter (<1 ns) feedback signal to give maximum performance.

The 77.76 MHz is fed to DPLL1 LF Output DFS block and to APLL1. The low frequency DPLL1 LF Output DFS block is used to produce three frequencies; two of them, Digital1 and Digital2, are available for selection to be produced at outputs 01 and 02, and the third frequency can produce multiple E1/DS1 rates via the filtering APLLs. The input clock to the DPLL1 LF Output DFS block is 77.76 MHz from APLL1 (post jitter filtering) or 77.76 MHz direct from the DPLL1 77M Forward DFS.

Utilizing the clock from APLL1 will result in lower jitter outputs from the DPLL1 LF Output DFS block. However, when the input to the APLL1 is taken from the DPLL1 LF Output DFS block, the input to that block comes directly from the DPLL1 77M Forward DFS block so that a “loop” is not created.

APLL1 is for multiplying and filtering. The input to APLL1 is controlled by MUX 1 (see “Multiplexers” on page 13). The frequency from APLL1 is four times its input frequency i.e. 311.04 MHz when used with a 77.76 MHz input. APLL1 is subsequently divided by 1, 2, 4, 6, 8, 12, 16 and 48 and these are available at the 01 and 02 Outputs.

DPLL2 & APLLs

DPLL2 is simpler than DPLL1. DPLL2 offers no low frequency output. The DPLL2 input can only be used to lock to DPLL1. Unlike DPLL1, the DPLL2 Forward DFS block does not always generate 77.76 MHz. The possible

frequencies are listed in Table 12, “APLL2 Frequencies,” on page 24. Similarly to DPLL1, the output of the DPLL2 Forward DFS block is generated using DFS clocked by the 204.8 MHz system clock and will have an inherent jitter of 4.9 ns.

The DPLL2 feedback DFS also has the facility to be able to use the post APLL2 (jitter-filtered) clock to generate the feedback locking frequency. Again, this will give the maximum performance by using a low jitter feedback.

APLL2 block is also for multiplying and filtering. The input to APLL2 is controlled by MUX 2 (see “Multiplexers” on page 13) and can come either from the DPLL2 Forward DFS block or from DPLL1.

The frequency generated from the APLL2 is four times its input frequency i.e. 311.04 MHz when used with a 77.76 MHz input. APLL2 is subsequently divided by 2, 4, 8, 12, 16, 48 and 64 and these are available at the 01 and 02 Outputs.

“Digital” Frequencies

DFS is also carried out by DPLL1 LF Output DFS block in Figure 4 (E1/DS1 Synthesis block in Figure 1). This block is clocked either by the DPLL1 77M Forward DFS block or via the APLL1, and generates the single frequencies Digital1 and Digital2 (see Table 13 and Table 14). The input clock frequency of the DFS is always 77.76 MHz and as such has a period of approximately 12 ns. The jitter generated on the Digital outputs is relatively high, because they do not pass through an APLL for jitter filtering. The minimum level of jitter is when DPLL1 is in analog feedback mode, when the p-p jitter will be approximately 13 ns (equivalent to a period of the DFS clock). The maximum jitter is generated when in digital feedback mode, when the total is approximately 18 ns.

The E1/DS1 Synthesis block generates the E1/DS1 rates for the APLLs, using the output from DPLL1. It generates 12E1, 16E1, 16DS1 or 24DS1, for selection by MUX1.

FrSync, MFrSync, 2 kHz and 8 kHz Clock Outputs

Whilst the FrSync and MFrSync Outputs are always supplied from DPLL1, the 2 kHz and 8 kHz options available from the 01 and 02 Outputs can be supplied from either DPLL1 or DPLL2 (Reg. 7A Bit 7).

Multiplexers

Multiplexers MUX1 and MUX2 are used to select the appropriate inputs to the Analog PLLs. The function they represent is controlled by *cnfg_DPLL1_frequency* Reg. 65.

APLL2 Input Selection using MUX 2

- DPLL2 selected for input to APLL2 (Reg. 65 Bit 6 = 0) The input frequency is selected from the operating frequency of DPLL2 (Reg. 64 Bits [2:0])
- DPLL1 + LF Output DFS selected for Input to APLL2
  - 12E1 (Reg. 65 Bit 6 = 1 and Bits [5:4] set to 00)
  - 16E1 (Reg. 65 Bit 6 = 1 and Bits [5:4] set to 01)
  - 24DS1 (Reg. 65 Bit 6 = 1 and Bits [5:4] set to 10)
  - 16DS1 (Reg. 65 Bit 6 = 1 and Bits [5:4] set to 11)

APLL1 Input Selection using MUX 1

- DPLL1 (77.76 MHz) output fed to input of APLL1. Analog feedback used in DPLL1 (Reg. 65 Bits [2:0] set to 000)
- DPLL1 (77.76 MHz) output fed to input of APLL1. Digital feedback used in DPLL1 (Reg. 65 Bits [2:0] set to 001)
- DPLL1 + LF Output DFS selected for input to APLL1
  - 12E1 (Reg. 65 Bits [2:0] set to 010)
  - 16E1 (Reg. 65 Bits [2:0] set to 011)
  - 24DS1 (Reg. 65 Bits [2:0] set to 100)
  - 16DS1 (Reg. 65 Bits [2:0] set to 101)

Notes: (i) DPLL2 output cannot be selected for input to APLL1

(ii) If both multiplexers select LF Output DFS, the same frequency value must be selected in Reg. 65 Bits [2:0] and Reg. 65 Bits [5:4].

APLLs

There are three main APLLs. APLL1 and APLL2 provide a lower final output jitter reducing the 4.9 ns p-p jitter from the digital down to 500 ps p-p and 60 ps RMS as typical final outputs measured broadband (from 10 Hz to 1 GHz). The feedback APLL (APLL3) is selected by default; it provides improved performance over the digital feedback.

APLL Output Dividers

Each APLL has its own divider. Each divider simultaneously outputs a series of fixed ratios of its APLL input. Any of these divided outputs may be selected as the output on Outputs 01 or 02 by configuring Reg. 61 and Reg. 62, with the following exceptions: (APLL1)/2 and (APLL1)/1 only available for Output 01 (differential port), and (APLL1)/48 only available for Output 02.

PFD and Loop Filters

The PFD compares the input reference with that of the locking frequency (feedback) giving a phase error which is then filtered by a 100Hz low pass filter, to give the average phase error for input into a loop filter. The PFD is quite complex and has several programmable options to determine what phase error value is fed to the loop (See "Phase and Frequency Detectors" on page 15.") depending on the type of jitter/wander expected.

The loop filter bandwidth and damping is programmable to optimize the locking time/ability to track the input. See Figure 5 and "Damping Factor Programmability" on page 15.

PLL Operational Controls

The main factors controlling the operation of the PLL are:

1. Input reference and feedback frequency selection - See "PLL Architecture" on page 11., and "Input Locking Frequency Modes" on page 7.
2. Loop Bandwidth and Damping factor of the DPLLs - these determine how fast the device can to lock to the selected input, or how tightly it can track the input.
3. PFD settings - these affect the input phase error to the Loop filter and relate to jitter and wander tolerance - See "Phase/Frequency/Lock Detection" on page 15.

DPLL1 initially tries to lock to the input frequency of the selected input SEC. By default, it uses a wide "acquisition" bandwidth setting until it has achieved frequency lock, then DPLL1 switches to using a narrower "Locked" bandwidth setting as it locks to the phase of the input.

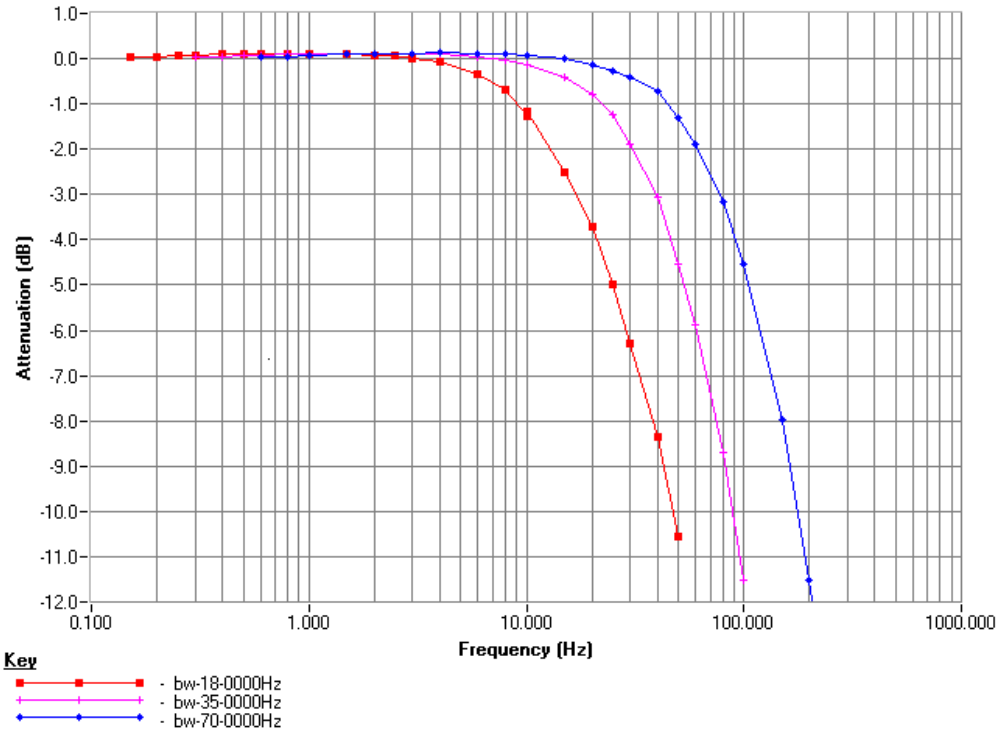
Input Acquisition Bandwidth

DPLL1 has programmable acquisition bandwidth of 18, 35 or 70 Hz. The default is set to 70 Hz.

Input Locked Bandwidth

The ACS8526 has programmable "Locked" bandwidth of 18, 35 or 70 Hz. These bandwidth settings correspond to the -3 dB jitter attenuation point on the ACS8526's jitter transfer characteristic shown in Figure 5. If the ACS8526 is used with only DPLL1, the highest bandwidth setting is recommended to ensure the closest tracking of the input SEC. If DPLL2 is also to be used, DPLL1 should be set to a lower bandwidth setting than DPLL2. The lowest bandwidth setting will provide the highest jitter attenuation, although this is not the main function of the ACS8526 device.

Figure 5 DPLL1 Jitter Transfer Characteristic, (Freq. = 1.544 MHz, Jitter = 0.2 UI p-p, Damping Factor = 5)



Damping Factor Programmability

The DPLL damping factor is set by default to provide a maximum wander gain peak of around 0.1 dB. Many of the specifications (e.g. GR-1244-CORE [13], G.812[7] and G.813[8]) specify a wander transfer gain of less than 0.2 dB. GR-253[11] specifies jitter (not wander) transfer of less than 0.1 dB. To accommodate the required levels of transfer gain, the ACS8526 provides a choice of damping factors, with more choice given as the bandwidth setting increases into the frequency regions classified as jitter. Table 5 shows which damping factors are available for selection at the different bandwidth settings, and the corresponding jitter transfer approximate gain peak.

Table 5 Available Damping Factors for different DPLL Bandwidths, and Associated Gain Peak Values

Bandwidth/Hz	Reg. 6B [2:0]	Damping Factor selected	Gain Peak/dB
18	1	1.2	0.4
	2	2.5	0.2
	3, 4, 5	5	0.1
35	1	1.2	0.4
	2	2.5	0.2
	3	5	0.1
	4, 5	10	0.06
70	1	1.2	0.4
	2	2.5	0.2
	3	5	0.1
	4	10	0.06
	5	20	0.03

Phase/Frequency/Lock Detection

Two main types of detector are available in the ACS8526:

- Phase and frequency detectors, and
- Phase Loss/Lock detectors.

Phase and Frequency Detectors

There are two multi-phase and frequency detectors, one for each DPLL. The multi-phase and frequency detectors are used to compare input and feedback clocks. They operate at input frequencies up to 77.76 MHz (155.52 MHz is internally divided down to 77.76 MHz).

A common arrangement however is to use Lock8k mode (See Bit 6 of Reg. 22 and 23), where all input frequencies are divided down to 8 kHz internally. Marginally better MTIE figures may be possible in direct lock mode due to more regular phase updates. This direct locking capability is one of the unique features of the ACS8526.

A multi-phase detector (patent pending) approach is used in order to give an infinitesimally small input phase resolution combined with large jitter tolerance. A multi-phase detector comprises the following phase detectors:

- Phase and frequency detector (±360°, or ±180° range).
- An Early/Late phase detector for fine resolution.
- A multi-cycle phase detector for large input jitter tolerance (up to 8191 UI), which captures and remembers phase differences of many cycles between input and feedback clocks.

The phase detectors can be configured to be immune to occasional missing input clock pulses by using nearest edge detection (±180° capture) or the normal ±360° phase capture range which gives frequency locking. The device will automatically switch to nearest edge locking when the multi-UI phase detector is not enabled, and the other phase detectors have detected that phase lock has been achieved. It is possible to disable the selection of nearest edge locking via Reg. 03 Bit 6 (set to 1). In this setting, frequency locking will always be enabled.

The balance between the first two types of phase detector employed can be adjusted via Reg. 6A to 6D. The default settings should be sufficient for all modes. Adjustment of these settings affects only small signal overshoot and bandwidth.

The multi-cycle phase detector (wide-range) is enabled via Reg. 74, Bit 6 set to 1 and the range is set in exponentially increasing steps from ±1 UI up to 8191 UI via Reg. 74, Bits [3:0].

When this detector is enabled it keeps a track of the correct phase position over many cycles of phase difference to give excellent jitter tolerance. This provides an alternative to switching to Lock8k mode as a method of achieving high jitter tolerance.

An additional control (Reg. 74 Bit 5) enables the multi-phase detector value to be used in the final phase value as part of the DPLL loop. When enabled by setting *High*, the multi cycle phase value will be used in the loop and gives faster pull-in (but more overshoot).

The characteristics of the loop will be similar to Lock8k mode where again large input phase differences contribute to the loop dynamics. Setting the bit *Low* only uses a max figure of 360° in the loop and will give slower pull-in but gives less overshoot. The final phase position that the loop has to pull in to is still tracked and remembered by the multi-cycle phase detector in either case.

Phase Lock/Loss Detectors

Phase lock/loss detection is handled in several ways. Phase loss can be triggered from:

- The fine phase lock detector, which measures the phase between input and feedback clock
- The coarse phase lock detector, which monitors whole cycle slips
- Detection that the DPLL is at min. or max. frequency
- Detection of no activity on the input.

Each of these sources of phase loss indication is individually enabled via registers bits (see Reg. 73 and 74). Phase lock or loss is used to determine whether to switch to nearest edge locking and whether to use acquisition or normal bandwidth settings for the DPLL. Acquisition bandwidth is used for faster pull-in from an unlocked state.

The coarse phase lock detector detects phase differences of n cycles between input and feedback clocks, where n is set by Reg. 74, Bits [3:0]; the same register that is used for the coarse phase detector range, since these functions go hand in hand. This detector may be used in the case where it is required that a phase loss indication is not given for reasonable amounts of input jitter and so the fine phase loss detector is disabled and the coarse detector is used instead.

DPLL Feature Summary

(* = hardware default selection)

DPLL1 Main Features

- Multiple E1 and DS1 outputs supported
- Low jitter MFrSync (2 kHz) and FrSync (8 kHz) outputs
- Multiple phase loss and multiple phase detectors (see “DPLL1 Advanced Features”)
- Direct PLL locking to common SONET/SDH input frequencies or any multiple of 8 kHz
- Fast detection on input failure and entry into Digital Holdover mode (holds at the current frequency value)
- Frequency translation between input and output rates via direct digital synthesis
- High accuracy digital architecture for stable PLL dynamics combined with an APLL for low jitter final output clocks
- Selectable Automatic DPLL bandwidth control (auto* selects either Locked bandwidth, or Acquisition bandwidth), or Locked DPLL bandwidth (Reg. 3B Bit 7)
- Two programmable bandwidth controls:
  - Locked bandwidth: 18, 35* or 70 Hz (Reg. 67)
  - Acquisition bandwidth: 18, 35 or 70* Hz (Reg. 69)
- Programmable damping factor, (For optional faster locking and peaking control) Factors = 1.2, 2.5, 5, 10* or 20 (Reg. 6B, Bits [2:0])
- Programmable DPLL pull-in frequency range (Reg. 41, Reg. 42).

DPLL1 Advanced Features

Phase Loss Indicators

- Phase loss fine limit. on*/off (Reg. 73 Bit 7) and programmable range 0 to 7 Dec. (Reg. 73 Bits [2:0])
- Multi-cycle phase loss course limit, on*/off (Reg. 74 Bit 7) and selectable range from ±(1 to 8191) UI in 13 steps (Reg. 74 Bits [3:0]).

Phase Detector Controls

- Multi-cycle phase detector - Course phase detector & capture range on*/off (Reg. 74 Bit 6) and selectable range from ±(1 to 8191) UI in 13 steps (Reg. 74 Bits [3:0]). If selected, this feature increases jitter and wander tolerance to a maximum of 8192 UI (normally limited to ±0.5 UI)
- Use of coarse phase detector result in DPLL algorithm, on*/off (Reg. 74 Bit 5) - speeds up phase locking
- Limit DPLL1 Integral when at DPLL frequency limit, on*/off (Reg. 3B Bit 3) - reduces overshoot
- Anti-noise filter for low frequency inputs, on/off* (Reg. 76 Bit 7).

Advanced Phase Detector Controls

- DPLL1 PD2 gain enable, on*/off (Reg. 6D Bit 7)
  If on, this allows automatic gain selection according to the type of feedback to the DPLL (For the digital feedback setting, the gain used for PD2 is given by Reg. 6D Bits [2:0]). If off, PD2 is not used.

- Adjustable gain settings for PD2 (when enabled), for the following feedback cases:
  - Digital feedback (Reg. 6D Bits [2:0])
  - Analog feedback (all frequencies above 8 kHz) (Reg. 6D Bits [6:4])
  - Analog 8k (or less) feedback (Reg. 6B Bits [2:0]).

DPLL2 Main Features

- Always locked to DPLL1
- A single programmable bandwidth control: 18*, 35 or 70 Hz
- Programmable damping factor, (For optional faster locking and peaking control) Factors = 1.2, 2.5, 5*, 10 or 20.
- Digital feedback, on*/off (Reg. 35 Bit 6)
- Output frequency selection (Reg. 64)
  - DS3/E3 support (44.736 MHz / 34.368 MHz) independent of rates from DPLL1
  - Low jitter E1/DS1 options independent of rates from DPLL1
  - Frequencies of n x E1/DS1 including 16 and 12 x E1, and 16 and 24 x DS1 supported
  - Squelched (clock off)
- Can provide the source for the 2 kHz and 8 kHz outputs available at Outputs 01 and 02 (Reg. 7A Bit 7).

DPLL2 Advanced Features

The advanced features are the same as those for DPLL1, with DPLL2 using the configuration values for DPLL1, with the following exceptions:

Advanced Phase Detector Controls

- PD2 gain control enable, on*/off (Reg. 6C Bit 7) If on, this allows automatic gain selection according to the type of feedback to the DPLL (For the digital feedback setting, the gain used for PD2 is given by (Reg. 6C Bits [2:0]). If off, PD2 is not used
- Adjustable gain settings for PD2 (with auto switching enabled), for the following feedback cases:
  - Digital feedback (Reg. 6C Bits [2:0])
  - Analog feedback (all frequencies above 8K) (Reg. 6C Bits [6:4])
  - Analog 8k (or less) feedback (Reg. 6A Bits [2:0]).

Outputs

The ACS8526 delivers four output signals on the following ports: Two clocks, one each on Output 01 and 02, and two Sync signals, one each on output ports FrSync and MFrSync. Outputs 01 and 02 are independent of each other and are individually selectable. Output 01 is a differential port (pins 01POS and 01NEG), and can be selected to be PECL or LVDS via Reg. 3A *cnfg_differential_output*. Output 02 (pin 02) and the Sync outputs are TTL/CMOS compatible.

The two Sync outputs, FrSync (8 kHz) and MFrSync (2 kHz), are derived from DPLL1.

The frequencies available on the outputs can be selected from a range of spot frequencies by either:

- Hardware selection: configuring the hardware pins OP_FREQ1 [2:0], OP_FREQ2[2:0] and SONSDH, which are read on reset, or
- Register programming: writing to the registers after the end of the initialization period.

Output Frequency Selection by Hardware

Tables 6 and 7 show the hardware settings for selecting particular output frequencies on Outputs 01 and 02. Note that the hardware frequency selection method provides only a subset (11) of the total number of frequencies (55) available when selecting by register programming.

Output Frequency Selection by Register Programming

The output frequencies on 01 and 02 are controlled by a number of interdependent parameters (refer to “PLL Architecture” on page 11). The frequencies of the output clocks are selectable from a range of pre-defined spot frequencies/port technologies, as defined in Table 8.

Outputs 01 & 02 Frequency Configuration Steps

The output frequency selection is performed in the following steps:

1. Refer to Table 10, Frequency Divider Look-up, to choose a set of output frequencies.
2. Refer to the Table 10 to determine the required APLL frequency to support the frequency set.
3. Refer to Table 11, APLL1 Frequencies, and Table 12, APLL2 Frequencies, to determine in what mode DPLL1 and DPLL2 need to be configured, considering the output jitter level.

4. Refer to Table 13, 01 and 02 Output Frequency Selection, and the column headings in Table 10, Frequency Divider Look-up, to select the appropriate frequency from either of the APLLs on each output as required.

Table 6 Output 01 Frequency Selection by Hardware Configuration

01_FREQ			SONSDHB Pin	Output Frequency/ MHz	DPLL Selected	DPLL Mode	Jitter Level (typ)	
2	1	0					rms (ps)	p-p (ns)
0	0	0	X	0	-	-	-	-
0	0	1	0	34.368	DPLL2	E3	120	1
			1	44.736	DPLL2	DS3	110	1
0	1	0	X	19.44	DPLL1	Analog feedback	60	0.6
0	1	1	X	25.92	DPLL1	Analog feedback	60	0.6
1	0	0	X	38.88	DPLL1	Analog feedback	60	0.6
1	0	1	X	51.84	DPLL1	Analog feedback	60	0.6
1	1	0	X	77.76	DPLL1	Analog feedback	60	0.6
1	1	1	X	155.52	DPLL1	Analog feedback	60	0.6

Table 7 Output 02 Frequency Selection by Hardware Configuration

02_FREQ			SONSDHB Pin	01_FREQ = "001"	Output Frequency/ MHz	DPLL Selected	DPLL Mode	Jitter Level (typ)	
2	1	0						rms (ps)	p-p (ns)
0	0	0	X	X	0	-	-	-	-
0	0	1	0	FALSE	2.048	DPLL2	16E1	400	2
			1		1.544	DPLL2	16DS1	200	1.2
0	0	1	0	TRUE	2.048	DPLL1	12E1	900	0.45
			1		3.088	DPLL1	24DS1	110	0.75
0	1	0	0	X	34.368	DPLL2	E3	120	1
			1	X	44.736	DPLL2	DS3	110	1
0	1	1	X	X	19.44	DPLL1	Analog feedback	60	0.6
1	0	0	X	X	25.92	DPLL1	Analog feedback	60	0.6
1	0	1	X	X	38.88	DPLL1	Analog feedback	60	0.6
1	1	0	X	X	51.84	DPLL1	Analog feedback	60	0.6
1	1	1	X	X	77.76	DPLL1	Analog feedback	60	0.6

Table 8 Output Reference Source Selection Table

Port Name	Output Port Technology	Frequencies Supported
Output 01	LVDS/PECL (LVDS default)	Frequency selection as per Table 9 and Table 13
Output 02	TTL/CMOS	
FrSync	TTL/CMOS	FrSync, 8 kHz programmable pulse width and polarity, see Reg. 7A.
MFrSync	TTL/CMOS	MFrSync, 2 kHz programmable pulse width and polarity, see Reg. 7A.

Note...1.544 MHz/2.048 MHz are shown for SONET/SDH respectively. Pin SONSDHB controls default. When High, SONET is default.

Table 9 Output Frequency Selection

Frequency (MHz, unless stated otherwise)	DPLL1 Mode	DPLL2 Mode	APLL2 Input Mux	Jitter Level (typ)	
				rms (ps)	p-p (ns)
2 kHz	77.76 MHz Analog	-	-	60	0.6
2 kHz	Any digital feedback mode	-	-	1400	5
8 kHz	77.76 MHz Analog	-	-	60	0.6
8 kHz	Any digital feedback mode	-	-	1400	5
1.536	-	12E1 mode	Select DPLL2	500	2.3
1.536	-	-	Select DPLL1 12E1	250	1.5
1.544	-	16DS1 mode	Select DPLL2	200	1.2
1.544	-	-	Select DPLL1 16DS1	150	1.0
1.544 via Digital1 or Digital2 (not Output 01)	77.76 MHz Analog	-	-	3800	13
1.544 via Digital1 or Digital2 (not Output 01)	Any digital feedback mode	-	-	3800	18
2.048	-	12E1 mode	Select DPLL2	500	2.3
2.048	-	-	Select DPLL1 12E1	250	1.5
2.048	-	16E1 mode	Select DPLL2	400	2.0
2.048	-	-	Select DPLL1 16E1	220	1.2
2.048 (not Output 01)	12E1 mode	-	-	900	4.5
2.048 via Digital1 or Digital2 (not Output 01)	77.76 MHz Analog	-	-	3800	13
2.048 via Digital1 or Digital2 (not Output 01)	Any digital feedback mode	-	-	3800	18
2.059	-	16DS1 mode	Select DPLL2	200	1.2
2.059	-	-	Select DPLL1 16DS1	150	1.0

Table 9 Output Frequency Selection (cont...)

Frequency (MHz, unless stated otherwise)	DPLL1 Mode	DPLL2 Mode	APLL2 Input Mux	Jitter Level (typ)	
				rms (ps)	p-p (ns)
2.059 (not Output 01)	16DS1 mode	-	-	760	2.6
2.316	-	24DS1 mode	Select DPLL2	110	0.75
2.316	-	-	Select DPLL1 24DS1	110	0.75
2.731	-	16E1 mode	Select DPLL2	400	1.5
2.731	-	-	Select DPLL1 16E1	220	1.2
2.731 (not Output 01)	16E1 mode	-	-	250	1.6
2.796	-	DS3 mode	Select DPLL2	110	1.0
3.088	-	24DS1 mode	Select DPLL2	110	0.75
3.088	-	-	Select DPLL1 24DS1	110	0.75
3.088 (not Output 01)	24DS1 mode	-	-	110	0.75
3.088 via Digital1 or Digital2 (not Output 01)	77.76 MHz Analog	-	-	3800	13
3.088 via Digital1 or Digital2 (not Output 01)	Any digital feedback mode	-	-	3800	18
3.728	-	DS3 mode	Select DPLL2	110	1.0
4.096 via Digital1 or Digital2 (not Output 01)	77.76 MHz Analog	-	-	3800	13
4.096 via Digital1 or Digital2 (not Output 01)	Any digital feedback mode	-	-	3800	18
4.296	-	E3 mode	Select DPLL2	120	1.0
4.86	-	77.76 MHz mode	Select DPLL2	60	0.6
5.728	-	E3 mode	Select DPLL2	120	1.0
6.144	12E1 mode	-	-	900	4.5
6.144	-	12E1 mode	Select DPLL2	500	2.3
6.144	-	-	Select DPLL1 12E1	250	1.5
6.176	16DS1 mode	-	-	760	2.6
6.176	-	16DS1 mode	Select DPLL2	200	1.2
6.176	-	-	Select DPLL1 16DS1	150	1.0
6.176 via Digital1 or Digital2 (not Output 01)	77.76 MHz Analog	-	-	3800	13
6.176 via Digital1 or Digital2 (not Output 01)	Any digital feedback mode	-	-	3800	18
6.48	-	77.76 MHz mode	Select DPLL2	60	0.6
6.48 (not Output 01)	77.76 MHz analog	-	-	60	0.6
6.48 (not Output 01)	77.76 MHz digital	-	-	60	0.6

Table 9 Output Frequency Selection (cont...)

Frequency (MHz, unless stated otherwise)	DPLL1 Mode	DPLL2 Mode	APLL2 Input Mux	Jitter Level (typ)	
				rms (ps)	p-p (ns)
8.192	12E1 mode	-	-	900	4.5
8.192	16E1 mode	-	-	250	1.6
8.192	-	16E1 mode	Select DPLL2	400	2.0
8.192	-	-	Select DPLL1 16E1	220	1.2
8.192 via Digital1 or Digital2 (not Output 01)	77.76 MHz Analog	-	-	3800	13
8.192 via Digital1 or Digital2 (not Output 01)	Any digital feedback mode	-	-	3800	18
8.235	16DS1 mode	-	-	760	2.6
9.264	24DS1 mode	-	-	110	0.75
9.264	-	24DS1 mode	Select DPLL2	110	0.75
9.264	-	-	Select DPLL1 24DS1	110	0.75
10.923	16E1 mode	-	-	250	1.6
11.184	-	DS3 mode	Select DPLL2	110	1.0
12.288	12E1 mode	-	-	900	4.5
12.288	-	12E1 mode	Select DPLL2	500	2.3
12.288	-	-	Select DPLL1 12E1	250	1.5
12.352	24DS1 mode	-	-	110	0.75
12.352	16DS1 mode	-	-	760	2.6
12.352	-	16DS1 mode	Select DPLL2	200	1.2
12.352	-	-	Select DPLL1 16DS1	150	1.0
12.352 via Digital1 or Digital2 (not Output 01)	77.76 MHz Analog	-	-	3800	13
12.352 via Digital1 or Digital2 (not Output 01)	Any digital feedback mode	-	-	3800	18
16.384	12E1 mode	-	-	900	4.5
16.384	16E1 mode	-	-	250	1.6
16.384	-	16E1 mode	Select DPLL2	400	2.0
16.384	-	-	Select DPLL1 16E1	220	1.2
16.384 via Digital1 or Digital2 (not Output 01)	77.76 MHz Analog	-	-	3800	13
16.384 via Digital1 or Digital2 (not Output 01)	Any digital feedback mode	-	-	3800	18
16.469	16DS1 mode	-	-	760	2.6
17.184	-	E3 mode	Select DPLL2	120	1.0

Table 9 Output Frequency Selection (cont...)

Frequency (MHz, unless stated otherwise)	DPLL1 Mode	DPLL2 Mode	APLL2 Input Mux	Jitter Level (typ)	
				rms (ps)	p-p (ns)
18.528	24DS1 mode	-	-	110	0.75
18.528	-	24DS1 mode	Select DPLL2	110	0.75
18.528	-	-	Select DPLL1 24DS1	110	0.75
19.44	77.76 MHz analog	-	-	60	0.6
19.44	77.76 MHz digital	-	-	60	0.6
19.44	-	77.76MHz mode	Select DPLL2	60	0.6
21.845	16E1 mode	-	-	250	1.6
22.368	-	DS3 mode	Select DPLL2	110	1.0
24.576	12E1 mode	-	-	900	4.5
24.576	-	12E1 mode	Select DPLL2	500	2.3
24.576	-	-	Select DPLL1 12E1	250	1.5
24.704	24DS1 mode	-	-	110	0.75
24.704	16DS1 mode	-	-	760	2.6
24.704	-	16DS1 mode	Select DPLL2	200	1.2
24.704	-	-	Select DPLL1 16DS1	150	1.0
25.92	77.76 MHz analog	-	-	60	0.6
25.92	77.76 MHz digital	-	-	60	0.6
32.768	16E1 mode	-	-	250	1.6
32.768	-	16E1 mode	Select DPLL2	400	2.0
32.768	-	-	Select DPLL1 16E1	220	1.2
34.368	-	E3 mode	Select DPLL2	120	1.0
37.056	24DS1 mode	-	-	110	0.75
37.056	-	24DS1 mode	Select DPLL2	110	0.75
37.056	-	-	Select DPLL1 24DS1	110	0.75
38.88	77.76 MHz analog	-	-	60	0.6
38.88	77.76 MHz digital	-	-	60	0.6
38.88	-	77.76 MHz mode	Select DPLL2	60	0.6
44.736	-	DS3 mode	Select DPLL2	110	1.0
49.152 (Output 01 only)	12E1 mode	-	-	900	4.5
49.408 (Output 01 only)	16DS1 mode	-	-	760	2.6
51.84	77.76 MHz analog	-	-	60	0.6

Table 9 Output Frequency Selection (cont...)

Frequency (MHz, unless stated otherwise)	DPLL1 Mode	DPLL2 Mode	APLL2 Input Mux	Jitter Level (typ)	
				rms (ps)	p-p (ns)
51.84	77.76 MHz digital	-	-	60	0.6
65.536 (Output 01 only)	16E1 mode	-	-	250	1.6
68.736	-	E3 mode	Select DPLL2	120	1.0
74.112 (Output 01 only)	24DS1 mode	-	-	110	0.75
77.76	77.76 MHz analog	-	-	60	0.6
77.76	77.76 MHz digital	-	-	60	0.6
77.76	-	77.76 MHz mode	Select DPLL2	60	0.6
98.304 (Output 01 only)	12E1 mode	-	-	900	4.5
98.816 (Output 01 only)	16DS1 mode	-	-	760	2.6
131.07 (Output 01 only)	16E1 mode	-	-	250	1.6
148.22 (Output 01 only)	24DS1 mode	-	-	110	0.75
155.52 (Output 01 only)	77.76 MHz analog	-	-	60	0.6
155.52 (Output 01 only)	77.76 MHz digital	-	-	60	0.6
311.04 (Output 01 only)	77.76 MHz analog	-	-	60	0.6
311.04 (Output 01 only)	77.76 MHz digital	-	-	60	0.6

Table 10 Frequency Divider Look-up

Transmission Rate	APLL Frequency	APLL/2	APLL/4	APLL/6	APLL/8	APLL/12	APLL/16	APLL/48	APLL/64
OC-N Rates	311.04	155.52	77.76	51.84	38.88	25.92	19.44	6.48	4.86
E3	274.944	137.472	68.376	-	34.368	-	17.184	5.728	4.296
DS3	178.944	89.472	44.736	-	22.368	-	11.184	3.728	2.796
24DS1	148.224	74.112	37.056	24,704	18.528	12.352	9.264	3.088	2.316
16E1	131.072	65.536	32.768	21.84533	16.384	10.92267	8.192	2.730667	2.048
16DS1	98.816	49.408	24.704	16.46933	12.352	8.234667	6.176	2.058667	1.544
12E1	98.304	49.152	24.576	16.384	12.288	8.192	6.144	2.048	1.536

Note...All frequencies in MHz.

Table 11 APLL1 Frequencies

APLL1 Frequency	Synthesis/MUX setting for APLL1 input	DPLL1 Frequency Control Reg. 65 Bits[2:0]	Output Jitter Level ns (p-p)
311.04	Normal (digital feedback)	000	<0.5
311.04 MHz	Normal (analog feedback)	001	<0.5
98.304 MHz	12E1 (digital feedback)	010	<2
131.072 MHz	16E1 (digital feedback)	011	<2
148.224 MHz	24DS1 (digital feedback)	100	<2
98.816 MHz	16DS1 (digital feedback)	101	<2
-	Do not use	110	-
-	Do not use	111	-

Table 12 APLL2 Frequencies

APLL2 Frequency	DPLL Mode	DPLL2 Forward DFS Frequency (MHz)	DPLL2 Freq Control Register Bits Reg. 64 Bits [2:0]	APLL2 Input from DPLL1 or 2. Reg. 65 Bit 6	DPLL1 + Synthesis Freq to APLL2 Register Bits Reg. 65 Bits [5:4]	Output Jitter Level ns (p-p)
311.04 MHz	DPLL2-Squelched	77.76	000	0 (DPLL2 selected)	XX	<0.5
311.04 MHz	DPLL2-Normal	77.76	001	0 (DPLL2 selected)	XX	<0.5
98.304 MHz	DPLL2-12E1	24.576	010	0 (DPLL2 selected)	XX	<0.5
131.072 MHz	DPLL2-16E1	32.768	011	0 (DPLL2 selected)	XX	<0.5
148.224 MHz	DPLL2-24DS1	37.056 (2*18.528)	100	0 (DPLL2 selected)	XX	<0.5
98.816 MHz	DPLL2-16DS1	24.704	101	0 (DPLL2 selected)	XX	<0.5
274.944 MHz	DPLL2-E3	68.736 (2*34.368)	110	0 (DPLL2 selected)	XX	<0.5
178.944 MHz	DPLL2-DS3	44.736	111	0 (DPLL2 selected)	XX	<0.5
98.304 MHz	DPLL1-12E1	-	XXX	1 (DPLL1 selected)	00	<2
131.072 MHz	DPLL1-16E1	-	XXX	1 (DPLL1 selected)	01	<2
148.224 MHz	DPLL1-24DS1	-	XXX	1 (DPLL1 selected)	10	<2
98.816 MHz	DPLL1-16DS1	-	XXX	1 (DPLL1 selected)	11	<2

Note...If using Synthesis for inputs to both APLL1 and APLL2, then they must both use the same synthesis settings.

"Digital" Frequencies

Table 13, "O1 and O2 Output Frequency Selection," lists Digital1 and Digital2 as available for selection. Digital1 is a single frequency selected from the range shown in Table 14. Digital2 is another single frequency selected from the same range.

Table 13 O1 and O2 Output Frequency Selection

Value in Register	Output Frequency for given "Value in Register" for each Output Port's *Cnf_output_frequency* Register	
	Output O2 Reg. 61 Bits [3:0]	**Output O1 Reg. 62 Bits [7:4]**
0000	Off	Off
0001	2 kHz	2 kHz
0010	8 kHz	8 kHz
0011	Digital2	APLL1/2
0100	Digital1	Digital1
0101	APLL1/48	APLL1/1
0110	APLL1/16	APLL1/16
0111	APLL1/12	APLL1/12
1000	APLL1/8	APLL1/8
1001	APLL1/6	APLL1/6
1010	APLL1/4	APLL1/4
1011	APLL2/64	APLL2/64
1100	APLL2/48	APLL2/48
1101	APLL2/16	APLL2/16
1110	APLL2/8	APLL2/8
1111	APLL2/4	APLL2/4

Using Output O2 to Control Pulse Width of 2/8 kHz on FrSync, MFrSync and O1 Outputs

It can be seen from Table 13 (O1 and O2 Output Frequency Selection) that frequencies listed as 2 kHz and 8 kHz can be selected. Whilst the FrSync and MFrSync outputs are always supplied from DPLL1, the 2 kHz and 8 kHz options available from the O1 and O2 outputs are all supplied via DPLL1 or DPLL2 (Reg. 7A Bit 7).

The outputs can be either clocks (50:50 mark-space) or pulses, and can be inverted. When pulse configuration is used, the pulse width will be one cycle of the rate selected on Output O2 (Output O2 must be configured to generate at least 1,544 kHz to ensure that pulses are generated correctly). Figure 6 shows the various options with the 8 kHz controls in Reg. 7A. There is an identical arrangement with Reg. 7A Bits [1:0] for the 2 kHz O1 and MFrSync outputs. Outputs FrSync and MFrSync can be disabled via Reg. 63 Bits [7:6].

Power-On Reset

The Power-On Reset (PORB) pin resets the device if forced *Low*. The reset is asynchronous, the minimum *Low* pulse width is 5 ns. Reset is needed to initialize all of the register values to their defaults. Reset must be asserted at power on, and may be re-asserted at any time to restore defaults. This is implemented simply using an external capacitor to GND along with the internal pull-up resistor. The ACS8526 is held in a reset state for 250 ms after the PORB pin has been pulled *High*. In normal operation PORB should be held *High*.

Figure 6 Control of 8k Options.

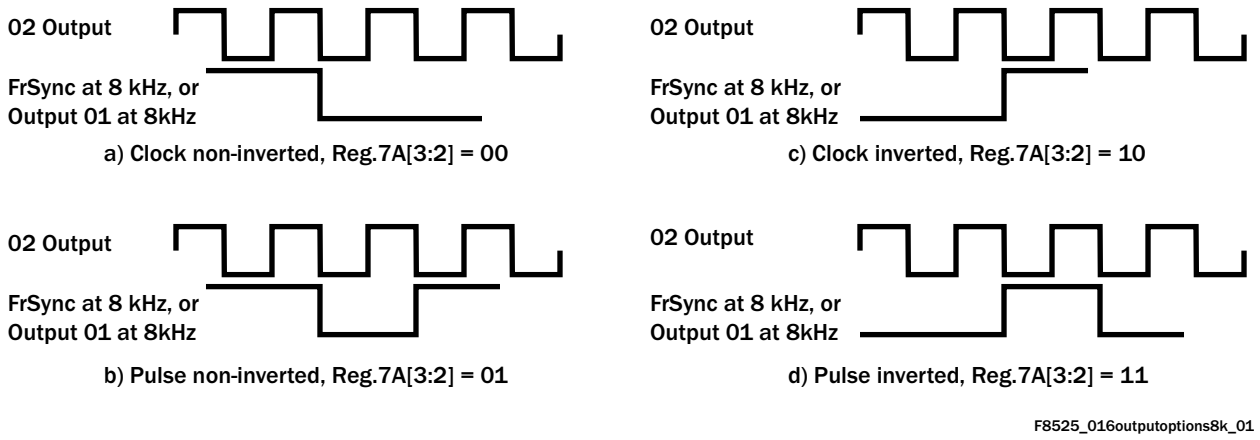


Table 14 Digital Frequency Selections

Digital1 Control Reg.39 Bits [5:4]	Digital1 SONET/ SDH Reg. 38 Bit5	Digital1 Freq. (MHz)
00	0	2.048
01	0	4.096
10	0	8.192
11	0	16.384
00	1	1.544
01	1	3.088
10	1	6.176
11	1	12.352

Digital2 Control Reg. 39 Bits[7:6]	Digital2 SONET/SDH Reg.38 Bit6	Digital2 Freq. (MHz)
00	0	2.048
01	0	4.096
10	0	8.192
11	0	16.384
00	1	1.544
01	1	3.088
10	1	6.176
11	1	12.352

Local Oscillator Clock

The Master system clock on the ACS8526 should be provided by an external clock oscillator of frequency 12.800 MHz. Wander on the local oscillator clock will not have a significant effect on the output clock whilst in Locked mode. In Free-Run or Holdover mode wander on the crystal is more significant. Variation in crystal temperature or supply voltage both cause drifts in operating frequency, as does ageing. These effects must be limited by careful selection of a suitable component for the local oscillator. Please contact Semtech for information on crystal oscillator suppliers.

Crystal Frequency Calibration

The absolute crystal frequency accuracy is less important than the stability since any frequency offset can be compensated by adjustment of register values in the IC. This allows for calibration and compensation of any crystal frequency variation away from its nominal value. An adjustment of ±50 ppm would be sufficient to cope with most crystals, in fact the range is an order of magnitude larger due to the use of two 8-bit register locations. The setting of the *cnfg_nominal_frequency* register allows for this adjustment. An increase in the register value increases the output frequencies by 0.0196229 ppm for each LSB step.

Note...The default register value (in decimal) = 39321 (9999 hex) = 0 ppm offset. The minimum to maximum offset range of the register is 0 to 65535 (dec), giving an adjustment range of -771 ppm to +514 ppm of the output frequencies, in 0.0196229 ppm steps.
Example: If the crystal was oscillating at 12.800 MHz + 5 ppm, then the calibration value in the register to give a - 5 ppm adjustment in output frequencies to compensate for the crystal inaccuracy, would be:
39321 - (5 / 0.0196229) = 39066 (dec) = 989A (hex).

Status Reporting

Loss of Input Signal - LOS Flag

In the event of loss of SEC input signal, LOS flag is raised on the LOS_ALARM pin. The LOS alarm is active *low*, and *high impedance* when inactive, i.e. when an LOS alarm exists, the output will be driven *low*; with no LOS alarm, the output will float. This is designed to be able to be connected to a processor together with other interrupt sources to trigger an interrupt. The output will require a pull-up resistor to pull the voltage up when the alarm is inactive.

Status Information

Status information can be read from the following Status Registers:

- *sts_current_DPLL_frequency* (Reg. 0C, 0D, and 07)
- *sts_reference_sources* (Reg. 11).

The registers *sts_current_DPLL_frequency* report the frequency of DPLL1 or DPLL2 with respect to the external crystal XO frequency (after calibration via Reg. 3C, 3D if used). The selection of DPLL2 or DPLL1 reporting is made via Reg. 4B, Bit 4. The value is a 19-bit signed number with one LSB representing 0.0003068 ppm (range of ±80 ppm). This value is actually the integral path value in the DPLL, and as such corresponds to an averaged measurement of the input frequency, with an averaging time inversely proportional to the DPLL bandwidth setting. Reading this regularly can show how the currently locked source is varying in value e.g. due to frequency wander on its input.

Serial Interface

The ACS8526 device has a serial interface which can be SPI compatible.

The Motorola SPI convention is such that address and data is transmitted and received MSB first. On the ACS8526, device address and data are transmitted and received LSB first. Address, read/write control and data on the SDI pin is latched into the device on the rising edge of the SCLK. During a read operation, serial data output on the SDO pin can be read out of the device on either the rising or falling edge of the SCLK depending on the logic level of CLKE. For standard Motorola SPI compliance, data should be clocked out of the SDO pin on the rising edge of the SCLK so that it may be latched into the microprocessor on the falling edge of the SCLK. Figure 7 and 8 show the timing diagrams of write and read accesses for this interface.

The serial interface clock (SCLK) is not required to run between accesses (i.e., when CSB = 1).

Figure 7 Write Access Timing for SERIAL Interface

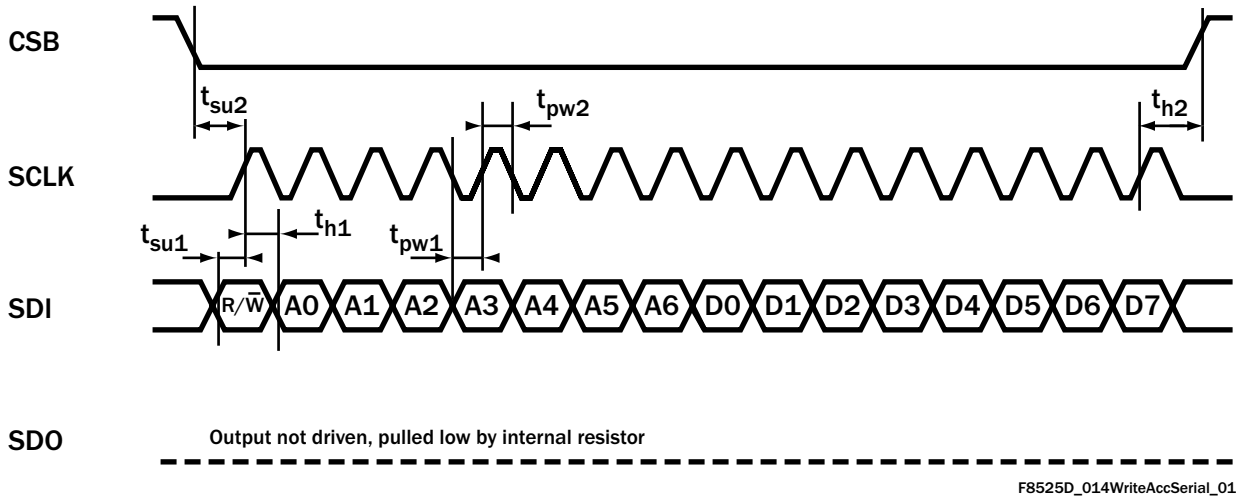


Table 15 Write Access Timing for SERIAL Interface (For use with Figure 7)

Symbol	Parameter	MIN	TYP	MAX
t_{SU1}	Setup SDI valid to $SCLK_{rising\ edge}$	4 ns	-	-
t_{SU2}	Setup $CSB_{falling\ edge}$ to $SCLK_{rising\ edge}$	14 ns	-	-
t_{pw1}	SCLK *Low* time	22 ns	-	-
t_{pw2}	SCLK *High* time	22 ns	-	-
t_{h1}	Hold SDI valid after $SCLK_{rising\ edge}$	6 ns	-	-
t_{h2}	Hold CSB *Low* after $SCLK_{rising\ edge}$	5 ns	-	-
t_p	Time between consecutive accesses ($CSB_{rising\ edge}$ to $CSB_{falling\ edge}$)	10 ns	-	-

Figure 8 Read Access Timing for SERIAL Interface

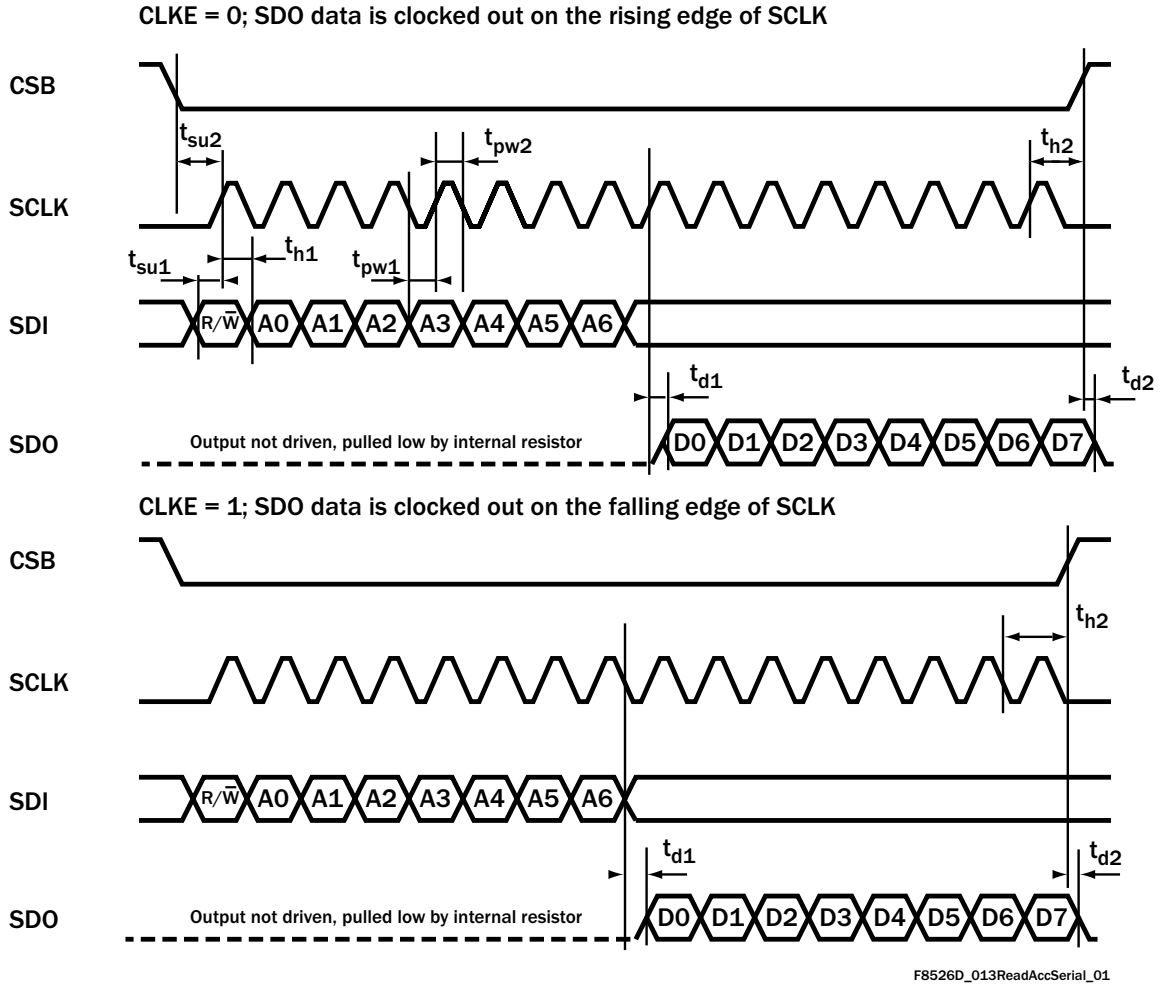


Table 16 Read Access Timing for SERIAL Interface (For use with Figure 8)

Symbol	Parameter	MIN	TYP	MAX
t_{su1}	Setup SDI valid to $SCLK_{rising\ edge}$	4 ns	-	-
t_{su2}	Setup $CSB_{falling\ edge}$ to $SCLK_{rising\ edge}$	14 ns	-	-
t_{d1}	Delay $SCLK_{rising\ edge}$ ($SCLK_{falling\ edge}$ for CLKE = 1) to SDO valid	-	-	18 ns
t_{d2}	Delay $CSB_{rising\ edge}$ to SDO *High*-Z	-	-	16 ns
t_{pw1}	SCLK *Low* time	22 ns	-	-
t_{pw2}	SCLK *High* time	22 ns	-	-
t_{h1}	Hold SDI valid after $SCLK_{rising\ edge}$	6 ns	-	-
t_{h2}	Hold CSB *Low* after $SCLK_{rising\ edge}$, for CLKE = 0 Hold CSB *Low* after $SCLK_{falling\ edge}$, for CLKE = 1	5 ns	-	-
t_p	Time between consecutive accesses ($CSB_{rising\ edge}$ to $CSB_{falling\ edge}$)	10 ns	-	-

Register Map

Each Register, or register group, is described in the following Register Map (Table 17) and subsequent Register Description Tables.

Register Organization

The ACS8526 LC/P LITE uses a total of 46 eight-bit registers, identified by a Register Name and corresponding hexadecimal Register Address. They are presented here in ascending order of Reg. address and each Register is organized with the most-significant bit positioned in the left-most bit, with bit significance decreasing towards the right-most bit. Some registers carry several individual data fields of various sizes, from single-bit values (e.g. flags) upwards. Several data fields are spread across multiple registers, as shown in the Register Map, Table 17.

Shaded areas in the map are “don’t care” and writing either 0 or 1 to them will not affect any function of the device.

Bits labelled “Set to 0” or “Set to 1” must be set as stated during initialization of the device, either following power-up, or after a power-on reset (POR). Failure to correctly set these bits may result in the device operating in an unexpected way.

CAUTION! Do not write to any undefined register addresses as this may cause the device to operate in a test mode. If an undefined register has been inadvertently addressed, the device should be reset to ensure the undefined registers are at default values.

Multi-word Registers

For multi-word registers (e.g. Reg. 0C and 0D), all the words have to be written to their separate addresses, and without any other access taking place, before their combined value can take effect. If the sequence is interrupted, the sequence of writes will be ignored.

Reading a multi-word address freezes the other address words of a multi-word address so that the bytes all correspond to the same complete word

Register Access

Most registers are either configuration registers or status registers, the exceptions being the *chip_id* and *chip_revision* registers. Configuration registers may be written to or read from at any time (the complete 8-bit register must be written, even if only one bit is being modified). All status registers may be read at any time. A description of each register is given in the Register Map, and Register Map Description.

Configuration Registers

Each configuration register reverts to a default value on power-up or following a reset. Most default values are fixed, but some will be pin-settable. All configuration registers can be read out over the serial port.

Status Registers

The Status Registers contain readable registers. They may all be read from outside the chip but are not writeable from outside the chip (except for a clearing operation). All status registers are read via shadow registers to avoid data hits due to dynamic operation. Each individual status register has a unique location.

Flags

In the event of loss of the currently selected input a no-activity flag is raised on pin LOS_ALARM indicating that the input to DPLL1 has failed. The active state (*High* or *Low*) of the LOS_ALARM pin is programmable and the pin can either be driven, or set to high impedance when non-active (Reg 7D refers).

Defaults

Each Register is given a defined default value at reset and these are listed in the Map and Description Tables. However, some read-only status registers may not necessarily show the same default values after reset as those given in the tables. This is because they reflect the status of the device which may have changed in the time it takes to carry out the read, or through reasons of pin configuration. In the same way, the default values given for shaded areas could also take different values to those stated.

Table 17 Register Map

Register Name RO = Read Only R/W = Read/Write	Address (hex)	Default (hex)	Data Bit 7 (msb)	6	5	4	3	2	1	0 (lsb)
chip_id (RO)	00	4E	chip_id[7:0], 8 LSBs of Chip ID							
	01	21	chip_id[15:8], 8 MSBs of Chip ID							
chip_revision (RO)	02	00	chip_revision[7:0]							
test_register1 (R/W)	03	14	Phase_alarm (RO)	Disable_180		Resync_ analog	Set to 0	8K Edge Polarity	Set to 0	Set to 0
sts_current_DPLL_frequency[7:0]	0C	00	Bits [7:0] of sts_current_DPLL_frequency							
(RO) [15:8]	0D	00	Bits [15:8] of sts_current_DPLL_frequencyy							
[18:16]	07	00						Bits [18:16] of sts_current_DPLL_frequency		
sts_reference_sources (RO) Alarm Status on inputs:SEC1 & 2	11	22			No Activity SEC2				No Activity SEC1	
cnfg_ref_source_frequency SEC1	22	00	divn_SEC1	lock8k_SEC1			reference_source_frequency_SEC1			
(R/W) SEC2	23	00	divn_SEC2	lock8k_SEC2			reference_source_frequency_SEC2			
cnfg_input_mode (R/W)	34	C2	auto_extsync_ en		XO_ edge			ip_sonsdhb		
cnfg_DPLL2_path (R/W)	35	40								
cnfg_dig_outputs_sonsdh (R/W)	38	14		dig2_sonsdh	dig1_sonsdh					
cnfg_digtial_frequencies (R/W)	39	08	digital2_frequency		digital1_frequency					
cnfg_differential_output (R/W)	3A	C2							Output 01 _LVDS_PECL	
cnfg_auto_bw_sel	3B	98	auto_BW_sel				DPLL1_lim_int			
cnfg_nominal_frequency [7:0]	3C	99	Bits[7:0] of cnfg_nominal_frequency							
(R/W) [15:8]	3D	99	Bits[15:8] of cnfg_nominal_frequency							
cnfg_DPLL_freq_limit (R/W) [7:0]	41	FF	Bits[7:0] of cnfg_DPLL_freq_limit							
cnfg_DPLL_freq_limit (R/W) [9:8]	42	03							Bits[9:8] cnfg_DPLL_freq_limit	
cnfg_freq_divn (R/W) [7:0].	46	FF	divn_value [7:0] (divide Input frequency by n)							
[13:8]	47	3F			divn_value [13:8] (divide Input frequency by n)					
cnfg_registers_source_select (R/W)	4B	00				DPLL1_DPLL2 _select				
cnfg_freq_lim_ph_loss	4D		freq_lim_ph_ loss							
cnfg_upper_threshold (R/W)	50	06	upper_threshold_value (Activity alarm, Leaky Bucket - set threshold)							
cnfg_lower_threshold (R/W)	51	04	lower_threshold_value (Activity alarm, Leaky Bucket - reset threshold)							
cnfg_bucket_size (R/W)	52	08	bucket_size_value (Activity alarm, Leaky Bucket - size)							
cnfg_decay_rate (R/W)	53	01							decay_rate_value (Activity alarm, Leaky Bucket - leak rate)	
cnfg_output_frequency(R/W) (02)	61	0A					output_freq_02			
(01)	62	00	output_freq_01							
(MFrSync/FrSync)	63	C0	MFrSync_en	FrSync_en						
cnfg_DPLL2_frequency (R/W)	64	00						DPLL2_frequency		
cnfg_DPLL1_frequency (R/W)	65	01		APLL2_for_ DPLL1_E1/ DS1	DPLL1_freq_to_APLL2			DPLL1_frequency		
cnfg_DPLL2_bw (R/W)	66	00							DPLL2_bandwidth	
cnfg_DPLL1_locked_bw (R/W)	67	10							DPLL1_locked_bandwidth	
cnfg_DPLL1_acq_bw (R/W)	69	11							DPLL1_acquisition_bandwidth	
cnfg_DPLL2_damping (R/W)	6A	13		DPLL2_PD2_gain_alog				DPLL2_damping		
cnfg_DPLL1_damping (R/W)	6B	14		DPLL1_PD2_gain_alog_8k				DPLL1_damping		
cnfg_DPLL2_PD2_gain (R/W)	6C	C2	DPLL2_PD2_ gain_enable					DPLL2_PD2_gain_digital		
cnfg_DPLL1_PD2_gain (R/W)	6D	C2	DPLL1_PD2_ gain_enable	DPLL1_PD2_gain_alog				DPLL1_PD2_gain_digital		
cnfg_phase_loss_fine_limit (R/W)	73	A2	fine_limit_en	noact_ph_loss	narrow_en			phase_loss_fine_limit		
cnfg_phase_loss_coarse_limit (R/W)	74	E5	coarse_lim_ phaseloss_en	wide_range_ en	multi_ph_resp		phase_loss_coarse_limit			
cnfg_ip_noise_window (R/W)	76	06	ip_noise_ window_en							
cnfg_sync_pulses (R/W)	7A	00	2k_8k_from_ DPLL2				8k_invert	8k_pulse	2k_invert	2k_pulse
cnfg_LOS_alarm (R/W)	7D	02						LOS_GPO_en	LOS_tristate_ en	LOS_ polarity
cnfg_protection (R/W)	7E	85	protection_value							

Register Descriptions

Address (hex): 00

Register Name	*chip_id*	Description	(RO) 8 least significant bits of the chip ID.	Default Value	0100 1110

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
chip_id[7:0], 8 LSBs of Chip ID							

Bit No.	Description	Bit Value	Value Description
[7:0]	*chip_id* Least significant byte of the 2-byte device ID.	4E (hex)	

Address (hex): 01

Register Name	*chip_id*	Description	(RO) 8 most significant bits of the chip ID.	Default Value	0010 0001

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
chip_id[15:8], 8 MSBs of Chip ID							

Bit No.	Description	Bit Value	Value Description
[7:0]	*chip_id* Most significant byte of the 2-byte device ID.	21 (hex)	

Address (hex): 02

Register Name	*chip_revision*	Description	(RO) Silicon revision of the device.	Default Value	0000 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
chip_revision[7:0]							

Bit No.	Description	Bit Value	Value Description
[7:0]	*chip_revision* Silicon revision of the device.	00 (hex)	

Address (hex): 03

Register Name	*test_register1*	**Description**	(R/W) Register containing various test controls (not normally used).	**Default Value**	00X1 0100

Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
phase_alarm	*disable_180*		*resync_analog*	Set to 0	*8k Edge Polarity*	Set to 0	Set to 0

Bit No.	**Description**	**Bit Value**	**Value Description**
7	*phase_alarm (*phase alarm (R/O)) Instantaneous result from DPLL1.	0 1	DPLL1 reporting phase locked. DPLL1 reporting phase lost.
6	*disable_180* Normally the DPLL will try to lock to the nearest edge (±180°) for the first 2 seconds when locking to a new reference. If the DPLL does not determine that it is phase locked after this time, then the capture range reverts to ±360°, which corresponds to frequency and phase locking. Forcing the DPLL into frequency locking mode may reduce the time to frequency lock to a new reference by up to two seconds. However, this may cause an unnecessary phase shift of up to 360° when the new and old references are very close in frequency and phase.	0 1	DPLL1 automatically determines frequency lock enable. DPLL1 forced to always frequency and phase lock.
5	Not used.	-	-
4	*resync_analog* (analog dividers re-synchronization) The analog output dividers include a synchronization mechanism to ensure phase lock at low frequencies between the input and the output.	0 1	Analog divider only synchronized during first 2 seconds after power-up. Analog dividers always synchronized.This keeps the clocks divided down from the APLL output, in sync with equivalent frequency digital clocks in the DPLL. Hence ensuring that 6.48 MHz output clocks, and above, are in sync with the DPLL even though only a 77.76 MHz clock drives the APLL.
3	*Set to 0* Test Control. Leave unchanged or set to 0.	0	-
2	*8k Edge Polarity* When Lock8k or DivN mode is selected for the current input SEC, this bit allows the system to lock on either the rising or the falling edge of the input clock.	0 1	Lock to falling clock edge. Lock to rising clock edge.
1	*Set to 0* Test Control. Leave unchanged or set to 0.	0	-
0	*Set to 0* Test Control. Leave unchanged or set to 0.	0	-

Address (hex): 07

Register Name	*sts_current_DPLL_frequency [18:16]*	Description	(RO) Bits [18:16] of the current DPLL frequency.	Default Value	0000 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
					Bits [18:16] of *sts_current_DPLL_frequency*		

Bit No.	Description	Bit Value	Value Description
[7:3]	Not used.	-	-
[2:0]	Bits [18:16] of *sts_current_DPLL_frequency* When Bit 4 (*DPLL1_DPLL2_select*) of Reg. 4B (*cnfg_registers_source_select*) = 0 the frequency for DPLL1 is reported. When this Bit 4 = 1 the frequency for DPLL2 is reported.	-	See register description of *sts_current_DPLL_frequency* at Reg. 0D.

Address (hex): 0C

Register Name	*sts_current_DPLL_frequency [7:0]*	Description	(RO) Bits [7:0] of the current DPLL frequency.	Default Value	0000 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bits [7:0] of *sts_current_DPLL_frequency*							

Bit No.	Description	Bit Value	Value Description
[7:0]	Bits [7:0] of *sts_current_DPLL_frequency* When Bit 4 (*DPLL1_DPLL2_select*) of Reg. 4B (*cnfg_registers_source_select*) = 0 the frequency for DPLL1 is reported. When this Bit 4 = 1 the frequency for DPLL2 is reported.	-	See register description of *sts_current_DPLL_frequency* at Reg. 0D.

Address (hex): 0D

Register Name	*sts_current_DPLL_frequency [15:8]*	Description	(RO) Bits [15:8] of the current DPLL frequency.	Default Value	0000 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bits [15:8] of *sts_current_DPLL_frequency*							

Bit No.	Description	Bit Value	Value Description
[7:0]	Bits [15:8] of *sts_current_DPLL_frequency* The value in this register is combined with the value in Reg. 0C and Reg. 07 to represent the current frequency offset of the DPLL. When Bit 4 (*DPLL1_DPLL2_select*) of Reg. 4B (*cnfg_registers_source_select*) = 0 the frequency for DPLL1 is reported. When this Bit 4 = 1 the frequency for DPLL2 is reported.	-	In order to calculate the ppm offset of the DPLL with respect to the crystal oscillator frequency, the value in Reg. 07, Reg. 0D and Reg. 0C need to be concatenated. This value is a 2's complement signed integer. The value multiplied by 0.0003068 dec. will give the value in ppm offset with respect to the XO frequency, allowing for any crystal calibration that has been performed, via *cnfg_nominal_frequency*, Reg. 3C and 3D. The value is actually the DPLL integral path value so it can be viewed as an average frequency, where the rate of change is related to the DPLL bandwidth. If Bit 3 of Reg. 3B is *High* then this value will freeze if the DPLL has been pulled to its min or max frequency.

Address (hex): 11

Register Name	*sts_reference_sources SEC1 & SEC2*	Description	(RO except for test when R/W) Reports any alarms active on inputs.	Default Value	0010 0010

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		No Activity SEC2 Input				*No Activity SEC1 Input*	

Bit No.	Description	Bit Value	Value Description
[7:6]	Not Used	-	-
5	*SEC2 Input Activity Alarm* Alarm indication from the activity monitors.	0 1	No alarm (input valid). Input has an active "no activity" alarm.
[3:2]	Not Used	-	-
1	*SEC1 Input Activity Alarm* Alarm indication from the activity monitors.	0 1	No alarm (input valid). Input has an active "no activity" alarm.
0	Not Used	-	-

Address (hex): 22

Register Name	*cnfg_ref_source_frequency SEC1*	**Description**	(R/W) Configuration of the frequency and input monitoring for input SEC<n>. For Reg. 22, <n> = 1.	**Default Value**	0000 XXXX Where XXXX is set by values on Pins IP_FREQ[2:0] and SONSDHB See Note in Description [3:0].

Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
divn_SEC<n>	*lock8k_SEC<n>*			*reference_source_frequency_SEC<n>*			

Bit No.	**Description**	**Bit Value**	**Value Description**
7	*divn_SEC<n>* This bit selects whether or not input SEC<n> is divided in the programmable pre-divider prior to being input to the DPLL and frequency monitor- see Reg. 46 and Reg. 47 (*cnfg_freq_divn*).	0 1	Input SEC<n> fed directly to DPLL and monitor. Input SEC<n> fed to DPLL and monitor via pre-divider.
6	*lock8k_SEC<n>* This bit selects whether or not input SEC<n> is divided in the preset pre-divider prior to being input to the DPLL. This results in the DPLL locking to the reference after it has been divided to 8 kHz. This bit is ignored when *divn_SEC<n>* is set (bit = 1).	0 1	Input SEC<n> fed directly to DPLL. Input SEC<n> fed to DPLL via preset pre-divider.
[5:4]	Not used.	-	-
[3:0]	*reference_source_frequency_SEC<n>* Programs the frequency of the SEC connected to input SEC<n>. If *divn_SEC<n>* is set then this value should be set to 0000 (8 kHz). *Note...The value on the pins IP_FREQ [2:0] and SONSDHB determines the default expected input frequency which, at power-up/reset is written to both cnfg_ref_source_frequency registers, giving each the same default value. The values in each register can, after the initialization period (251 ms after PORB goes High), be changed on an individual basis by writing to each register separately via the serial interface, however any subsequent reset will cause these registers' values to be overwritten by whatever value is on the pins at the time of the reset. See "Preconfiguring Inputs - Expected Input Frequency" and Table 4 on page 7.*	0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011-1111	8 kHz. 1544/2048 kHz (dependant on Bit 2 (*ip_sonsdhb*) in Reg. 34). 6.48 MHz. 19.44 MHz. 25.92 MHz. 38.88 MHz. 51.84 MHz. 77.76 MHz. Not used. 2 kHz. 4 kHz. Not used.

Address (hex): 23 *cnfg_ref_source_frequency SEC2* As Reg. 22, but for SEC2, i.e. <n> = 2 Default = 0000 0000

Address (hex): 34

Register Name	*cnfg_input_mode*	Description	(R/W) Register controlling various input modes of the device.	Default Value	1100 0010*

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		XO_edge			*ip_sonsdhb*		

Bit No.	Description	Bit Value	Value Description
[7:6]	Not used.	-	-
5	*XO_edge* If the 12.8 MHz oscillator module connected to REFCLK has one edge faster than the other, then for jitter performance reasons, the faster edge should be selected. This bit allows either the rising edge or the falling edge to be selected.	0 1	Device uses the rising edge of the external oscillator. Device uses the falling edge of the external oscillator.
[4:3]	Not used.	-	-
2	*ip_sonsdhb* Bit to configure input frequencies to be either SONET or SDH derived. This applies only to selections of 0001 (bin) in the *cnfg_ref_source_frequency* registers when the input frequency is either 1544 kHz or 2048 kHz. *The default value of Bit 2 is taken from the value of the SONSDHB pin at power-up.	0 1	SDH- inputs set to 0001 expected to be 2048 kHz. SONET- inputs set to 0001 expected to be 1544 kHz.
[1:0]	Not used.	-	-

Address (hex): 35

Register Name	*cnfg_DPLL2_path*	Description	(R/W) Register to configure the feedback mode of DPLL2.	Default Value	0100 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	DPLL2_dig_ feedback						

Bit No.	Description	Bit Value	Value Description
7	Not used.	-	-
6	*DPLL2_dig_feedback* Bit to select digital feedback mode for DPLL2.	0 1	DPLL2 in analog feedback mode. DPLL2 in digital feedback mode.
[5:0]	Not used.	-	-

Address (hex): 38

Register Name	*cnfg_dig_outputs_sonsdh*	Description	Configures *Digital1* and *Digital2* output frequencies to be SONET or SDH compatible frequencies.	Default Value	0001 0100

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	dig2_sonsdh	*dig1_sonsdh*					

Bit No.	Description	Bit Value	Value Description
7	Not used.	-	-
6	*dig2_sonsdh* Selects whether the frequencies generated by the *Digital2* frequency generator are SONET derived or SDH. Default value of this bit is set by the SONSDHB pin at power-up.	1 0	*Digital2* can be selected from 1,544/3,088/6,176/12,352 kHz. *Digital2* can be selected from 2,048/4,096/8,192/16,384 kHz.
5	*dig1_sonsdh* Selects whether the frequencies generated by the *Digital1* frequency generator are SONET derived or SDH. Default value of this bit is set by the SONSDHB pin at power-up.	1 0	*Digital1* can be selected from 1,544/3,088/6,176/12,352 kHz. *Digital1* can be selected from 2,048/4,096/8,192/16,384 kHz.
[4:0]	Not used.	-	-

Address (hex): 39

Register Name	*cnfg_digtial_frequencies*	Description	(R/W) Configures the actual frequencies of *Digital1* & *Digital2.*	Default Value	0000 1000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
digital2_frequency		*digital1_frequency*					

Bit No.	Description	Bit Value	Value Description
[7:6]	*digital2_frequency* Configures the frequency of *Digital2*. Whether this is SONET or SDH based is configured by Bit 6 (*dig2_sonsdh*) of Reg. 38.	00 01 10 11	*Digital2* set to 1,544 kHz or 2,048 kHz. *Digital2* set to 3,088 kHz or 4,096 kHz. *Digital2* set to 6,176 kHz or 8,192 kHz. *Digital2* set to 12,353 kHz or 16,384 kHz.
[5:4]	*digital1_frequency* Configures the frequency of *Digital1*. Whether this is SONET or SDH based is configured by Bit 5 (*dig1_sonsdh*) of Reg. 38.	00 01 10 11	*Digital1* set to 1,544 kHz or 2,048 kHz. *Digital1* set to 3,088 kHz or 4,096 kHz. *Digital1* set to 6,176 kHz or 8,192 kHz. *Digital1* set to 12,353 kHz or 16,384 kHz.
[3:0]	Not used.		

Address (hex): 3A

Register Name	*cnfg_differential_output*	Description	(R/W) Configures the electrical compatibility of the differential output driver to be 3 V PECL or 3 V LVDS.	Default Value	1100 0010

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
						Output O1_LVDS_PECL	

Bit No.	Description	Bit Value	Value Description
[7:2]	Not used.	-	-
[1:0]	*Output O1_LVDS_PECL* Selection of the electrical compatibility of Output O1 between 3 V PECL and 3 V LVDS.	00 01 10 11	Output O1 disabled. Output O1 3 V PECL compatible. Output O1 3 V LVDS compatible. Not used.

Address (hex): 3B

Register Name	*cnfg_auto_bw_sel*	Description	(R/W) Register to select automatic bandwidth selection for DPLL1 path	Default Value	1001 1000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
auto_BW_sel				DPLL1_lim_int			

Bit No.	Description	Bit Value	Value Description
7	*auto_BW_sel* Bit to select locked bandwidth (Reg. 67) or acquisition bandwidth (Reg. 69) for DPLL1.	1 0	Automatically selects either locked or acquisition bandwidth as appropriate. Always selects locked bandwidth.
[6:4]	Not used.	-	-
3	*DPLL1_lim_int* When set to 1 the integral path value of DPLL1 is limited or frozen when DPLL1 reaches either min. or max. frequency. This can be used to minimize subsequent overshoot when the DPLL is pulling in. Note that when this bit is enabled, the reported frequency value, via *current_DPLL_freq* (Reg. 0C, 0D and 07), is also frozen.	1 0	DPLL value frozen. DPLL not frozen.
[2:0]	Not used.	-	-

Address (hex): 3C

Register Name	*cnfg_nominal_frequency [7:0]*	**Description**	(R/W) Bits [7:0] of the register used to calibrate the crystal oscillator used to clock the device.	**Default Value**	1001 1001

Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
cnfg_nominal_frequency_value[7:0]							

Bit No.	**Description**	**Bit Value**	**Value Description**
[7:0]	*cnfg_nominal_frequency_value[7:0].*	-	See register description of Reg. 3D (*cnfg_nominal_frequency_value[15:8]*).

Address (hex): 3D

Register Name	*cnfg_nominal_frequency [15:8]*	**Description**	(R/W) Bits [15:8] of the register used to calibrate the crystal oscillator used to clock the device.	**Default Value**	1001 1001

Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
cnfg_nominal_frequency_value[15:8]							

Bit No.	**Description**	**Bit Value**	**Value Description**
[7:0]	*cnfg_nominal_frequency_value[15:8]* This register is used in conjunction with Reg. 3C (*cnfg_nominal_frequency_value[7:0].*) to be able to offset the frequency of the crystal oscillator by up to +514 ppm and –771 ppm. The default value represents 0 ppm offset from 12.800 MHz. This value is an unsigned integer.	-	In order to program the ppm offset of the crystal oscillator frequency, the value in Reg. 3C and Reg. 3D need to be concatenated. This value is an unsigned integer. The value multiplied by 0.0196229 dec. will give the value in ppm. To calculate the absolute value, the default 39321 (9999 hex) needs to be subtracted.

Address (hex): 41

Register Name	*cnfg_DPLL_freq_limit [7:0]*	Description	(R/W) Bits [7:0] of the DPLL frequency limit register.	Default Value	1111 1111

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bits[7:0] of *cnfg_DPLL_freq_limit*							

Bit No.	Description	Bit Value	Value Description
[7:0]	Bits [7:0] of *cnfg_DPLL_freq_limit* This register defines the extent of frequency offset to which DPLL1 will track a source before limiting- i.e. it represents the pull-in range of the DPLLs. The offset of the device is determined by the frequency offset of the DPLL when compared to the offset of the external crystal oscillator clocking the device. If the oscillator is calibrated using *cnfg_nominal_frequency* Reg. 3C and 3D, then this calibration is automatically taken into account. The DPLL frequency limit limits the offset of the DPLL when compared to the calibrated oscillator frequency.	-	In order to calculate the frequency limit in ppm, Bits [1:0] of Reg. 42 and Bits [7:0] of Reg. 41 need to be concatenated. This value is a unsigned integer and represents limit *both* positive and negative in ppm. The value multiplied by 0.078 will give the value in ppm.

Address (hex): 42

Register Name	*cnfg_DPLL_freq_limit [9:8]*	Description	(R/W) Bits [9:8] of the DPLL frequency limit register.	Default Value	0000 0011

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
						Bits [9:8] of *cnfg_DPLL_freq_limit*	

Bit No.	Description	Bit Value	Value Description
[7:2]	Not used.	-	-
[1:0]	Bits [9:8] of *cnfg_DPLL_freq_limit.*	-	See Reg. 41 (*cnfg_DPLL_freq_limit*) for details.

Address (hex): 46

Register Name	*cnfg_freq_divn [7:0].*	Description	(R/W) Bits [7:0] of the division factor for inputs using the DivN feature.	Default Value	1111 1111

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
divn_value [7:0] (divide input frequency by n)							

Bit No.	Description	Bit Value	Value Description
[7:0]	*divn_value[7:0].*	-	See Reg. 47 (*cnfg_freq_divn {13:8]*) for details.

Address (hex): 47

Register Name	*cnfg_freq_divn [13:8]*	Description	(R/W) Bits [13:8] of the division factor for inputs using the DivN feature.	Default Value	0011 1111

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		divn_value [13:8] (divide input frequency by n)					

Bit No.	Description	Bit Value	Value Description
[7:6]	Not used.	-	-
[5:0]	*divn_value[13:8]* This register, in conjunction with Reg. 46 (*cnfg_freq_divn*) represents the integer value by which to divide inputs that use the DivN pre-divider. The DivN feature supports input frequencies up to a maximum of 100 MHz; therefore, the maximum value that should be written to this register is 30D3 hex (12499 dec). Use of higher DivN values may result in unreliable behavior.	-	The input frequency will be divided by the value in this register plus 1. i.e. to divide by 8, program a value of 7.

Address (hex): 4B

Register Name	*cnfg_registers_source_select*	Description	(R/W) Register to select the source of many of the registers.	Default Value	0000 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
			DPLL1_DPLL2_ select				

Bit No.	Description	Bit Value	Value Description
[7:5]	Not used.	-	-

Address (hex): 4B (cont...)

Register Name	*cnfg_registers_source_select*	Description	(R/W) Register to select the source of many of the registers.	Default Value	0000 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
			DPLL1_DPLL2_ select				

Bit No.	Description	Bit Value	Value Description
4	*DPLL1_DPLL2_select* Bit to select between many of the registers associated with DPLL1 or DPLL2 e.g. frequency registers.	0 1	DPLL1 registers selected. DPLL2 registers selected.
[3:0]	Not used.	-	-

Address (hex): 4D

Register Name	*cnfg_freq_lim_ph_loss*	Description	(R/W) Register to enable the phase lost indication when DPLL hits its hard frequency limit.	Default Value	1000 1110

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
freq_lim_ph_ loss							

Bit No.	Description	Bit Value	Value Description
7	*freq_lim_ph_loss* Bit to enable the phase lost indication when the DPLL hits its *hard* frequency limit as programmed in Reg. 41 and Reg. 42 (*cnfg_DPLL_freq_limit*). This results in the DPLL entering the phase lost state any time the DPLL tracks to the extent of its hard limit.	0 1	Phase lost/locked determined normally. Phase lost forced when DPLL tracks to hard limit.
[6:0]	Not used.	-	-

Address (hex): 50

Register Name	*cnfg_upper_threshold*	Description	(R/W) Register to program the activity alarm setting limit for the Leaky Bucket Configuration.	Default Value	0000 0110

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
upper_threshold_value (Activity alarm, Leaky Bucket - set threshold)							

Bit No.	Description	Bit Value	Value Description
[7:0]	*upper_threshold_value* The Leaky Bucket operates on a 128 ms cycle. If, during a cycle, it detects that an input has either failed or has been erratic, then for each cycle in which this occurs, the accumulator is incremented by 1, and for each period of 1, 2, 4, or 8 cycles, as programmed in Reg. 53 (*cnfg_decay_rate*), in which this does not occur, the accumulator is decremented by 1. When the accumulator count reaches the value programmed as the *upper_threshold_value,* the Leaky Bucket raises an input inactivity alarm.	-	Value at which the Leaky Bucket will raise an inactivity alarm.

Address (hex): 51

Register Name	*cnfg_lower_threshold*	Description	(R/W) Register to program the activity alarm resetting limit for the Leaky Bucket Configuration.	Default Value	0000 0100

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
lower_threshold_value (Activity alarm, Leaky Bucket - reset threshold)							

Bit No.	Description	Bit Value	Value Description
[7:0]	*lower_threshold_value* The Leaky Bucket operates on a 128 ms cycle. If, during a cycle, it detects that an input has either failed or has been erratic, then for each cycle in which this occurs, the accumulator is incremented by 1, and for each period of 1, 2, 4, or 8 cycles, as programmed in Reg. 53 (*cnfg_decay_rate*), in which this does not occur, the accumulator is decremented by 1. The *lower_threshold_value* is the value at which the Leaky Bucket will reset an inactivity alarm.	-	Value at which the Leaky Bucket will reset an inactivity alarm.

Address (hex): 52

Register Name	*cnfg_bucket_size*	Description	(R/W) Register to program the maximum size limit for the Leaky Bucket Configuration.	Default Value	0000 1000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
bucket_size_value (Activity alarm, Leaky Bucket - size)							

Bit No.	Description	Bit Value	Value Description
[7:0]	*bucket_size_value* The Leaky Bucket operates on a 128 ms cycle. If, during a cycle, it detects that an input has either failed or has been erratic, then for each cycle in which this occurs, the accumulator is incremented by 1, and for each period of 1, 2, 4, or 8 cycles, as programmed in Reg. 53 (*cnfg_decay_rate*), in which this does not occur, the accumulator is decremented by 1. The number in the Bucket cannot exceed the value programmed into this register.	-	Value at which the Leaky Bucket will stop incrementing, even with further inactive periods.

Address (hex): 53

Register Name	*cnfg_decay_rate*	Description	(R/W) Register to program the "decay" or "leak" rate for the Leaky Bucket Configuration.	Default Value	0000 0001

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
						decay_rate_value (Activity alarm, Leaky Bucket - leak rate)	

Bit No.	Description	Bit Value	Value Description
[7:2]	Not used.	-	-
[1:0]	*decay_rate_value* The Leaky Bucket operates on a 128 ms cycle. If, during a cycle, it detects that an input has either failed or has been erratic, then for each cycle in which this occurs, the accumulator is incremented by 1, and for each period of 1, 2, 4, or 8 cycles, as programmed in this register, in which this does not occur, the accumulator is decremented by 1. The Leaky Bucket can be programmed to "leak" or "decay" at the same rate as the "fill" cycle, or effectively at one half, one quarter, or one eighth of the fill rate.	00 01 10 11	Bucket decay rate of 1 every 128 ms. Bucket decay rate of 1 every 256 ms. Bucket decay rate of 1 every 512 ms. Bucket decay rate of 1 every 1,024 ms.

Address (hex): 61

Register Name	*cnfg_output_frequency (Output 02)*	**Description**	(R/W) Register to configure and enable the frequencies available on Output 02.	**Default Value**	0000 XXXX Where XXXX is set by values on Pins 02_FREQ[2:0], SONSDHB and 01_FREQ[2:0]. See Note in [3:0] description.

Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
				output_freq_02			

Bit No.	**Description**	**Bit Value**	**Value Description**
[7:4]	Not used.	-	-
[3:0]	*output_freq_02* Configuration of the output frequency available at Output 02. Many of the frequencies available are dependent on the frequencies of the APLL1 and the APLL2. These are configured in Reg. 64 and Reg. 65. See “Output Frequency Selection by Register Programming” on page 17. *Note...The values on the pins 02_FREQ [2:0], SONSDHB and 01_FREQ[2:0] determine the default output frequency for Output 02, which, at power-up/reset is written to the cnfg_output_frequency register. The value in this register can, after the initialization period (251 ms after PORB goes High), be changed by writing to it via the serial interface, however any subsequent reset will cause this register’s value to be overwritten by whatever value is on the pins at the time of the reset. See “Output Frequency Selection by Hardware” and Table 7 on page 18.*	0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 1100 1101 1110 1111	Output disabled. 2 kHz. 8 kHz. Digital2 (Reg. 39 *cnfg_digital_frequencies*). Digital1 (Reg. 39 *cnfg_digital_frequencies*). APLL1 frequency/48. APLL1 frequency/16. APLL1 frequency/12. APLL1 frequency/8. APLL1 frequency/6. APLL1 frequency/4. APLL2 frequency/64. APLL2 frequency/48. APLL2 frequency/16. APLL2 frequency/8. APLL2 frequency/4.

Address (hex): 62

Register Name	*cnfg_output_frequency (Output 01)*	**Description**	(R/W) Register to configure and enable the frequencies available on Output 01.	**Default Value**	0000 XXXX Where XXXX is set by values on Pins 02_FREQ[2:0] and SONSDHB, See Note in [3:0] description.

Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
output_freq_01							

Bit No.	**Description**	**Bit Value**	**Value Description**
[7:4]	*output_freq_01* Configuration of the output frequency available at Output 01. Many of the frequencies available are dependent on the frequencies of the APLL1 and the APLL2. These are configured in Reg. 64 and Reg. 65. See "Output Frequency Selection by Register Programming" on page 17. *Note...The values on the pins 01_FREQ [2:0] and SONSDHB determine the default output frequency for Output 01, which, at power-up/reset is written to the cnfg_output_frequency register. The value in this register can, after the initialization period (251 ms after PORB goes High), be changed by writing to it via the serial interface, however any subsequent reset will cause this register's value to be overwritten by whatever value is on the pins at the time of the reset. See "Output Frequency Selection by Hardware" and Table 6 on page 18.*	0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 1100 1101 1110 1111	Output disabled. 2 kHz. 8 kHz. APLL1 frequency/2. Digital1 (Reg. 39 *cnfg_digital_frequencies*). APLL1 frequency. APLL1 frequency/16. APLL1 frequency/12. APLL1 frequency/8. APLL1 frequency/6. APLL1 frequency/4. APLL2 frequency/64. APLL2 frequency/48. APLL2 frequency/16. APLL2 frequency/8. APLL2 frequency/4.
[3:0]	Not used.	-	-

Address (hex): 63

Register Name	*cnfg_output_frequency (MFrSync/FrSync)*	**Description**	(R/W) Register to configure and enable the frequencies available on outputs MFrSync and FrSync.	**Default Value**	1100 0000

Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
MFrSync_en	*FrSync_en*						

Bit No.	**Description**	**Bit Value**	**Value Description**
7	*MFrSync_en* Register bit to enable the 2 kHz Sync output (MFrSync).	0 1	Output MFrSync disabled. Output MFrSync enabled.

Address (hex): 63 (cont...)

Register Name	*cnfg_output_frequency (MFrSync/FrSync)*	Description	(R/W) Register to configure and enable the frequencies available on outputs MFrSync and FrSync.	Default Value	1100 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MFrSync_en	*FrSync_en*						

Bit No.	Description	Bit Value	Value Description
6	*FrSync_en* Register bit to enable the 8 kHz Sync output (FrSync).	0 1	Output FrSync disabled. Output FrSync enabled.
[5:0]	Not used.	-	-

Address (hex): 64

Register Name	*cnfg_DPLL2_frequency*	Description	(R/W) Register to configure DPLL2 Frequency	Default Value	0000 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
					DPLL2_frequency		

Bit No.	Description	Bit Value	Value Description
[7:4]	Not used.	-	-
[2:0]	*DPLL2_frequency* Register to configure the frequency of operation of DPLL2. The frequency of DPLL2 will also affect the frequency of the APLL2 which, in turn, affects the frequencies available at outputs 01 and 02 see Reg. 61 and Reg. 62. It is also possible to not use DPLL2 at all, but use the APLL2 to run directly from DPLL1 output, see Reg. 65 (*cnfg_DPLL1_frequency*). If any frequencies are required from the APLL2 then DPLL2 should not be squelched, as the APLL2 input is squelched and the APLL2 will free run.	000 001 010 011 100 101 110 111	DPLL2 squelched (clock off). 77.76 MHz (OC-N rates), APLL2 frequency = 311.04 MHz. 12E1, APLL2 frequency = 98.304 MHz. 16E1, APLL2 frequency = 131.072 MHz. 24DS1, APLL2 frequency = 148.224 MHz. 16DS1, APLL2 frequency = 98.816 MHz. E3, APLL2 frequency = 274.944 MHz. DS3, APLL2 frequency = 178.944 MHz.

Address (hex): 65

Register Name	*cnfg_DPLL1_frequency*	Description	(R/W) Register to configure DPLL1 and MUX2 parameters.	Default Value	0000 0001

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	APLL2_for_ DPLL1_E1/DS1	*DPLL1_freq_to_APLL2*			*DPLL1_frequency*		

Bit No.	Description	Bit Value	Value Description
7	Not used.	-	-
6	*APLL2_for_DPLL1_E1/DS1* Register bit to control MUX2 which selects whether the APLL2 takes its input from DPLL2 or DPLL1. If DPLL1 is selected then the frequency is controlled by Bits [5:4], *DPLL1_freq_to_APLL2*.	0 1	APLL2 takes its input from DPLL2. APLL2 takes its input from DPLL1.
[5:4]	*DPLL1_freq_to_APLL2* Register to select the frequency/mode of DPLL1 which is driven to the APLL2 when selected by Bit 6, *APLL2_for_DPLL1_E1/DS1*.	00 01 10 11	12E1, APLL2 frequency = 98.304 MHz. 16E1, APLL2 frequency = 131.072 MHz. 24DS1, APLL2 frequency = 148.224 MHz. 16DS1, APLL2 frequency = 98.816 MHz.
3	Not used.	-	-
[2:0]	*DPLL1_frequency* Register to configure the frequency of operation of DPLL1/APLL1. This register affects the frequencies available at outputs 01 and 02, see Reg. 61 and Reg. 62.	000 001 010 011 100 101 110 111	77.76 MHz, digital feedback, APLL1 frequency = 311.04 MHz. 77.76 MHz, analog feedback, (via APLL3) APLL1 frequency = 311.04 MHz. 12E1, APLL1 frequency = 98.304 MHz. 16E1, APLL1 frequency = 131.072 MHz. 24DS1, APLL1 frequency = 148.224 MHz. 16DS1, APLL1 frequency = 98.816 MHz. Not used. Not used. Note...001 is the only selection that does not bypass APLL3. All other selections use digital feedback.

Address (hex): 66

Register Name	*cnfg_DPLL2_bw*	Description	(R/W) Register to configure the bandwidth of DPLL2.	Default Value	0000 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
						DPLL2_bandwidth	

Bit No.	Description	Bit Value	Value Description
[7:2]	Not used.	-	-

Address (hex): 66 (cont...)

Register Name	*cnfg_DPLL2_bw*	Description	(R/W) Register to configure the bandwidth of DPLL2.	Default Value	0000 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
						DPLL2_bandwidth	

Bit No.	Description	Bit Value	Value Description
[1:0]	*DPLL2_bandwidth* Register to configure the bandwidth of DPLL2.	00 01 10 11	DPLL2 18 Hz bandwidth. DPLL2 35 Hz bandwidth. DPLL2 70 Hz bandwidth. Not used.

Address (hex): 67

Register Name	*cnfg_DPLL1_locked_bw*	Description	(R/W) Register to configure the bandwidth of DPLL1, when phase locked to an input.	Default Value	0001 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
						DPLL1_locked_bandwidth	

Bit No.	Description	Bit Value	Value Description
[7:2]	Not used.	-	-
[1:0]	DPLL1_*locked_bandwidth* Register to configure the bandwidth of DPLL1 when locked to an input reference. Reg. 3B Bit 7 is used to control whether this bandwidth is used all of the time or automatically switched to when phase locked.	11 00 01 10	DPLL1, 18 Hz locked bandwidth. DPLL1, 35 Hz locked bandwidth. DPLL1, 70 Hz locked bandwidth. Not used.

Address (hex): 69

Register Name	*cnfg_DPLL1_acq_bw*	Description	(R/W) Register to configure the bandwidth of DPLL1, when not phase locked to an input.	Default Value	0001 0001

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
						DPLL1_acquisition_bandwidth	

Bit No.	Description	Bit Value	Value Description
[7:4]	Not used.	-	-

Address (hex): 69 (cont...)

Register Name	*cnfg_DPLL1_acq_bw*	Description	(R/W) Register to configure the bandwidth of DPLL1, when not phase locked to an input.	Default Value	0001 0001

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
						DPLL1_acquisition_bandwidth	

Bit No.	Description	Bit Value	Value Description
[3:0]	*DPLL1_acquisition_bandwidth* Register to configure the bandwidth of DPLL1 when acquiring phase lock on an input reference. Reg. 3B Bit 7 is used to control whether this bandwidth is not used or automatically switched to when not phase locked.	11 00 01 10	DPLL1, 18 Hz acquisition bandwidth. DPLL1, 35 Hz acquisition bandwidth. DPLL1, 70 Hz acquisition bandwidth. Not used.

Address (hex): 6A

Register Name	*cnfg_DPLL2_damping*	Description	(R/W) Register to configure the damping factor of DPLL2, along with the gain of Phase Detector 2 in some modes.	Default Value	0001 0011

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	DPLL2_PD2_gain_alog				*DPLL2_damping*		

Bit No.	Description	Bit Value	Value Description
7	Not used.	-	-
[6:4]	*DPLL2_PD2_gain_alog* Register to control the gain of the Phase Detector 2 This setting is only used if Reg. 6C Bit 7, *cnfg_DPLL2_PD2_gain* is enabled.	-	Gain value of the Phase Detector 2 when locking to an 8 kHz reference in analog feedback mode.
3	Not used.	-	-

Address (hex): 6A (cont...)

Register Name	*cnfg_DPLL2_damping*	Description	(R/W) Register to configure the damping factor of DPLL2, along with the gain of Phase Detector 2 in some modes.	Default Value	0001 0011

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	DPLL2_PD2_gain_alog				*DPLL2_damping*		

Bit No.	Description	Bit Value	Value Description		
[2:0]	*DPLL2_damping* Register to configure the damping factor of DPLL2. The bit values correspond to different damping factors, depending on the bandwidth selected. The Gain Peak for the Damping Factors given in the Value Description (right) are tabulated below:		**Damping Factor for Bandwidth of 18 Hz:**	**Damping Factor for Bandwidth of 35 Hz:**	**Damping Factor for Bandwidth of 70 Hz:**
		001	1.2	1.2	1.2
		010	2.5	2.5	2.5
		011	5	5	5
		100	5	10	10
		101	5	10	20

Damping Factor	Gain Peak
1.2	0.4 dB
2.5	0.2 dB
5	0.1 dB
10	0.06 dB
20	0.03 dB

Address (hex): 6B

Register Name	*cnfg_DPLL1_damping*	Description	(R/W) Register to configure the damping factor of DPLL1, along with the gain of the Phase Detector 2 in some modes.	Default Value	0001 0100

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	DPLL1_PD2_gain_alog_8k				*DPLL1_damping*		

Bit No.	Description	Bit Value	Value Description
7	Not used.	-	-
[6:4]	*DPLL1_PD2_gain_alog_8k* Register to control the gain of the Phase Detector 2 when locking to a reference of 8 kHz or less in analog feedback mode. This setting is only used if automatic gain selection is enabled in Reg. 6D Bit 7, *cnfg_DPLL1_PD2_gain*.	-	Gain value of the Phase Detector 2 when locking to an 8 kHz reference in analog feedback mode.
3	Not used.	-	-

Address (hex): 6B (cont...)

Register Name	*cnfg_DPLL1_damping*	Description	(R/W) Register to configure the damping factor of DPLL1, along with the gain of the Phase Detector 2 in some modes.	Default Value	0001 0100

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	DPLL1_PD2_gain_alog_8k				*DPLL1_damping*		

Bit No.	Description	Bit Value	Value Description		
[2:0]	*DPLL1_damping* Register to configure the damping factor of DPLL1. The bit values correspond to different damping factors, depending on the bandwidth selected. The Gain Peak for the Damping Factors given in the Value Description (right) are the same as those tabulated in the description for Reg. 6A.		**Damping Factor for Bandwidth of 18 Hz:**	**Damping Factor for Bandwidth of 35 Hz:**	**Damping Factor for Bandwidth of 70 Hz:**
		001	1.2	1.2	1.2
		010	2.5	2.5	2.5
		011	5	5	5
		100	5	10	10
		101	5	10	20

Address (hex): 6C

Register Name	*cnfg_DPLL2_PD2_gain*	Description	(R/W) Register to configure the gain of Phase Detector 2 in some modes for DPLL2.	Default Value	1100 0010

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DPLL2_PD2_ gain_enable					*DPLL2_PD2_gain_digital*		

Bit No.	Description	Bit Value	Value Description
7	*DPLL2_PD2_gain_enable*	0 1	DPLL2 Phase Detector 2 not used. DPLL2 Phase Detector 2 gain enabled and choice of gain determined according to the locking mode: - digital feedback mode - analog feedback mode
[6:3]	Not used.	-	-
[2:0]	*DPLL2_PD2_gain_digital* Register to control the gain of Phase Detector 2 when locking in digital feedback mode. This setting is always used if gain is disabled in Bit 7, *DPLL2_PD2_gain_enable*.	-	Gain value of Phase Detector 2 when locking in digital feedback mode.

Address (hex): 6D

Register Name	*cnfg_DPLL1_PD2_gain*	**Description**	(R/W) Register to configure the gain of Phase Detector 2 in some modes for DPLL1.	**Default Value**	1100 0010

Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
DPLL1_PD2_gain_enable	*DPLL1_PD2_gain_alog*				*DPLL1_PD2_gain_digital*		

Bit No.	**Description**	**Bit Value**	**Value Description**
7	*DPLL1_PD2_gain_enable*	0	DPLL1 Phase Detector 2 not used.
		1	DPLL1 Phase Detector 2 gain enabled and choice of gain determined according to the locking mode: - digital feedback mode - analog feedback mode - analog feedback at 8 kHz
[6:4]	*DPLL1_PD2_gain_alog* Register to control the gain of Phase Detector 2 when locking to a reference, higher than 8 kHz, in analog feedback mode. This setting is not used if automatic gain selection is disabled in Bit 7, *DPLL1_PD2_gain_enable*.	-	Gain value of Phase Detector 2 when locking to a high frequency reference in analog feedback mode.
3	Not used.	-	-
[2:0]	*DPLL1_PD2_gain_digital* Register to control the gain of Phase Detector 2 when locking to a reference in digital feedback mode. Automatic gain selection must be enabled (Bit 7, *DPLL1_PD2_gain_enable*), for *DPLL1_PD2_gain_digital* to have any effect.	-	Gain value of Phase Detector 2 when locking to any reference in digital feedback mode.

Address (hex): 73

Register Name	*cnfg_phase_loss_fine_limit*	**Description**	(R/W) Register to configure some of the parameters of the DPLL phase detectors.	**Default Value**	1010 0010

Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
fine_limit_en	*noact_ph_loss*	*narrow_en*			*phase_loss_fine_limit*		

Bit No.	**Description**	**Bit Value**	**Value Description**
7	*fine_limit_en* Register bit to enable the *phase_loss_fine_limit* Bits [2:0]. When disabled, phase lock/loss is determined by the other means within the device. This must be disabled when multi-UI jitter tolerance is required, see Reg. 74, *cnfg_phase_loss_course_limit*.	0 1	Phase loss indication only triggered by other means. Phase loss triggered when phase error exceeds the limit programmed in *phase_loss_fine_limit*, Bits [2:0].
6	*noact_ph_loss* The DPLL detects that an input has failed very rapidly. Normally, when the DPLL detects this condition, it does not consider phase lock to be lost and will phase lock to the nearest edge (±180°) when a source becomes available again, hence giving tolerance to missing cycles. If phase loss is indicated, then frequency and phase locking is instigated (±360° locking). This bit can be used to force the DPLL to indicate phase loss immediately when no activity is detected.	0 1	No activity on reference does not trigger phase lost indication. No activity triggers phase lost indication.
5	*narrow_en* (test control bit) Set to 1 (default value).	0 1	Do not use. Set to 1.
[4:3]	Not used.	-	-
[2:0]	*phase_loss_fine_limit* When enabled by Bit 7, this register coarsely sets the phase limit at which the device indicates phase lost or locked. The default value of 2 (010) gives a window size of around ±(90° to 180°). The phase position of the inputs to the DPLL has to be within the window limit for 1 – 2 seconds before the device indicates phase lock. If it is outside the window for any time then phase loss is immediately indicated. For most cases the default value of 2 (010) is satisfactory. The window size changes in proportion to the value, so a value of 1 (001) will give a narrow phase acceptance or lock window of approximately ±(45° to 90°).	000 001 010 011 100 101 110 111	Do not use. Indicates phase loss continuously. Small phase window for phase lock indication. Recommended value.))) Larger phase window for phase lock indication.))

Address (hex): 74

Register Name	*cnfg_phase_loss_coarse_limit*	Description	(R/W) Register to configure some of the parameters of DPLL phase detectors.	Default Value	1110 0101

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
coarse_lim_ phaseloss_en	*wide_range_en*	*multi_ph_resp*		*phase_loss_coarse_limit*			

Bit No.	Description	Bit Value	Value Description
7	*coarse_lim_phaseloss_en* Register bit to enable the coarse phase detector, whose range is determined by *phase_loss_coarse_limit* Bits [3:0]. This register sets the limit in the number of input clock cycles (UI) that the input phase can move by before the DPLL indicates phase lost.	0 1	Phase loss not triggered by the coarse phase lock detector. Phase loss triggered when phase error exceeds the limit programmed in *phase_loss_coarse_limit*, Bits [3:0].
6	*wide_range_en* To enable the device to be tolerant to large amounts of applied jitter and still do direct phase locking at the input frequency rate (up to 77.76 MHz), a wide range phase detector and phase lock detector is employed. This bit enables the wide range phase detector. This allows the device to be tolerant to, and therefore keep track of, drifts in input phase of many cycles (UI). The range of the phase detector is set by the same register used for the phase loss coarse limit (Bits [3:0]).	0 1	Wide range phase detector off. Wide range phase detector on.
5	*multi_ph_resp* Enables the phase result from the coarse phase detector to be used in the DPLL algorithm. Bit 6 should also be set when this is activated. The coarse phase detector can measure and keep track over many thousands of input cycles, thus allowing excellent jitter and wander tolerance. This bit enables that phase result to be used in the DPLL algorithm, so that a large phase measurement gives a faster pull-in of the DPLL. If this bit is not set then the phase measurement is limited to ±360° which can give a slower pull-in rate at higher input frequencies, but could also be used to give less overshoot. Setting this bit in direct locking mode, for example with a 19.44 MHz input, would give the same dynamic response as a 19.44 MHz input used with 8 k locking mode, where the input is divided down internally to 8 kHz first.	0 1	DPLL phase detector limited to ±360° (±1 UI). However it will still remember its original phase position over many thousands of UI if Bit 6 is set. DPLL phase detector also uses the full coarse phase detector result. It can now measure up to: ±360° x 8191 UI = ±2,948,760°.
4	Not used.	-	-

Address (hex): 74 (cont...)

Register Name	*cnfg_phase_loss_coarse_limit*	Description	(R/W) Register to configure some of the parameters of DPLL phase detectors.	Default Value	1110 0101

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
coarse_lim_ phaseloss_en	*wide_range_en*	*multi_ph_resp*		*phase_loss_coarse_limit*			

Bit No.	Description	Bit Value	Value Description
[3:0]	*phase_loss_coarse_limit* Sets the range of the coarse phase loss detector and the coarse phase detector. When locking to a high frequency signal, and jitter tolerance greater than 0.5 UI is required, then the DPLL can be configured to track phase errors over many input clock periods. This is particularly useful with very low bandwidths. This register configures how many UI over which the input phase can be tracked. It also sets the range of the coarse phase loss detector, which can be used with or without the multi-UI phase capture range capability. This register value is used by Bits 6 and 7.	0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 1100-1111	Input phase error tracked over ±1 UI. Input phase error tracked over ±3 UI. Input phase error tracked over ±7 UI. Input phase error tracked over ±15 UI. Input phase error tracked over ±31 UI. Input phase error tracked over ±63 UI. Input phase error tracked over ±127 UI. Input phase error tracked over ±255 UI. Input phase error tracked over ±511 UI. Input phase error tracked over ±1023 UI. Input phase error tracked over ±2047 UI. Input phase error tracked over ±4095 UI. Input phase error tracked over ±8191 UI.

Address (hex): 76

Register Name	*cnfg_ip_noise_window*	Description	(R/W) Register to enable the noise rejection function for low frequency inputs.	Default Value	0000 0110

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ip_noise_ window_en							

Bit No.	Description	Bit Value	Value Description
7	*ip_noise_window_en* Register bit to enable a window of 5% tolerance around low-frequency inputs (2, 4 and 8 kHz). This feature ensures that any edge caused by noise outside the 5% window where the edge is expected will not be considered within the DPLL. This reduces any possible phase hit when a low-frequency connection is removed and contact bounce is possible.	0 1	DPLL considers all edges for phase locking. DPLL ignores input edges outside a 95% to 105% window.
[6:0]	Not used.	-	-

Address (hex): 7A

Register Name	*cnfg_sync_pulses*	**Description**	(R/W) Register to configure the Sync outputs available from FrSync and MFrSync and select the source for the 2 kHz and 8 kHz outputs from 01 and 02.	**Default Value**	0000 0000

Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
2k_8k_from_ DPLL2				*8k_invert*	*8k_pulse*	*2k_invert*	*2k_pulse*

Bit No.	**Description**	**Bit Value**	**Value Description**
7	*2k_8k_from_DPLL2* Register to select the source (DPLL1 or DPLL2) for the 2 kHz and 8 kHz outputs available from 01 and 02.	0 1	2/8 kHz on 01 and 02 generated from DPLL1. 2/8 kHz on 01 and 02 generated from DPLL2.
[6:4]	Not used.	-	-
3	*8k_invert* Register bit to invert the 8 kHz output from FrSync.	0 1	8 kHz FrSync output not inverted. 8 kHz FrSync output inverted.
2	*8k_pulse* Register bit to enable the 8 kHz output from FrSync to be either pulsed or 50:50 duty cycle. Output 02 must be enabled to use “pulsed output” mode on the FrSync output, and then the pulse width on the FrSync output will be equal to the period of the output programmed on 02.	0 1	8 kHz FrSync output not pulsed. 8 kHz FrSync output pulsed.
1	*2k_invert* Register bit to invert the 2 kHz output from MFrSync.	0 1	2 kHz MFrSync output not inverted. 2 kHz MFrSync output inverted.
0	*2k_pulse* Register bit to enable the 2 kHz output from MFrSync to be either pulsed or 50:50 duty cycle. Output 03 must be enabled to use “pulsed output” mode on the MFrSync output, and then the pulse width on the MFrSync output will be equal to the period of the output programmed on 03.	0 1	2 kHz MFrSync output not pulsed. 2 kHz MFrSync output pulsed.

Address (hex): 7D

Register Name	*cnfg_LOS_alarm*	**Description**	(R/W) Register to configure LOS (Loss of Signal) Alarm.	**Default Value**	0000 0010

Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
					LOS_GPO_en	*LOS_tristate_en*	*LOS_ polarity*

Bit No.	**Description**	**Bit Value**	**Value Description**
[7:3]	Not used.	-	-
2	*LOS_GPO_en* (General Purpose Output). If the LOS_ALARM output pin is not required, then setting this bit will allow the pin to be used as a general purpose output. The pin will be driven to the state of the polarity control bit, *int_polarity*.	0 1	LOS_ALARM output pin used for interrupts. LOS_ALARM output pin used for GPO purpose.
1	*LOS_tristate_en* The LOS_ALARM pin can be configured to be either connected directly to a processor, or wired together with other sources.	0 1	LOS_ALARM pin always driven when inactive. LOS_ALARM pin only driven when active, high-impedance when inactive.
0	*LOS_polarity* The LOS_ALARM pin can be configured to be active *High* or *Low*.	0 1	Active *Low* - pin driven *Low* to indicate active alarm. Active *High* - pin driven *High* to indicate active alarm.

Address (hex): 7E

Register Name	*cnfg_protection*	**Description**	(R/W) Protection register to protect against erroneous software writes.	**Default Value**	1000 0101

Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
protection_value							

Bit No.	**Description**	**Bit Value**	**Value Description**
[7:0]	*protection_value* This register can be used to ensure that the software writes a specific value to this register, before being able to modify any other register in the device. Three modes of protection are offered, (i) protected, (ii) fully unprotected, (iii) single unprotected. When protected, no other register in the device can be written to. When fully unprotected, any writeable register in the device can be written to. When single unprotected, only one register can be written before the device automatically re-protects itself. *Note...This register cannot be protected.*	0000 0000 – 1000 0100	Protected mode.
		1000 0101	Fully unprotected.
		1000 0110	Single unprotected.
		1000 0111 – 1111 1111	Protected mode.

JTAG

The JTAG connections on the ACS8526 allow a full boundary scan to be made. The JTAG implementation is fully compliant to IEEE 1149.1[4], with the following minor exceptions, and the user should refer to the standard for further information.

1. The output boundary scan cells do not capture data from the core, and so do not support INTEST. However this does not affect board testing.
2. In common with some other manufacturers, pin TRST is internally pulled *Low* to disable JTAG by default. The standard is to pull *High*. The polarity of TRST is as the standard: TRST *High* to enable JTAG boundary scan mode, TRST *Low* for normal operation.

The JTAG timing diagram is shown in Figure 9.

Over-voltage Protection

The ACS8526 may require Over-voltage Protection on input reference clock ports according to ITU recommendation K.41[10]. Semtech protection devices are recommended for this purpose (see separate Semtech data book).

ESD Protection

Suitable precautions should be taken to protect against electrostatic damage during handling and assembly. This device incorporates ESD protection structures that protect the device against ESD damage at ESD input levels up to at least +/2kV using the Human Body Model (HBD) MIL-STD-883D Method 3015.7, for all pins.

Latchup Protection

This device is protected against latchup for input current pulses of magnitude up to at least ±100 mA to JEDEC Standard No. 78 August 1997.

Figure 9 JTAG Timing

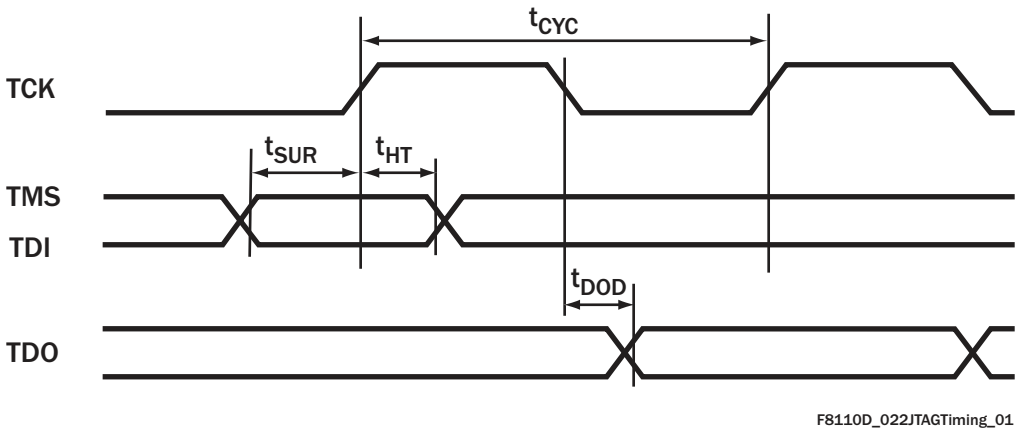


Table 18 JTAG Timing (for use with Figure 9)

Parameter	Symbol	Minimum	Typical	Maximum	Units
Cycle Time	t_{CYC}	50	-	-	ns
TMS/TDI to TCK rising edge time	t_{SUR}	3	-	-	ns
TCK rising to TMS/TDI hold time	t_{HT}	23	-	-	ns
TCK falling to TDO valid	t_{DOD}	-	-	5	ns

Maximum Ratings

Important Note: The Absolute Maximum Ratings, Table 19, are stress ratings only, and functional operation of the device at conditions other than those indicated in the Operating Conditions sections of this specification are not implied. Exposure to the absolute maximum ratings for an extended period may reduce the reliability or useful lifetime of the product.

Table 19 Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Units
Supply Voltage VDD1, VDD2, VDD3, VD1+,VD2+, VD3+, VA1+, VA2+, VA3+, VDD_DIFF	V_{DD}	-0.5	3.6	V
Input Voltage (non-supply pins)	V_{IN}	-	5.5	V
Output Voltage (non-supply pins)	V_{OUT}	-	5.5	V
Ambient Operating Temperature Range	T_A	-40	+85	^oC
Storage Temperature	T_{STOR}	-50	+150	^oC

Operating Conditions

Table 20 Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Units
Power Supply (dc voltage) VDD1, VDD2, VDD3, VD1+,VD2+, VD3+, VA1+, VA2+, VA3+, VDD_DIFF	V_{DD}	3.0	3.3	3.6	V
Power Supply (dc voltage) VDD5V	V_{DD5V}	3.0	3.3/5.0	5.5	V
Ambient Temperature Range	T_A	-40	-	+85	^oC
Supply Current (Typical - one 19 MHz output)	I_{DD}		110	200	mA
Total Power Dissipation	P_{TOT}		360	720	mW

DC Characteristics

Table 21 DC Characteristics: TTL Input Port

Across all operating conditions, unless otherwise stated

PARAMETER	Symbol	Minimum	Typical	Maximum	Units
V_{IN} High	V_{IH}	2	-	-	V
V_{IN} Low	V_{IL}	-	-	0.8	V
Input Current	I_{IN}	-	-	10	µA

Table 22 DC Characteristics: TTL Input Port with Internal Pull-up

Across all operating conditions, unless otherwise stated

Parameter	Symbol	Minimum	Typical	Maximum	Units
V_{IN} High	V_{IH}	2	-	-	V
V_{IN} Low	V_{IL}	-	-	0.8	V
Pull-up Resistor	PU	25	-	95	kΩ
Input Current	I_{IN}	-	-	120	µA

Table 23 DC Characteristics: TTL Input Port with Internal Pull-down

Across all operating conditions, unless otherwise stated

Parameter	Symbol	Minimum	Typical	Maximum	Units
V_{IN} High	V_{IH}	2	-	-	V
V_{IN} Low	V_{IL}	-	-	0.8	V
Pull-down Resistor (except TCK input)	PD	25	-	95	kΩ
Pull-down Resistor (TCK input only)	PD	12.5	-	47.5	kΩ
Input Current	I_{IN}	-	-	120	µA

Table 24 DC Characteristics: TTL Output Port

Across all operating conditions, unless otherwise stated

Parameter	Symbol	Minimum	Typical	Maximum	Units
V_{OUT} Low (I_{OL} = 4mA)	V_{OL}	0	-	0.4	V
V_{OUT} High (I_{OH} = 4mA)	V_{OH}	2.4	-	-	V
Drive Current	I_D	-	-	4	mA

Table 25 DC Characteristics: PECL Output Port

Across all operating conditions, unless otherwise stated

Parameter	Symbol	Minimum	Typical	Maximum	Units
PECL Output Low Voltage (Note (i))	V_{OLPECL}	V_{DD}-2.10	-	V_{DD}-1.62	V
PECL Output High Voltage (Note (i))	V_{OHPECL}	V_{DD}-1.25	-	V_{DD}-0.88	V
PECL Output Differential Voltage (Note (i))	V_{ODPECL}	580	-	900	mV

Note: (i) With 50 Ω load on each pin to V_{DD}-2 V, i.e. 82 Ω to GND and 130 Ω to V_{DD}.

Figure 10 Recommended Line Termination for PECL Output Port

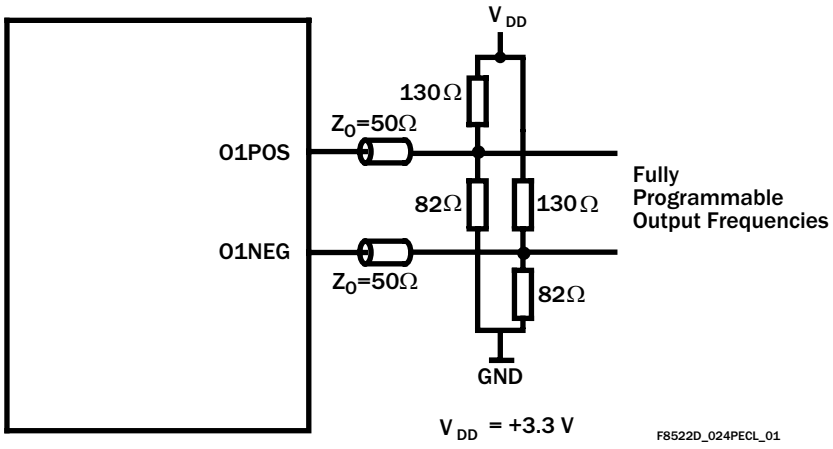


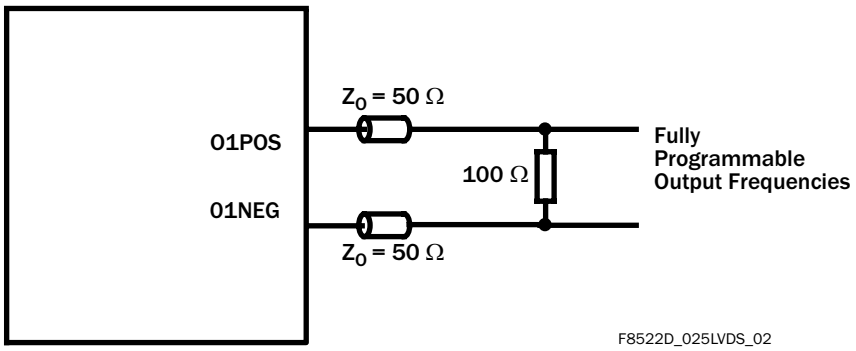
Table 26 DC Characteristics: LVDS Output Port

Across all operating conditions, unless otherwise stated

Parameter	Symbol	Minimum	Typical	Maximum	Units
LVDS Output High Voltage (Note (i))	V_{OHLVDS}	-	-	1.585	V
LVDS Output Low Voltage (Note (i))	V_{OLLVDS}	0.885	-	-	V
LVDS Differential Output Voltage	V_{ODLVDS}	250	-	450	mV
LVDS Change in Magnitude of Differential Output Voltage for complementary States (Note (i))	$V_{DOSLVDS}$	-	-	25	mV
LVDS Output Offset Voltage Temperature = 25°C (Note (i))	V_{OSLVDS}	1.125	-	1.275	V

Notes: (i) With 100 Ω load between the differential outputs.

Figure 11 Recommended Line Termination for LVDS Output Port



Jitter Performance

Output jitter generation measured over 60 second interval, UI p-p max measured using C-MAC E2747 12.8 MHz TCXO on ICT Flexacom tester.

Table 27 Output Jitter Generation at 35 Hz bandwidth and 8 kHz Input

Test Definition		Jitter Spec	ACS8526 Jitter
Specification	**Filter**	**UI**	**UI (TYP)**
G813[8] for 155 MHz o/p option 1	65 kHz - 1.3 MHz	0.1 p-p	0.073 p-p
G813[8] & G812[7] for 2.048 MHz option 1	20 Hz - 100 kHz	0.05 p-p	0.012 p-p
G813[8] for 155 MHz o/p option 2	12 kHz - 1.3 MHz	0.1 p-p	0.069 p-p
G812[7] for 1.544 MHz o/p	10 Hz - 40 kHz	0.05 p-p	0.011 p-p
G812[7] for 155 MHz electrical	500 Hz - 1.3 MHz	0.5 p-p	0.083 p-p
G812[7] for 155 MHz electrical	65 kHz - 1.3 MHz	0.075 p-p	0.073p-p
ETS-300-462-3[2] for 2.048 MHz SEC o/p	20 Hz - 100 kHz	0.5 p-p	0.012 p-p
ETS-300-462-3[2] for 2.048 MHz SEC o/p	49 Hz - 100 kHz	0.2 p-p	0.012 p-p
ETS-300-462-3[2] for 2.048 MHz SSU o/p	20 Hz - 100 kHz	0.05 p-p	0.012 p-p
ETS-300-462-5[3] for 155 MHz o/p	500 Hz - 1.3 MHz	0.5 p-p	0.083 p-p
ETS-300-462-5[3] for 155 MHz o/p	65 kHz - 1.3 MHz	0.1 p-p	0.073 p-p
GR-253-CORE[11] net i/f, 51.84 MHz o/p	100 Hz - 0.4 MHz	1.5 p-p	0.038 p-p
GR-253-CORE[11] net i/f, 51.84 MHz o/p	20 kHz to 0.4 MHz	0.15 p-p	0.019 p-p
GR-253-CORE[11] net i/f, 155 MHz o/p	500 Hz - 1.3 MHz	1.5 p-p	0.083 p-p
GR-253-CORE[11] net i/f, 155 MHz o/p	65 kHz - 1.3 MHz	0.15 p-p	0.073 p-p
GR-253-CORE[11] cat II elect i/f, 155 MHz	12 kHz - 1.3 MHz	0.1 p-p	0.069 p-p
		0.01 rms	0.009 rms
GR-253-CORE[11] cat II elect i/f, 51.84 MHz	12 kHz - 400 kHz	0.1 p-p	0.008 p-p
		0.01 rms	0.004 rms
GR-253-CORE[11] DS1 i/f, 1.544 MHz	10 Hz - 40 kHz	0.1 p-p	0.001 p-p
		0.01 rms	<0.001 rms
AT&T 62411[1] for 1.544 MHz	10 Hz - 8 kHz	0.02 rms	<0.001 rms
AT&T 62411[1] for 1.544 MHz	8 Hz - 40 kHz	0.025 rms	<0.001 rms
AT&T 62411[1] for 1.544 MHz	10 Hz - 40 kHz	0.025 rms	<0.001 rms
AT&T 62411[1] for 1.544 MHz	Broadband	0.05 rms	<0.001 rms
G-742[6] for 2.048 MHz	DC - 100 kHz	0.25 rms	0.012 rms
G-742[6] for 2.048 MHz	18 kHz - 100 kHz	0.05 p-p	0.012 p-p
G-736[5] for 2.048 MHz	20 Hz - 100 kHz	0.05 p-p	0.012 p-p

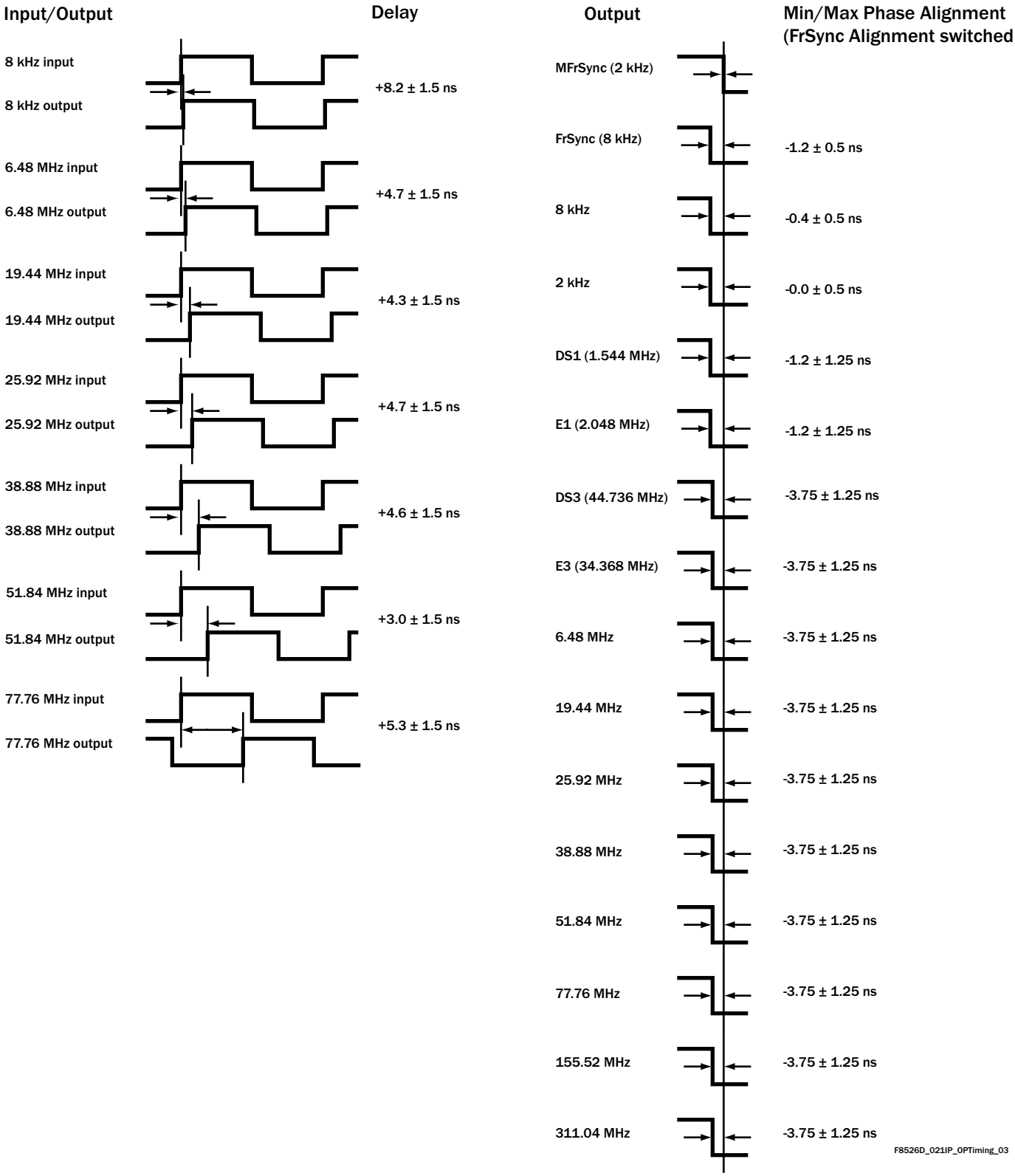
Table 27 Output Jitter Generation at 35 Hz bandwidth and 8 kHz Input (cont...)

Test Definition		Jitter Spec	ACS8526 Jitter
Specification	**Filter**	**UI**	**UI (TYP)**
GR-499-CORE[12] & G824[9] for 1.544 MHz	10 Hz - 40kHz	5.0 p-p	0.001 p-p
GR-499-CORE[12] & G824[9] for 1.544 MHz	8 kHz - 40kHz	0.1 p-p	0.001 p-p
GR-1244-CORE[13] for 1.544 MHz	> 10 Hz	0.05 p-p	0.001 p-p

Note...This table is only for comparing the ACS8526 output jitter performance against values and quoted in various specifications for given conditions. It should not be used to infer compliance to any other aspects of these specifications.

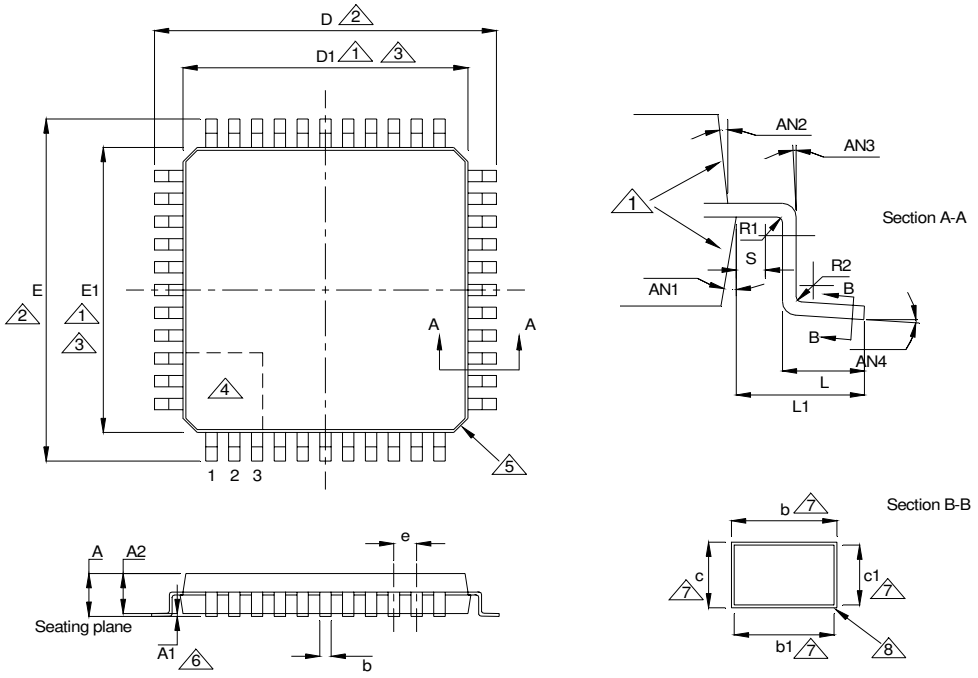
Input/Output Timing

Figure 12 Input/Output Timing (Typical Conditions)



Package Information

Figure 13 LQFP Package



Notes

1. The top package body may be smaller than the bottom package body by as much as 0.15 mm.
2. To be determined at seating plane.
3. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.
4. Details of pin 1 identifier are optional but will be located within the zone indicated.
5. Exact shape of corners can vary.
6. A1 is defined as the distance from the seating plane to the lowest point of the package body.
7. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
8. Shows plating.

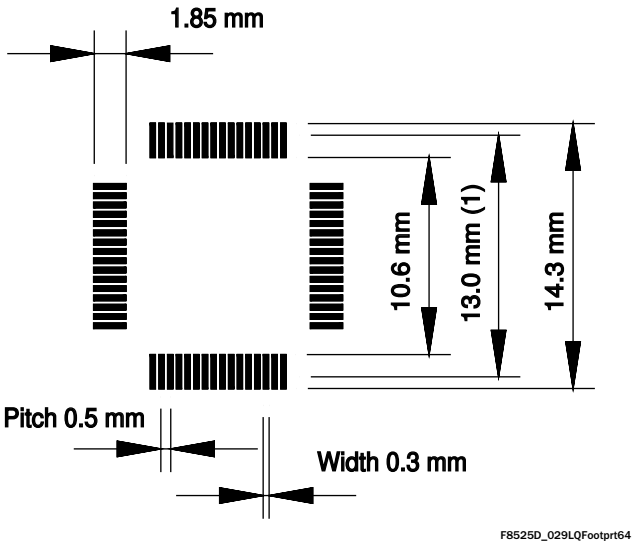
Table 28 64 Pin LQFP Package Dimension Data (for use with Figure 13)

Dimensions in mm	D/E	D1/ E1	A	A1	A2	e	AN1	AN2	AN3	AN4	R1	R2	L	L1	S	b	b1	c	c1
Min.			1.40	0.05	1.35		11°	11°	0°	0°	0.08	0.08	0.45		0.20	0.17	0.17	0.09	0.09
Nom.	12.00	10.00	1.50	0.10	1.40	0.50	12°	12°	-	3.5°	-	-	0.60	1.00 (ref)	-	0.22	0.20	-	-
Max.			1.60	0.15	1.45		13°	13°	-	7°	-	0.20	0.75		-	0.27	0.23	0.20	0.16

Thermal Conditions

The device is rated for full temperature range when this package is used with a 4 layer or more PCB. Copper coverage must exceed 50%. All pins must be soldered to the PCB. Maximum operating temperature must be reduced when the device is used with a PCB with less than these requirements.

Figure 14 Typical 64-Pin LQFP Package Landing Pattern



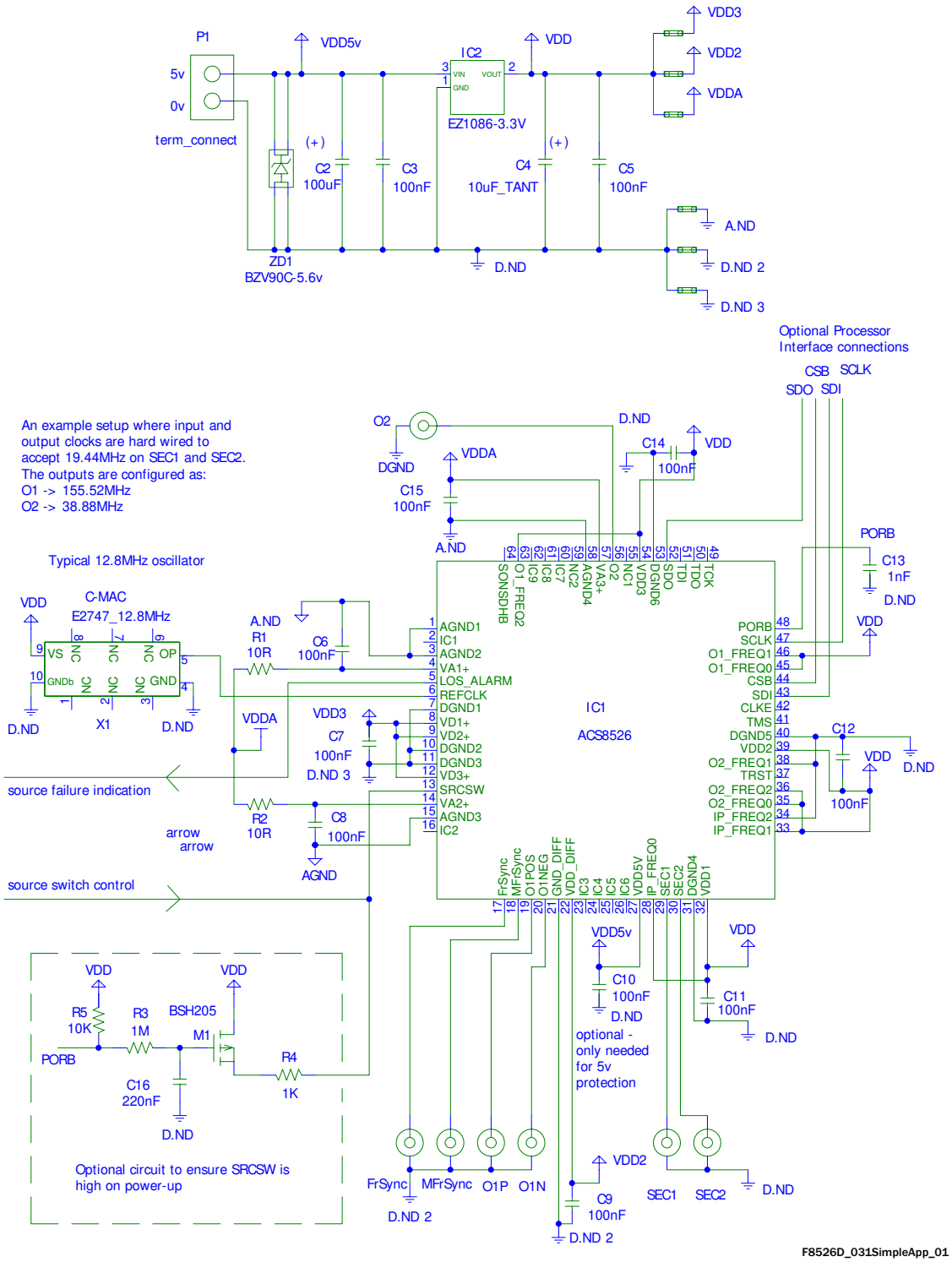
Notes: (i) Solderable to this limit.

(ii) Square package - dimensions apply in both X and Y directions.

(iii) Typical example. The User is responsible for ensuring compatibility with PCB manufacturing process, etc.

Application Information

Figure 15 Simplified Application Schematic



Abbreviations

APLL	Analogue Phase Locked Loop
BITS	Building Integrated Timing Supply
DFS	Digital Frequency Synthesis
DPLL	Digital Phase Locked Loop
DS1	1544 kbit/s interface rate
DTO	Discrete Time Oscillator
E1	2048 kbit/s interface rate
I/O	Input - Output
LOS	Loss Of Signal
LQFP	Low profile Quad Flat Pack
LVDS	Low Voltage Differential Signal
MTIE	Maximum Time Interval Error
NE	Network Element
PBO	Phase Build-out
PDH	Plesiochronous Digital Hierarchy
PD2	Phase Detector 2
PECL	Positive Emitter Coupled Logic
PFD	Phase and Frequency Detector
PLL	Phase Locked Loop
POR	Power-On Reset
ppb	parts per billion
ppm	parts per million
p-p	peak-to-peak
R/W	Read/Write
rms	root-mean-square
RO	Read Only
RoHS	Restrictive Use of Certain Hazardous Substances (directive)
SDH	Synchronous Digital Hierarchy
SEC	SDH/SONET Equipment Clock
SETS	Synchronous Equipment Timing source
SONET	Synchronous Optical Network
SSU	Synchronization Supply Unit
STM	Synchronous Transport Module
TDEV	Time Deviation
TCXO	Temperature Compensated Crystal Oscillator
UI	Unit Interval
WEEE	Waste Electrical and Electronic Equipment (directive)
XO	Crystal Oscillator

References

[1] AT & T 62411 (12/1990)
ACCUNET® T1.5 Service description and Interface Specification

[2] ETSI ETS 300 462-3, (01/1997)
Transmission and Multiplexing (TM); Generic requirements for synchronization networks; Part 3: The control of jitter and wander within synchronization networks

[3] ETSI ETS 300 462-5 (09/1996)
Transmission and Multiplexing (TM); Generic requirements for synchronization networks; Part 5: Timing characteristics of slave clocks suitable for operation in Synchronous Digital Hierarchy (SDH) equipment

[4] IEEE 1149.1 (1990)
Standard Test Access Port and Boundary-Scan Architecture

[5] ITU-T G.736 (03/1993)
Characteristics of a synchronous digital multiplex equipment operating at 2048 kbit/s

[6] ITU-T G.742 (1988)
Second order digital multiplex equipment operating at 8448 kbit/s, and using positive justification

[7] ITU-T G.812 (06/1998)
Timing requirements of slave clocks suitable for use as node clocks in synchronization networks

[8] ITU-T G.813 (08/1996)
Timing characteristics of SDH equipment slave clocks (SEC)

[9] ITU-T G.824 (03/2000)
The control of jitter and wander within digital networks which are based on the 1544 kbit/s hierarchy

[10] ITU-T K.41 (05/1998)
Resistability of internal interfaces of telecommunication centres to surge overvoltages

[11] Telcordia GR-253-CORE, Issue 3 (09/ 2000)
Synchronous Optical Network (SONET) Transport Systems: Common Generic Criteria

[12] Telcordia GR-499-CORE, Issue 2 (12/1998)
Transport Systems Generic Requirements (TSGR) Common requirements

[13] Telcordia GR-1244-CORE, Issue 2 (12/2000)
Clocks for the Synchronized Network: Common Generic Criteria

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Notes

Revision Status/History

The Revision Status of the datasheet, as shown in the center of the datasheet header bar, may be DRAFT, PRELIMINARY, or FINAL, and refers to the status of the Device (not the datasheet) within the design cycle. DRAFT status is used when the design is being realized but is not yet physically available, and the datasheet content reflects the intention of the design. The datasheet is raised to PRELIMINARY status when initial prototype devices are physically available, and the datasheet content more accurately represents the realization of the design. The datasheet is only raised to FINAL status after the device has been fully characterized, and the datasheet content updated with measured, rather than simulated parameter values.

This is a FINAL release (Revision 4.01) of the ACS8526 datasheet. Changes made for this document revision are given in Table 29, together with a summary of previous revisions. For specific changes between earlier revisions, refer (where available) to those earlier revisions. Always use the current version of the datasheet.

Table 29 Revision History

Revision	Reference	Description of changes
2.00/ December 2002	All pages	First full release.
3.00/ January 2003	All pages	Updated to FINAL status.
4.00/September 2003	All Pages	Major revision. All pages reformatted. General update of cross-references.
	Reg. 38, 3C, 3D, 41, 6A, and 6B	Register descriptions updated.
	Reg. 4D	New register inserted.
	Table 3 ,Table 13 , Table 15, Table 22, Table 23, Figure 2 and Figure 12	Tables and Figures updated.
	“Crystal Frequency Calibration” on page 27, “Multiplexers” on page 13, “Phase and Frequency Detectors” on page 15, “Register Map” on page 30, “JTAG” on page 61, “Abbreviations” on page 71. “Revision Status/History” on page 73	Sections updated.
	“ESD Protection” on page 61, “Latchup Protection” on page 61	New Sections inserted.
4.01/June 2006	Front and back pages and “Abbreviations” on page 71	Interim update to reflect availability of lead(Pb)-free packaged part and change to Semtech US address.
	“Trademark Acknowledgements” on page 72 and “Revision Status/History” on page 73	Minor non-technical changes.
	Back page	Taiwan address updated.

Ordering Information

Table 30 Parts List

Part Number	Description
ACS8526	LC/P LITE Line Card Protection Switch for PDH, SONET or SDH Systems
ACS8526T	Lead (Pb)-free package version of ACS8526; RoHS and WEEE compliant.

Disclaimers

Life support- This product is not designed or intended for use in life support equipment, devices or systems, or other critical applications. This product is not authorized or warranted by Semtech for such use.

Right to change- Semtech Corporation reserves the right to make changes, without notice, to this product. Customers are advised to obtain the latest version of the relevant information before placing orders.

Compliance to relevant standards- Operation of this device is subject to the User's implementation and design practices. It is the responsibility of the User to ensure equipment using this device is compliant to any relevant standards.

Contacts

For Additional Information, contact the following:

Semtech Corporation Advanced Communications Products

E-mail: sales@semtech.com acsupport@semtech.com

Internet: http://www.semtech.com

USA: 200 Flynn Road, Camarillo, CA 93012-8790
Tel: +1 805 498 2111, Fax: +1 805 498 3804

FAR EAST: 12F, No. 89 Sec. 5, Nanking E. Road, Taipei, 105, TWN, R.O.C.
Tel: +886 2 2748 3380 Fax: +886 2 2748 3390

EUROPE: Semtech Ltd., Units 2 and 3, Park Court, Premier Way,
Abbey Park Industrial Estate, Romsey, Hampshire, SO51 9DN
Tel: +44 (0)1794 527 600 Fax: +44 (0)1794 527 601

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