

N-channel 30 V 3.0 mΩ logic level MOSFET in D2PAK Rev. 1 — 21 March 2012 Product of

Product data sheet

Product profile 1.

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1.1 General description

Logic level N-channel MOSFET in D2PAK package qualified to 175 °C. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

1.2 Features and benefits

- High efficiency due to low switching and conduction losses
- Suitable for logic level gate drive sources

1.3 Applications

- DC-to-DC converters
- Load switiching

- Motor control
- Server power supplies

1.4 Quick reference data

Table 1.	Quick reference data					
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V _{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C	-	-	30	V
I _D	drain current	T_{mb} = 25 °C; V_{GS} = 10 V; see <u>Figure 1</u>	<u>[1]</u> -	-	100	А
P _{tot}	total power dissipation	T _{mb} = 25 °C; see <u>Figure 2</u>	-	-	170	W
Tj	junction temperature		-55	-	175	°C
Static cha	aracteristics					
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 25 A; T _j = 100 °C; see <u>Figure 13</u> ; see <u>Figure 12</u>	-	3.6	4.2	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _j = 25 °C; see <u>Figure 12</u>	-	2.57	3	mΩ
Dynamic	characteristics					
Q _{GD}	gate-drain charge	V_{GS} = 4.5 V; I_{D} = 25 A; V_{DS} = 15 V	-	8	-	nC
Q _{G(tot)}	total gate charge	V_{GS} = 4.5 V; I_D = 25 A; V_{DS} = 15 V; see <u>Figure 14</u> ; see <u>Figure 15</u>	-	32	-	nC
Avalanch	e ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$\label{eq:VGS} \begin{array}{l} V_{GS} = 10 \text{ V}; \text{T}_{j(init)} = 25 \text{ °C}; \text{I}_{D} = 100 \text{ A}; \\ V_{sup} \leq 30 \text{ V}; \text{R}_{GS} = 50 \Omega; \text{ unclamped} \end{array}$	-	-	300	mJ

[1] Continuous current is limited by package.

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2. Pinning information

Table 2.	Pinning	information		
Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		-
2	D	drain ^[1]	mb	D D
3	S	source		
mb	D	mounting base; connected to drain		mbb076 S
			SOT404 (D2PAK)	

[1] It is not possible to make connection to pin 2.

3. Ordering information

Table 3.	Ordering in	formation		
Type numb	ber	Package		
		Name	Description	Version
PSMN2R7-	30BL	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

4. Marking

Table 4. Marking codes	
Type number	Marking code
PSMN2R7-30BL	PSMN2R7-30BL

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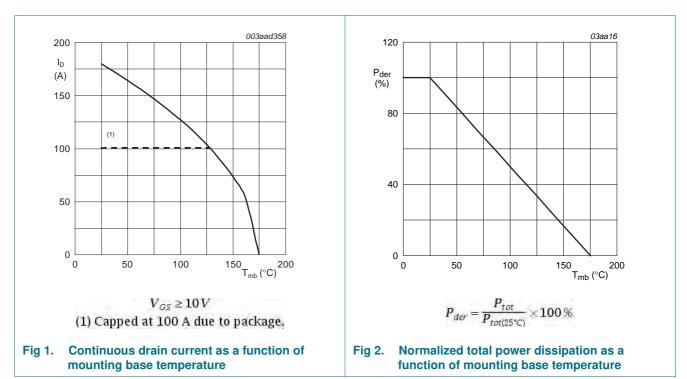
5. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C	-	30	V
V _{DGR}	drain-gate voltage	T _j ≥ 25 °C; T _j ≤ 175 °C; R _{GS} = 20 kΩ	-	30	V
V _{GS}	gate-source voltage		-20	20	V
I _D	drain current	V_{GS} = 10 V; T_{mb} = 100 °C; see <u>Figure 1</u>	<u>[1]</u> _	100	А
		V_{GS} = 10 V; T_{mb} = 25 °C; see <u>Figure 1</u>	<u>[1]</u> _	100	А
I _{DM}	peak drain current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C; see <u>Figure 3</u>	-	730	A
P _{tot}	total power dissipation	T _{mb} = 25 °C; see <u>Figure 2</u>	-	170	W
T _{stg}	storage temperature		-55	175	°C
Tj	junction temperature		-55	175	°C
T _{sld(M)}	peak soldering temperature		-	260	°C
Source-drai	in diode				
I _S	source current	T _{mb} = 25 °C	<u>[1]</u> -	100	А
I _{SM}	peak source current	pulsed; $t_p \le 10 \ \mu s$; $T_{mb} = 25 \ ^{\circ}C$	-	730	А
Avalanche r	ruggedness				
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	$ \begin{array}{l} V_{GS} = 10 \text{ V}; \text{T}_{j(init)} = 25 ^{\circ}\text{C}; \text{I}_{\text{D}} = 100 \text{ A}; \\ V_{sup} \leq 30 \text{ V}; \text{R}_{GS} = 50 \Omega; \text{ unclamped} \end{array} $	-	300	mJ

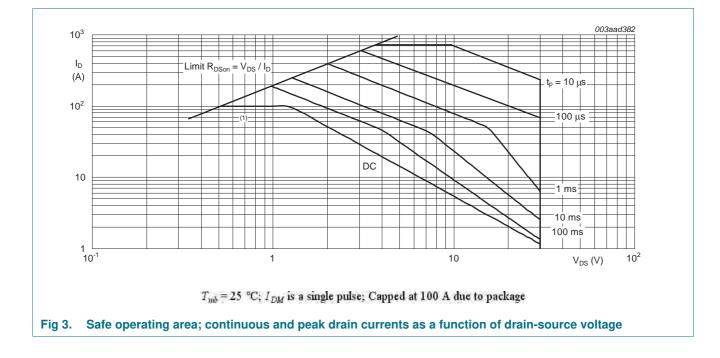
[1] Continuous current is limited by package.



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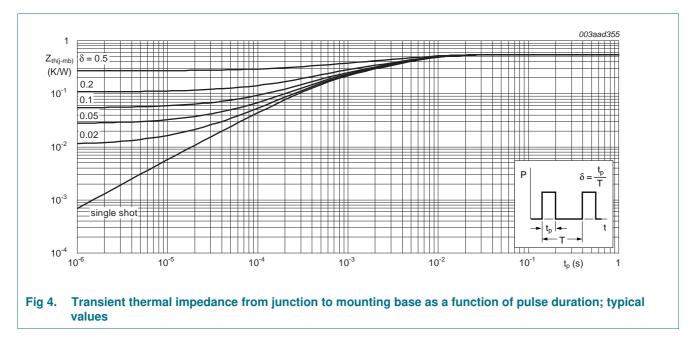
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N-channel 30 V 3.0 m Ω logic level MOSFET in D2PAK

6. Thermal characteristics

Table 6.	Thermal characteristics					
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	0.54	0.88	K/W
R _{th(j-a)}	thermal resistance from junction to ambient	minimum footprint; mounted on a printed-circuit board	-	50	-	K/W



N-channel 30 V 3.0 mΩ logic level MOSFET in D2PAK

7. Characteristics

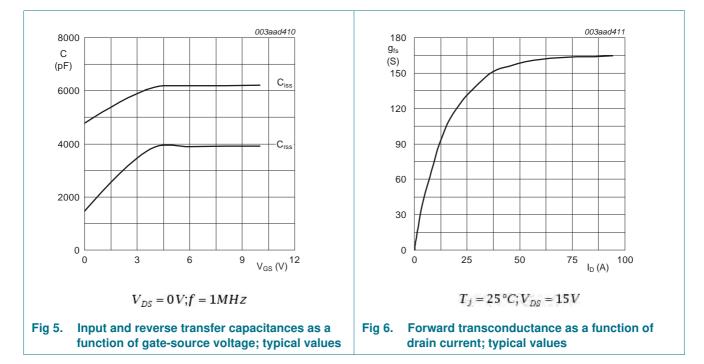
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static chara	cteristics					
V _{(BR)DSS}	drain-source	$I_D = 250 \ \mu A; \ V_{GS} = 0 \ V; \ T_j = 25 \ ^\circ C$	30	-	-	V
	breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = -55 °C	27	-	-	V
V _{GS(th)}	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ °C};$ see <u>Figure 10</u> ; see <u>Figure 11</u>	1.3	1.7	2.15	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ °C};$ see Figure 11	0.5	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ °C};$ see Figure 11	-	-	2.45	V
I _{DSS}	drain leakage current	$V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	0.3	5	μA
		V_{DS} = 30 V; V_{GS} = 0 V; T_j = 125 °C	-	-	100	μA
I _{GSS}	gate leakage current	V_{GS} = 16 V; V_{DS} = 0 V; T_j = 25 °C	-	10	100	nA
		$V_{GS} = -16 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	10	100	nA
R _{DSon}	drain-source on-state resistance	V_{GS} = 4.5 V; I _D = 25 A; T _j = 25 °C; see <u>Figure 12</u>	-	3.16	3.7	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _j = 175 °C; see <u>Figure 13</u> ; see <u>Figure 12</u>	-	4.88	5.7	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 100 \text{ °C};$ see Figure 13; see Figure 12	-	3.6	4.2	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _j = 25 °C; see <u>Figure 12</u>	-	2.57	3	mΩ
R _G	gate resistance	f = 1 MHz	-	1	-	Ω
Dynamic ch	aracteristics					
Q _{G(tot)}	total gate charge	$I_D = 25 \text{ A}; V_{DS} = 15 \text{ V}; V_{GS} = 10 \text{ V};$ see Figure 14; see Figure 15	-	66	-	nC
		$I_D = 0 \text{ A}; V_{DS} = 0 \text{ V}; V_{GS} = 10 \text{ V}$	-	60	-	nC
		$I_D = 25 \text{ A}; V_{DS} = 15 \text{ V}; V_{GS} = 4.5 \text{ V};$	-	32	-	nC
Q _{GS}	gate-source charge	see Figure 14; see Figure 15	-	12	-	nC
Q _{GS(th)}	pre-threshold gate-source charge		-	6.4	-	nC
Q _{GS(th-pl)}	post-threshold gate-source charge		-	5.6	-	nC
Q _{GD}	gate-drain charge	$I_D = 25 \text{ A}; V_{DS} = 15 \text{ V}; V_{GS} = 4.5 \text{ V}$	-	8	-	nC
V _{GS(pl)}	gate-source plateau voltage	$I_D = 25 \text{ A}; V_{DS} = 15 \text{ V};$ see <u>Figure 14</u> ; see <u>Figure 15</u>	-	2.6	-	V
C _{iss}	input capacitance	$V_{DS} = 15 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz};$	-	3954	-	pF
C _{oss}	output capacitance	T _j = 25 °C; see <u>Figure 16</u>	-	822	-	pF
C _{rss}	reverse transfer capacitance		-	356	-	pF
t _{d(on)}	turn-on delay time	$\label{eq:VDS} \begin{array}{l} V_{DS} = 12 \; V; \; R_{L} = 0.5 \; \Omega; \; V_{GS} = 4.5 \; V; \\ R_{G(ext)} = 4.7 \; \Omega \end{array}$	-	46	-	ns

N-channel 30 V 3.0 m Ω logic level MOSFET in D2PAK

Table 7. Characteristics ... continued

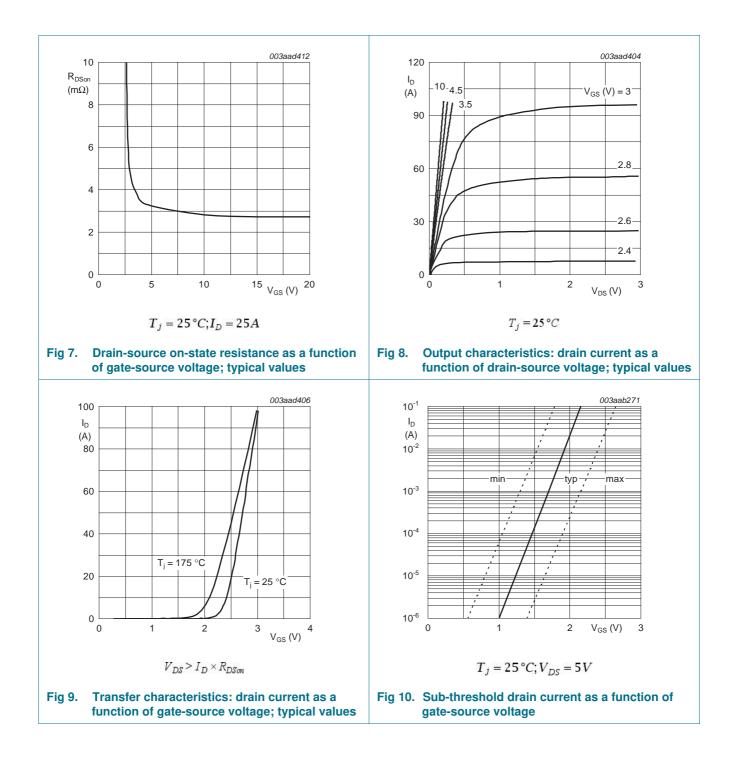
Tested to JEDEC standards where applicable.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
t _r	rise time	$V_{DS} = 15 \text{ V}; \text{ R}_{L} = 0.5 \Omega; \text{ V}_{GS} = 4.5 \text{ V};$	-	82	-	ns
t _{d(off)}	turn-off delay time	$R_{G(ext)} = 4.7 \ \Omega$	-	74	-	ns
t _f	fall time		-	35	-	ns
Source-drai	in diode					
V_{SD}	source-drain voltage	I _S = 25 A; V _{GS} = 0 V; T _j = 25 °C; see <u>Figure 17</u>	-	0.7	1.2	V
t _{rr}	reverse recovery time	$I_{S} = 25 \text{ A}; dI_{S}/dt = -100 \text{ A}/\mu s; V_{GS} = 0 \text{ V};$	-	40	-	ns
Q _r	recovered charge	V _{DS} = 15 V	-	33	-	nC



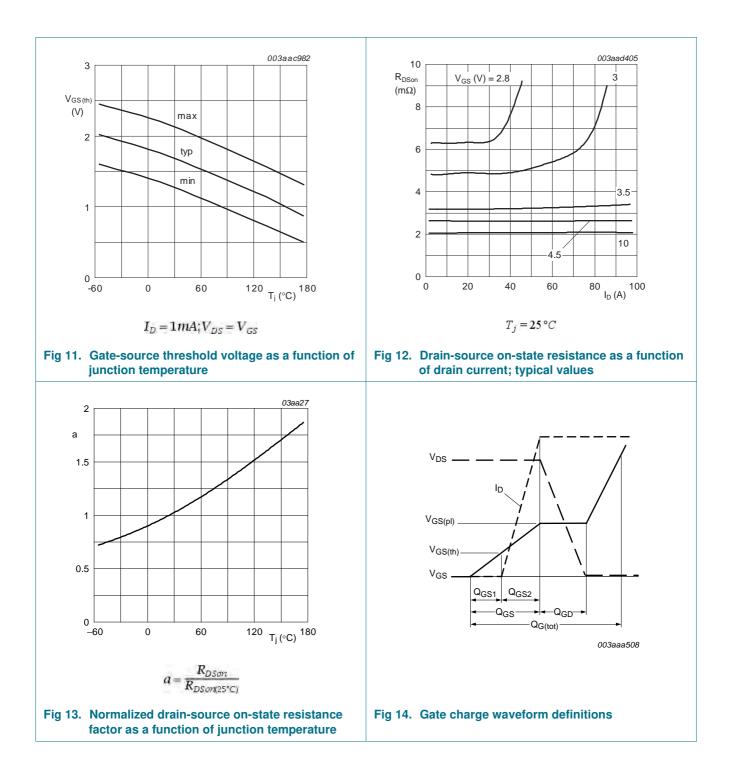
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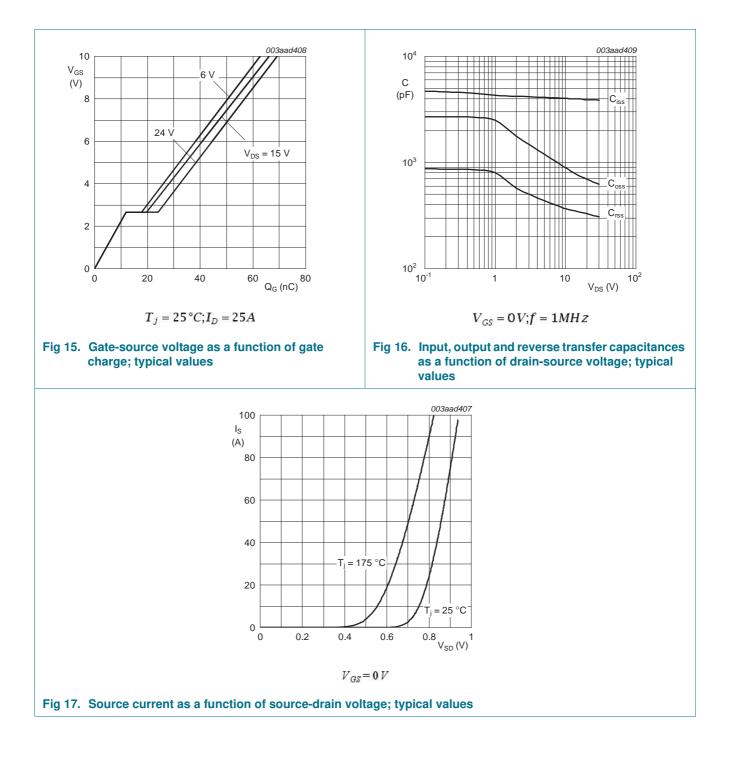
N-channel 30 V 3.0 m Ω logic level MOSFET in D2PAK



Rev. 1 — 21 March 2012

PSMN2R7-30BL

N-channel 30 V 3.0 m Ω logic level MOSFET in D2PAK



N-channel 30 V 3.0 mΩ logic level MOSFET in D2PAK

8. Package outline

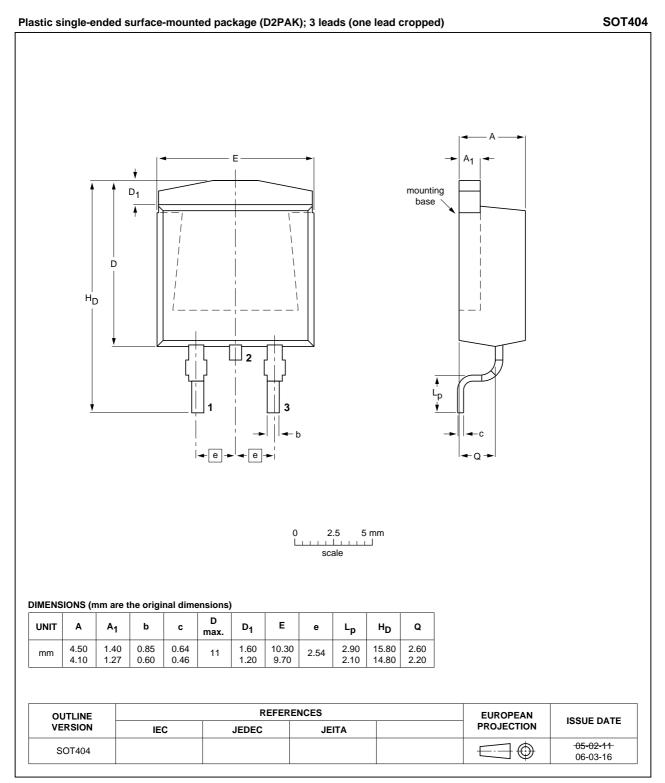


Fig 18. Package outline SOT404 (D2PAK)

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N-channel 30 V 3.0 mΩ logic level MOSFET in D2PAK

9. Revision history

Table 8. Revision h	e 8. Revision history				
Document ID	Release date	Data sheet status	Change notice	Supersedes	
PSMN2R7-30BL v.1	20120321	Product data sheet	-	-	

N-channel 30 V 3.0 mΩ logic level MOSFET in D2PAK

10. Legal information

10.1 Data sheet status

Document status ^[1] [2]	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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N-channel 30 V 3.0 m Ω logic level MOSFET in D2PAK

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N-channel 30 V 3.0 mΩ logic level MOSFET in D2PAK

12. Contents

1	Product profile1
1.1	General description1
1.2	Features and benefits1
1.3	Applications1
1.4	Quick reference data1
2	Pinning information2
3	Ordering information2
4	Marking2
5	Limiting values
6	Thermal characteristics5
7	Characteristics6
8	Package outline11
9	Revision history12
10	Legal information13
10.1	Data sheet status13
10.2	Definitions
10.3	Disclaimers
10.4	Trademarks14
11	Contact information14