Compact Seven-Channel Regulator with Li+/Polymer Linear Battery Charger and I2C Interface

General Description

The AAT3608 is a member of Skyworks' Total Power Management IC (TPMIC™) product family. It contains a single-cell lithium ion/polymer battery charger, two 800mA switching regulators, and five low dropout (LDO) regulators in a small Pb-free 40-pin 5mmx5mm TQFN package, making it ideal for portable space-constrained systems. The single-input linear charger powers up from an adapter or a USB port. The adapter charge current is programmable with an external resistor or pin selectable between 100mA and 500mA when connected to a USB port. The device integrates a load switch for dynamic power path and features deep sleep mode operation. The step-down regulators are monolithic synchronous converters integrating the compensation network and soft start circuitry. The 1.5MHz operating frequency enables the use of tiny 2.2µH inductors and small 4.7µF output capacitors. External resistors set the output voltage for Buck 1 and Buck 2; the output voltage of Buck 2 is dynamically adjustable with I^2C. The LDO regulators feature 3% output voltage accuracy over the full operating temperature range. The fast control loop of the LDO regulators also provide excellent transient response with a typical output voltage deviation of 1.5%. The AAT3608 provides protection features to safeguard from over-temperature operation, over-current operation, and a digital thermal loop to protect the battery during battery charging. The device is rated over an ambient temperature range of -40°C to 85°C.

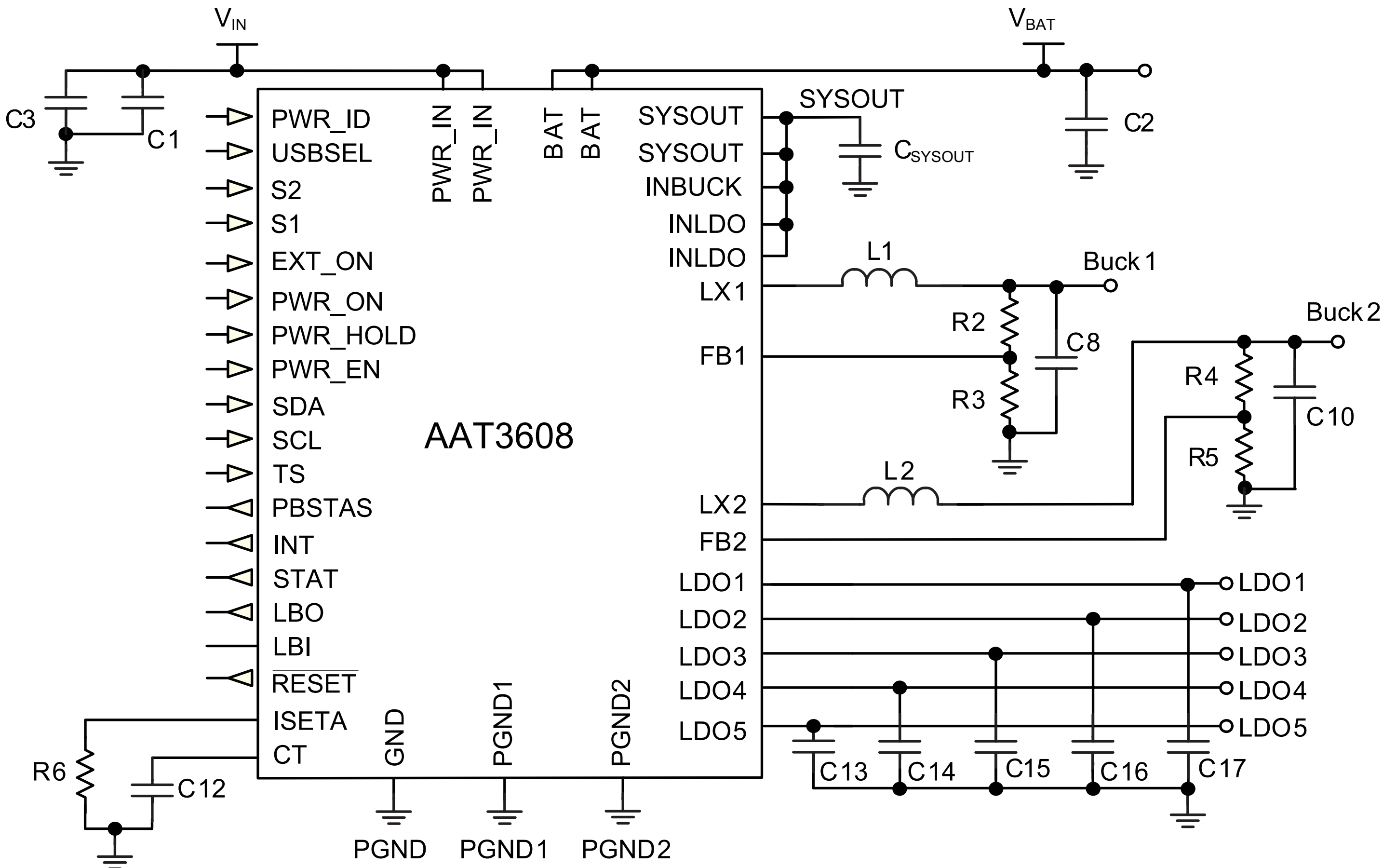
Features

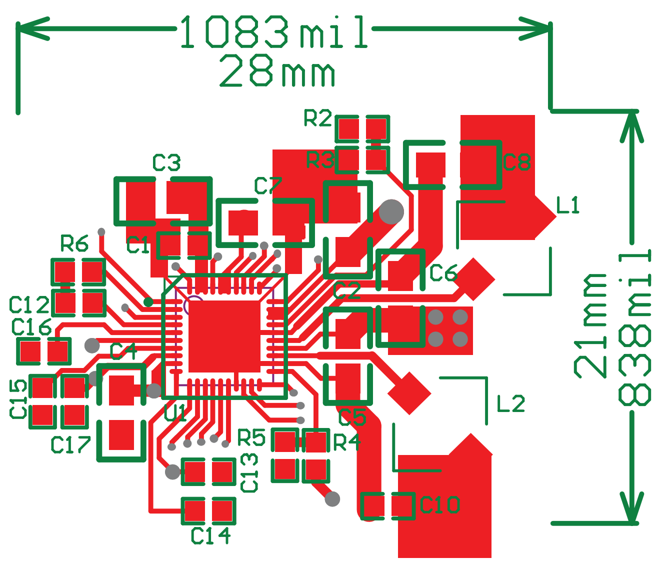
- 2.7V to 5.5V Operating Input Voltage Range
- Adapter or USB Single Input Linear Charger
- Battery Charger Digital Thermal Regulation
- Battery Temperature Monitoring
- Battery Charger Includes Programmable Timer
- Input Load Switch
- Dual 800mA Monolithic Switching Converters
  - 1.5MHz Switching Frequencies
  - 95% Efficiency
  - Independent Input Power and Ground
  - Buck1 Output Programmable With External Resistors
  - Buck 2 Feedback Voltage is Dynamically Adjustable between 0.5V and 0.7V with I^2C Interface
- Five Channel LDO Regulators
  - 300mA, Output Adjustable via Two Logic Inputs
  - 80mA, Output Adjustable via I^2C Interface
  - 50mA, 2.5V Output Voltage
  - 50mA, 3.3V Output Voltage
  - 80mA with 1.2V Fixed Output
  - 3% Accuracy and 1.5% Typical Transient Accuracy
- Very Low Shutdown Current
- Power-On Push Button
- Status Outputs
  - Interrupt, Reset and Status Pins, Low Battery Flag
- Separate Enable Pin for LDO2, LDO4, LDO5, and Buck2 (when mask is removed)
- Over-Current and Over-Thermal Protection
- 5mmx5mm, 40-Pin TQFN Package

Applications

- GPS
- Handheld Devices
- Mobile Media Players
- MP3
- Portable Navigation

Typical Application Circuit



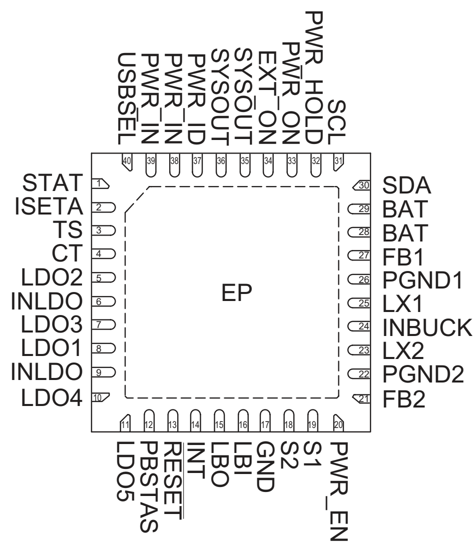


Pin Descriptions

Pin #	Symbol	Function
1	STAT	Open drain (pull-down) output for battery charging status.
2	ISETA	Input pin for charge current programming for the adapter. Connect a 1.24kΩ resistor to get 800mA of charging current. Can be used to monitor charging current.
3	TS	Battery temperature sense pin with 75µA output current. Connect the battery's NTC 10kΩ resistor from this pin to ground. A Beta range of 3300 to 4000 will place the typical charging temperature between -4°C and 48°C.
4	CT	Charger safety timer pin. A 0.1µF ceramic capacitor should be connected between this pin and GND. Connect directly to GND to disable the timer function.
5	LDO2	Output for LDO2 regulator.
6	INLDO	Input power for LDO regulators.
7	LDO3	Output for LDO3 regulator.
8	LDO1	Output for LDO1 regulator.
9	INLDO	Input power for LDO regulators.
10	LDO4	Output for LDO4 regulator.
11	LDO5	Output for LDO5 regulator.
12	PBSTAS	Open drain (pull-down) output for PWR_ON status. When PWR_ON is high, PBSTAS will be low (after the debounce time). When PWR_ON is low, PBSTAS will be high (or equal to the voltage to which that external pull-up resistor is connected).
13	$\overline{\text{RESET}}$	Open drain (pull-down) active-low output for reset. After Buck2 is OK, there is a delay of 200ms before $\overline{\text{RESET}}$ goes High. $\overline{\text{RESET}}$ pin is low in shutdown.
14	INT	Open drain (pull-down) active-low output for interrupt. When any of the I^{2}C read bits (except the DS_RDY and PWR_DS bits) change state this pin will pull low. It will be released again after a read from the I^{2}C is complete.
15	LBO	Open drain (pull-down) active-low output for low-battery comparator. When the battery is low, LBO will pull down.
16	LBI	Feedback input for low-battery comparator. The LBI threshold is 1.0V.
17	GND	Ground.
18	S2	S1 and S2 bits set the output voltage for LDO1.
19	S1	S1 and S2 bits set the output voltage for LDO1.
20	PWR_EN	Enable for LDO2, LDO4, and LDO5 for default condition. Buck2 can also be controlled by PWR_EN only if the SOC masks PWR_EN through I^{2}C, refer to the "I^{2}C Serial Interface and Programmability" section of this datasheet for additional information.
21	FB2	Feedback input for Buck2 regulator.
22	PGND2	Power ground for Buck2 regulator.
23	LX2	Switching node for Buck2 regulator.
24	INBUCK	Input power for Buck regulators.
25	LX1	Switching node for Buck1 regulator.
26	PGND1	Power ground for Buck1 regulator.
27	FB1	Feedback input for Buck1 regulator.
28, 29	BAT	Input for lithium-ion battery.
30	SDA	I^{2}C serial data pin.
31	SCL	I^{2}C serial clock pin.
32	PWR_HOLD	Enable for the system. PWR_HOLD must be held high by the processor to keep system turned on. To shut down the device, the microcontroller should pull PWR_HOLD to ground.
33	PWR_ON	Enable for the system. Connect a push-button from this pin to BAT to activate system. It is debounced for 320ms.
34	EXT_ON	Alternate system enable; may be used by the RTC alarm or other system input. This pin's function is similar to PWR_ON; it has a similar 320ms debounce but does not affect the PBSTAS pin.
35, 36	SYSOUT	System output. Connect to the INLDO and INBUCK input supply pins.
37	PWR_ID	Logic input to identify the source of PWR_IN.
38, 39	PWR_IN	Power Input. System input from adapter or USB.
40	USBSEL	Logic input to select 500mA current limit and fast charge current (USBSEL=H) or 100mA current limit and fast charge (USBSEL=L). An internal pull-down resistor is connected to this pin. If is left floating,USBSEL is pulled to ground.
EP	EP	For best thermal performance the exposed thermal pad must be thermally connected to a large exposed copper pad underneath the package. Additionally, the exposed thermal pad (EP), GND, and PGND must be electrically connected to ground copper.

Pin Configuration

TQFN55-40
(Top View)



Absolute Maximum Ratings[1]

Symbol	Pin Name	Value	Units
	PWR_IN, PWR_ID, BAT, SYSOUT, SDA, SCL, $\overline{RESET}$, STAT, USBSEL, ISETA, TS, CT, LBI, LBO, INT, PWR_EN, PWR_HOLD, PWR_ON, PBSTAS, EXT_ON, S1, S2 Voltage to GND	-0.3 to 6.5	V
	INBUCK, INLDO Voltage to GND	-0.3 to V_{SYSOUT} + 0.3	V
	LX1, LX2, FB1, FB2 Voltage to PGND1, PGND2	-0.3 to V_{INBUCK} + 0.3	V
	LDO1, LDO2, LDO3, LDO4, LDO5 Voltage to GND	-0.3 to V_{INLDO} + 0.3	V
	PGND1, PGND2 to GND	-0.3 to +0.3	V
T_J	Operating Junction Temperature Range	-40 to 150	°C
T_A	Ambient Temperature Range	-40 to 85	
T_S	Storage Temperature Range	-65 to 150	
T_{LEAD}	Maximum Junction Soldering Temperature (at leads, 10 sec.)	300	

Thermal Information[2, 3, 4]

Symbol	Description	Value	Units
θ_{JA}	Thermal Resistance	25	°C/W
P_D	Maximum Power Dissipation	4	W

1. Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum Rating should be applied at any one time.
2. Thermal Resistance will be measured with the AAT3608 device on the 4-layer FR4 evaluation board in a thermal oven. The amount of power dissipation which will cause the thermal shutdown to activate will depend on the ambient temperature and the PC board layout ability to dissipate the heat.
3. Measured on the AAT3608 demo board.
4. Derate the maximum power dissipation by 40mW/°C above 25°C ambient temperature.

Compact Seven-Channel Regulator with Li+/Polymer Linear Battery Charger and I2C Interface

Electrical Characteristics[1]

V_{PWR_IN} = 5V, V_{PWR_ID} = 5V, V_{BAT} = 3.6V, -40°C ≤ T_A ≤ +85°C, unless noted otherwise. Typical values are T_A = 25°C.

Symbol	Description	Conditions	Min	Typ	Max	Units
Power Supply						
V_{IN}	V_{INBUCK}, V_{INLDO} Input Operating Voltage		2.7		5.5	V
	PWR_IN UVLO Threshold	Rising (100mV hysteresis)		4.5		V
I_{OPS}	Sleep Mode Battery Operating Current	V_{PWR_IN} = 0V, Only LDO1, LDO3, and Buck1 are on		200		μA
I_{OPDS}	Deep-Sleep Mode Battery Operating Current	V_{PWR_IN} = 0V, Only Buck1 is on		100		μA
I_{SHDN}	Battery Shutdown Current	V_{PWR_IN} = 0V and system is shut down			10	μA
Charger Voltage Regulation						
V_{BAT_REG}	Output Charge Voltage Regulation	0°C ≤ T_A ≤ +70°C	4.158	4.2	4.242	V
V_{MIN}	Preconditioning Voltage Threshold		2.6	2.8	3.0	V
V_{RCH}	Battery Recharge Voltage Threshold			4.00		V
Charger Current Regulation						
I_{CH_CC}	Constant-Current Mode ADP Charge Current	R_{ISETA} = 1.24kΩ (for 0.8A) (Can be set to up to 1.2A)		800		mA
	USB Charge Current	USBSEL = H, PWR_ID = L		500		mA
	USB Charge Current	USBSEL = L, PWR_ID = L		100		mA
K_{ISET}	Charge Current Set Factor: I_{CH_CC}/I_{ISET}	Constant Current Mode		800		mA/mA
I_{CH_PRE}	Preconditioning Charge Current	R_{ISETA} = 1.24kΩ		12		% I_{CH_CC}
I_{CH_TERM}	Charge Termination Threshold Current			5		% I_{CH_CC}
Charging Device						
$R_{DS(ON),CHG}$	On-Resistance of Charging Transistor	SYSOUT to BAT Switch		0.6	0.9	Ω
Logic Control / Protection						
V_{PWR_HOLD}, V_{PWR_ON}, V_{USBSEL}	Input High Threshold		1.4			V
	Input Low Threshold				0.3	V
V_{INT}, V_{STAT}	Output Low Voltage	Pin Sinks 4mA			0.4	V
V_{OVP}	Over-Voltage Protection Threshold			4.3		V
I_{OCP}	Over Current Protection Threshold			105		% I_{CH_CC}
T_C	Constant Current Mode Time Out	C_{CT} = 100nF		3		Hours
T_K	Trickle Charge Time Out			T_C/8		Hours
T_V	Constant Voltage Mode Time Out			3		Hours
I_{TS}	Current Source from TS Pin		69	75	79	μA
TS_1	TS Hot Temperature Fault	Falling Threshold	318	331	346	mV
		Hysteresis		25		mV
TS_2	TS Cold Temperature Fault	Rising Threshold	2.30	2.39	2.48	V
		Hysteresis		25		mV
T_{LOOP_IN}	Thermal Loop Entering Threshold			115		°C
T_{LOOP_OUT}	Thermal Loop Exiting Threshold			85		°C
T_{REG}	Thermal Loop Regulation			100		°C
Load Switches / SYSOUT LDO						
$R_{DS(ON),BAT-SYSOUT}$	On-Resistance of BAT-SYSOUT Load Switch			100	150	mΩ
$R_{DS(ON),PWR\_IN-SYSOUT}$	On-Resistance of PWR_IN-SYSOUT Load Switch			0.2	0.3	Ω
	PWR_IN-SYSOUT Current Limit			2		A
	PWR_IN-SYSOUT Current Limit	USBSEL = High, PWR_ID = L	400	450	500	mA
		USBSEL = Low, PWR_ID = L		100		mA
	BAT-SYSOUT Current Limit			2		A

1. Specification over the -40°C to +85°C operating temperature range is assured by design, characterization and correlation with statistical process controls.

Electrical Characteristics (continued)[1]

V_{PWR_IN} = 5V, V_{PWR_ID} = 5V, V_{BAT} = 3.6V, -40°C ≤ T_A ≤ +85°C, unless noted otherwise. Typical values are T_A = 25°C.

Symbol	Description	Conditions	Min	Typ	Max	Units
Step-Down Buck Regulator (Buck1)						
V_{INBUCK}	Input Voltage Range		2.7		5.5	V
V_{OUT}	Output Voltage Programmable Range	Using External Feedback Resistors, No Load	0.6		V_{INBUCK}	V
V_{REG}	Output Voltage Accuracy	I_{OUT} = 10mA	0.582	0.600	0.618	V
I_{LIM}	P-Channel Current Limit			2600		mA
$R_{DS(ON)H}$	High-Side Switch On-Resistance			450		mΩ
$R_{DS(ON)L}$	Low-Side Switch On-Resistance			400		mΩ
$\Delta V_{OUT} / (V_{OUT}\ \Delta V_{IN})$	Line Regulation			0.2		%/V
F_{OSC}	Oscillator Frequency			1.5		MHz
Step-Down Buck Regulator (Buck2)						
V_{INBUCK}	Input Voltage Range		2.7		5.5	V
V_{FB}	Feedback Voltage Programmable Range	Using I²C, with Default FB = 0.6V	0.5		0.7	V
V_{REG}	Output Voltage Accuracy	I_{OUT} = 10mA	-3		+3	%
I_{LIM}	P-Channel Current Limit			2600		mA
$R_{DS(ON)H}$	High-Side Switch On-Resistance			450		mΩ
$R_{DS(ON)L}$	Low-Side Switch On-Resistance			400		mΩ
$\Delta V_{OUT} / (V_{OUT}\ \Delta V_{IN})$	Line Regulation			0.2		%/V
F_{OSC}	Oscillator Frequency			1.5		MHz
Low-Dropout Regulator (LDO1)						
V_{INLDO}	Input Voltage Range		2.7		5.5	V
V_{LDO}	LDO Output Voltage	I_{LDO} = 1mA to 300mA, S1 = 0, S2 = 0	2.91	3.00	3.09	V
		I_{LDO} = 1mA to 300mA, S1 = 0, S2 = 1	3.20	3.30	3.40	V
		I_{LDO} = 1mA to 300mA, S1 = 1, S2 = 0	2.71	2.80	2.89	V
I_Q	LDO Quiescent Current	V_{INLDO} = 5V, added quiescent current when LDO is enabled		50	90	µA
	Line Regulation	I_{LDO} = 10mA		0.09		%/V
	Dropout Voltage	I_{LDO} = 300mA		100	170	mV
I_{LDO}	LDO Maximum Load Current		500			mA
$I_{LDO(LIM)}$	LDO Current Limit			800		mA
Low-Dropout Regulator (LDO2)						
V_{INLDO}	Input Voltage Range		2.7		5.5	V
V_{LDO}	LDO Output Voltage	I_{LDO} = 1mA to 80mA	1.164	1.2	1.236	V
I_Q	LDO Quiescent Current	V_{INLDO} = 5V, added quiescent current when LDO is enabled		35	80	µA
	Line Regulation	I_{LDO} = 10mA		0.09		%/V
I_{LDO}	LDO Maximum Load Current		200			mA
$I_{LDO(LIM)}$	LDO Current Limit			800		mA
Low-Dropout Regulator (LDO3)						
V_{INLDO}	Input Voltage Range		2.7		5.5	V
	Output Voltage Range	Using I²C. Default=1.2V	0.8		1.4	V
V_{LDO}	LDO Output Voltage	I_{LDO} = 1mA to 80mA	-3		+3	%
I_Q	LDO Quiescent Current	V_{INLDO} = 5V, added quiescent current when LDO is enabled		35	80	µA
	Line Regulation	I_{LDO} = 10mA		0.09		%/V
I_{LDO}	LDO Maximum Load Current		200			mA
$I_{LDO(LIM)}$	LDO Current Limit			800		mA

1. Specification over the -40°C to +85°C operating temperature range is assured by design, characterization and correlation with statistical process controls.

Electrical Characteristics (continued)[1]

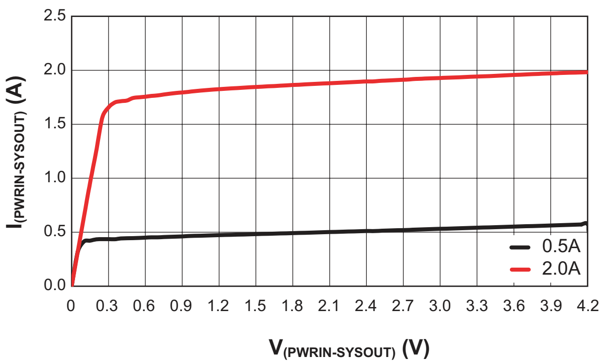
V_{PWR_IN} = 5V, V_{PWR_ID} = 5V, V_{BAT} = 3.6V, -40°C ≤ T_A ≤ +85°C, unless noted otherwise. Typical values are T_A = 25°C.

Symbol	Description	Conditions	Min	Typ	Max	Units
Low-Dropout Regulator (LDO4)						
V_{INLDO}	Input Voltage Range		2.7		5.5	V
V_{LDO}	LDO Output Voltage	I_{LDO} = 1mA to 50mA	2.425	2.5	2.575	V
I_Q	LDO Quiescent Current	V_{INLDO} = 5V, added quiescent current when LDO is enabled		50	80	μA
	Line Regulation	I_{LDO} = 10mA		0.09		%/V
I_{LDO}	LDO Maximum Load Current		200			mA
$I_{LDO(LIM)}$	LDO Current Limit			800		mA
Low-Dropout Regulator (LDO5)						
V_{INLDO}	Input Voltage Range		2.7		5.5	V
V_{LDO}	LDO Output Voltage	I_{LDO} = 1mA to 50mA	3.2	3.3	3.4	V
I_Q	LDO Quiescent Current	V_{INLDO} = 5V, added quiescent current when LDO is enabled		50	80	μA
	Line Regulation	I_{LDO} = 10mA		0.09		%/V
I_{LDO}	LDO Maximum Load Current		200			mA
$I_{LDO(LIM)}$	LDO Current Limit			800		mA
Reset and Low-Battery Comparator						
	Buck2 Power OK Threshold	Rising threshold			91	%
		Hysteresis		3		%
	Reset Time	From Power OK of $BUCK_2$ output to RESET pin rising edge		200		ms
	Low-Battery Threshold Voltage	Falling Edge	0.96	1.0	1.04	V
		Hysteresis		50		mV
Thermal						
T_{SD}	Over-Temperature Shutdown Threshold	Rising		140		°C
T_{HYS}	Over-Temperature Shutdown Hysteresis			15		°C
SCL, SDA (I^2C Interface)						
F_{SCL}	Clock Frequency		0		400	kHz
T_{LOW}	Clock Low Period		1.3			μs
T_{HIGH}	Clock High Period		0.6			μs
T_{HD_STA}	Hold Time for START Condition		0.6			μs
T_{SU_STA}	Set-up Time for Repeated START Condition		0.6			μs
T_{SU_DAT}	Data Setup Time		100			ns
T_{HD_DAT}	Data Hold Low Time				0.9	μs
T_{SU_STO}	Setup Time for STOP Condition		0.6			μs
T_{BUF}	Bus Free Time Between STOP and START Condition		1.3			μs
V_{IL}	Input Threshold Low	2.7V ≤ V_{IN} ≤ 5.5V			0.3	V
V_{IH}	Input Threshold High	2.7V ≤ V_{IN} ≤ 5.5V	1.4			V
I_I	Input Leakage Current		-1.0		1.0	μA
V_{OL}	Output Logic Low (SDA)	I_{PULLUP} = 3mA			0.3	V

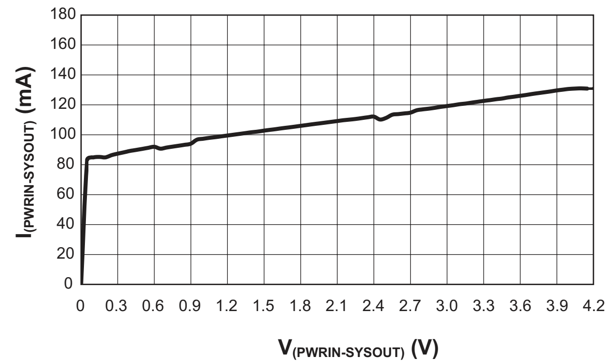
1. Specification over the -40°C to +85°C operating temperature range is assured by design, characterization and correlation with statistical process controls.

Typical Characteristics—Charger

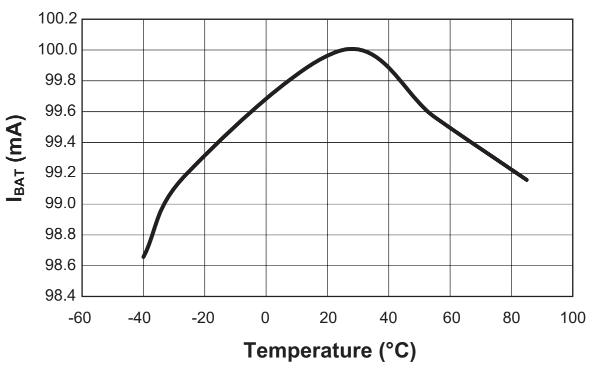
Power-In to SYSOUT Switch Current Limit



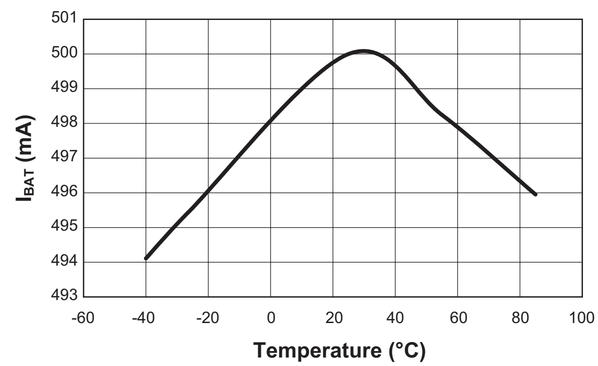
Power-In to SYSOUT Switch Current Limit (100mA)



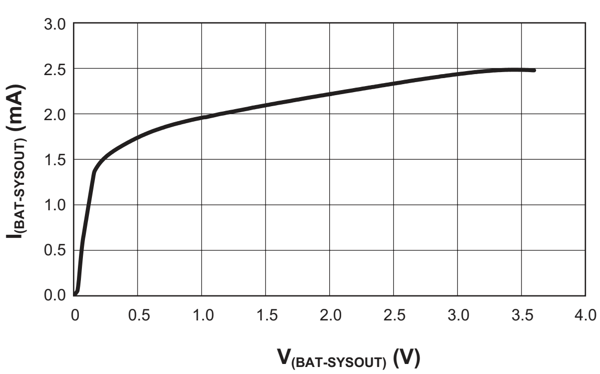
I_{BAT} vs. Temperature (100mA)



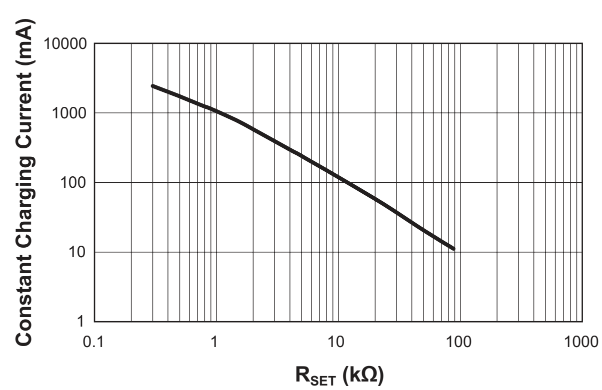
I_{BAT} vs. Temperature (500mA)



Ideal Diode Load Switch between V_{BAT} and V_{SYSOUT}

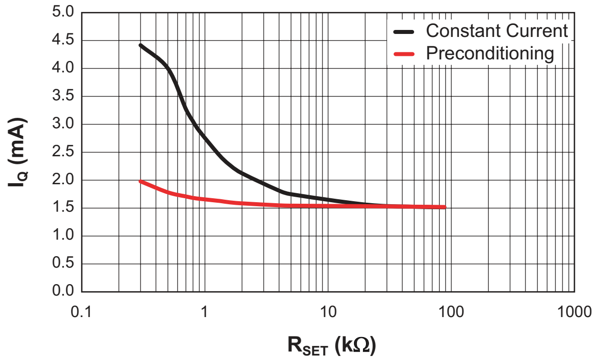


Constant Charging Current vs. R_{SET}



Typical Characteristics–Charger

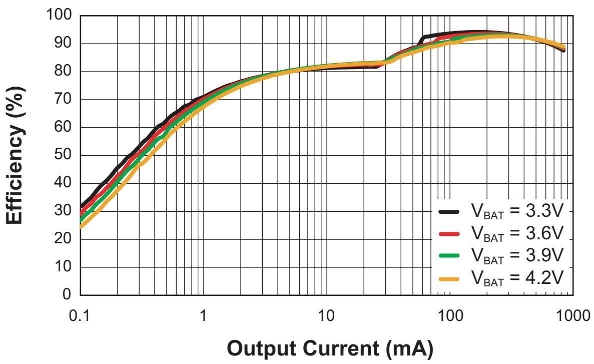
Adapter Mode Supply Current vs. R_{SET} Resistor



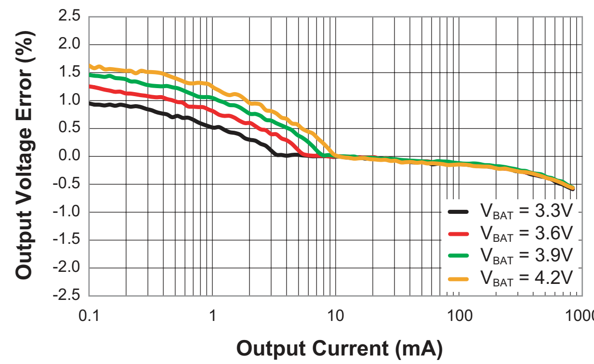
Compact Seven-Channel Regulator with Li+/Polymer Linear Battery Charger and I2C Interface

Typical Characteristics—Buck1

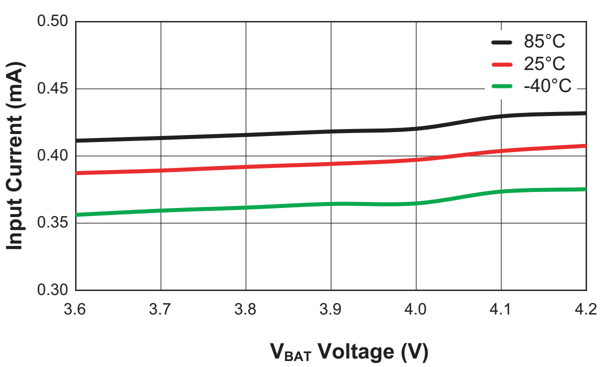
Efficiency vs. Load
(V_{B1} = 2.5V; L_1 = 2.2µH)



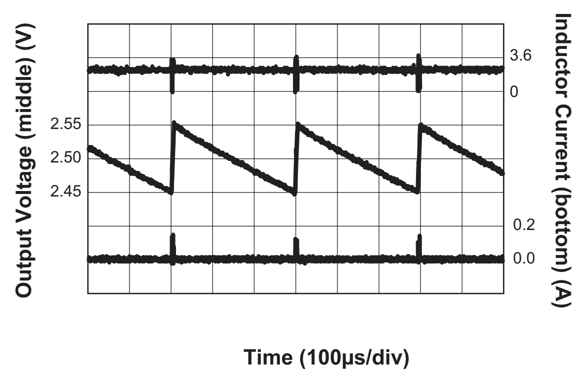
Load Regulation
(V_{B1} = 2.5V; L_1 = 2.2µH)



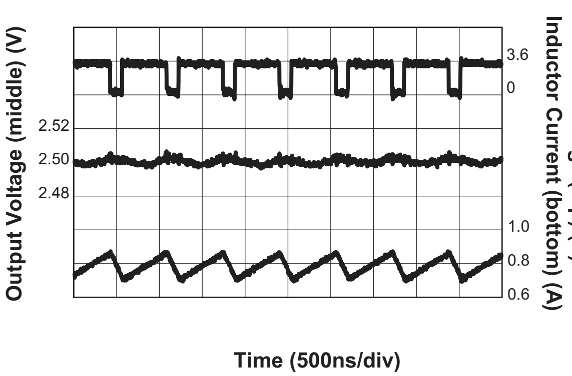
No Load Total Input Current vs. V_{BAT} Voltage
(V_{EN} = V_{BAT}; Closed Loop)



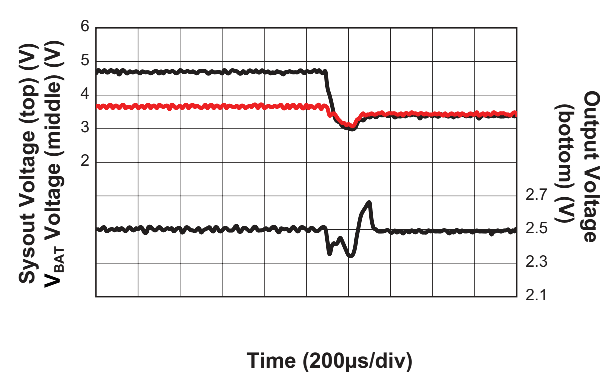
Output Ripple
(V_{BAT} = 3.6V; V_{B1} = 2.5V; I_{OUTB1} = 1mA)



Output Ripple
(V_{BAT} = 3.6V; V_{B1} = 2.5V; I_{OUTB1} = 800mA)



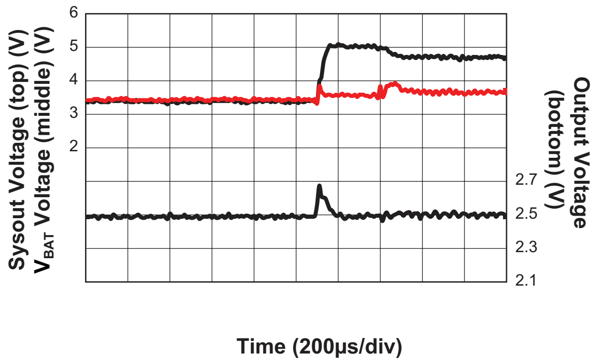
System Line Transient Response
(V_{IN} = 3.5V to 5V; V_{BAT} = 3.6V; V_{OUTB1} = 2.5V; I_{OUTB1} = 800mA; falling)



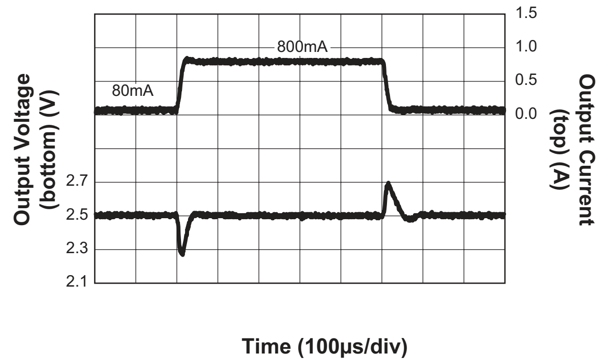
Skyworks Solutions, Inc. • Phone [781] 376-3000 • Fax [781] 376-3100 • sales@skyworksinc.com • www.skyworksinc.com

Typical Characteristics–Buck1 (continued)

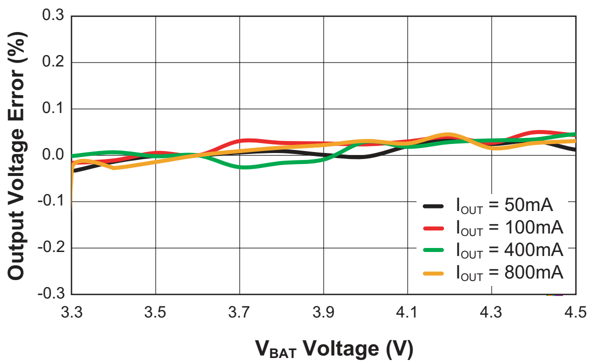
System Line Transient Response
(V_{IN} = 3.5V to 5V; V_{BAT} = 3.6V; V_{OUTB1} = 2.5V; I_{OUTB1} = 800mA; rising)



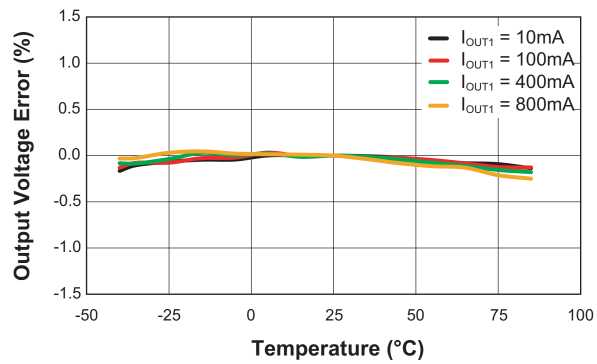
System Load Transient Response
(I_{OUTB1} = 80mA to 800mA; V_{BAT} = 3.6V; C_{OUTB1} = 4.7µF; C_{FF1} = 0pF)



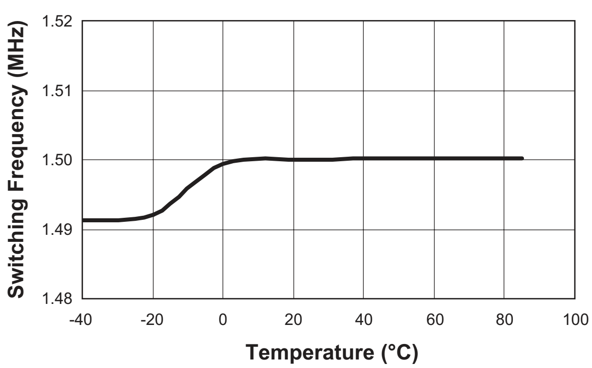
Line Regulation
(V_{OUT1} = 2.5V; L_1 = 2.2µH)



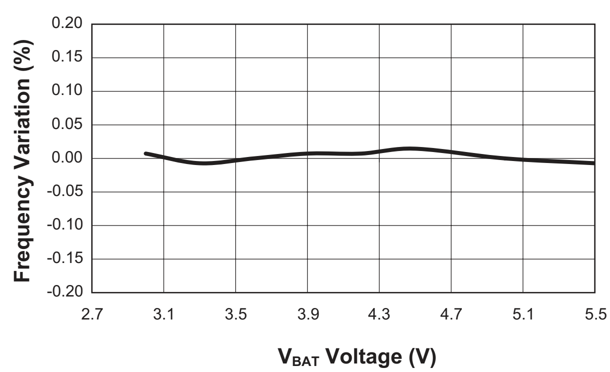
Output Voltage Error vs. Temperature
(V_{BAT} = 3.6V; V_{OUT1} = 2.5V)



Switching Frequency vs. Temperature
(V_{IN} = 3.6V; V_{OUT1} = 2.5V; I_{OUT1} = 800mA)

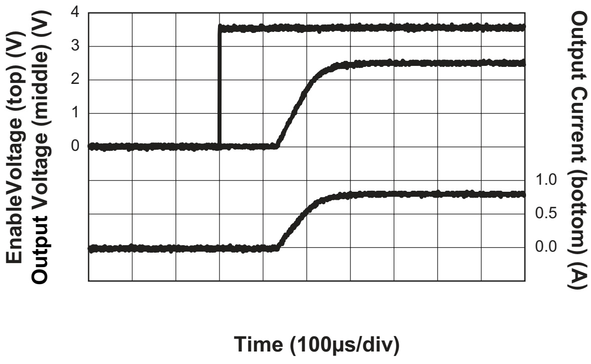


Switching Frequency vs. V_{BAT} Voltage
(V_{OUT1} = 2.5V; I_{OUT1} = 800mA)



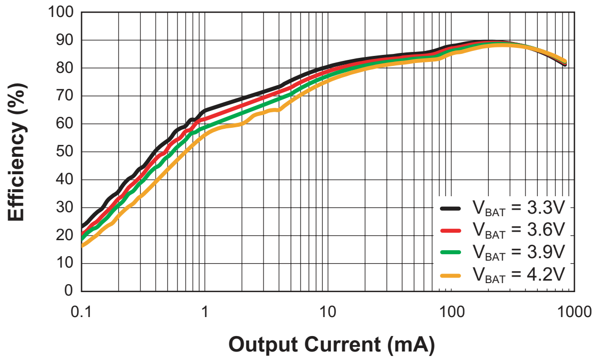
Typical Characteristics−Buck1 (continued)

Soft Start
(V_{BAT} = 3.6V; V_{OUT1} = 2.5V; I_{OUT1} = 800mA; C_{FF} = 100pF)

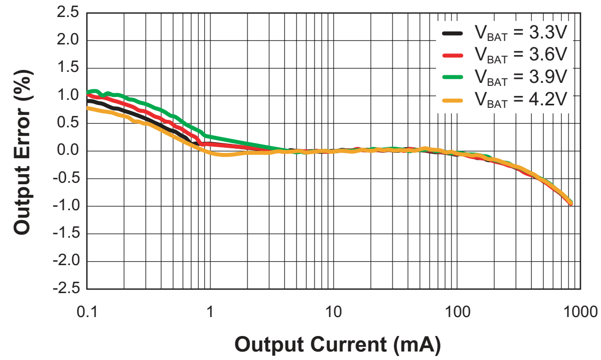


Typical Characteristics—Buck2

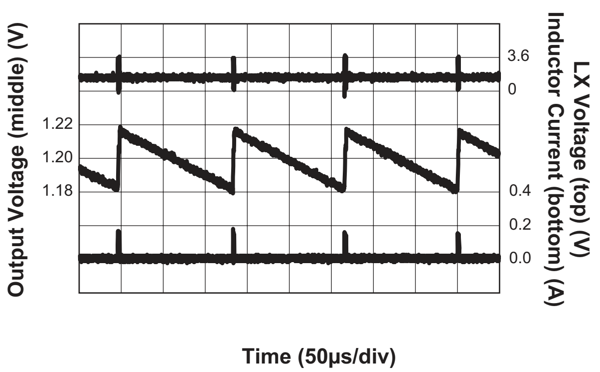
Efficiency vs. Load
(V_{B2} = 1.2V; L_2 = 2.2µH)



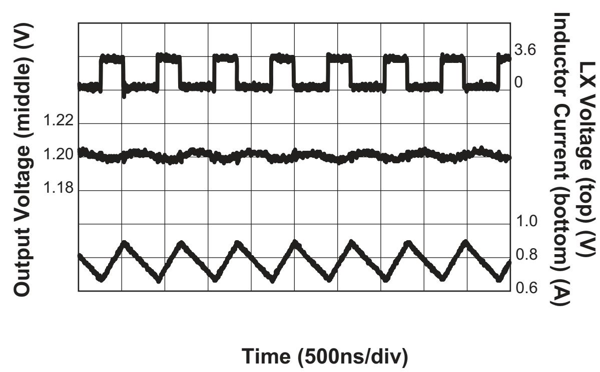
DC Regulation vs. Load
(V_{B2} = 1.2V; L_2 = 2.2µH)



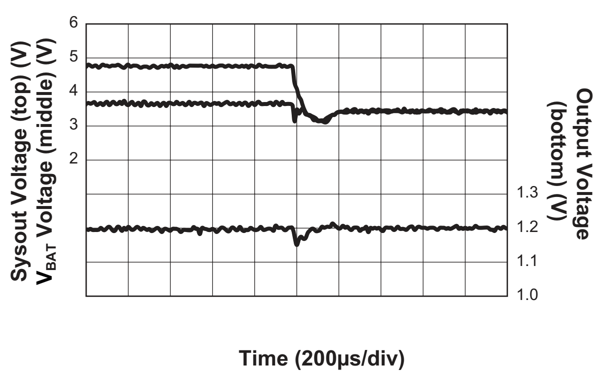
Output Ripple
(V_{BAT} = 3.6V; V_{OUTB2} = 1.2V; I_{OUTB2} = 1mA)



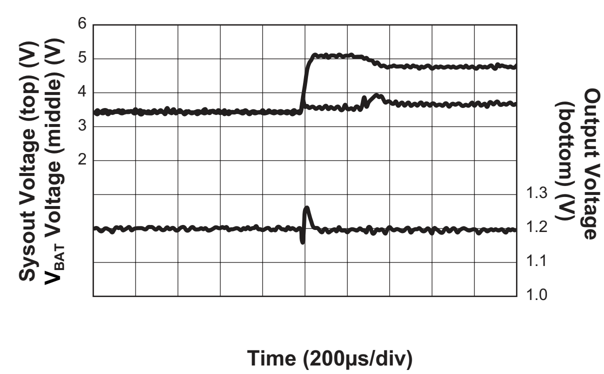
Output Ripple
(V_{BAT} = 3.6V; V_{OUTB2} = 1.2V; I_{OUTB2} = 800mA)



System Line Transient Response
(V_{IN} = 3.5V to 5V; V_{BAT} = 3.6V; V_{OUTB2} = 1.2V; I_{OUTB2} = 800mA; falling)

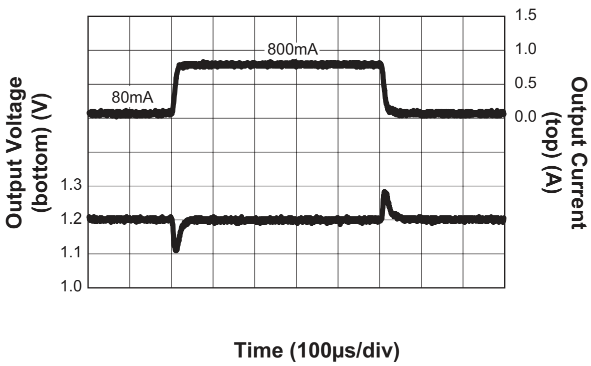


System Line Transient Response
(V_{IN} = 3.5V to 5V; V_{BAT} = 3.6V; V_{OUTB2} = 1.2V; I_{OUTB2} = 800mA; rising)

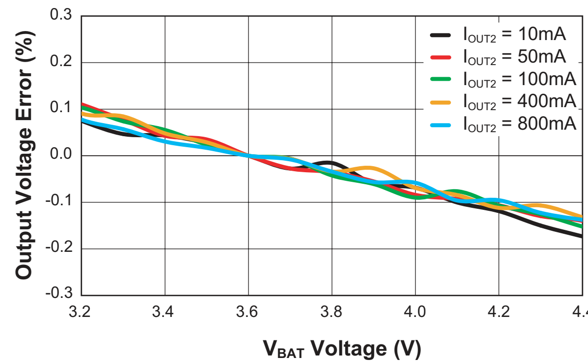


Typical Characteristics—Buck2 (continued)

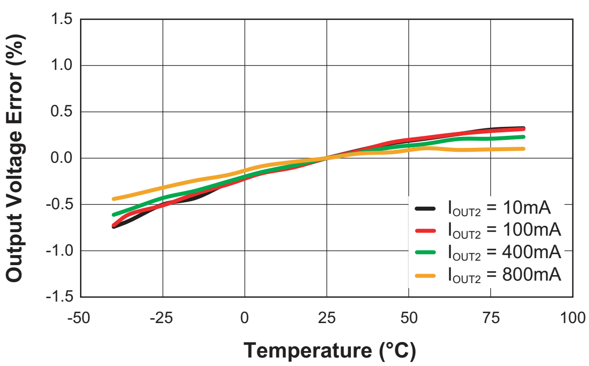
System Load Transient Response
(I_{OUTB2} = 80mA to 800mA; V_{BAT} = 3.6V; C_{OUTB2} = 4.7µF; C_{FF1} = 0pF)



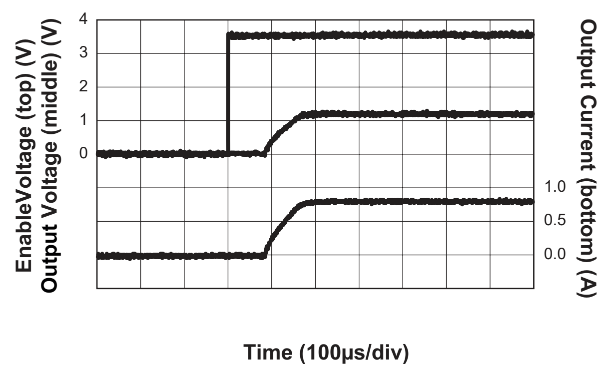
Line Regulation
(V_{OUT2} = 2.5V; L_2 = 2.2µH)



Output Voltage Error vs. Temperature
(V_{BAT} = 3.6V; V_{OUT2} = 1.2V)

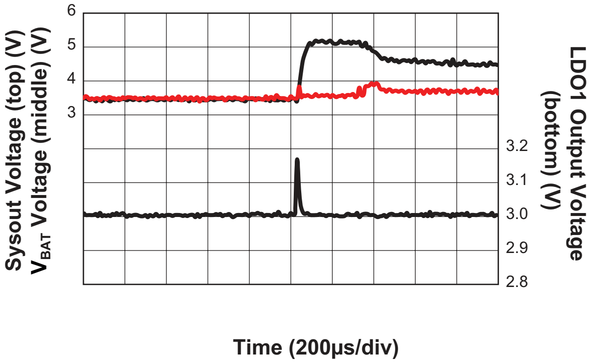


Soft Start
(V_{BAT} = 3.6V; V_{OUT1} = 1.2V; I_{OUT2} = 800mA; C_{FF} = 100pF)

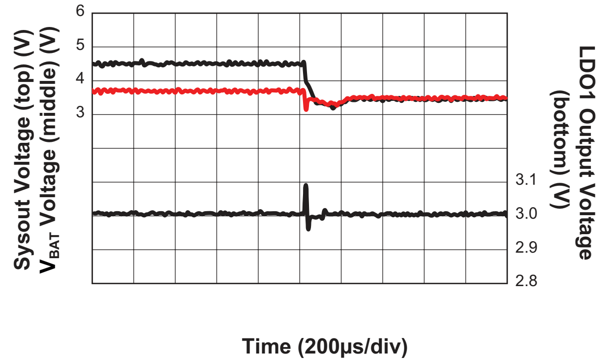


Typical Characteristics–LDO1

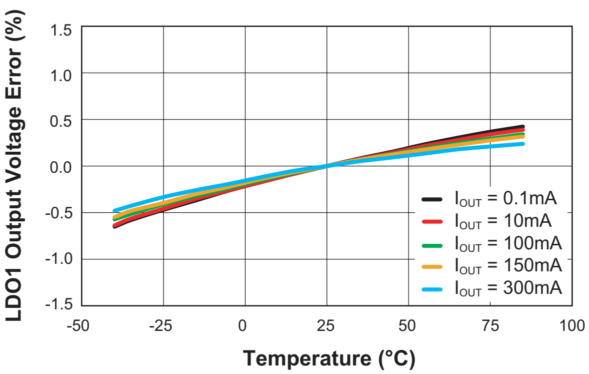
System Line Transient Response
(V_{IN} = 3.5V to 5V; V_{BAT} = 3.6V; V_{LDO1} = 3V; I_{LDO1} = 300mA; rising)



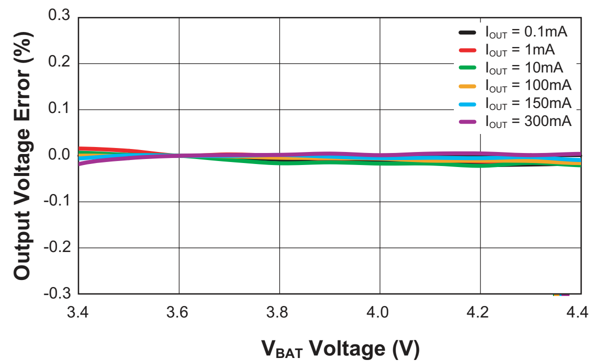
System Line Transient Response
(V_{IN} = 3.5V to 5V; V_{BAT} = 3.6V; V_{LDO1} = 3V; I_{LDO1} = 300mA; falling)



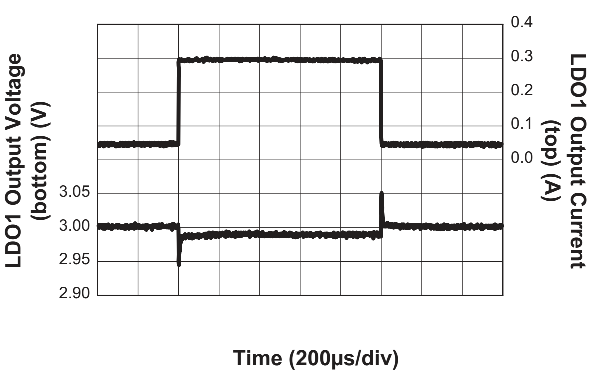
Output Voltage Error vs. Temperature
(V_{BAT} = 3.6V; V_{LDO1} = 3.0V)



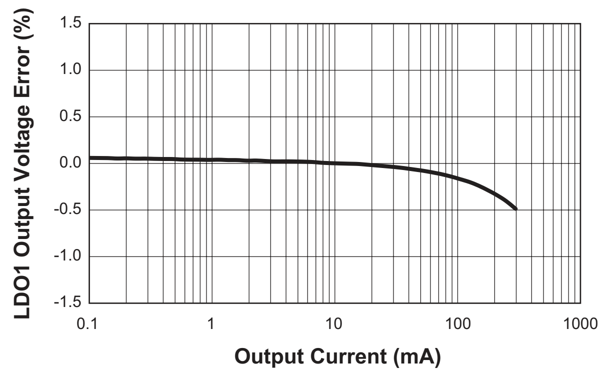
Line Regulation
(V_{LDO1} = 3.0V)



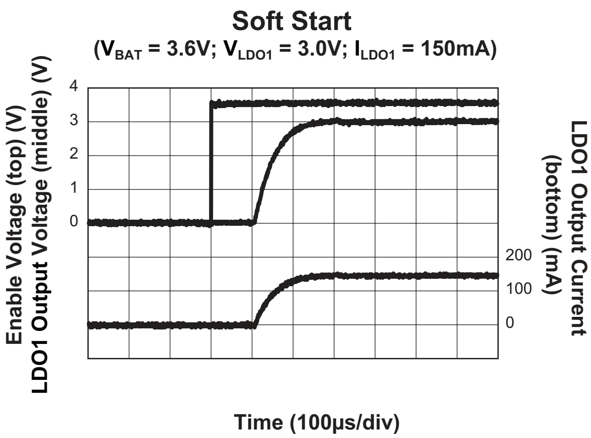
Load Transient Response
(I_{LDO1} = 30mA to 300mA; V_{BAT} = 3.6V; V_{LDO1} = 3V; C_{LDO1} = 4.7µF)



Load Regulation
(V_{BAT} = 3.6V; V_{LDO1} = 3.0V)

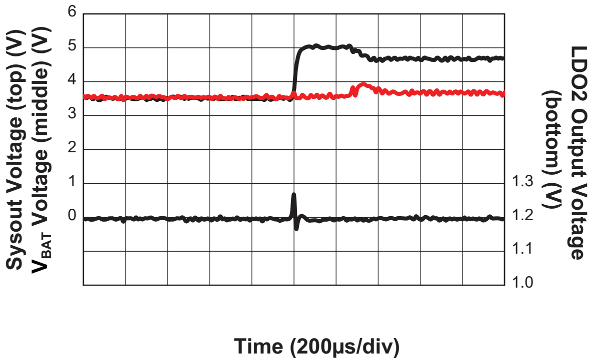


Typical Characteristics−LDO1 (continued)

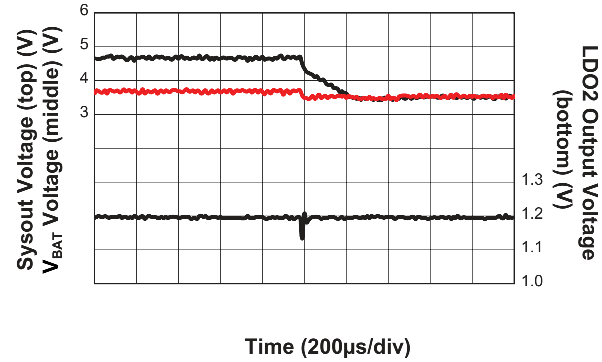


Typical Characteristics—LDO2

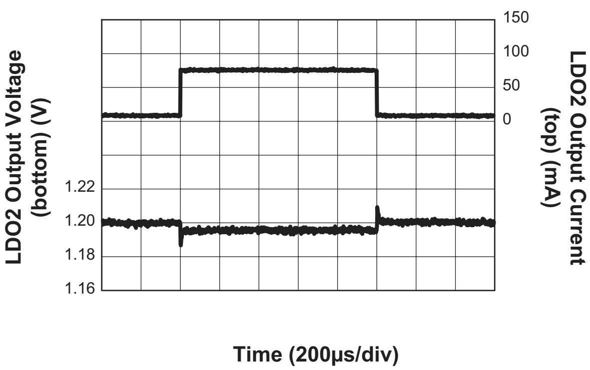
System Line Transient Response
(V_{IN} = 3.5V to 5V; V_{BAT} = 3.6V; V_{LDO2} = 1.2V; I_{LDO2} = 80mA; rising)



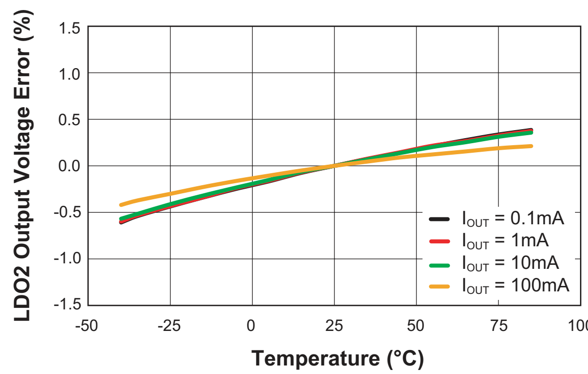
System Line Transient Response
(V_{IN} = 3.5V to 5V; V_{BAT} = 3.6V; V_{LDO2} = 1.2V; I_{LDO2} = 80mA; falling)



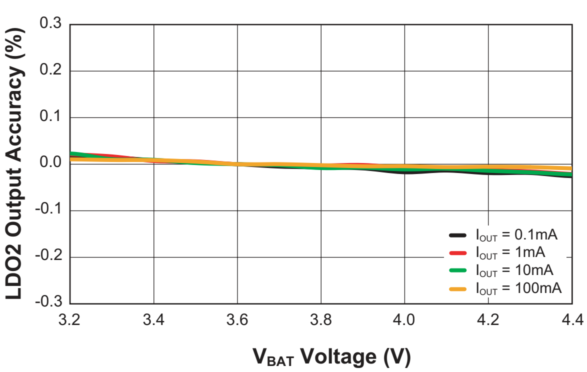
Load Transient Response
(I_{LDO2} = 8mA to 80mA; V_{BAT} = 3.6V; V_{LDO2} = 1.2V; C_{LDO2} = 4.7µF)



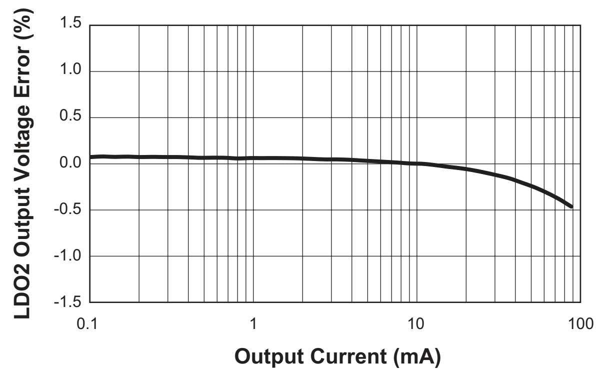
Output Voltage Error vs. Temperature
(V_{BAT} = 3.6V; V_{LDO2} = 1.2V)



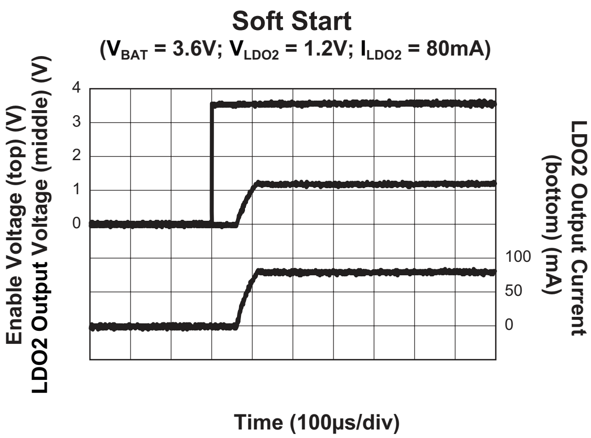
Line Regulation
(V_{LDO2} = 1.2V)



Load Regulation
(V_{BAT} = 3.6V; V_{LDO2} = 1.2V)

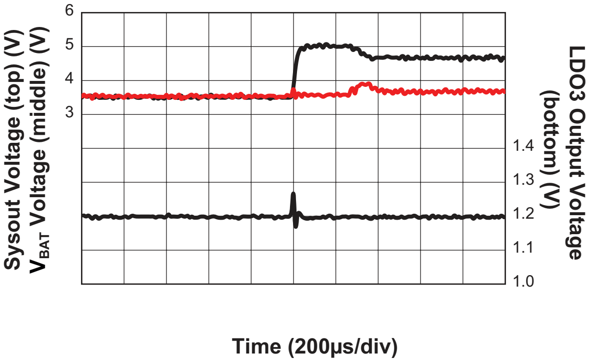


Typical Characteristics−LDO2 (continued)

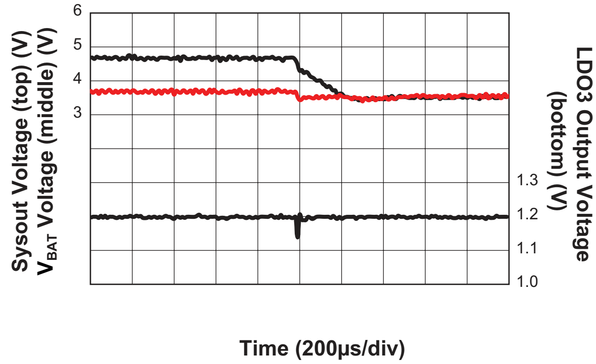


Typical Characteristics–LDO3

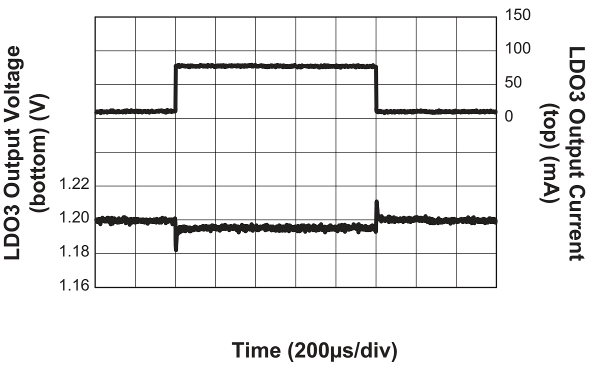
System Line Transient Response
(V_{IN} = 3.5V to 5V; V_{BAT} = 3.6V; V_{LDO3} = 1.2V; I_{LDO3} = 80mA; rising)



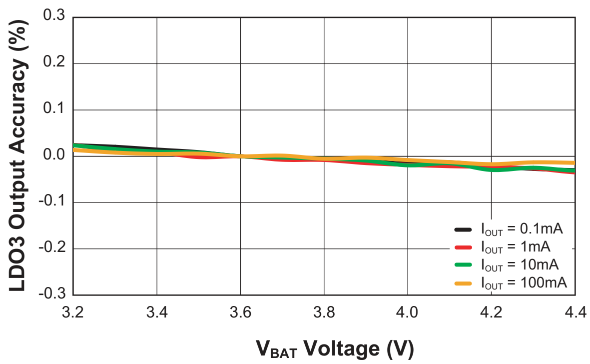
System Line Transient Response
(V_{IN} = 3.5V to 5V; V_{BAT} = 3.6V; V_{LDO3} = 1.2V; I_{LDO3} = 80mA; falling)



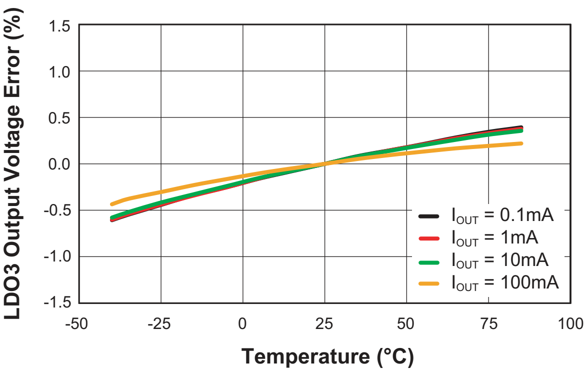
Load Transient Response
(I_{LDO3} = 8mA to 80mA; V_{BAT} = 3.6V; C_{LDO3} = 4.7µF)



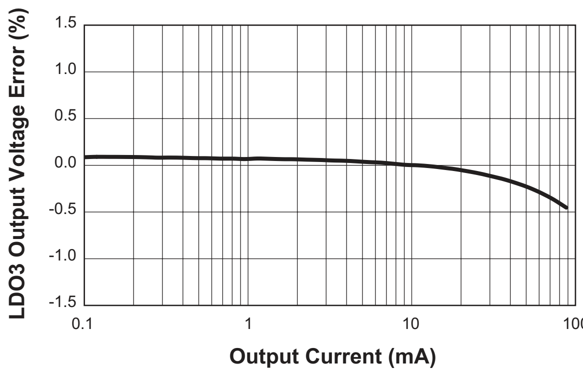
Line Regulation
(V_{LDO3} = 1.2V)



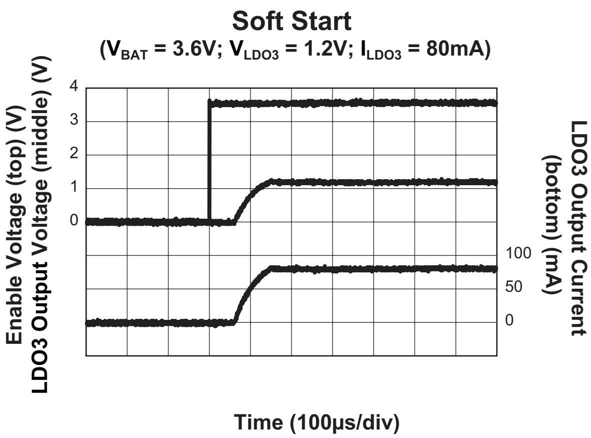
Output Voltage Error vs. Temperature
(V_{BAT} = 3.6V; V_{LDO3} = 1.2V)



Load Regulation
(V_{BAT} = 3.6V; V_{LDO3} = 1.2V)

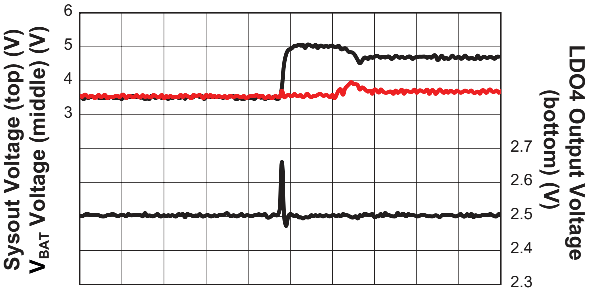


Typical Characteristics−LDO3 (continued)

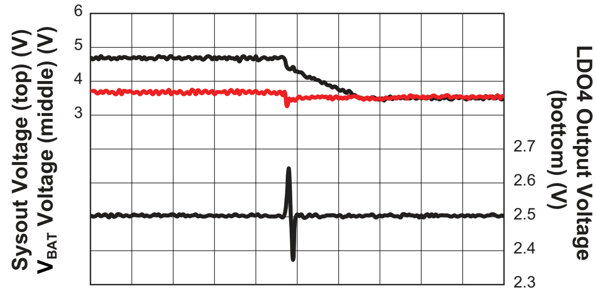


Typical Characteristics–LDO4

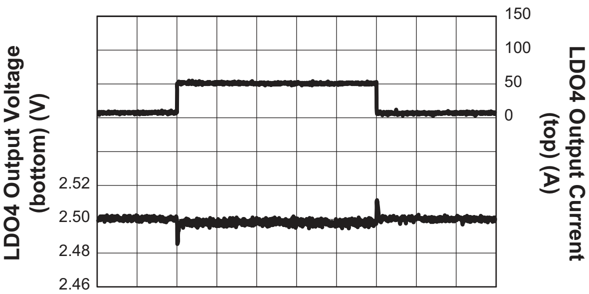
System Line Transient Response
(V_{IN} = 3.5V to 5V; V_{BAT} = 3.6V; V_{LDO4} = 2.5V; I_{LDO4} = 50mA; rising)



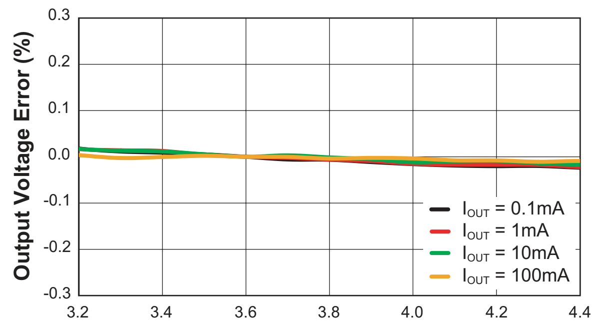
System Line Transient Response
(V_{IN} = 3.5V to 5V; V_{BAT} = 3.6V; V_{LDO4} = 2.5V; I_{LDO4} = 50mA; falling)



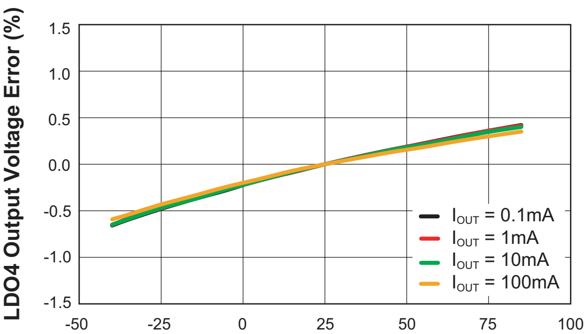
Load Transient Response
(I_{LDO4} = 5mA to 50mA; V_{BAT} = 3.6V; V_{LDO4} = 2.5V; C_{LDO4} = 4.7µF)



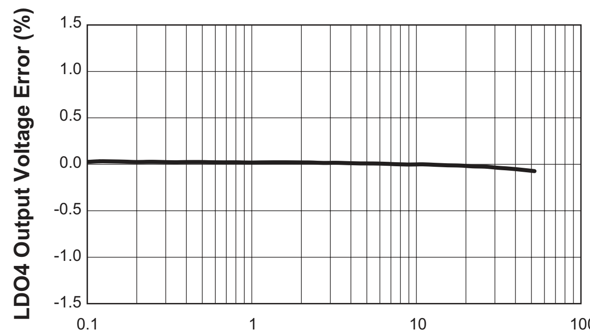
Line Regulation
(V_{LDO4} = 2.5V)



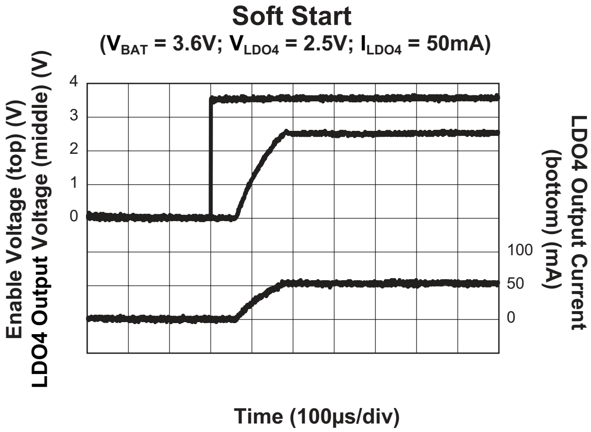
Output Voltage Error vs. Temperature
(V_{BAT} = 3.6V; V_{LDO4} = 2.5V)



Load Regulation
(V_{BAT} = 3.6V; V_{LDO4} = 2.5V)

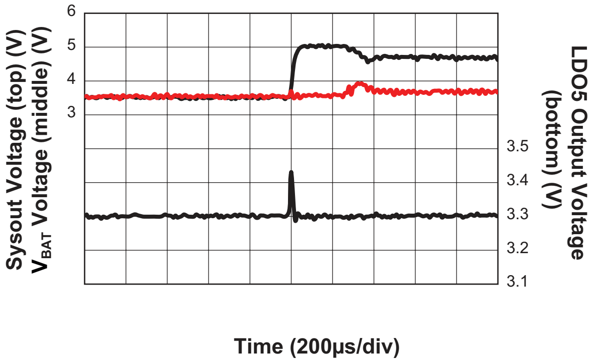


Typical Characteristics–LDO4 (continued)

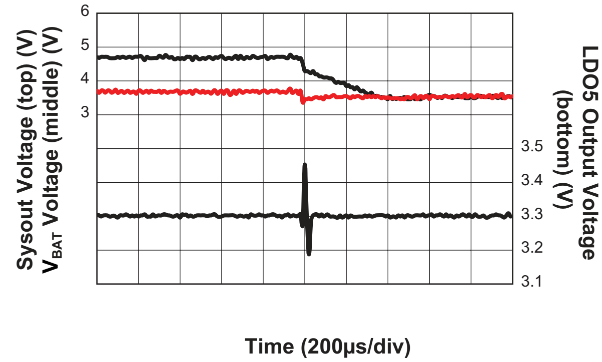


Typical Characteristics–LDO5

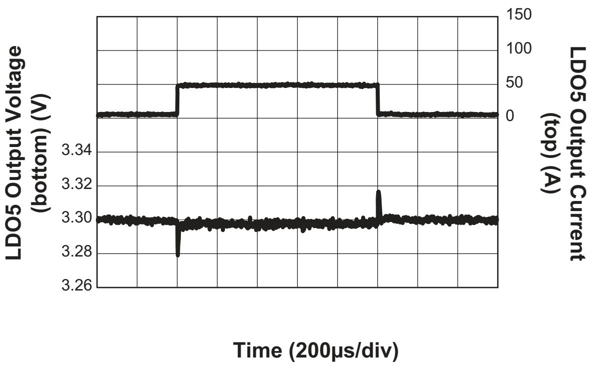
System Line Transient Response
(V_{IN} = 3.5V to 5V; V_{BAT} = 3.6V; V_{LDO5} = 3.3V; I_{LDO5} = 50mA; rising)



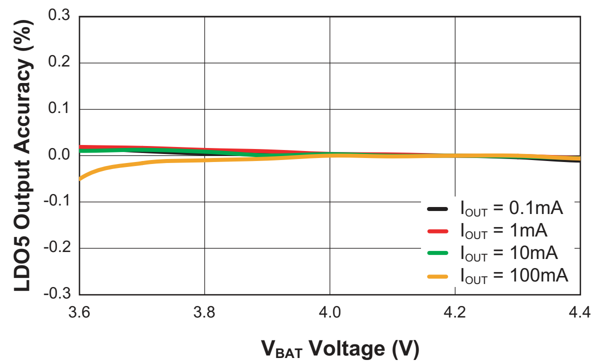
System Line Transient Response
(V_{IN} = 3.5V to 5V; V_{BAT} = 3.6V; V_{LDO5} = 3.3V; I_{LDO5} = 50mA; falling)



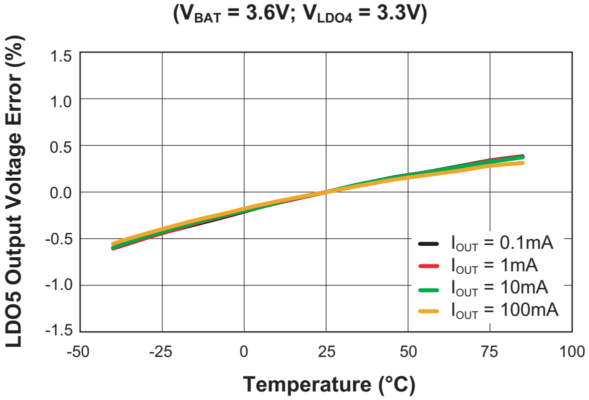
Load Transient Response
(I_{LDO5} = 5mA to 50mA; V_{BAT} = 3.9V; C_{LDO5} = 4.7µF)



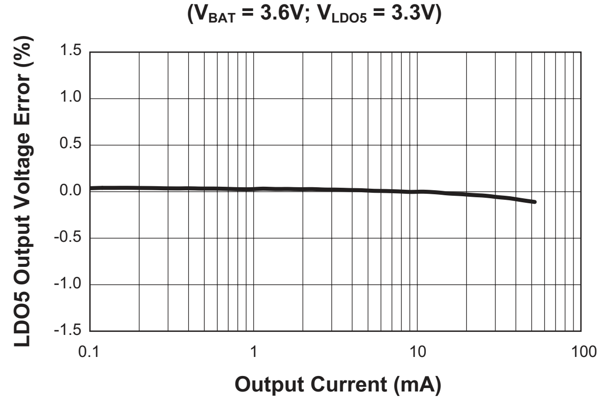
Line Regulation
(V_{LDO5} = 3.3V)



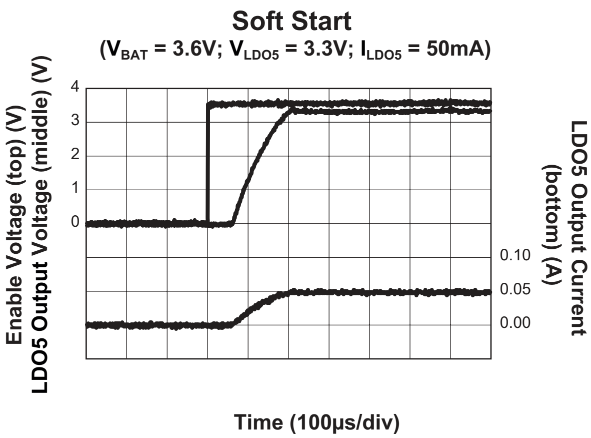
Output Voltage Error vs. Temperature
(V_{BAT} = 3.6V; V_{LDO4} = 3.3V)



Load Regulation
(V_{BAT} = 3.6V; V_{LDO5} = 3.3V)

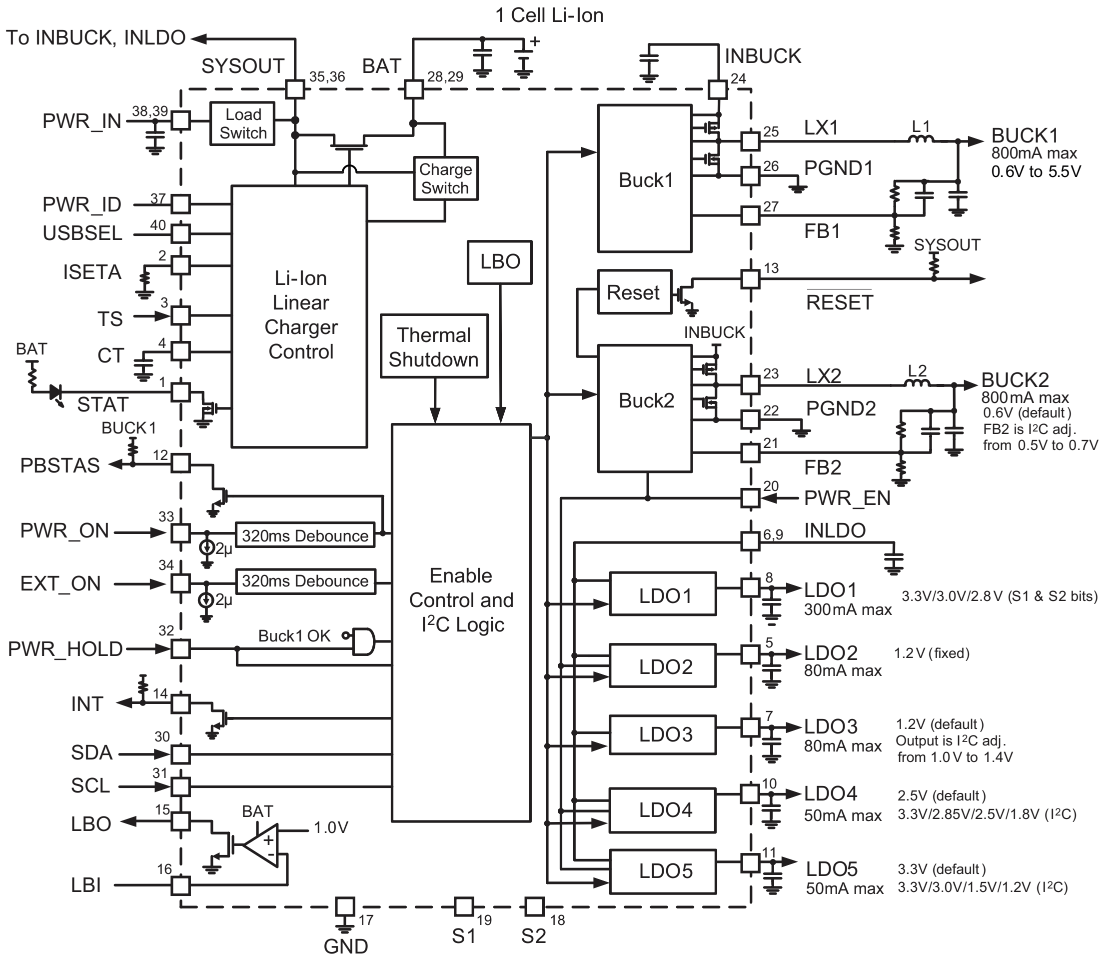


Typical Characteristics–LDO5 (continued)



Compact Seven-Channel Regulator with Li+/Polymer Linear Battery Charger and I2C Interface

Functional Block Diagram



Functional Description

The AAT3608 is a complete power management solution. It seamlessly integrates a battery charger with two step-down converters and five low-dropout regulators to provide power from either an external power source or a single-cell Lithium Ion/Polymer battery. Internal load switches allow the converters to operate from the best available power source.

If only the battery is available, then the voltage converters are powered directly from the battery through a 100 mΩ load switch (BAT to SYSOUT). During this condition, the charger is put into sleep mode and draws less than 1μA quiescent current. If the system is connected to a wall adapter, then the voltage converters are powered directly from the adapter through a 200mΩ load-switch (PWR_IN to SYSOUT) and the battery is disconnected from the voltage converter inputs. This allows the system to operate regardless of the state of the battery. It can even operate with no battery.

System Output (SYSOUT)

Intelligent control of the integrated load switches is managed by the switch control circuitry. If the voltage across PWR_IN and GND pin is above the UVLO typical threshold voltage of 4.5, then the switch control will automatically short the load switch connecting PWR_IN to SYSOUT. Additionally, the charging switch will be enabled and switch connecting BAT and SYSOUT will be turned off. The location of the two switches and the battery charging switch allows the step-down converter and LDO to always have the best available source of power. Furthermore, AAT3806 control logic allows the voltage converters to operate with no battery, or with a battery voltage below the trickle charge threshold.

Battery Charging

Battery charging commences only after the AAT3608 battery charger checks several conditions in order to maintain a safe charging environment. When an adapter input is connected to PWR_IN and is greater than 4.5V, the EN_{CHG} bit is set (default) and the PWR_HOLD signal is high, the charger is enabled. The charger can be disabled by clearing the EN_{CHG} bit through the I^2C interface.

Figure 1 illustrates the entire battery charging profile or operation, which consists of three phases:

1. Preconditioning (Trickle) Charge
2. Constant Current Charge
3. Constant Voltage Charge

During battery charging, the battery charger initially checks the condition of the battery and determines which charging mode to apply. If the battery voltage is below V_{MIN}, then the battery charger initiates trickle charge mode and charges the battery at 12% of the programmed constant-current magnitude. For example, if the programmed current (I_{SETA}) is 500mA, then the trickle charge current will be 60mA. Trickle charge is a safety precaution for a deeply discharged cell. It is intended to reduce stress on the battery, but also reduces the power dissipation in the internal series pass MOSFET when the input-output voltage differential is at its highest.

Trickle charge continues until the battery voltage reaches 2.8V. At this point the battery charger begins constant-current charging. The current level for this mode is programmed using a resistor from the ISETA pin to ground, or can be selected through the USBSEL pin with settings of 100mA or 500mA; refer to the logic settings in Table 2. Constant-current charging continues until the voltage reaches the charge voltage regulation point.

V_{BAT_REG} is factory programmed to 4.2V (nominal). Charging in constant-voltage mode will continue until the charge current has reduced to the charge termination current threshold. After the charge cycle is complete, the battery charger turns off the series pass device and automatically goes into a power saving sleep mode. During this time, the series pass device will block current in both directions to prevent the battery from discharging through the battery charger.

The battery charger will remain in sleep mode even if the charger source is disconnected. It will come out of sleep mode when either the battery terminal voltage drops below the V_{RCH} threshold, or the charging source is removed and reconnected. In all cases, the battery charger will monitor all parameters and resume charging in the most appropriate mode.

Battery Temperature Fault Monitoring

The TS pin is available to monitor the battery temperature. Connect a 10k NTC resistor from the TS pin to ground. The TS pin outputs a 75µA constant current into the resistor and monitors the voltage to ensure that the battery temperature does not fall outside the operating limits depending on the temperature coefficient of the resistor used. When the voltage goes above 2.39V or goes below 0.331V, the charging will be suspended. A Beta range of 3300 to 4000 will place the typical charging temperature between -4°C and 48°C.

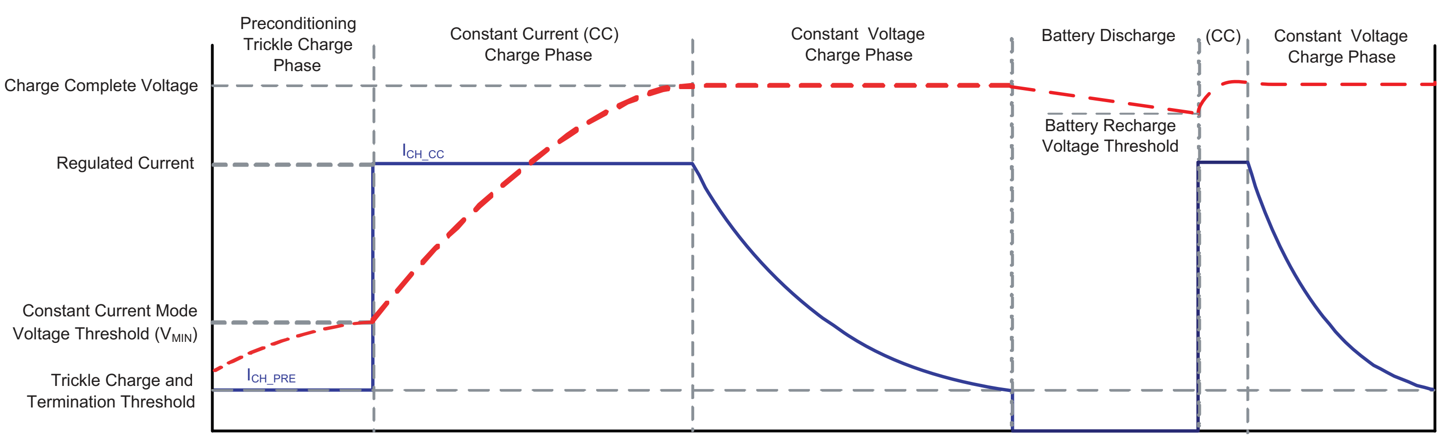
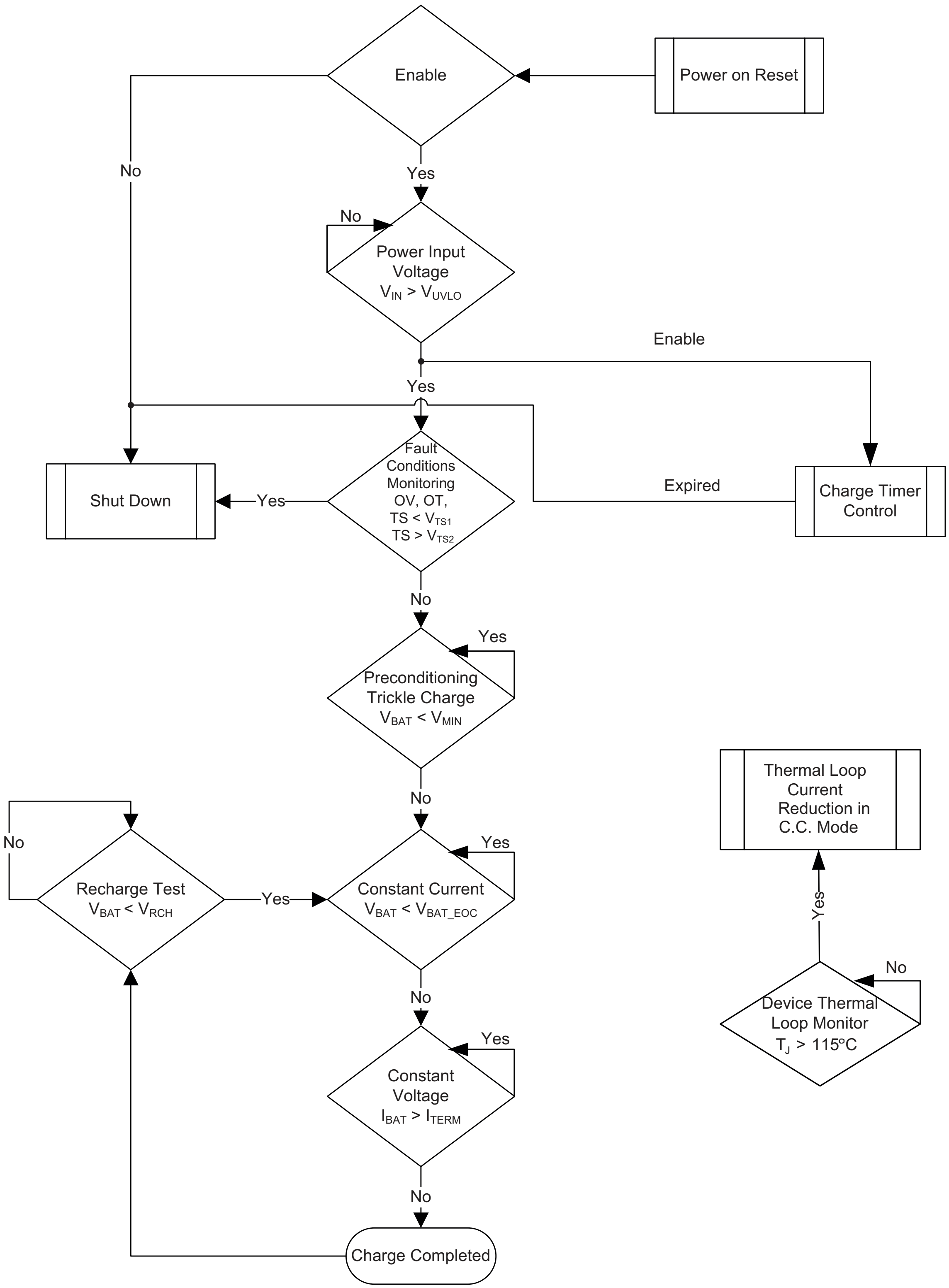


Figure 1: Current vs. Voltage Profile During Charging Phases.

Battery Charging Flowchart



Buck Regulators

The AAT3608 step-down converters are peak current mode PWM converters operating at 1.5MHz frequency. The input voltage range is 2.7V to 5.5V. The converters provide internal compensation. Power devices are sized for 800mA output current while maintaining over 85% efficiency at full load. Peak efficiency is above 90%. Light load efficiency is maintained at greater than 80% down to 85% of full load current. Soft start limits the current surge seen at the input and eliminates output voltage overshoot.

The input pin, INBUCK (Pin 24) must be connected to the SYSOUT output pin. The Buck1 output voltage is adjustable from 0.6V to 5.5V and is programmed through an external resistor divider. Buck2 output default value is set by external resistor feedback and then the feedback voltage can be dynamically adjusted via I^2C in 12.5mV increments from 0.5V to 0.7V.

For overload conditions, the peak input current is limited. Also, thermal protection completely disables switching if internal dissipation becomes excessive, thus protecting the device from damage. The junction over-temperature threshold is 140°C with 15°C of hysteresis. Under-voltage lockout (UVLO) guarantees sufficient V_{IN} bias and proper operation of all internal circuits prior to activation.

The current through the P-channel MOSFET (high side) is sensed for current loop control, as well as short circuit and overload protection. A fixed slope compensation signal is added to the sensed current to maintain stability for duty cycles greater than 50%. The peak current mode loop appears as a voltage-programmed current source in parallel with the output capacitor. The output of the voltage error amplifier programs the current mode loop for the necessary peak switch current to force a constant output voltage for all load and line conditions. Internal loop compensation terminates the transconductance voltage error amplifier output. The reference voltage is internally set to program the converter output voltage greater than or equal to 0.6V.

For conditions where the input voltage drops to the output voltage level, the converter duty cycle increases to 100%. As the converter approaches the 100% duty cycle, the minimum off-time initially forces the high side on-time to exceed the 1.5MHz clock cycle and reduces the effective switching frequency. Once the input drops below the level where the converter can regulate the output, the high side P-channel MOSFET is enabled continuously for 100% duty cycle. At 100% duty cycle the output voltage tracks the input voltage minus the I*R drop of the high side P-channel MOSFET.

For overload conditions, the peak input current is limited. The bucks use a cycle-by-cycle current limit to protect itself and the load from an external fault condition. Thermal protection completely disables switching when internal dissipation becomes excessive. The junction over-temperature threshold is 140°C with 15°C of hysteresis. Once an over-temperature or over-current fault conditions is removed, the output voltage automatically recovers.

Low-Dropout Regulators

The advanced circuit design of the linear regulators has been specifically optimized for very fast start-up and shutdown timing. These proprietary LDOs are tailored for superior transient response characteristics. These traits are particularly important for applications which require fast power supply timing.

The high-speed turn-on capability is enabled through the implementation of a fast start control circuit, which accelerates the power up behavior of fundamental control and feedback circuits within the LDO regulator. For fast turn-off time response is achieved by an active output pull down circuit, which is enabled when the LDO regulator is placed in the shutdown mode. This active fast shutdown circuit has no adverse effect on normal device operation.

There are two LDO input pins, INLDO (pins 6 and 9), which must be connected to the SYSOUT output pin.The LDO1 output voltage is selectable using pins S1 and S2 as shown in Table 1. LDO2 is fixed at 1.2V, LDO4 is fixed at 2.5V and LDO5 is fixed at 3.3V. LDO3 output default value is 1.2V and then can be dynamically adjusted via I^2C in 25mV increments from 1.0V to 1.4V.

S1	S2	LDO1
0	0	3.0V
0	1	3.3V
1	0	2.8V
1	1	Reserved

Table 1: LDO1 Output Voltages.

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Controlling the System Outputs

The AAT3608 has a specific startup and shutdown conditions depending on its mode of operation.

Shutdown Mode

"Shutdown Mode" is defined as the mode where the entire PMU (Power Management Unit) is shut down. This is a state that normally happens after all power has been disconnected from PWR_IN and BAT. Typically, after power has been applied and the part has been turned on, it will normally never need to be turned off. For GPS applications, the amount of time required for the SOC to start up from shutdown is prohibitively long, so the only time that it will go into Shutdown Mode (from any other mode) is when PWR_IN is disconnected and the BAT is below the Low-Battery comparator threshold.

Normal Mode

"Normal Mode" is defined as the mode where all regulators are active. Once the part is in Normal Mode, it will typically go into Sleep or Deep-Sleep Mode when trying to save current.

SOC Sleep Mode

"Sleep Mode" is an SOC-defined mode which simply means that all regulators are shut down except SYSOUT, Buck1, LDO1, and LDO3. To get into this mode from Normal, the SOC will pull the PWR_EN pin low to turn off LDO2, LDO4, and LDO5. Buck2 can also be controlled by PWR_EN only if the SOC masks PWR_EN through I^{2}C. From a PMU point of view, it is no different from Normal Mode except for the regulators that have been switched off by pulling PWR_EN low.

Deep Sleep Mode

"Deep Sleep Mode" is both an SOC and PMU-defined mode where all regulators have been turned off except for SYSOUT and Buck1. Data is backed up by the SOC and Buck1 stays alive to maintain the memory. LDO4 and LDO5 would be turned off separately by I^{2}C, but the DS_RDY and PWR_DS I^{2}C bits are used to get into and out of Deep Sleep Mode. See the flowchart diagrams for more detail.

PWR_ID Pin

The PWR_ID pin is an input logic pin which determines the current limits and fast charge currents that will be used by PMU. PWR_ID settings are listed in Table 2.

Timing Sequences

The AAT3608 has a specific startup sequence when the device is activated. See the timing diagrams in Figures 2 through 7.

RESET

The $\overline{\text{RESET}}$ pin is an open drain active low output signal for system reset. Connect a pull-up resistor from the $\overline{\text{RESET}}$ pin to SYSOUT pin with a recommended resistance value of 100kΩ. After Buck2 and LDO2 reach their target nominal output voltage, a delay of 200ms exists before $\overline{\text{RESET}}$ goes high; refer to the timing diagram in Figure 2.

PWR_ID Pin	USBSEL Pin	PWR_IN – SYSOUT Switch Current Limit	Battery Fast Charge Current
L	L	100mA (typical)	100mA (typical)
L	H	500mA (typical)	500mA (typical)
H	X	Up to 1.2A (typical)	Set by the resistor at the ISETA pin.

Table 2: PWR_ID Settings.

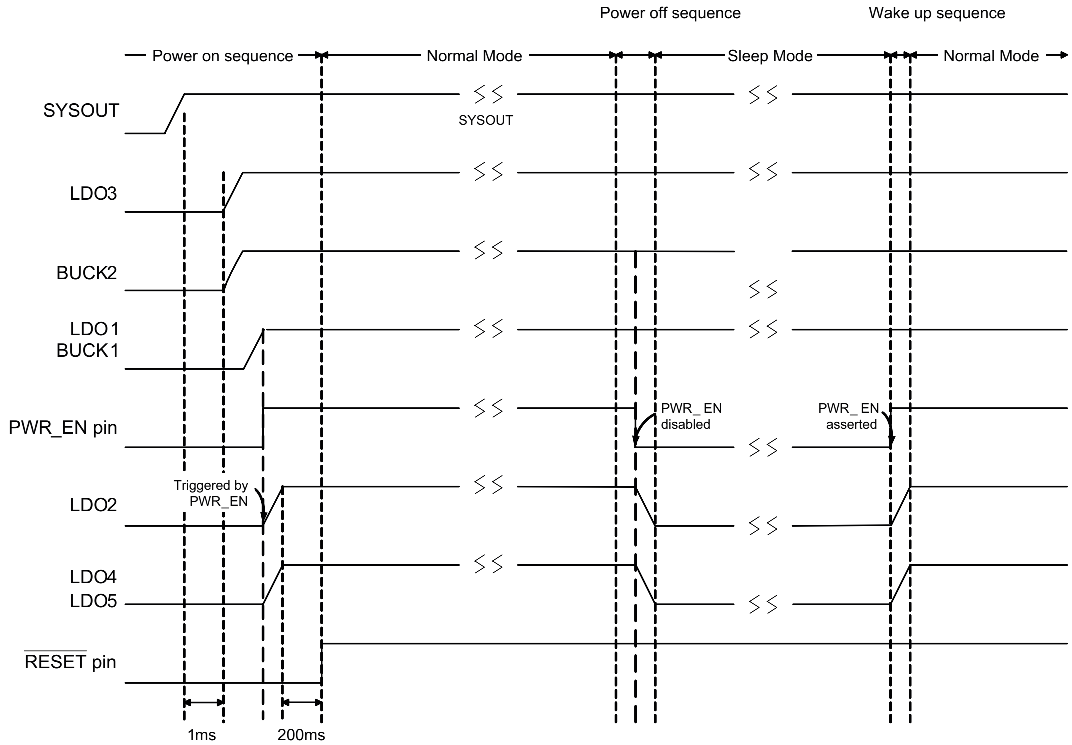


Figure 2: Normal ⇔ Sleep Mode Sequence.

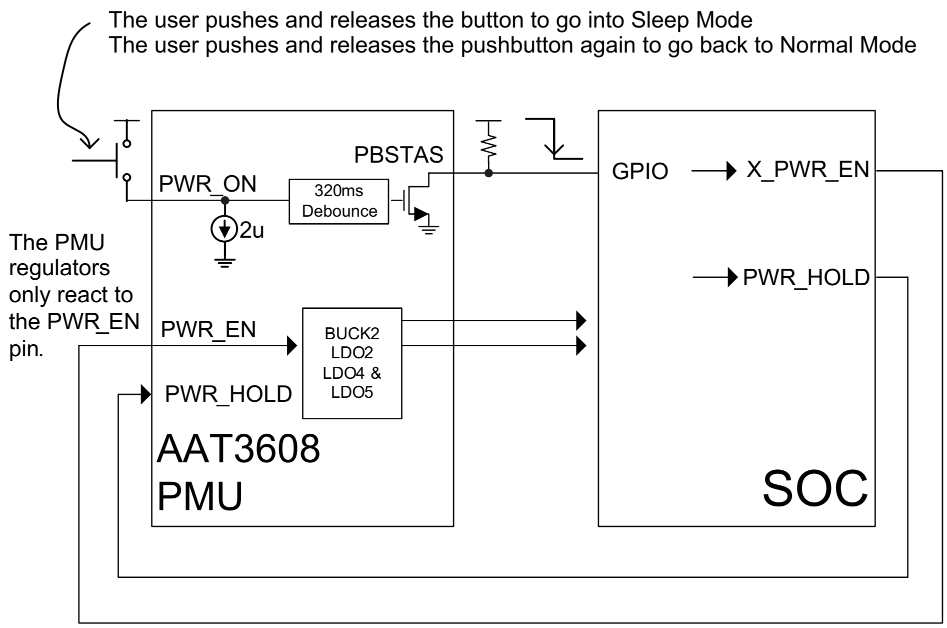


Figure 3: Normal ⇔ Sleep Mode Block Diagram.

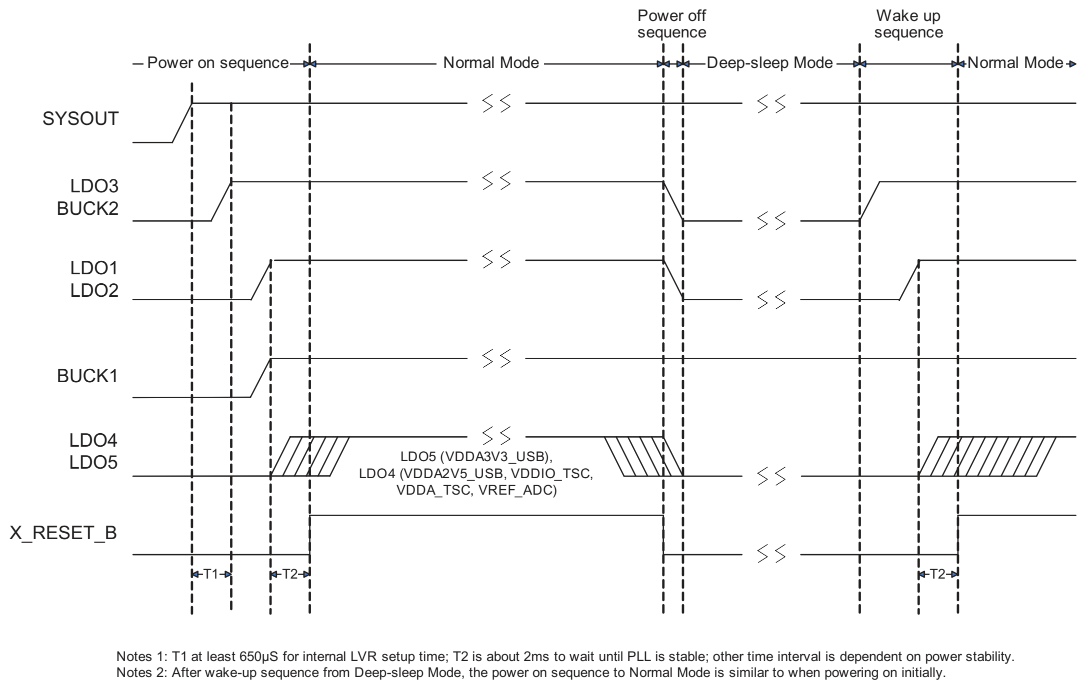


Figure 4: Normal ⇔ Deep-Sleep Mode Sequence.

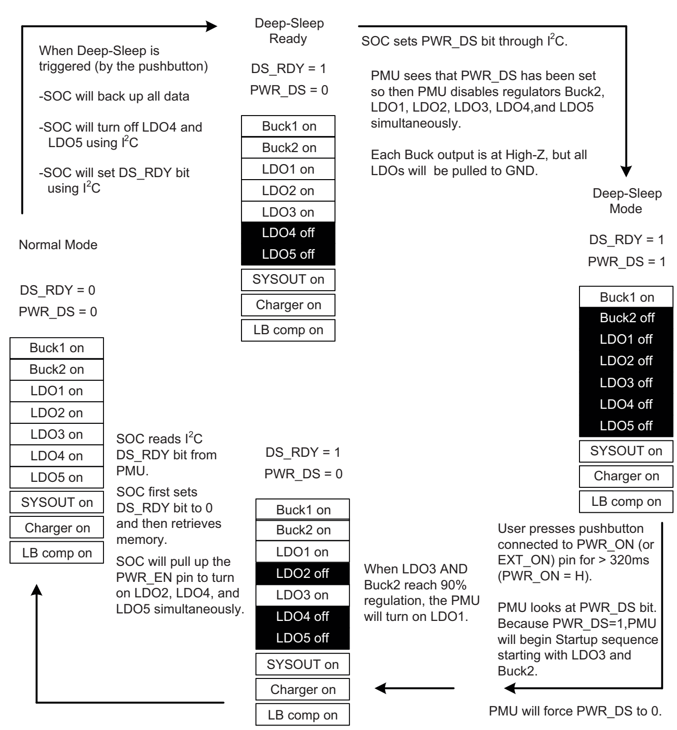


Figure 5: Normal Mode ➔ Deep-Sleep Mode ➔ Normal Mode Flowchart.

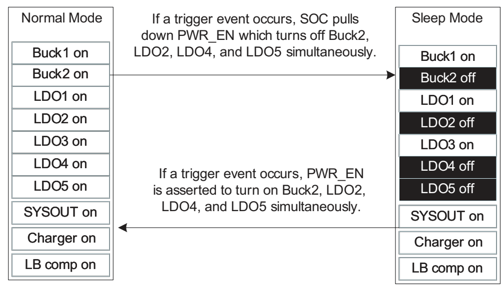


Figure 6: Normal Mode ⬄ Sleep Mode Flowchart.

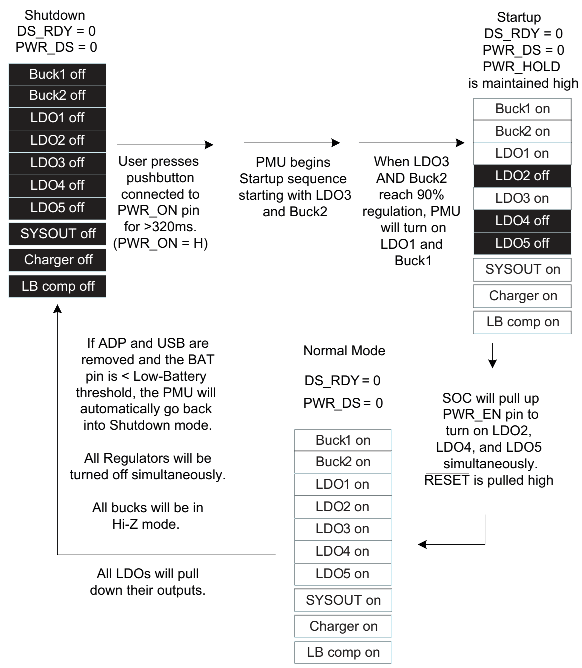


Figure 7: System Shutdown ⬄ Normal Mode (Initial Start-Up) Flowchart.

I^{2}C Serial Interface and Programmability

Serial Interface

Many of the features of the AAT3608 can be controlled via the I^{2}C serial interface. The I^{2}C serial interface is a widely used interface where it requires a master to initiate all the communications with the slave devices. The I^{2}C protocol consists of 2 active wires, SDA (serial data line) and SCL (serial clock line). Both wires are open drain and require an external pull up resistor to V_{CC} (SYSOUT may be used as V_{CC}). The SDA pin serves I/O function, and the SCL pin controls and references the I^{2}C bus. I^{2}C protocol is a bidirectional bus which allows both read and write actions to take place. The timing diagram in Figure 8 depicts the transmission protocol.

START and STOP Conditions

START and STOP conditions are always generated by the master. Prior to initiating a START condition, both the SDA and SCL pin are idle mode (idle mode is when there is no activity on the bus and SDA and SCL are pulled to V_{CC} via external resistor). As depicted in Figure 9, a START condition is defined to be when the master pulls the SDA line low and after a short period pulls the SCL line low. A START condition acts as a signal to all ICs that something is about to be transmitted on the BUS. A STOP condition, also shown in Figure 9, is when the master releases the bus and SCL changes from low to high followed by SDA low to high transition. The master does not issue an ACKNOWLEDGE and releases the SCL and SDA pins.

Transferring Data

Every byte on the bus must be 8 bits long. A byte is always sent with the most significant bit first (see Figure 8).

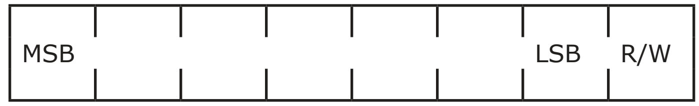


Figure 8: Bit Order.

Acknowledge Bit

The acknowledge bit is the ninth bit of data. It is used to send back a confirmation to the master that the data has been received properly. For acknowledge to take place, the MASTER must first release the SDA line, then the SLAVE will pull the data line low as shown in Figure 9.

The address is embedded in the first seven bits of the byte. The eighth bit is reserved for the direction of the information flow for the next byte of information. For the AAT3608, this bit must be set to "0" when writing and "1" when reading. The full 8-bit address including the R/W bit is 0x9C (hex) or 10011100 in binary for writing and 0x9D(hex) or 10011101 in binary for reading.

I^{2}C Write Code

After sending the chip address, the master should send an 8-bit data stream ("2^{ND} Word"). The "2^{ND} Word" can consist of any one of the four sets of data listed in Table 3.

The "3^{RD} Word" should be entered into the I^{2}C only if (Bit_7,Bit_6,Bit_5) = (0,0,0) in the "2^{ND} Word". In this case, the bits (G2,G1,G0) are used to set the bit assignments as shown in Tables 4 and 5.

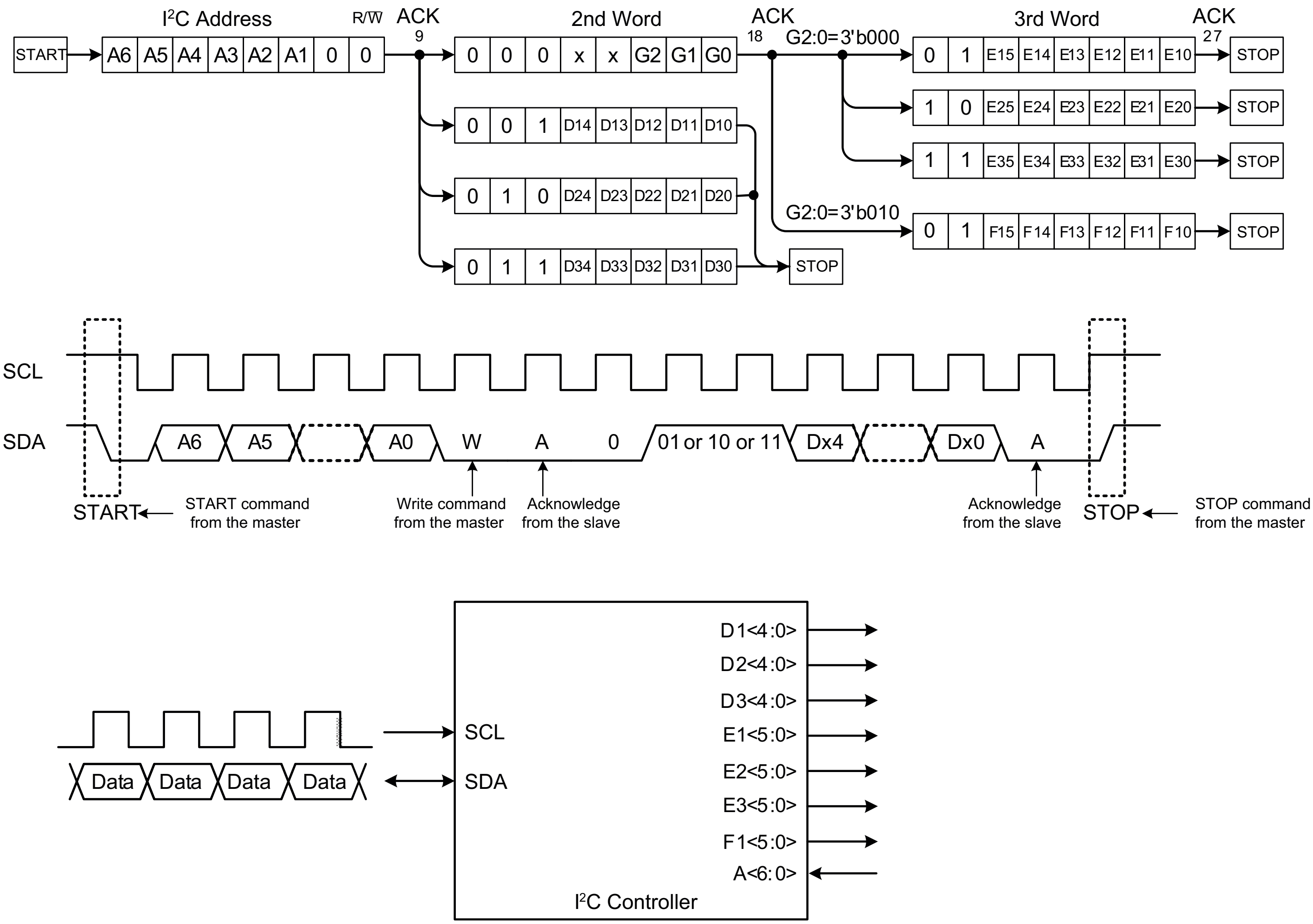


Figure 9: I²C Protocol.

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0	0	0	0	G2	G1	G0
0	0	1	EN_{LDO5}	EN_{LDO4}	DS_RDY	PWR_DS	Reserved
0	1	0	$LDO5_1$	$LDO5_0$	$LDO4_1$	$LDO4_0$	EN_{CHG}
0	1	1	$BUCK2_4$ and $LDO3_4$	$BUCK2_3$ and $LDO3_3$	$BUCK2_2$ and $LDO3_2$	$BUCK2_1$ and $LDO3_1$	$BUCK2_0$ and $LDO3_0$

Table 3: I²C "2nd Word" Bit Assignments.

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	1	EN_{LDO3}	EN_{LDO2}	EN_{LDO1}	EN_{BUCK1}	EN_{BUCK2}	PWR_EN Mask
1	0	PWR_IN IN Mask	PWR_IN OUT Mask	Reserved	LBO Mask	TIME OUT Mask	CHG DONE Mask

Table 4: I²C "3rd Word" Bit Assignments for (G2,G1,G0) = (0,0,0)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	1	Test Modes					

Table 5: I²C "3rd Word" Bit Assignments for (G2,G1,G0) = (0,1,0).

$BUCK2_4$ $LDO3_4$	$BUCK2_3$ $LDO3_3$	$BUCK2_2$ $LDO3_2$	$BUCK2_1$ $LDO3_1$	$BUCK2_0$ $LDO3_0$	LDO3 Output Voltage	BUCK2 FB Voltage
0	0	0	0	0	1.000V	0.5000V
0	0	0	0	1	1.025V	0.5125V
0	0	0	1	0	1.050V	0.5250V
0	0	0	1	1	1.075V	0.5375V
0	0	1	0	0	1.100V	0.5500V
0	0	1	0	1	1.125V	0.5625V
0	0	1	1	0	1.150V	0.5750V
0	0	1	1	1	1.175V	0.5875V
0	1	0	0	0	1.200V (Default)	0.6000V (Default)
0	1	0	0	1	1.225V	0.6125V
0	1	0	1	0	1.250V	0.6250V
0	1	0	1	1	1.275V	0.6375V
0	1	1	0	0	1.300V	0.6500V
0	1	1	0	1	1.325V	0.6625V
0	1	1	1	1	1.350V	0.6750V
0	1	1	1	1	1.375V	0.6875V
1	X	X	X	X	1.400V	0.7000V

Table 6: Buck2 and LDO3 Output Voltage.

$LDO4_1$	$LDO4_0$	LDO4 Output Voltage
0	0	1.8V
0	1	**2.5V (Default)**
1	0	2.85V
1	1	3.3V

Table 7: LDO4 Output Voltage.

$LDO5_1$	$LDO5_0$	LDO5 Output Voltage
0	0	1.2V
0	1	1.5V
1	0	3.0V
1	1	**3.3V (Default)**

Table 8: LDO5 Output Voltage.

EN_{CHG}	Description	DS_RDY	Description
0	Turn off Battery Charger	0	**(Default)**
1	Turn on Battery Charger **(Default)**	1	Deep Sleep Recognition Flag
EN_{BUCK1}	**Description**	**PWR_DS**	**Description**
0	Turn off Buck1	0	**(Default)**
1	Turn on Buck1 **(Default)**	1	Force PMU to go into Deep Sleep Mode
EN_{BUCK2}	**Description**	**PWR_EN Mask**	**Description**
0	Turn OFF Buck2	0	No Masking
1	Turn ON Buck2 **(Default)**	1	Mask the PWR_EN pin ability to control BUCK2 (Default)
EN_{LDO1}	**Description**	**PWR_IN IN Mask**	**Description**
0	Turn OFF LDO1	0	No Masking
1	Turn ON LDO1 **(Default)**	1	Prevent an interrupt from being generated if the PWR_IN IN bit has been asserted (Default)
EN_{LDO2}	**Description**	**PWR_IN OUT Mask**	**Description**
0	Turn OFF LDO2	0	No Masking
1	Turn ON LDO2 only if PWR_EN pin is High **(Default)**	1	Prevent an interrupt from being generated if the PWR_IN OUT bit has been asserted (Default)
EN_{LDO3}	**Description**	**LBO Mask**	**Description**
0	Turn OFF LDO3	0	No Masking
1	Turn ON LDO3 **(Default)**	1	Prevent an interrupt from being generated if the LBO comparator has been asserted (Default)
EN_{LDO4}	**Description**	**TIMEOUT Mask**	**Description**
0	Turn OFF LDO4	0	No Masking
1	Turn ON LDO4 **(Default)**	1	Prevents an interrupt from being generated if the TIMEOUT bit has been asserted (Default)
EN_{LDO5}	**Description**	**CHG_DONE Mask**	**Description**
0	Turn OFF LDO5	0	No Masking
1	Turn ON LDO5 **(Default)**	1	Prevent an interrupt from being generated if the charger has reached End-of-Charge (Default)

Table 9: Enable Settings.

Interrupt (Read from I²C)

A single byte is used when reading I²C data from the AAT3608. The R/W address should be set to 1 so that complete address of the chip would be 0x9D or 10011101 in binary.

The INT (interrupt) pin is an open drain output which pulls low when there is an assertion in any one of the status bits (except the DS_RDY and PWR_DS bits). When a Read from the I²C is initiated AND completed by the SOC, the INT pin is released and the voltage will go high through the external pull-up resistor.

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWR_IN IN	PWR_IN OUT	Reserved	LBO	TIME OUT	CHG_DONE	DS_RDY	PWR_DS

Table 10: I²C Read Table.

PWR_IN IN Bit	Description	Interrupt Signal Produced?
0	Default	Only if PWR_IN IN Mask bit is not set
1	If V_{PWR_IN} > UVLO threshold, this bit will be set	
PWR_IN OUT Bit	**Description**	**Interrupt Signal Produced?**
0	Default	Only if PWR_IN OUT Mask bit is not set
1	If V_{PWR_IN} < UVLO threshold, this bit will be set	
TIMEOUT Bit	**Description**	**Interrupt Signal Produced?**
0	Default	Only if TIMEOUT Mask bit is not set
1	If the charger watchdog timer has reached Timeout, this bit will be set.	
LBO Bit	**Description**	**Interrupt Signal Produced?**
0	Default	Only if LBO Mask bit is not set
1	If Low-Battery comparator is tripped then this bit will be set.	
CHG DONE Bit	**Description**	**Interrupt Signal Produced?**
0	Default	Only if CHG_DONE Mask bit is not set
1	If the Charger has reached End-Of-Charge (EOC), this bit will be set	
DS_RDY Bit	**Description**	**Interrupt Signal Produced?**
0	Default	No INT signal
1	Same as the DS_RDY bit described in the "I^{2}C Write" section of this datasheet	
PWR_DS Bit	**Description**	**Interrupt Signal Produced?**
0	Default	No INT signal
1	Same as the PWR_DS bit described in the "I^{2}C Write" section of this datasheet	

Table 11: Status Bit Descriptions.

Application Information

The two bucks are high performance 800mA 1.5MHz monolithic step-down converters. They have been designed with the goal of minimizing external component size and optimizing efficiency over the complete load range. Apart from the small bypass input capacitor, only a small L-C filter is required at the output.

Both bucks can be programmed with external feedback resistors to any voltage, ranging from 0.6V to the input voltage in default feedback voltage condition.

At dropout, the step down converters duty cycle increases to 100% and the output voltage tracks the input voltage minus the R_{DSON} drop of the P-channel high-side MOSFET.

Output Voltage Resistor Selection

Resistors R2 through R5 in Figure 10 program the output to regulate at a voltage higher than 0.6V in default mode. The feedback voltage of Buck2 can have a wider range and can be adjusted down to 0.5V through I^2C. To limit the bias current required for the external feedback resistor string while maintaining good noise immunity, a suggested value for R3 and R5 is 59kΩ to provide a bias current of 10uA with a feedback voltage of 0.6V. Although a larger value will further reduce quiescent current, it will also increase the impedance of the feedback node, making it more sensitive to external noise and interference. Table 12 summarizes the resistor values for various output voltages with R3 and R5 set to either 59kΩ for good noise immunity or 100kΩ for reduced no load input current.

V_{OUT} (V)	R3 and R5 = 59kΩ R2 and R4 (kΩ)	R3 and R5 = 100kΩ R2 and R4 (kΩ)
0.8	19.6	33.2
0.9	29.4	49.9
1	39.2	66.5
1.1	49.9	82.5
1.2	59	100
1.3	68.1	118
1.4	78.7	133
1.5	88.7	150
1.8	118	200
1.85	124	210
2	137	232
2.5	187	316
3.3	267	453

Table 12: Feedback Resistors (Feedback Voltage = 0.6V).

Input Capacitor (Bucks)

All input capacitors should be located as physically close to the power pin (INBUCK) and power ground pins (PGND1 and 2). Ceramic capacitors are recommended for their higher current operation and small profile. Also, ceramic capacitors are inherently capable to withstand input current surges from low impedance sources such as batteries in portable devices over tantalum capacitors. Typically, 10V or 16V rated capacitors are required.

The following are the typical recommended capacitance values:

Two 10μF capacitors for INBUCK
One 10μF capacitor for INLDO
One 10μF capacitor for SYSOUT
One 10μF capacitor for PWR_IN
One 10μF capacitor for BAT

Output Capacitor (Bucks)

For proper load voltage regulation and operational stability, a capacitor is required on the output of each buck. The output capacitor connection to the ground pin should be made as directly as practically possible for maximum device performance. Since the bucks have been designed to function with very low ESR capacitors, a 4.7μF ceramic capacitor is recommended for best performance.

Inductor Selection

The two bucks use peak current mode control with slope compensation to maintain stability for duty cycles greater than 50%. The output inductor value must be selected so the inductor current down slope meets the internal slope compensation requirements. The internal slope compensation is 1A/μs. The inductor should be set equal to the output voltage numeric value in micro henries (μH). This guarantees that there is sufficient internal slope compensation.

Inductor manufacturer's specifications list both the inductor DC current rating, which is a thermal limitation, and the peak current rating, which is determined by the saturation characteristics. The inductor should not show any appreciable saturation under normal load conditions. Some inductors may meet the peak and average current ratings yet result in excessive losses due to a high DCR. Always consider the losses associated with the DCR and its effect on the total converter efficiency when selecting an inductor.

Input Capacitor (LDOs)

Typically, a 10μF or larger capacitor, C4 (see Figure 10), is recommended as close as possible to the device INLDO pin. The input capacitor value of 10μF will offer superior input line transient response and will assist in maximizing the highest possible power supply ripple rejection.

There is no specific capacitor ESR requirement; therefore ceramic, tantalum, or aluminum electrolytic capacitors may be selected for capacitor C4. However, ceramic capacitors are recommended due to their inherent capability over tantalum capacitors to withstand input current surges from low impedance sources such as batteries in portable devices.

Output Capacitor (LDOs)

For proper load voltage regulation and operational stability, a 4.7μF ceramic capacitor is required between the output of the LDOs and GND. If desired, the output capacitor may be increased without limit. The output capacitor connection to the LDO regulator ground pin should be made as direct as practically possible for maximum device performance.

Although the device is intended to operate with low ESR capacitors, it is stable over a very wide range of capacitor ESR, thus it will also work with higher ESR tantalum or aluminum electrolytic capacitors. However, for best performance, ceramic capacitors are recommended.

Layout Guidance

Figure 10 is the schematic for the evaluation board. The evaluation board has extra components for easy evaluation; the bill of materials for the system is shown in Table 12. When laying out the PC board, the following layout guidelines should be followed to ensure proper operation of the AAT3608:

1. The exposed pad (EP) must be reliably soldered to exposed copper pad on the board and electrically connected to GND/PGND pins.
2. The power traces, including GND traces, the LX traces and the VIN trace should be kept short, direct and wide to allow large current flow. Use several via pads when routing between layers.
3. The input capacitors should be connected as close as possible from SYSOUT and INBUCK to PGND1 and PGND2 to get good power filtering.
4. Keep the switching node LX away from the sensitive buck feedback nodes, FB1 and FB2.
5. The feedback trace for the bucks should be separate from any power trace and connected as closely as possible to the load point. Sensing along a high current load trace will degrade DC load regulation.
6. The output capacitors and inductors should be connected as close as possible and there should not be any signal lines under the inductor.
7. The resistance of the trace from the load return to PGND1 and PGND2 should be kept to a minimum. This will help to minimize any error in DC regulation due to differences in the potential of the internal signal ground and the power ground.

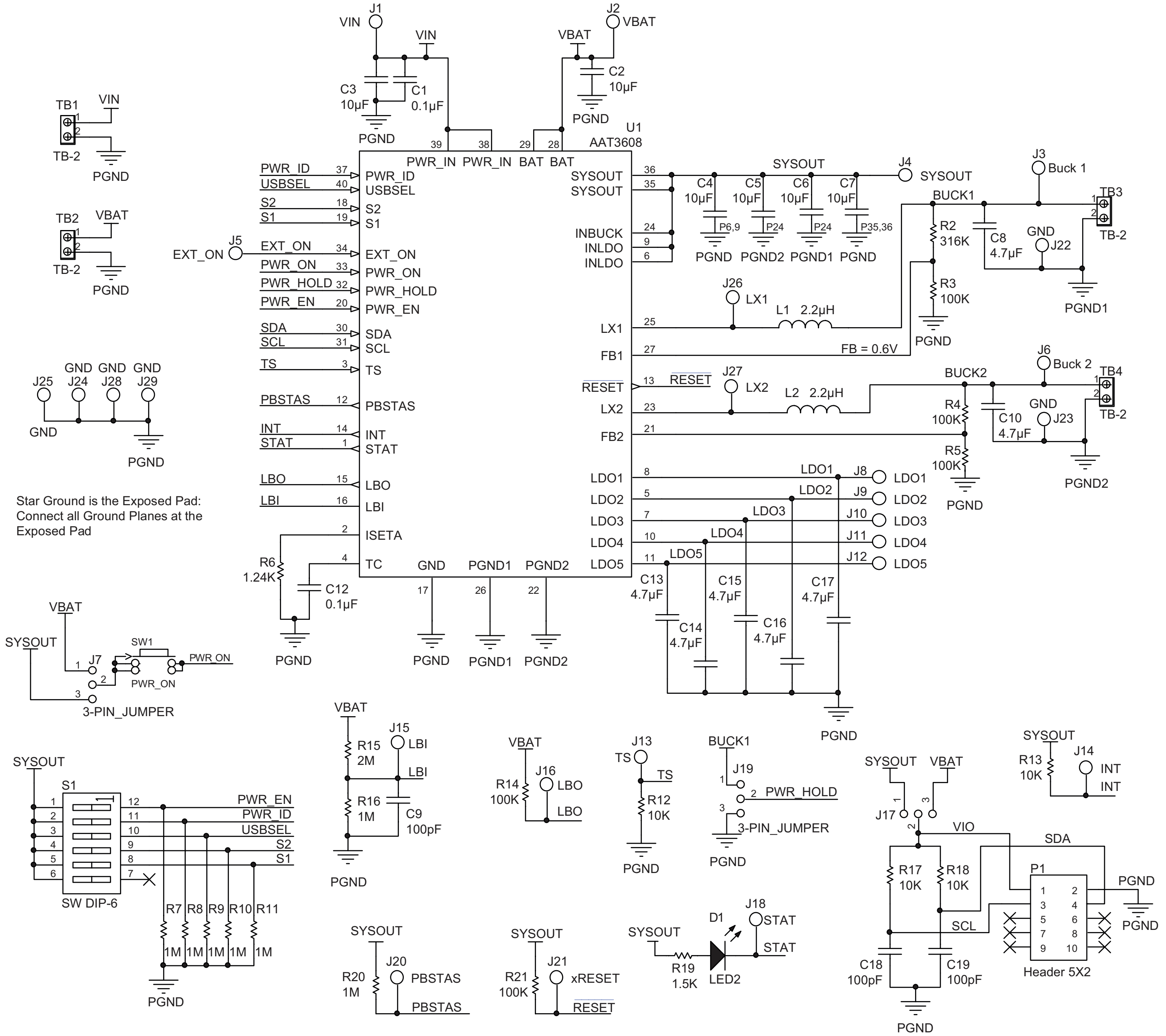


Figure 10: AAT3608 Evaluation Board Schematic.

Compact Seven-Channel Regulator with Li+/Polymer Linear Battery Charger and I2C Interface

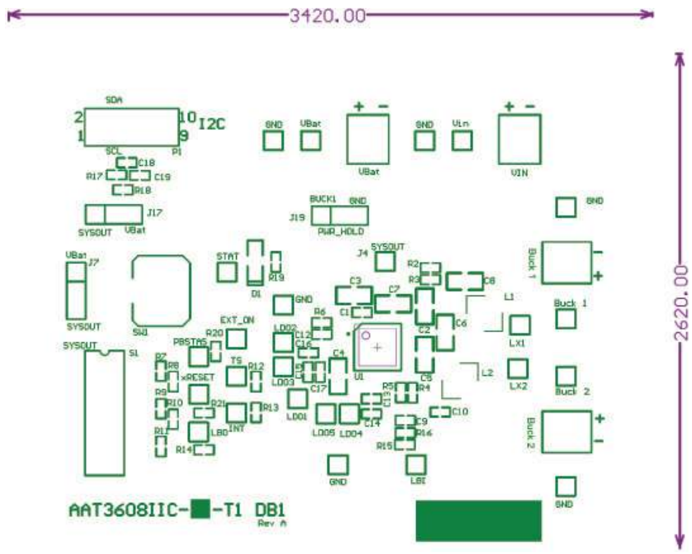


Figure 11: AAT3608 Evaluation Board Silk Screen Layer.

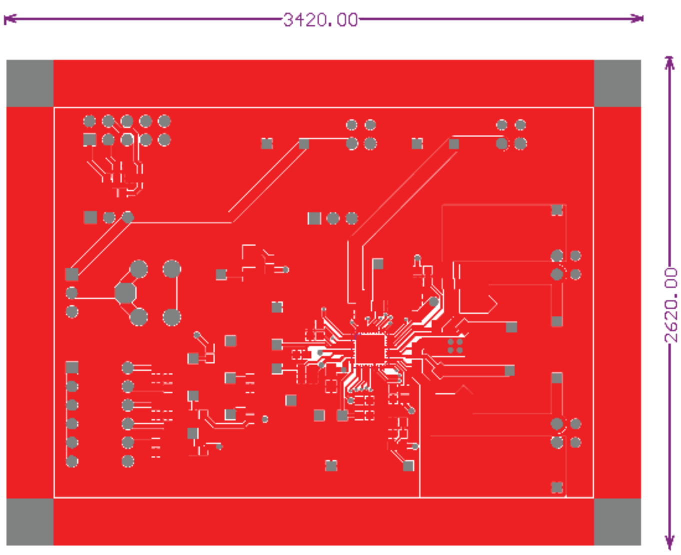


Figure 12: AAT3608 Evaluation Board Top Layer.

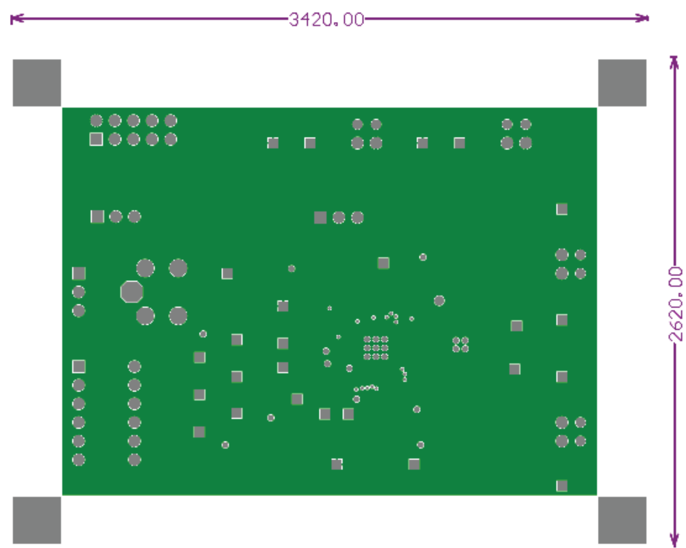


Figure 13: AAT3608 Evaluation Board Mid Layer 1 (GND Plane).

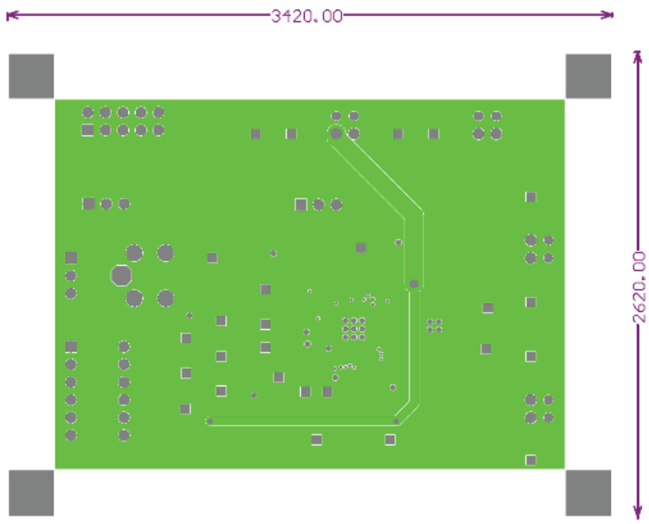


Figure 14: AAT3608 Evaluation Board Mid Layer 2 (SYSOUT).

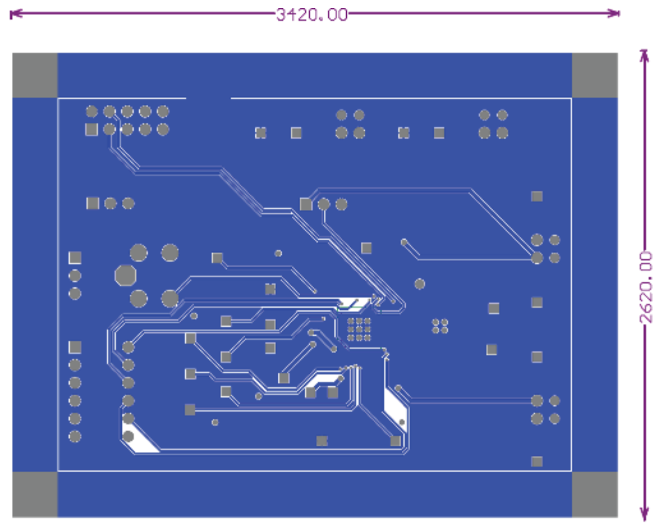


Figure 15: AAT3608 Evaluation Board Bottom Layer.

	Description	Value	Quantity	Footprint
U1	Battery Charger PMU		1	TQFN55-40L
J1, J2, J3, J4, J5, J6, J8, J9, J10, J11, J12, 13, J14,J15, J16, J18, J20, J21, J22, J23, J24, J25, J26, J27, J28, J29	Test Point		26	TP
TB1, TB2, TB3, TB4	Terminal Block Connector 2 Positions - DigiKey 277-1273-ND		4	TBLOK2
SW1	Switch Tact, SPST, 5mm - C&K Components PTS645TL50 LFS		1	SW-2
P1	Header, 5-Pin, Dual row		1	HDR2X5
J7, J17, J19	1X3 Header		3	HDR1X3
S1	DIP Switch, 6 Position, SPST		1	DIP-12/SW
L1, L2	Inductor	2.2μH	2	CDRH4D16
D1	Typical red, green, yellow, amber GaAs LED		1	1206LED - duplicate
C2, C3, C4, C5,C6,C7	Ceramic Capacitor	10μF	6	0805
C8	Ceramic Capacitor	4.7μF	1	0805
C1, C12	Ceramic Capacitor	0.1μF	2	0603
C10, C13, C14, C15, C16, C17	Ceramic Capacitor	4.7μF	6	0603
C9, C18, C19	Ceramic Capacitor	100pF	3	0603
R12, R13, R17, R18	Resistor	10K	4	0603
R15	Resistor	2M	1	0603
R19	Resistor	1.5K	1	0603
R2	Resistor	316K	1	0603
R3, R4, R5, R14, R21	Resistor	100K	5	0603
R6	Resistor	1.24K	1	0603
R7, R8, R9, R10, R11, R16, R20	Resistor	1M	7	0603

Table 12: AAT3608 Evaluation Board Bill of Materials (BOM).

Compact Seven-Channel Regulator with Li+/Polymer Linear Battery Charger and I2C Interface

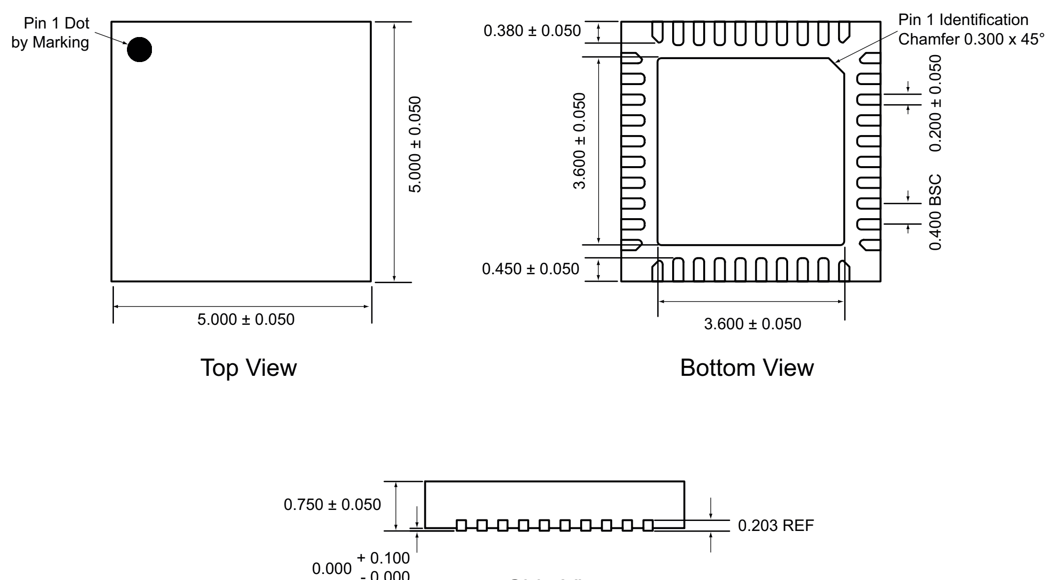
Ordering Information

Package	Marking[1]	Part Number (Tape and Reel)[2, 3]
TQFN55-40	C8XYY	AAT3608IIC-1-T1

Skyworks Green™ products are compliant with all applicable legislation and are halogen-free. For additional information, refer to *Skyworks Definition of Green™*, document number SQ04-0074.

Package Information

TQFN55-40[4]



Top View

Bottom View

Side View

All dimensions in millimeters.

1. XYY = assembly and date code.
2. Sample stock is generally held on part numbers listed in **BOLD**.
3. Available exclusively outside of the United States and its territories.
4. The leadless package family, which includes QFN, TQFN, DFN, TDFN and STDFN, has exposed copper (unplated) at the end of the lead terminals due to the manufacturing process. A solder fillet at the exposed copper edge cannot be guaranteed and is not required to ensure a proper bottom solder connection.