19-2999; Rev 0; 10/03

EVALUATION KIT AVAILABLE

Dual, 10-Bit, 300Msps, DAC with 4x/2x/1x Interpolation Filters and PLL

General Description

The MAX5858A dual, 10-bit, 300Msps digital-to-analog converter (DAC) provides superior dynamic performance in wideband communication systems. The MAX5858A integrates two 10-bit DAC cores, 4x/2x/1x programmable digital interpolation filters, phase-lock loop (PLL) clock multiplier, and a 1.24V reference. The MAX5858A supports single-ended and differential modes of operation. The MAX5858A dynamic performance is maintained over the entire power-supply operating range of 2.7V to 3.3V. The analog outputs support a compliance voltage of -1.0V to +1.25V.

The 4x/2x/1x programmable interpolation filters feature excellent passband distortion and noise performance. Interpolating filters minimize the design complexity of analog reconstruction filters while lowering the data bus and the clock speeds of the digital interface. The PLL multiplier generates all internal, synchronized high-speed clock signals for interpolating filter operation and DAC core conversion. The internal PLL helps minimize system complexity and lower cost. To reduce the I/O pin count, the DAC can also operate in interleave data mode. This allows the MAX5858A to be updated on a single 10-bit bus.

The MAX5858A features digital control of channel gain matching to within ±0.4dB in sixteen 0.05dB steps. Channel matching improves sideband suppression in analog quadrature modulation applications. The on-chip 1.24V bandgap reference includes a control amplifier that allows external full-scale adjustments of both channels through a single resistor. The internal reference can be disabled and an external reference can be applied for high-accuracy applications.

The MAX5858A features full-scale current outputs of 2mA to 20mA and operates from a 2.7V to 3.3V single supply. The DAC supports three modes of power-control operation: normal, low-power standby, and complete power-down. In power-down mode, the operating current is reduced to 1µA.

The MAX5858A is packaged in a 48-pin TQFP with exposed paddle (EP) for enhanced thermal dissipation and is specified for the extended (-40°C to +85°C) operating temperature range.

Applications

Communications
SatCom, LMDS, MMDS, HFC, DSL, WLAN, Point-to-Point Microwave Links

Wireless Base Stations

Direct Digital Synthesis

Instrumentation/ATE

Features

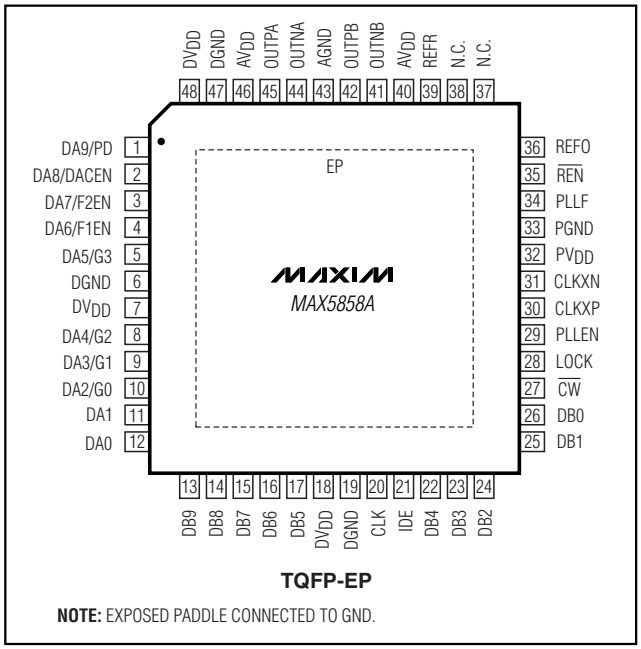
- **10-Bit Resolution, Dual DAC**
- **300Msps Update Rate**
- **Integrated 4x/2x/1x Interpolating Filters**
- **Internal PLL Multiplier**
- **2.7V to 3.3V Single Supply**
- **Full Output Swing and Dynamic Performance at 2.7V Supply**
- **Superior Dynamic Performance**
  73dBc SFDR at f_{OUT} = 20MHz
  UMTS ACLR = 63dB at f_{OUT} = 30.7MHz
- **Programmable Channel Gain Matching**
- **Integrated 1.24V Low-Noise Bandgap Reference**
- **Single-Resistor Gain Control**
- **Interleave Data Mode**
- **Differential Clock Input Modes**
- **EV Kit Available—MAX5858AEVKit**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX5858AECM	-40°C to +85°C	48 TQFP-EP*

**EP = Exposed paddle.*

Pin Configuration



TQFP-EP

NOTE: EXPOSED PADDLE CONNECTED TO GND.

Dual, 10-Bit, 300Msps, DAC with 4x/2x/1x Interpolation Filters and PLL

ABSOLUTE MAXIMUM RATINGS

AV_{DD}, DV_{DD}, PV_{DD} to AGND, DGND, PGND .....-0.3V to +4V
DA9–DA0, DB9–DB0, $\overline{CW}$, $\overline{REN}$, PLLF, PLLEN to AGND, DGND, PGND.....-0.3V to +4V
IDE to AGND, DGND, PGND.....-0.3V to (DV_{DD} + 0.3V)
CLKXN, CLKXP to PGND .....-0.3V to +4V
OUTP_, OUTN_ to AGND.....-1.25V to (AV_{DD} + 0.3V)
CLK, LOCK to DGND.....-0.3V to (DV_{DD} + 0.3V)
REFR, REFO to AGND .....-0.3V to (AV_{DD} + 0.3V)
AGND to DGND, DGND to PGND, AGND to PGND.....-0.3V to +0.3V
Maximum Current into Any Pin (excluding power supplies) .....±50mA
Continuous Power Dissipation (T_A = +70°C)
48-Pin TQFP-EP (derate 36.2mW/°C above +70°C) 2.899W
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Junction Temperature.....+150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(AV_{DD} = DV_{DD} = PV_{DD} = 3V, AGND = DGND = PGND = 0, f_{DAC} = 165Msps, no interpolation, PLL disabled, external reference, V_{REFO} = 1.2V, I_{FS} = 20mA, output amplitude = 0dB FS, differential output, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. T_A > +25°C guaranteed by production test. T_A < +25°C guaranteed by design and characterization. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STATIC PERFORMANCE							
Resolution				10			Bits
Integral Nonlinearity	INL	R_L = 0		-1.25	±0.5	+1.25	LSB
Differential Nonlinearity	DNL	Guaranteed monotonic, R_L = 0		-0.75	±0.25	+0.75	LSB
Offset Error	V_{OS}			-0.5	±0.1	+0.5	LSB
Gain Error (See *Gain Error Parameter Definitions* Section)	GE	Internal reference (Note 1)		-10	±1.6	+11	%
		External reference		-8	±1.2	+8	
DYNAMIC PERFORMANCE							
Maximum DAC Update Rate	f_{DAC}	4x/2x interpolation modes		300			Msps
Glitch Impulse					5		pV-s
Spurious-Free Dynamic Range to Input Update Rate Nyquist	SFDR	f_{DAC} = 165Msps	f_{OUT} = 5MHz, T_A ≥ +25°C	68	76		dBc
			f_{OUT} = 20MHz		73		
			f_{OUT} = 50MHz		66		
			f_{OUT} = 70MHz		65		
		f_{DAC} = 300Msps, 2x interpolation	f_{OUT} = 5MHz		76		
			f_{OUT} = 40MHz		73		
			f_{OUT} = 60MHz		72		
Spurious-Free Dynamic Range Within a Window	SFDR	f_{DAC} = 200Msps, 2x interpolation, f_{OUT} = 40MHz, span = 20MHz			85		dBc
		f_{DAC} = 165Msps, f_{OUT} = 5MHz, span = 4MHz		76.5	85		
Multitone Power Ratio, 8 Tones, ~300kHz Spacing	MTPR	f_{DAC} = 165Msps, f_{OUT} = 20MHz			76		dBc
Adjacent Channel Leakage Ratio with UMTS	ACLR	f_{DAC} =122.88Msps, f_{OUT} = 30.72MHz			63		dB

ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = DV_{DD} = PV_{DD} = 3V, AGND = DGND = PGND = 0, f_{DAC} = 165Msps, no interpolation, PLL disabled, external reference, V_{REFO} = 1.2V, I_{FS} = 20mA, output amplitude = 0dB FS, differential output, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. T_A > +25°C guaranteed by production test. T_A < +25°C guaranteed by design and characterization. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Total Harmonic Distortion to Nyquist	THD	f_{DAC} = 165Msps, f_{OUT} = 5MHz		-72		dBc
Noise Spectral Density	n_D	f_{DAC} = 165Msps, f_{OUT} = 5MHz		-143		dBm/Hz
Output Channel-to-Channel Isolation		f_{OUT} = 5MHz		80		dB
Gain Mismatch Between Channels		f_{OUT} = 5MHz		±0.05		dB
Phase Mismatch Between Channels		f_{OUT} = 5MHz		±0.15		Degrees
Wideband Output Noise				50		pA/√Hz
ANALOG OUTPUT						
Full-Scale Output Current Range	I_{FS}		2		20	mA
Output Voltage Compliance Range			-1.0		+1.25	V
Output Leakage Current		Power-down or standby mode	-5		+5	µA
REFERENCE						
Reference Output Voltage	V_{REF0}	$\overline{REN}$ = AGND	1.14	1.24	1.34	V
Output-Voltage Temperature Drift	TCV_{REF}			±50		ppm/°C
Reference Output Drive Capability				50		µA
Reference Input Voltage Range		$\overline{REN}$ = AV_{DD}	0.10		1.32	V
Reference Supply Rejection				0.2		mV/V
Current Gain	I_{FS}/I_{REF}			32		mA/mA
INTERPOLATION FILTER (2x interpolation)						
Passband Width	f_{OUT}/ $0.5f_{DAC}$	-0.005dB		0.398		MHz/ MHz
		-0.01dB		0.402		
		-0.1dB		0.419		
		-3dB		0.478		
Stopband Rejection		$0.604f_{DAC}$ / 2 to $1.396f_{DAC}$ / 2		74		dB
		$0.600f_{DAC}$ / 2 to $1.400f_{DAC}$ / 2		62		
		$0.594f_{DAC}$ / 2 to $1.406f_{DAC}$ / 2		53		
		$0.532f_{DAC}$ / 2 to $1.468f_{DAC}$ / 2		14		
Group Delay				18		Data clock cycles
Impulse Response Duration				22		Data clock cycles

Dual, 10-Bit, 300Msps, DAC with 4x/2x/1x Interpolation Filters and PLL

ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = DV_{DD} = PV_{DD} = 3V, AGND = DGND = PGND = 0, f_{DAC} = 165Msps, no interpolation, PLL disabled, external reference, V_{REFO} = 1.2V, I_{FS} = 20mA, output amplitude = 0dB FS, differential output, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. T_A > +25°C guaranteed by production test. T_A < +25°C guaranteed by design and characterization. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
INTERPOLATION FILTER (4x interpolation)							
Passband Width	f_{OUT}/ $0.5f_{DAC}$	-0.005dB			0.200		MHz/ MHz
		-0.01dB			0.201		
		-0.1dB			0.210		
		-3dB			0.239		
Stopband Rejection		$0.302f_{DAC}$ / 2 to $1.698f_{DAC}$ / 2			74		dB
		$0.300f_{DAC}$ / 2 to $1.700f_{DAC}$ / 2			63		
		$0.297f_{DAC}$ / 2 to 1.703 f_{DAC} / 2			53		
		$0.266f_{DAC}$ / 2 to $1.734f_{DAC}$ / 2			14		
Group Delay					22		Data clock cycles
Impulse Response Duration					27		Data clock cycles
LOGIC INPUTS (IDE, $\overline{CW}$, $\overline{REN}$, DA9–DA0, DB9–DB0, PLLEN)							
Digital Input-Voltage High	V_{IH}			2			V
Digital Input-Voltage Low	V_{IL}					0.8	V
Digital Input-Current High	I_H	V_{IH} = 2V		-1		+1	µA
Digital Input-Current Low	I_{IL}	V_{IL} = 0.8V		-1		+1	µA
Digital Input Capacitance	C_{IN}				3		pF
DIGITAL OUTPUTS (CLK, LOCK)							
Digital Output-Voltage High	V_{OH}	I_{SOURCE} = 0.5mA, Figure 1		0.9 × DV_{DD}			V
Digital Output-Voltage Low	V_{OL}	I_{SINK} = 0.5mA, Figure 1				0.1 × DV_{DD}	V
DIFFERENTIAL CLOCK INPUT (CLKXP, CLKXN)							
Clock Input Internal Bias					PV_{DD}/2		V
Differential Clock Input Swing				0.5			V_{P-P}
Clock Input Impedance		Single-ended clock drive			5		kΩ
TIMING CHARACTERISTICS							
Input Data Rate	f_{DATA}	No interpolation				165	Msps
		2x interpolation	PLL disabled			150	
			PLL enabled	75		150	
		4x interpolation	PLL disabled			75	
			PLL enabled	37.5		75	
Clock Frequency at CLK Input	f_{CLK}	No interpolation, PLL enabled				165	MHz
		2x interpolation, PLL enabled		75		150	
		4x interpolation, PLL enabled		37.5		75	

ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = DV_{DD} = PV_{DD} = 3V, AGND = DGND = PGND = 0, f_{DAC} = 165Msps, no interpolation, PLL disabled, external reference, V_{REFO} = 1.2V, I_{FS} = 20mA, output amplitude = 0dB FS, differential output, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. T_A > +25°C guaranteed by production test. T_A < +25°C guaranteed by design and characterization. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Settling Time	t_S	To ±0.1% error band (Note 2)		11		ns
Output Rise Time		10% to 90% (Note 2)		2.5		ns
Output Fall Time		90% to 10% (Note 2)		2.5		ns
Data-to-CLK Rise Setup Time (Note 3)	t_{DCSR}	PLL disabled	1.5			ns
		PLL enabled	2.2			
Data-to-CLK Rise Hold Time (Note 3)	t_{DCHR}	PLL disabled	0.4			ns
		PLL enabled	1.4			
Data-to-CLK Fall Setup Time (Note 3)	t_{DCSF}	PLL disabled	1.8			ns
		PLL enabled	2.4			
Data-to-CLK Fall Hold Time (Note 3)	t_{DCHF}	PLL disabled	1.2			ns
		PLL enabled	1.3			
Control Word to $\overline{CW}$ Fall Setup Time	t_{CWS}		2.5			ns
Control Word to $\overline{CW}$ Fall Hold Time	t_{CWH}		2.5			ns
$\overline{CW}$ High Time			5			ns
$\overline{CW}$ Low Time			5			ns
DACEN Rise-to-V_{OUT} Stable	t_{STB}			0.7		µs
PD Fall-to-V_{OUT} Stable	t_{PDSTB}	External reference		0.5		ms
Clock Frequency at CLKXP/CLKXN Input	$f_{CLKDIFF}$	Differential clock, PLL disabled			300	MHz
CLKXP/CLKXN Differential Clock Input to CLK Output Delay	t_{CXD}	PLL disabled		4.6		ns
Minimum CLKXP/CLKXN Clock High Time	t_{CXH}			1.5		ns
Minimum CLKXP/CLKXN Clock Low Time	t_{CXL}			1.5		ns
POWER REQUIREMENTS						
Analog Power-Supply Voltage	AV_{DD}		2.7		3.3	V
Analog Supply Current	I_{AVDD}	(Note 4)		45	49	mA
Digital Power-Supply Voltage	DV_{DD}		2.7		3.3	V

Dual, 10-Bit, 300Msps, DAC with 4x/2x/1x Interpolation Filters and PLL

ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = DV_{DD} = PV_{DD} = 3V, AGND = DGND = PGND = 0, f_{DAC} = 165Msps, no interpolation, PLL disabled, external reference, V_{REFO} = 1.2V, I_{FS} = 20mA, output amplitude = 0dB FS, differential output, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. T_A > +25°C guaranteed by production test. T_A < +25°C guaranteed by design and characterization. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Digital Supply Current (Note 4)	I_{DVDD}	f_{DAC} = 60Msps	No interpolation		34		mA
			2x interpolation		75		
			4x interpolation		72		
		f_{DAC} = 165Msps	No interpolation		54	61	
			2x interpolation		146		
			4x interpolation		140		
		f_{DAC} = 200Msps	2x interpolation		172	186	
			4x interpolation		165	178	
PLL Power-Supply Voltage	PV_{DD}			2.7		3.3	V
PLL Supply Current (Note 4)	I_{PVDD}	f_{DAC} = 60Msps			17		mA
		f_{DAC} = 165Msps			46	52	
		f_{DAC} = 200Msps, 2x interpolation or 4x interpolation			55	61	
Standby Current	$I_{STANDBY}$	(Note 5)			4.4	4.8	mA
Power-Down Current	I_{PD}	(Note 5)			1		µA
Total Power Dissipation (Note 4)	P_{TOT}	f_{DAC} = 60Msps	No interpolation		324		mW
			2x interpolation		487		
			4x interpolation		498		
		f_{DAC} = 165Msps	No interpolation		438	486	
			2x interpolation		735		
			4x interpolation		721		
		f_{DAC} = 200Msps	2x interpolation		816		
			4x interpolation		795		

Note 1: Including the internal reference voltage tolerance.
Note 2: Measured single ended with 50Ω load and complementary output connected to ground.
Note 3: Guaranteed by design, not production tested.
Note 4: Tested with an output frequency of f_{OUT} = 5MHz.
Note 5: All digital inputs at 0 or DV_{DD}. Clock signal disabled.

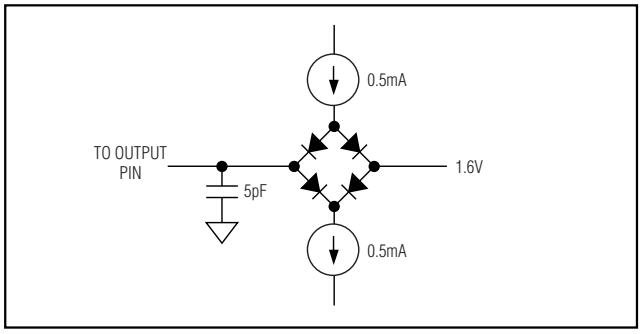
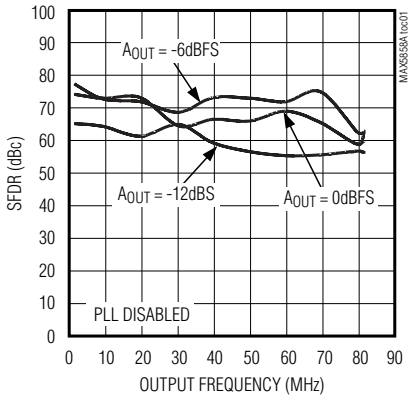


Figure 1. Load Test Circuit for CLK Outputs

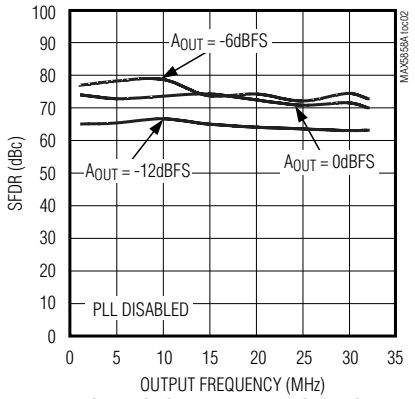
Typical Operating Characteristics

(AV_{DD} = DV_{DD} = PV_{DD} = 3V, AGND = DGND = PGND = 0, external reference = 1.2V, no interpolation, PLL disabled, I_{FS} = 20mA, differential output, T_A = +25°C, unless otherwise noted.)

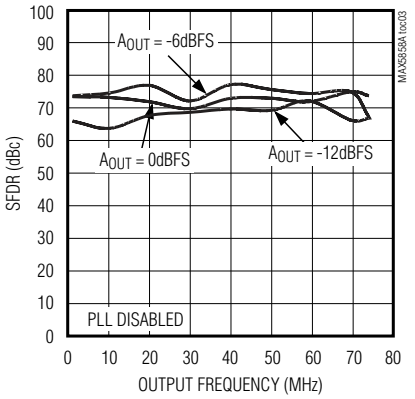
SPURIOUS-FREE DYNAMIC RANGE vs. OUTPUT FREQUENCY (NO INTERPOLATION, f_{DAC} = 165MHz)



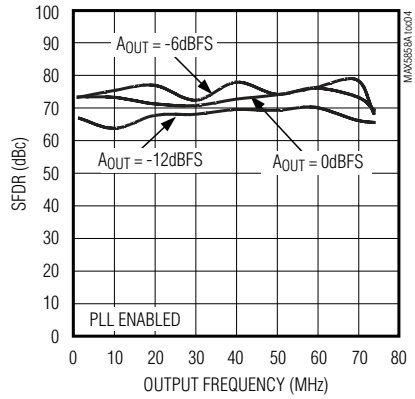
SPURIOUS-FREE DYNAMIC RANGE vs. OUTPUT FREQUENCY (NO INTERPOLATION, f_{DAC} = 65MHz)



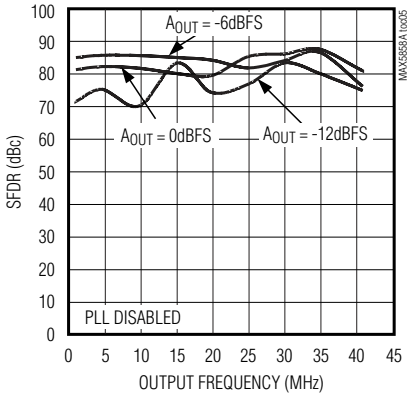
SPURIOUS-FREE DYNAMIC RANGE vs. OUTPUT FREQUENCY (2x INTERPOLATION, f_{DAC} = 300MHz)



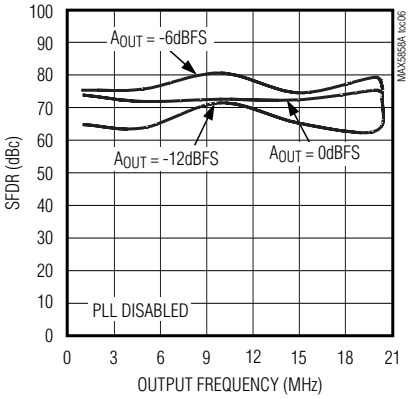
SPURIOUS-FREE DYNAMIC RANGE vs. OUTPUT FREQUENCY (2x INTERPOLATION, f_{DAC} = 300MHz)



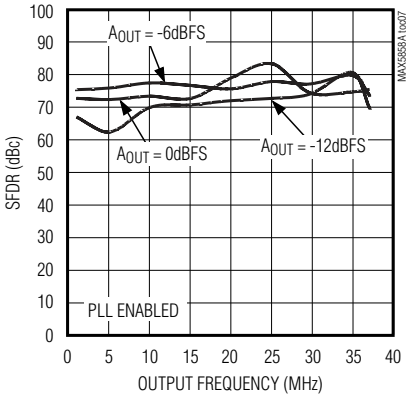
SPURIOUS-FREE DYNAMIC RANGE vs. OUTPUT FREQUENCY (2x INTERPOLATION, f_{DAC} = 165MHz)



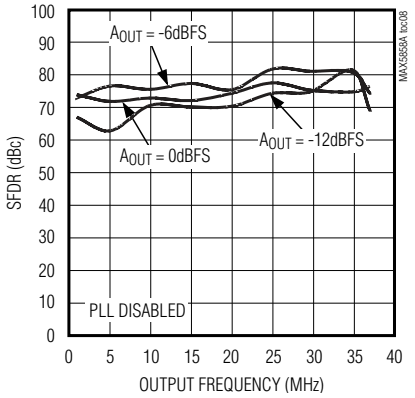
SPURIOUS-FREE DYNAMIC RANGE vs. OUTPUT FREQUENCY (4x INTERPOLATION, f_{DAC} = 165MHz)



SPURIOUS-FREE DYNAMIC RANGE vs. OUTPUT FREQUENCY (4x INTERPOLATION, f_{DAC} = 300MHz)



SPURIOUS-FREE DYNAMIC RANGE vs. OUTPUT FREQUENCY (4x INTERPOLATION, f_{DAC} = 300MHz)

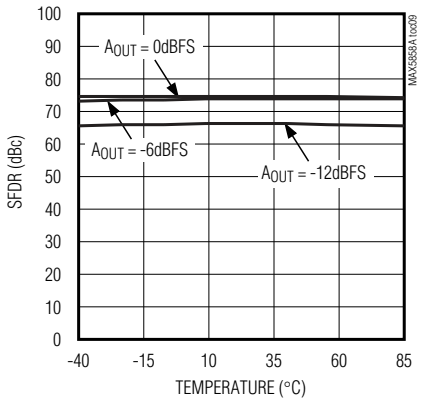


Dual, 10-Bit, 300Msps, DAC with 4x/2x/1x Interpolation Filters and PLL

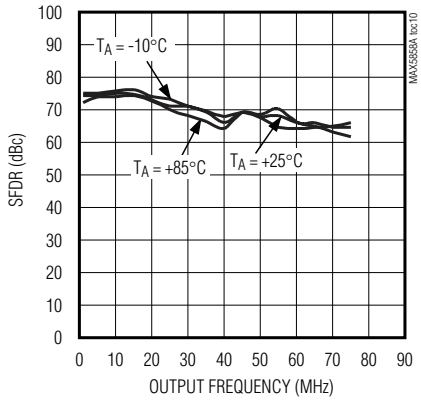
Typical Operating Characteristics (continued)

(AV_{DD} = DV_{DD} = PV_{DD} = 3V, AGND = DGND = PGND = 0, external reference = 1.2V, no interpolation, PLL disabled, I_{FS} = 20mA, differential output, T_A = +25°C, unless otherwise noted.)

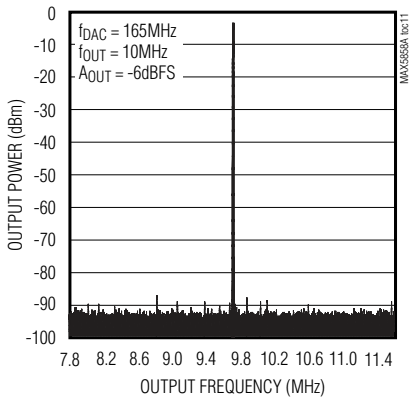
SPURIOUS-FREE DYNAMIC RANGE vs. TEMPERATURE (NO INTERPOLATION, f_{DAC} = 165MHz, f_{OUT} = 5MHz)



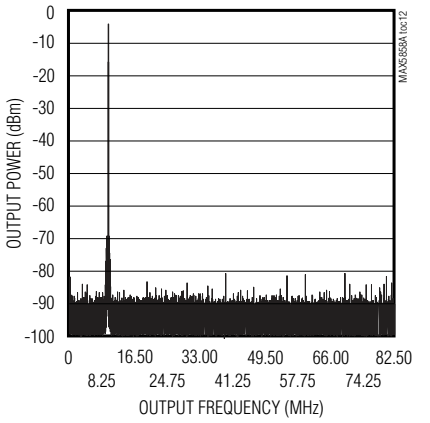
SPURIOUS-FREE DYNAMIC RANGE vs. OUTPUT FREQUENCY (NO INTERPOLATION, f_{DAC} = 165MHz)



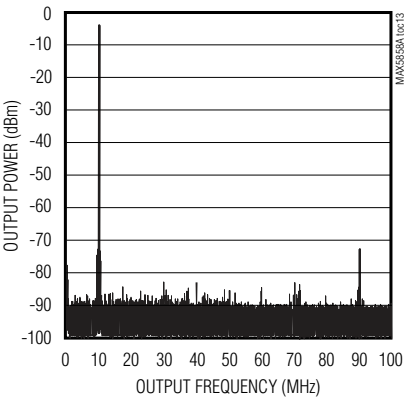
FFT PLOT (±2MHz WINDOW)



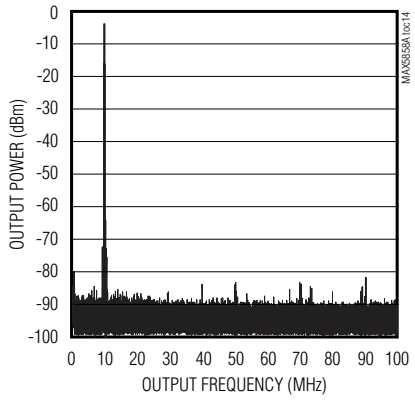
FFT PLOT FOR DAC UPDATE NYQUIST WINDOW (NO INTERPOLATION, f_{DAC} = 165MHz, f_{OUT} = 10MHz, A_{OUT} = 0dBFS)



FFT PLOT FOR DAC UPDATE NYQUIST WINDOW (2x INTERPOLATION, f_{DAC} = 200MHz, f_{OUT} = 10MHz, A_{OUT} = 0dBFS)



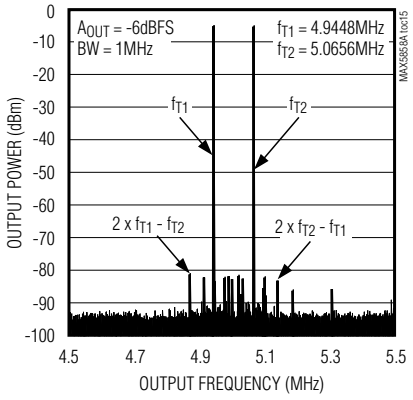
FFT PLOT FOR DAC UPDATE NYQUIST WINDOW (4x INTERPOLATION, f_{DAC} = 200MHz, f_{OUT} = 10MHz, A_{OUT} = 0dBFS)



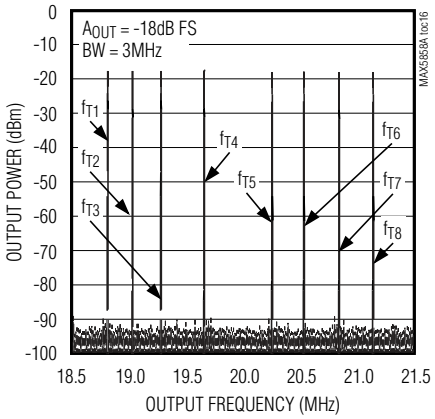
Typical Operating Characteristics (continued)

(AV_{DD} = DV_{DD} = PV_{DD} = 3V, AGND = DGND = PGND = 0, external reference = 1.2V, no interpolation, PLL disabled, I_{FS} = 20mA, differential output, T_A = +25°C, unless otherwise noted.)

2-TONE IMD PLOT
(NO INTERPOLATION, f_{DAC} = 165MHz)

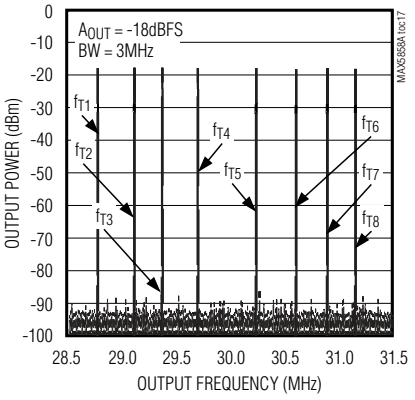


8-TONE MTPR PLOT (NO INTERPOLATION, f_{DAC} = 165MHz, f_{CENTER} = 19.9503MHz)



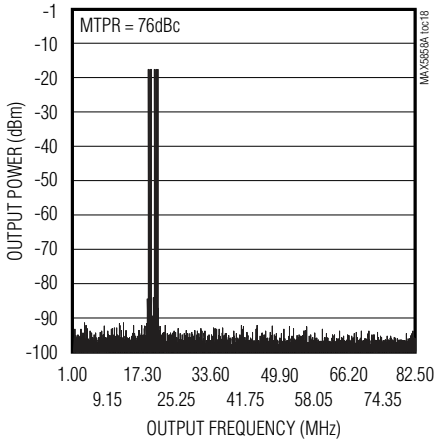
f_{T1} = 18.8022MHz f_{T5} = 20.2524MHz
f_{T2} = 19.0237MHz f_{T6} = 20.5344MHz
f_{T3} = 19.2654MHz f_{T7} = 20.8365MHz
f_{T4} = 19.6481MHz f_{T8} = 21.1386MHz

8-TONE MTPR PLOT (4x INTERPOLATION, f_{DAC} = 286.4MHz, f_{CENTER} = 29.9572MHz)

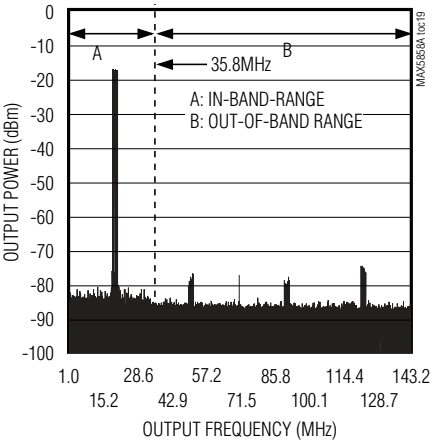


f_{T1} = 28.7597MHz f_{T5} = 30.2281MHz
f_{T2} = 29.1008MHz f_{T6} = 30.5952MHz
f_{T3} = 29.3628MHz f_{T7} = 30.8924MHz
f_{T4} = 29.6862MHz f_{T8} = 31.1546MHz

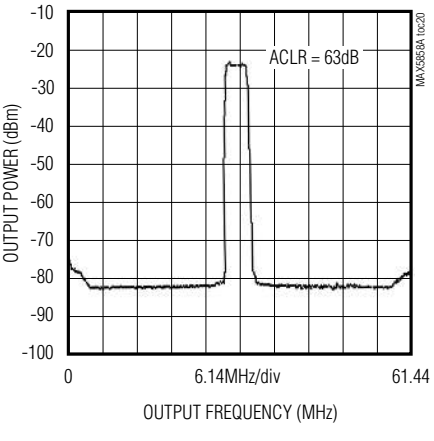
8-TONE MTPR PLOT FOR NYQUIST WINDOW
(NO INTERPOLATION, f_{DAC} = 165MHz, f_{CENTER} = 19.9569MHz, A_{OUT} = -18dBFS)



8-TONE MTPR PLOT FOR NYQUIST WINDOW
(4x INTERPOLATION, f_{DAC} = 286.4MHz, f_{CENTER} = 20MHz, INPUT TONES SPACING ~ 300kHz, A_{OUT} = -18dBFS)



ACLR UMTS PLOT
(NO INTERPOLATION, f_{DAC} = 122.88MHz, f_{DATA} = 122.88MHz, f_{CENTER} = 30.72MHz)

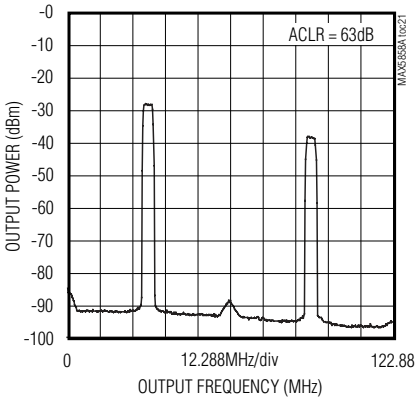


Dual, 10-Bit, 300Msps, DAC with 4x/2x/1x Interpolation Filters and PLL

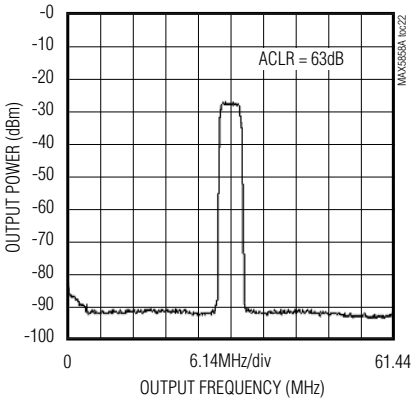
Typical Operating Characteristics (continued)

(AV_{DD} = DV_{DD} = PV_{DD} = 3V, AGND = DGND = PGND = 0, external reference = 1.2V, no interpolation, PLL disabled, I_{FS} = 20mA, differential output, T_A = +25°C, unless otherwise noted.)

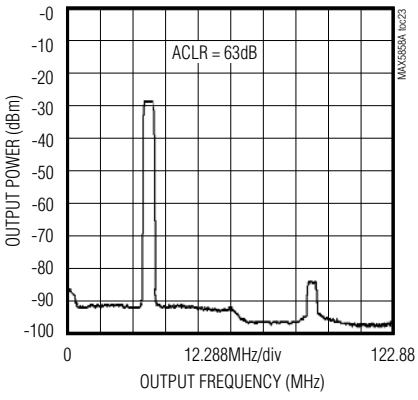
ACLR WITH UMTS PLOT (NO INTERPOLATION, f_{DAC} = 122.88MHz, f_{DATA} = 122.88MHz, f_{CENTER} = 30.72MHz)



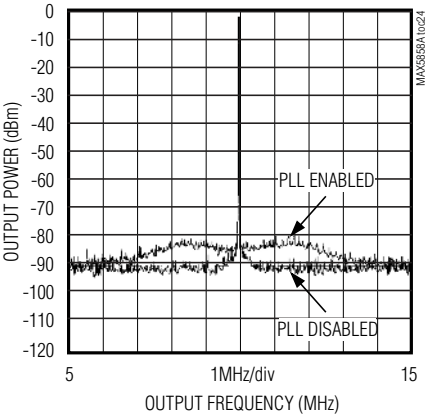
ACLR WITH UMTS PLOT (2x INTERPOLATION, f_{DAC} = 245.76MHz, f_{DATA} = 122.88MHz, f_{CENTER} = 30.72MHz)



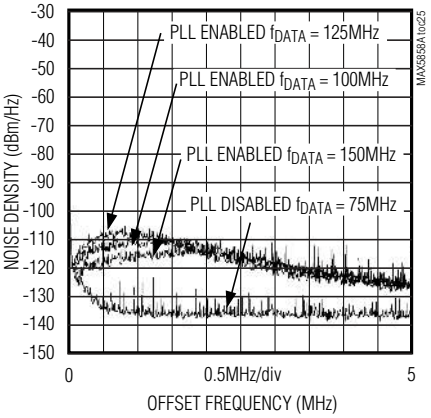
ACLR WITH UMTS PLOT (2x INTERPOLATION, f_{DAC} = 245.76MHz, f_{DATA} = 122.88MHz, f_{CENTER} = 30.72MHz)



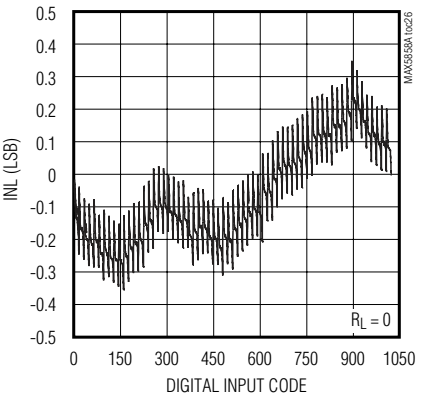
FFT PLOT FOR PLL DISABLED AND PLL ENABLED (f_{OUT} = 10MHz, 2x INTERPOLATION)



PHASE NOISE WITH PLL DISABLED AND ENABLED (f_{OUT} = f_{DATA}/4, 2x INTERPOLATION)



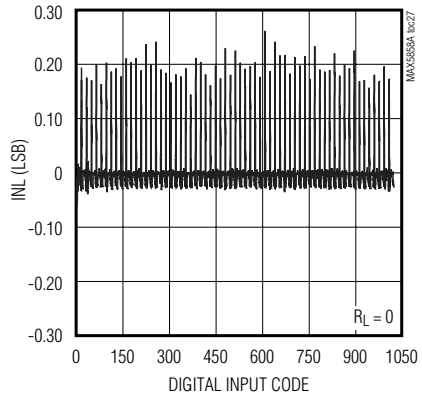
INTEGRAL NONLINEARITY vs. DIGITAL INPUT CODE



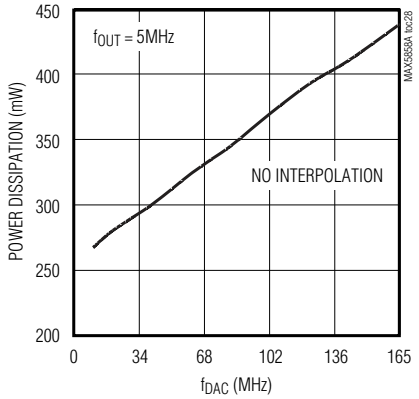
Typical Operating Characteristics (continued)

(AV_{DD} = DV_{DD} = PV_{DD} = 3V, AGND = DGND = PGND = 0, external reference = 1.2V, no interpolation, PLL disabled, I_{FS} = 20mA, differential output, T_A = +25°C, unless otherwise noted.)

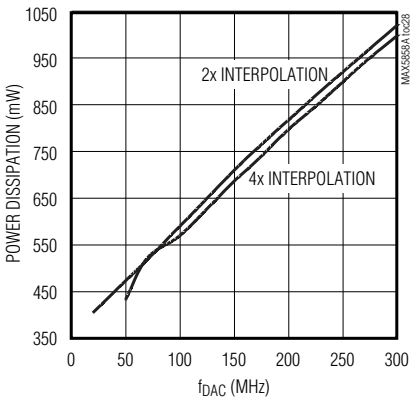
DIFFERENTIAL NONLINEARITY vs. DIGITAL INPUT CODE



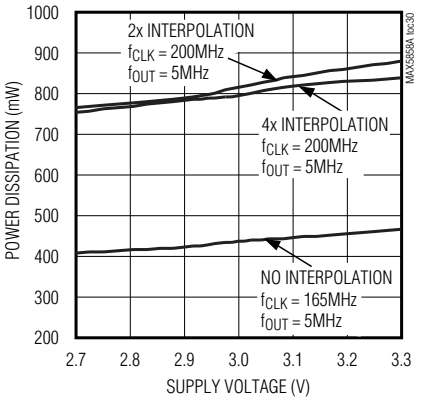
POWER DISSIPATION vs. f_{DAC}



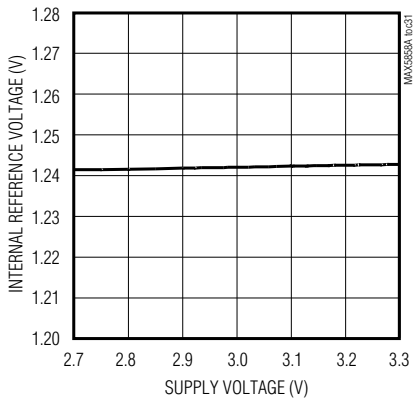
POWER DISSIPATION vs. f_{DAC}



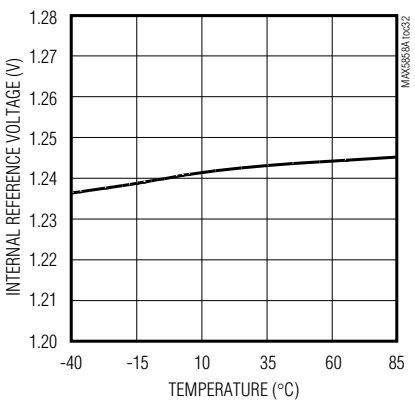
POWER DISSIPATION vs. SUPPLY VOLTAGE



INTERNAL REFERENCE VOLTAGE vs. SUPPLY VOLTAGE



INTERNAL REFERENCE VOLTAGE vs. TEMPERATURE

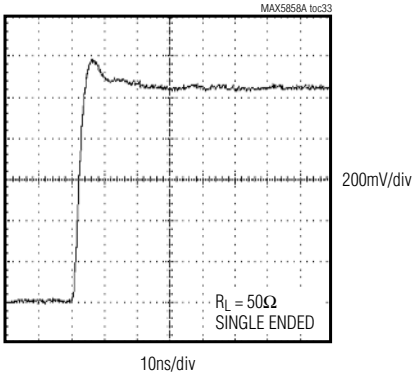


Dual, 10-Bit, 300Msps, DAC with 4x/2x/1x Interpolation Filters and PLL

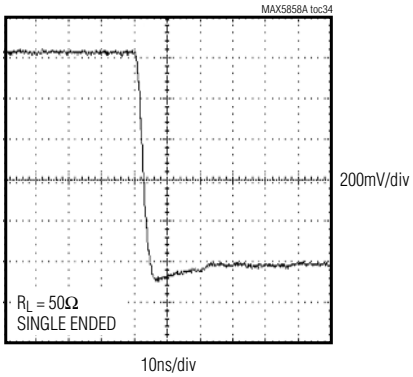
Typical Operating Characteristics (continued)

(AV_{DD} = DV_{DD} = PV_{DD} = 3V, AGND = DGND = PGND = 0, external reference = 1.2V, no interpolation, PLL disabled, I_{FS} = 20mA, differential output, T_A = +25°C, unless otherwise noted.)

DYNAMIC RESPONSE RISE TIME



DYNAMIC RESPONSE FALL TIME



Pin Description

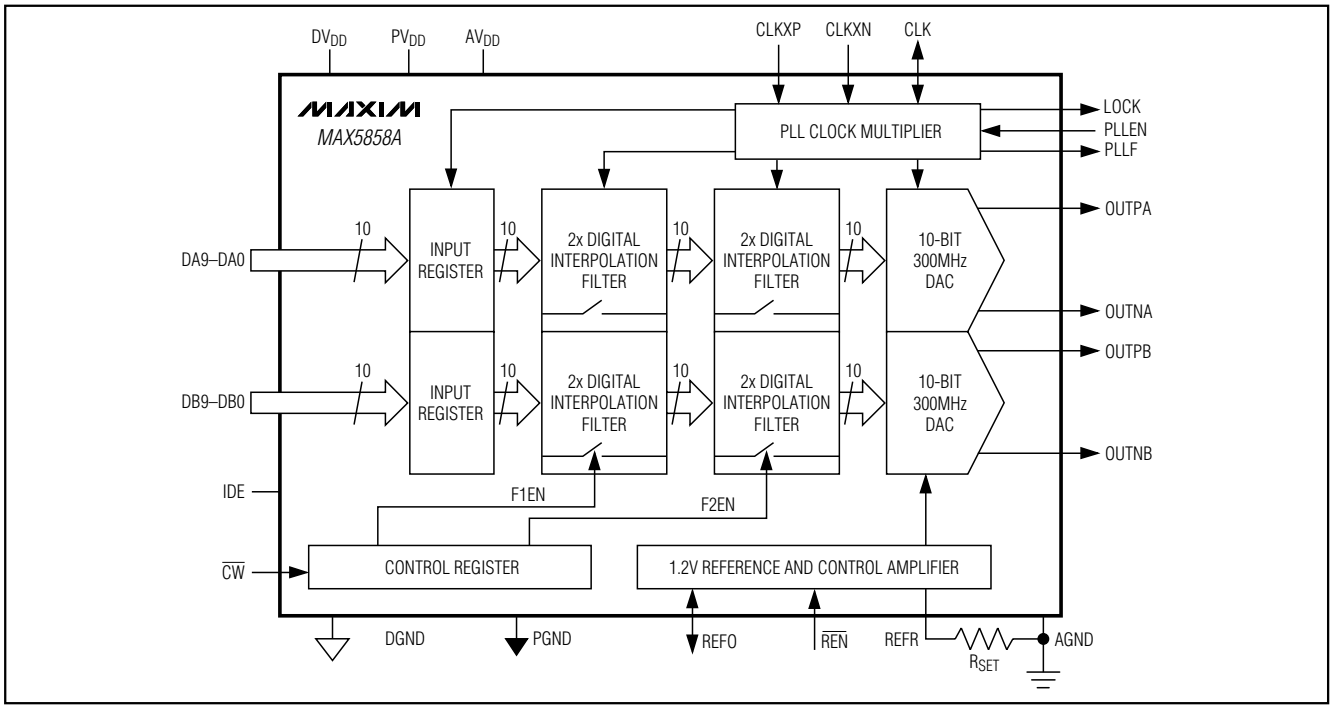
PIN	NAME	FUNCTION
1	DA9/PD	Channel A Input Data Bit 9 (MSB)/Power-Down Control Bit: 0: Enter DAC standby mode (DACEN = 0) or power up DAC (DACEN = 1). 1: Enter power-down mode.
2	DA8/DACEN	Channel A Input Data Bit 8/DAC Enable Control Bit: 0: Enter DAC standby mode with PD = 0. 1: Power up DAC with PD = 0. X: Enter power-down mode with PD = 1 (X = don't care.)
3	DA7/F2EN	Channel A Input Data Bit 7/Second Interpolation Filter Enable Bit: 0: Interpolation mode is determined by F1EN. 1: Enable 4x interpolation mode. (F1EN must equal 1.)
4	DA6/F1EN	Channel A Input Data Bit 6/First Interpolation Filter Enable Bit: 0: Interpolation disable. 1: Enable 2x interpolation.
5	DA5/G3	Channel A Input Data Bit 5/Channel A Gain Adjustment Bit 3
6, 19, 47	DGND	Digital Ground
7, 18, 48	DV_{DD}	Digital Power Supply. See *Power Supplies, Bypassing, Decoupling, and Layout* section.
8	DA4/G2	Channel A Input Data Bit 4/Channel A Gain Adjustment Bit 2
9	DA3/G1	Channel A Input Data Bit 3/Channel A Gain Adjustment Bit 1
10	DA2/G0	Channel A Input Data Bit 2/Channel A Gain Adjustment Bit 0
11	DA1	Channel A Input Data Bit 1
12	DA0	Channel A Input Data Bit 0 (LSB)

Pin Description (continued)

PIN	NAME	FUNCTION
13	DB9	Channel B Input Data Bit 9 (MSB)
14	DB8	Channel B Input Data Bit 8
15	DB7	Channel B Input Data Bit 7
16	DB6	Channel B Input Data Bit 6
17	DB5	Channel B Input Data Bit 5
20	CLK	Clock Output/Input. CLK becomes an input when the PLL is enabled. CLK is an output when the PLL is disabled.
21	IDE	Interleave Data Mode Enable. When IDE is high, data for both DAC channels is written through port A (bits DA9–DA0). When IDE is low, channel A data is latched on the rising edge of CLK and channel B data is latched on the falling edge of CLK.
22	DB4	Channel B Input Data Bit 4
23	DB3	Channel B Input Data Bit 3
24	DB2	Channel B Input Data Bit 2
25	DB1	Channel B Input Data Bit 1
26	DB0	Channel B Input Data Bit 0 (LSB)
27	$\overline{CW}$	Active-Low Control-Word Write Pulse. The control word is latched on the falling edge of $\overline{CW}$.
28	LOCK	PLL Lock Signal Output. High level indicates that PLL is locked to the CLK signal.
29	PLLEN	PLL Enabled Input. PLL in enabled when PLLEN is high.
30	CLKXP	Differential Clock Input Positive Terminal. Connect to PGND when the PLL is enabled. Bypass CLKXP with a 0.01µF capacitor to PGND when CLKXN is in single-ended mode.
31	CLKXN	Differential Clock Input Negative Terminal. Connect to PV_{DD} when the PLL is enabled. Bypass CLKXN with a 0.01µF capacitor to PGND when CLKXP is in single-ended mode.
32	PV_{DD}	PLL Power Supply. See *Power Supplies, Bypassing, Decoupling, and Layout* section.
33	PGND	PLL Ground
34	PLLF	PLL Loop Filter. Connect a 4.12kΩ resistor in series with a 100pF capacitor between PLLF and PGND.
35	$\overline{REN}$	Active-Low Reference Enable. Connect $\overline{REN}$ to AGND to activate the on-chip 1.24V reference.
36	REFO	Reference I/O. REFO serves as the reference input when the internal reference is disabled. If the internal 1.24V reference is enabled, REFO serves as the output for the internal reference. When the internal reference is enabled, bypass REFO to AGND with a 0.1µF capacitor.
37, 38	N.C.	No Connection. Not connected internally.
39	REFR	Full-Scale Current Adjustment. To set the output full-scale current, connect an external resistor R_{SET} between REFR and AGND. The output full-scale current is equal to $32 \times V_{REFO}/R_{SET}$.
40, 46	AV_{DD}	Analog Power Supply. See *Power Supplies, Bypassing, Decoupling, and Layout* section.
41	OUTNB	Channel B Negative Analog Current Output
42	OUTPB	Channel B Positive Analog Current Output
43	AGND	Analog Ground
44	OUTNA	Channel A Negative Analog Current Output
45	OUTPA	Channel A Positive Analog Current Output
—	EP	Exposed Paddle. Connect to the ground plane.

Dual, 10-Bit, 300Msps, DAC with 4x/2x/1x Interpolation Filters and PLL

Block Diagram



Detailed Description

The MAX5858A dual, high-speed, 10-bit, current-output DAC provides superior performance in communication systems requiring low-distortion analog-signal reconstruction. The MAX5858A combines two DAC cores with 2x/4x programmable digital interpolation filters, a PLL clock multiplier, divide-by-N clock output, and an on-chip 1.24V reference. The current outputs of the DACs can be configured for differential or single-ended operation. The full-scale output current range is adjustable from 2mA to 20mA to optimize power dissipation and gain control.

The MAX5858A accepts an input data rate of up to 165MHz or a DAC conversion rate of up to 300MHz. The inputs are latched on the rising edge of the clock whereas the output latches on the following rising edge.

The two-stage digital interpolation filters are programmable to 4x, 2x, or no interpolation. When operating in 4x interpolation mode, the interpolator increases the DAC conversion rate by a factor of four, providing a four-fold increase in separation between the reconstructed waveform spectrum and its first image.

The on-chip PLL clock multiplier generates and distributes all internal, synchronized high-speed clock signals required by the input data latches, interpolation filters, and DAC cores. The on-chip PLL includes phase-detector, VCO, prescalar, and charge-pump circuits. The PLL can be enabled or disabled through PLLEN.

The analog and digital sections of the MAX5858A have separate power-supply inputs (AV_{DD} and DV_{DD}). Also, a separate supply input is provided for the PLL clock multiplier (PV_{DD}). AV_{DD}, DV_{DD}, and PV_{DD} operate from a 2.7V to 3.3V single supply.

The MAX5858A features three modes of operation: normal, standby, and power-down. These modes allow efficient power management. In power-down, the MAX5858A consumes only 1µA of supply current. Wake-up time from standby mode to normal DAC operation is 0.7µs.

Programming the DAC

An 8-bit control word routed through channel A's data port programs the gain matching, interpolator configuration, and operational mode of the MAX5858A. The control word is latched on the falling edge of $\overline{CW}$. Table 1 describes the control word format and function.

The gain on channel A can be adjusted to achieve gain matching between two channels in a user's system. The gain on channel A can be adjusted from +0.4dB to -0.35dB in steps of 0.05dB by using bits G3 to G0 (see Table 3).

Device Power-Up and States of Operation

At power-up, the MAX5858A is configured in no-interpolation mode with a gain adjustment setting of 0dB and a fully operational converter. In shutdown, the MAX5858A consumes only 1µA of supply current, and in standby the current consumption is 4.4mA. Wake-up time from standby mode to normal operation is 0.7µs.

Interpolation Filters

The MAX5858A features a two stage, 2x digital interpolating filter based on 43-tap and 23-tap FIR topology. F1EN and F2EN enable the interpolation filters. F1EN = 1 enables the first filter for 2x interpolation and F2EN = 2 enables the second filter for combined 4x interpolation. To bypass and disable both interpolation filters (no-interpolation mode or 1x mode) set F1EN = F2EN = 0. When set for 1x mode the filters are powered down and consume virtually no current. An illegal condition is defined by: F1EN = 0, F2EN = 1 (see Table 2 for configuration modes).

The programmable interpolation filters multiply the MAX5858A input data rate by a factor of two or four to separate the reconstructed waveform spectrum and the first image. The original spectral images, appearing around multiples of the DAC input data rate, are attenuated at least 60dB by the internal digital filters. This feature provides three benefits:

1) Image separation reduces complexity of analog reconstruction filters.
2) Lower input data rates eliminate board level high-speed data transmission.
3) Sin(x)/x roll-off is reduced over the effective bandwidth.

Figure 2 shows an application circuit and Figure 3 illustrates a practical example of the benefits when using the MAX5858A with 4x-interpolation mode. The example illustrates signal synthesis of a 20MHz IF with a ±10MHz bandwidth. Three options can be considered to address the design requirements. The tradeoffs for each solution are depicted in Table 4.

Table 1. Control Word Format and Function

MSB									LSB
PD	DACEN	F2EN	F1EN	G3	G2	G1	G0	X	X

CONTROL WORD	FUNCTION
PD	Power-down: The part enters power-down mode if PD = 1.
DACEN	DAC Enable: When DACEN = 0 and PD = 0, the part enters standby mode.
F2EN	Filter Enable: When F2EN = 1 and F1EN = 1, 4x interpolation is enabled. When F2EN = 0, the interpolation mode is determined by F1EN.
F1EN	Filter Enable: When F1EN = 1 and F2EN = 0, 2x interpolation is active. With F1EN = 0 and F2EN = 0, the interpolation is disabled.
G3	Bit 3 (MSB) of gain adjust word.
G2	Bit 2 of gain adjust word.
G1	Bit 1 of gain adjust word.
G0	Bit 0 (LSB) of gain adjust word.

Table 2. Configuration Modes

MODE	PD	DACEN	F2EN	F1EN
No interpolation	0	1	0	0
2x interpolation	0	1	0	1
4x interpolation	0	1	1	1
Standby	0	0	X	X
Power-down	1	X	X	X
Power-up	0	1	X	X

X = Don't care.
F1EN = 0, F2EN = 1: illegal condition

Table 3. Gain Difference Setting

GAIN ADJUSTMENT ON CHANNEL A (dB)	G3	G2	G1	G0
+0.4	0	0	0	0
0	1	0	0	0
-0.35	1	1	1	1

Dual, 10-Bit, 300Msps, DAC with 4x/2x/1x Interpolation Filters and PLL

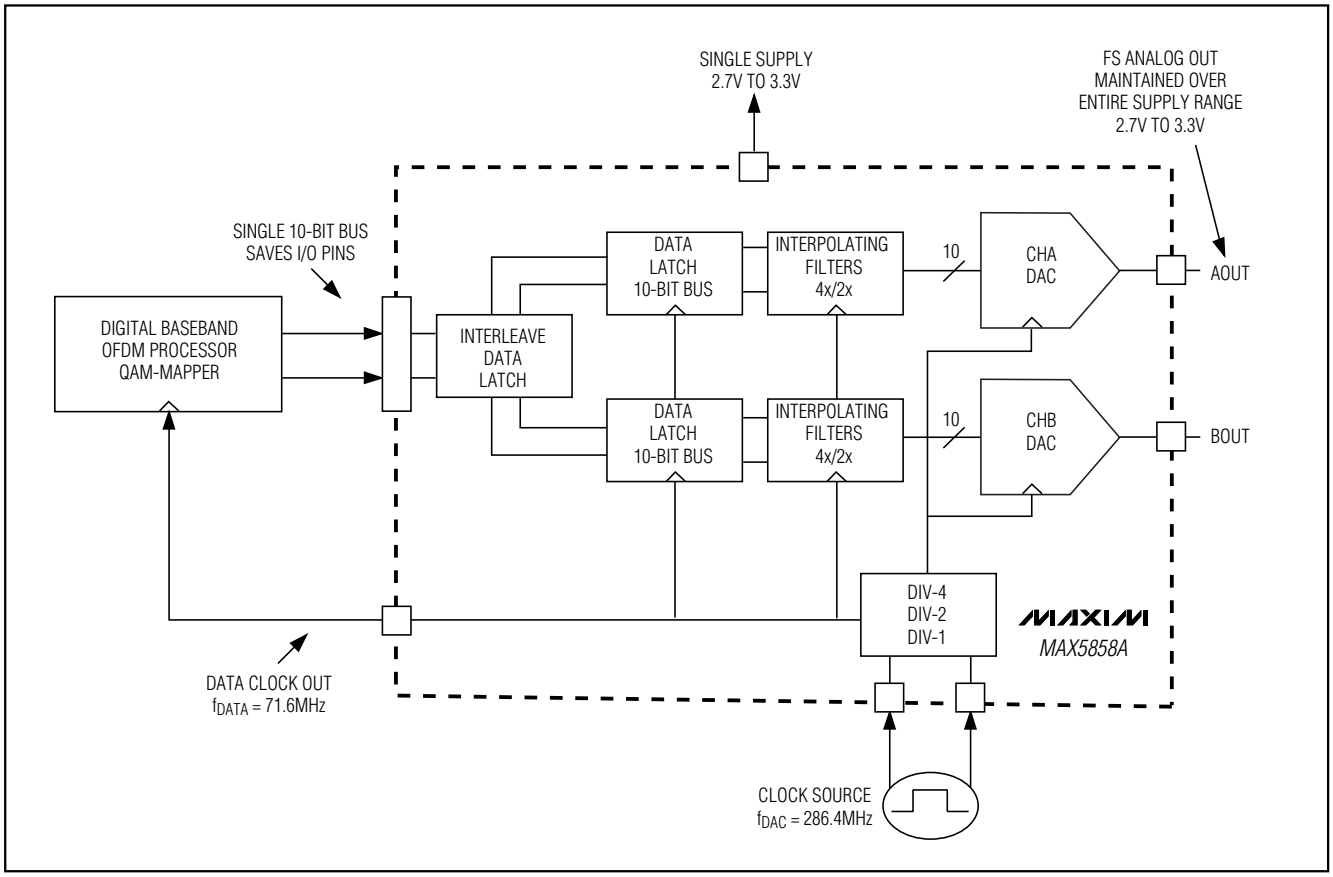


Figure 2. Typical Application Circuit

Table 4. Benefits of Interpolation

OPTION	SOLUTION	ADVANTAGE	DISADVANTAGE
1	• No interpolation • 2.6x oversample • $f_{DAC} = f_{DATA}$ = 78MHz	• Low data rate • Low clock rate	• High order filter • Filter gain/phase match
2	• No interpolation • 8x oversample • $f_{DAC} = f_{DATA}$ = 240MHz • Push image to f_{IMAGE} = 210MHz	• Lower order filter • Filter gain/phase match	• High clock rate • High data rate
3	• 4x interpolation • f_{DAC} = 286.4MHz, f_{DATA} = 71.6MHz • Passband attenuation = 0.1dB • Push image to 256MHz	• Low data rate • Low order filter • 60dB image attenuate • Filter gain/phase match	• None

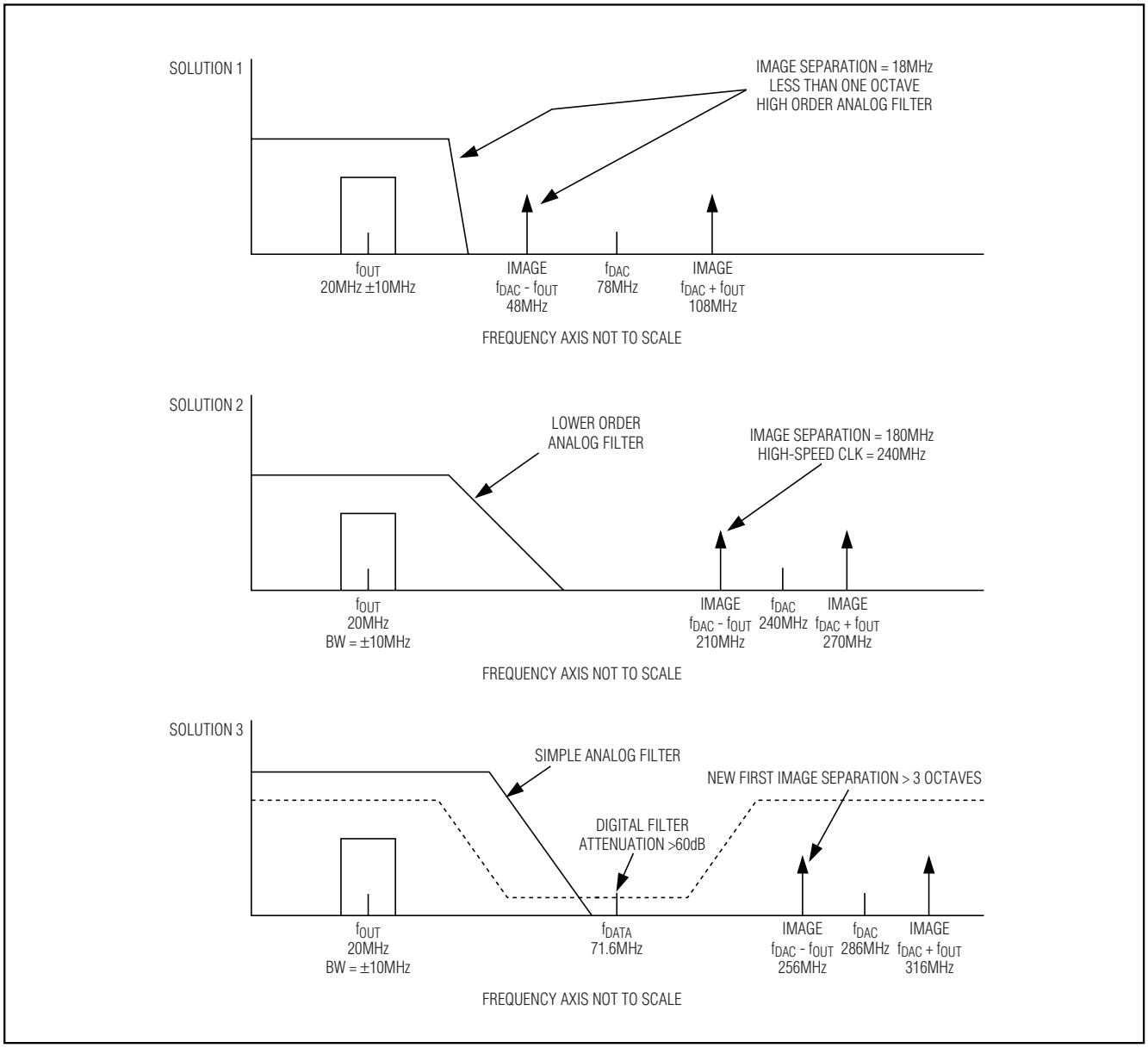


Figure 3. MAX5858A in 4x Interpolation Mode

This example demonstrates that 4x interpolation with digital filtering yields significant benefits in reducing system complexity, improving dynamic performance and lowering cost. Data can be written to the MAX5858A at much lower speeds while achieving image attenuation greater than 60dB and image separation beyond three octaves. The main benefit is in analog reconstruction filter design. Reducing the filter order eases gain/phase matching while lowering filter cost and saving board space. Because the data rate is lowered to 71.6MHz, the setup and hold times are manageable and the clock signal source is simplified, which results in improved system reliability and lower cost.

Dual, 10-Bit, 300Msps, DAC with 4x/2x/1x Interpolation Filters and PLL

PLL Clock Multiplier and Clocking Modes

The MAX5858A features an on-chip PLL clock multiplier that generates all internal, synchronized high-speed clock signals required by the input data latches, interpolation filters, and DAC cores. The on-chip PLL includes a phase-detector, VCO, prescalar, and charge-pump circuits. The PLL can be enabled or disabled through PLLEN. To enable PLL set PLLEN = 1.

With the PLL enabled (PLLEN = 1) and 4x/2x interpolation enabled, an external low-frequency clock reference source is applied to CLK pin. The clock reference source serves as the input data clock. The on-chip PLL multiplies the clock reference by a factor of two (2x) or a factor of four (4x). The input data rate range and CLK frequency are set by the selected interpolation mode. In 2x interpolation mode, the data rate range is 75MHz to 150MHz. In 4x interpolation mode the data rate range is 37.5MHz to 75MHz.

Note: When the PLL is enabled, CLK becomes an input, requiring CLKXP to be pulled low and CLKXN to be pulled high. To obtain best phase noise performance, disable the PLL function.

With the PLL disabled (PLLEN = 0) and 4x/2x interpolation enabled, an external conversion clock is applied at CLKXN/CLKXP. The conversion clock at CLKXN/CLKXP has a frequency range of 0MHz to 300MHz (see Table 5). This clock is buffered and distributed by the MAX5858A to drive the interpolation filters and DAC cores. In this mode, CLK becomes a divide-by-N (DIV-N) output at either a divide-by-two or divide-by-four rate. The DIV-N factor is set by the selected interpolation mode. The CLK output, at DIV-N rate, must be used to synchronize data into the MAX5858A data ports. In this mode, keep the capacitive load at the CLK output low (10pF or less at f_{DAC} = 165MHz).

With the interpolation disabled (1x mode) and the PLL disabled (PLLEN = 0), the input clock at CLKXN/CLKXP can be used to directly update the DAC cores. In this mode, the maximum data rate is 165MHz.

Internal Reference and Control Amplifier

The MAX5858A provides an integrated 50ppm/°C, 1.24V, low-noise bandgap reference that can be disabled and overridden with an external reference voltage. REFO serves either as an external reference input or an integrated reference output. If $\overline{REN}$ is connected to AGND, the internal reference is selected and REFO provides a 1.24V (50µA) output. Buffer REFO with an external amplifier, when driving a heavy load.

The MAX5858A also employs a control amplifier designed to simultaneously regulate the full-scale output current (I_{FS}) for both outputs of the devices. Calculate the output current as:

$$I_{FS} = 32 \times I_{REF}$$

where I_{REF} is the reference output current ($I_{REF} = V_{REFO}/R_{SET}$) and I_{FS} is the full-scale output current. R_{SET} is the reference resistor that determines the amplifier output current of the MAX5858A (Figure 4). This current is mirrored into the current-source array where I_{FS} is equally distributed between matched current segments and summed to valid output current readings for the DACs.

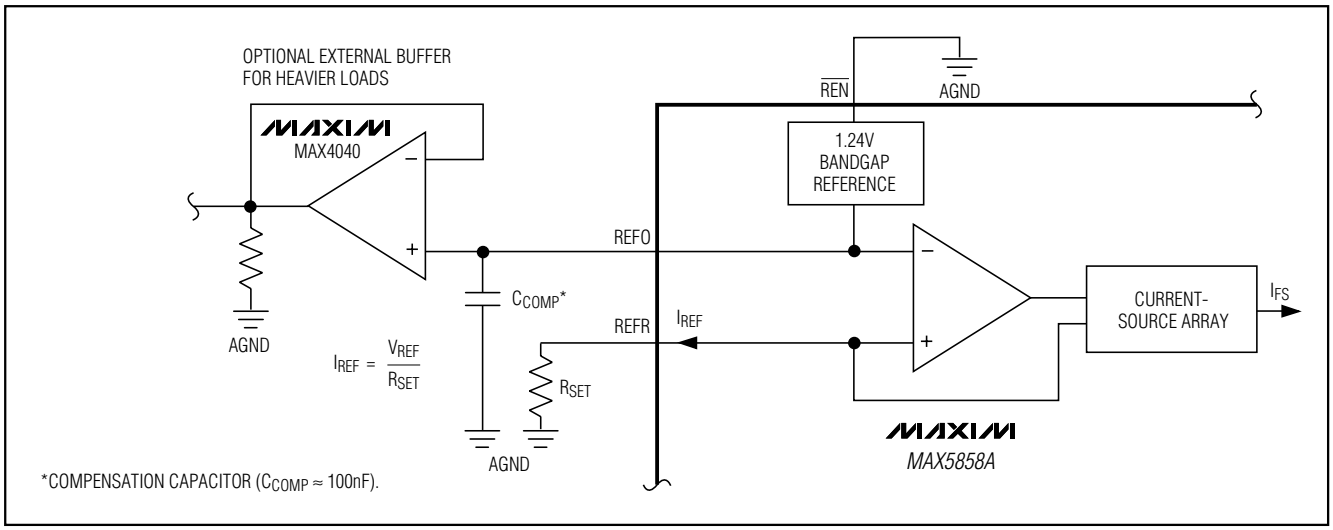


Figure 4. Setting IFS with the Internal 1.24V Reference and the Control Amplifier

External Reference

To disable the internal reference of the MAX5858A, connect $\overline{REN}$ to AV_{DD}. Apply a temperature-stable, external reference to REFO to set the full-scale output (Figure 5). For improved accuracy and drift performance, choose a fixed output voltage reference such as the MAX6520 bandgap reference.

Detailed Timing

The MAX5858A accepts an input data rate up to 165MHz or the DAC conversion rate of 300MHz. The input latches on the rising edge of the clock, whereas the output latches on the following rising edge.

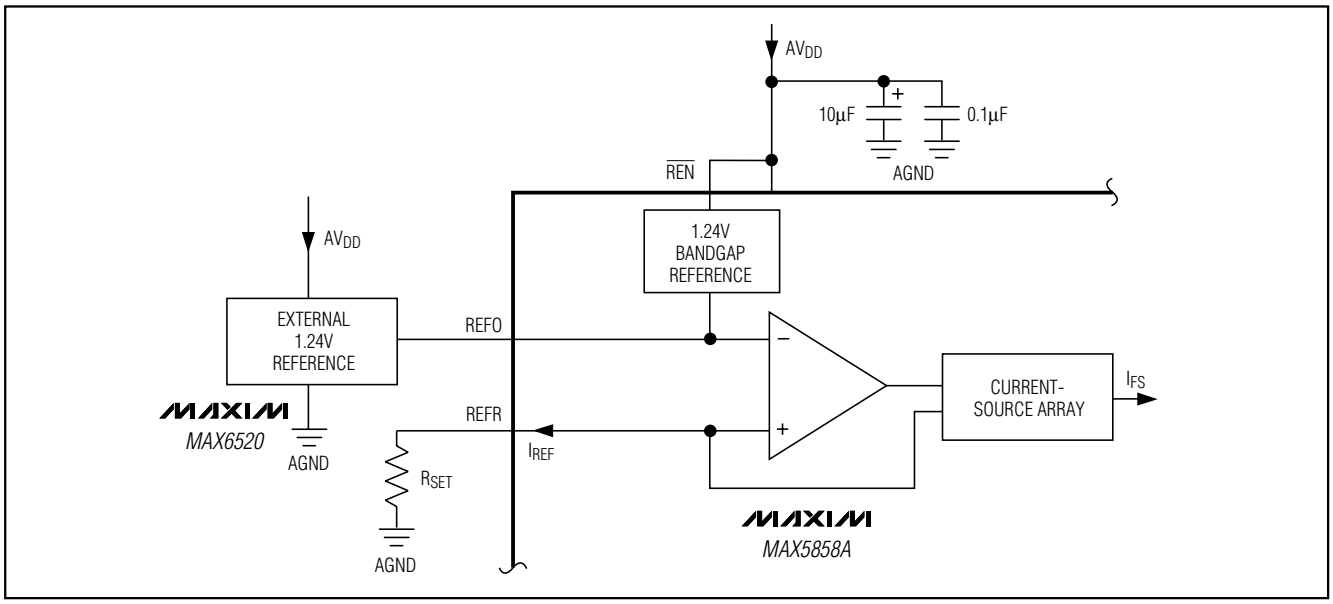


Figure 5. MAX5858A with External Reference

Table 5. PLL Clocking Modes

PLLEN	F2EN	F1EN	DIFFERENTIAL CLOCK FREQUENCY $f_{CLKDIFF}$ (MHz)	CLOCK FREQUENCY f_{CLK} (MHz)	DAC RATE f_{DAC}	INTERPOLATION	MAX SIGNAL BANDWIDTH (MHz)
1	0	0	N/A (connect CLXP low and CLXN high)	0 to 165 (input)	f_{CLK}	1x	82
1	0	1	N/A (connect CLXP low and CLXN high)	75 to 150 (input)	2 x f_{CLK}	2x	63
1	1	1	N/A (connect CLXP low and CLXN high)	37 to 75 (input)	4 x f_{CLK}	4x	31
0	0	0	0 to 165	$f_{CLKDIFF}$ (output)	$f_{CLKDIFF}$	1x	82
0	0	1	0 to 300	$f_{CLKDIFF}$ /2 (output)	$f_{CLKDIFF}$	2x	63
0	1	1	0 to 300	$f_{CLKDIFF}$ /4 (output)	$f_{CLKDIFF}$	4x	31
0	1	0	Illegal				
1	1	0					

Dual, 10-Bit, 300Msps, DAC with 4x/2x/1x Interpolation Filters and PLL

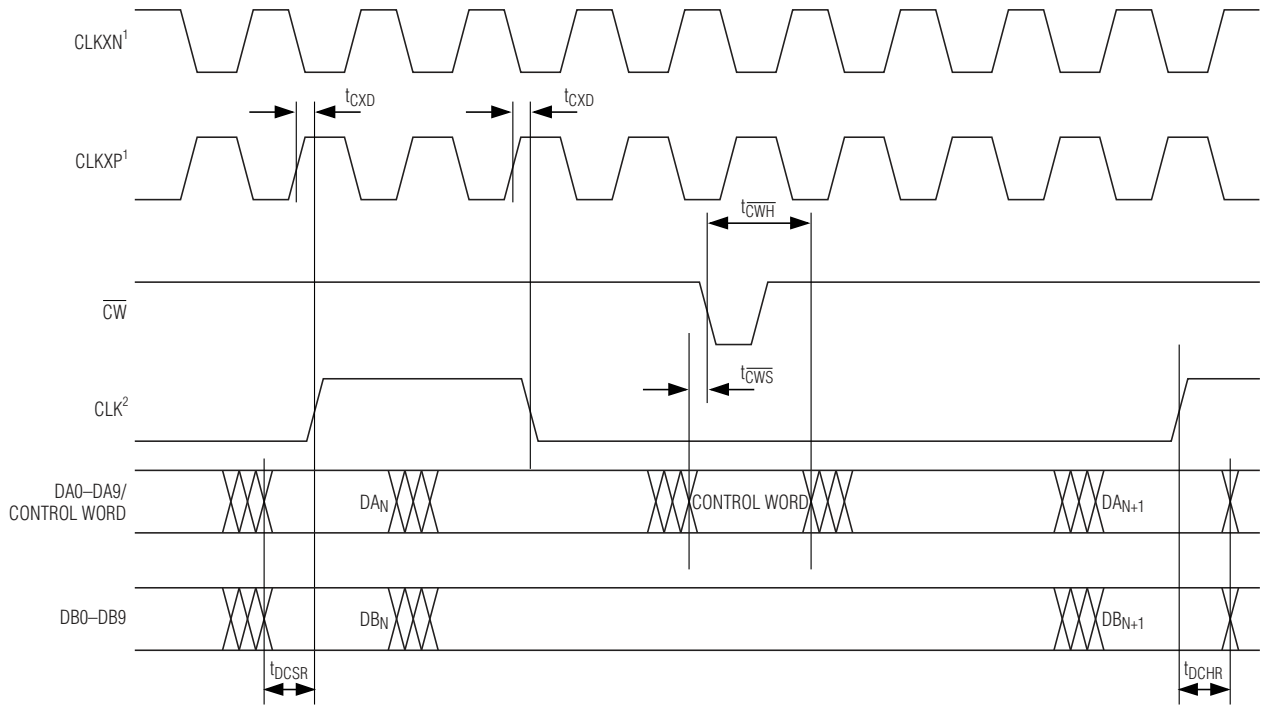
Figure 6 depicts the write cycle of the MAX5858A in 4x interpolation mode. With the interpolation feature enabled, the device can operate with the PLL enabled or disabled.

With the PLL disabled (PLLEN = 0), the clock signal is applied to CLKXP/CLKXN and internally divided by 4 to generate the DAC's CLK signal. The CLK signal is a divide-by-four output used to synchronize data into the MAX5858A data ports. The CLKXP/CLKXN signal drives the interpolation filters and DAC cores at the desired conversion rate.

If the PLL is enabled (PLLEN = 1), CLK becomes an input and the clock signal is applied to CLK. In Figure 6, the CLK signal is multiplied by a factor of four by the PLL and distributed to the interpolation filters and DAC cores. In this mode, CLKXP must be pulled low and CLKXN pulled high.

The MAX5858A can operate with a single-ended clock input used as both data clock and conversion clock. To operate the device in this mode, disable the interpolation filters and enable the PLL (PLLEN = 1). Apply a single-ended clock input at CLK. The CLK signal acts as the data synchronization clock and DAC core conversion clock. Though the PLL is enabled, the lock pin (LOCK) is not valid and the PLL is internally disconnected from interpolating filters and DAC cores. In this mode, CLKXP must be pulled low and CLKXN pulled high.

Figure 6 shows the timing for the control word write pulse ($\overline{CW}$). An 8-bit control word routed through channel A's data port programs the gain matching, interpolator configuration, and operational mode of the MAX5858A. The control word is latched on the falling edge of $\overline{CW}$. The $\overline{CW}$ signal is asynchronous with conversion clocks CLK and CLKXN/CLKXP; therefore, the conversion clock (CLK or CLKXN/CLKXP) can run uninterrupted when a control word is written to the device.



1. CLKXP AND CLKXN MUST BE PRESENT WHEN PLL IS DISABLED, WITH PLLEN CONNECTED TO GND. THE DIAGRAM SHOWS 4x INTERPOLATION.
2. CLK IS AN OUTPUT WHEN PLL IS DISABLED WITH PLLEN CONNECTED TO GND, OTHERWISE, IT IS AN INPUT.

Figure 6. Timing Diagram for Noninterleave Data Mode (IDE = Low)

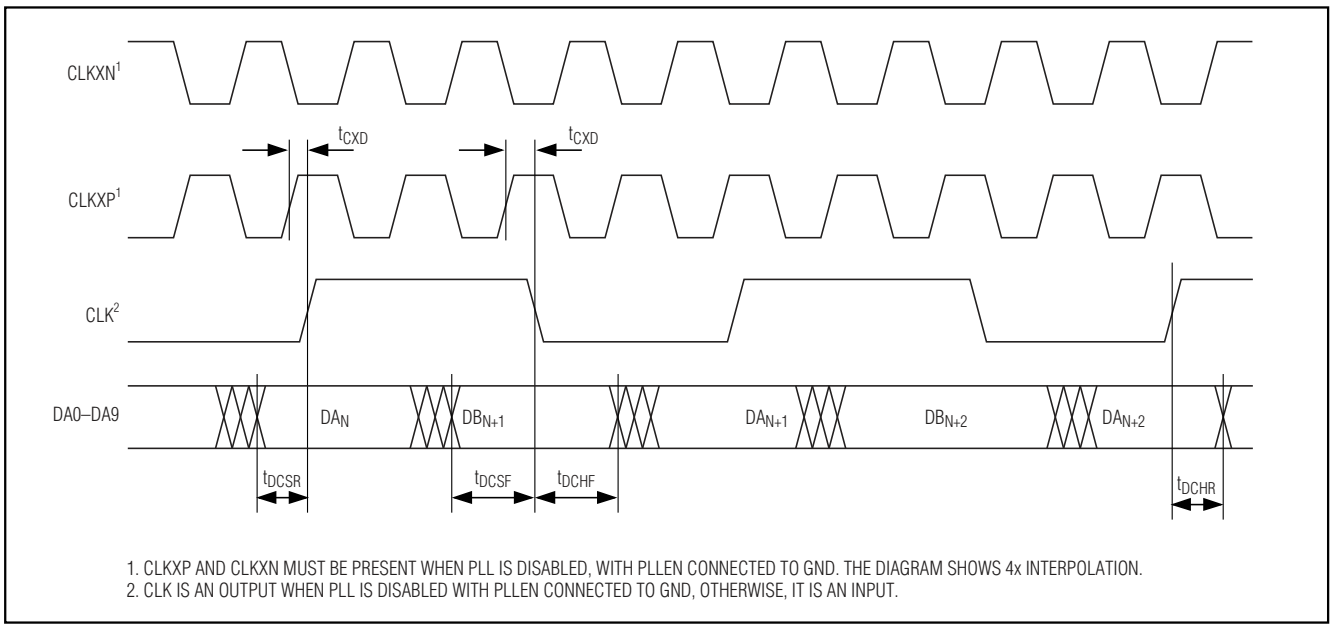


Figure 7. Timing Diagram for Interleave Data Mode (IDE = High)

The MAX5858A can operate in interleave data mode by setting IDE = 1. In interleave data mode, data for both DAC channels is written through input port A. Channel B data is written on the falling edge of the CLK signal and then channel A data is written on the following rising edge of the CLK signal. Both DAC outputs (channel A and B) are updated simultaneously on the next rising edge of CLK. In interleave data mode, the maximum input data rate per channel is one-half the rate of noninterleave mode. Interleave data mode is an attractive feature that lowers digital I/O pin count, reduces digital ASIC cost and improves system reliability (Figure 7).

Applications Information

Differential-to-Single-Ended Conversion

The MAX5858A exhibits excellent dynamic performance to synthesize a wide variety of modulation schemes, including high-order QAM modulation with OFDM.

Figure 8 shows a typical application circuit with output transformers performing the required differential-to-single-ended signal conversion. In this configuration, the MAX5858A operates in differential mode, which reduces even-order harmonics, and increases the available output power.

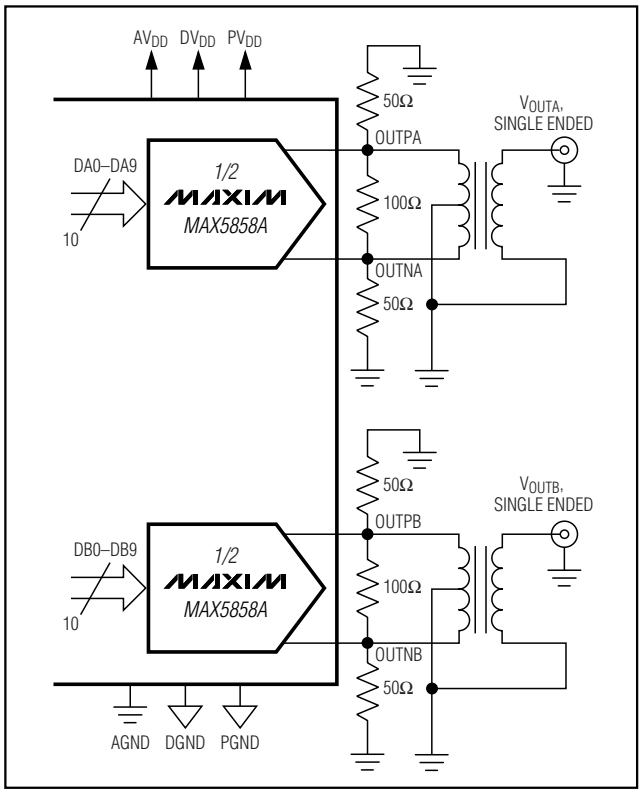


Figure 8. Application with Output Transformer Performing Differential to Single-Ended Conversion

Dual, 10-Bit, 300Msps, DAC with 4x/2x/1x Interpolation Filters and PLL

Differential DC-Coupled Configuration

Figure 9 shows the MAX5858A output operating in differential, DC-coupled mode. This configuration can be used in communication systems employing analog quadrature upconverters and requiring a baseband sampling, dual-channel, high-speed DAC for I/Q synthesis. In these applications, information bandwidth can extend from 10MHz down to several hundred kilohertz. DC-coupling is desirable in order to eliminate long discharge time constants that are problematic with large, expensive coupling capacitors. Analog quadrature upconverters have a DC common-mode input requirement of typically 0.7V to 1.0V. The MAX5858A differential I/Q outputs can maintain the desired full-scale original level at the required 0.7V to 1.0V DC common-mode voltage when powered from a single 2.85V (±5%) supply. The MAX5858A meets this low-power requirement with minimal reduction in dynamic range while eliminating the need for level-shifting resistor networks.

Power Supplies, Bypassing, Decoupling, and Layout

Grounding and power-supply decoupling strongly influence the MAX5858A performance. Unwanted digital crosstalk can couple through the input, reference, power-supply, and ground connections, which can affect dynamic specifications, like signal-to-noise ratio or spurious-free dynamic range. In addition, electromagnetic interference (EMI) can either couple into or be generated by the MAX5858A. Observe the grounding and power-supply decoupling guidelines for high-speed, high-frequency applications. Follow the power supply and filter configuration to achieve optimum dynamic performance.

Use of a multilayer printed circuit (PC) board with separate ground and power-supply planes is recommended. Run high-speed signals on lines directly above the ground plane. The MAX5858A has separate analog and digital ground buses (AGND, PGND, and DGND, respectively). Provide separate analog, digital, and clock ground sections on the PC board with only one point connecting the three planes. The ground connection points should be located underneath the device and connected to the exposed paddle. Run digital signals above the digital ground plane and analog/clock signals above the analog/clock ground plane. Digital signals should be kept away from sensitive analog, clock, and reference inputs. Keep digital signal paths short and metal trace lengths matched to avoid propagation delay and data skew mismatch.

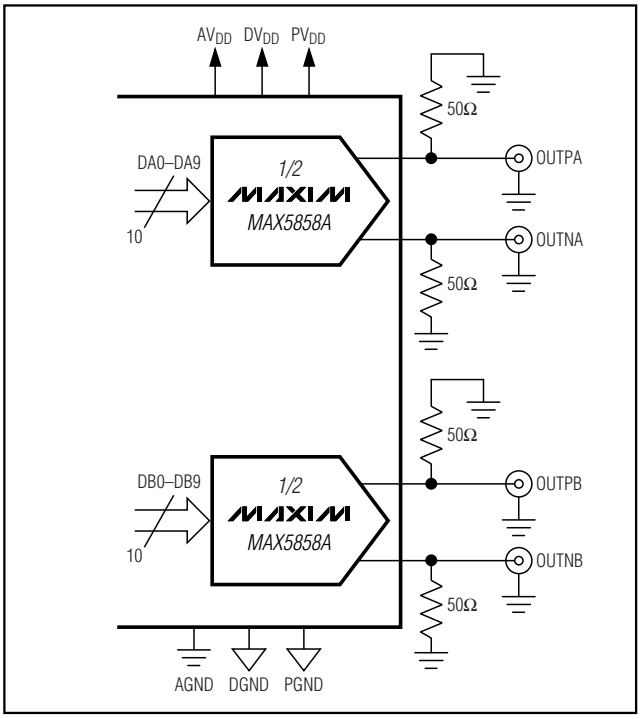


Figure 9. Application with DC-Coupled Differential Outputs

The MAX5858A includes three separate power-supply inputs: analog (AV_{DD}), digital (DV_{DD}), and clock (PV_{DD}). Use a single linear regulator power source to branch out to three separate power-supply lines (AV_{DD}, DV_{DD}, PV_{DD}) and returns (AGND, DGND, PGND). Filter each power-supply line to the respective return line using LC filters comprising ferrite beads and 10µF capacitors. Filter each supply input locally with 0.1µF ceramic capacitors to the respective return lines.

Note: To maintain the dynamic performance of the *Electrical Characteristics*, ensure the voltage difference between DV_{DD}, AV_{DD}, and PV_{DD} does not exceed 150mV.

Thermal Characteristics and Packaging

Thermal Resistance

48-lead TQFP-EP:

$$\theta_{JA} = 27.6°C/W$$

Keep the device junction temperature below +125°C to meet specified electrical performance. Lower the power-supply voltage to maintain specified performance when the DAC update rate approaches 300Msps and the ambient temperature equals +85°C.

The MAX5858A is packaged in a 48-pin TQFP-EP package, providing design flexibility, increased thermal efficiency, and optimized AC performance of the DAC. The EP enables the implementation of grounding techniques, which are necessary to ensure highest performance operation.

In this package, the data converter die is attached to an EP leadframe with the back of the frame exposed at the package bottom surface, facing the PC board side of the package. This allows a solid attachment of the package to the PC board with standard infrared (IR)-flow soldering techniques. A specially created land pattern on the PC board, matching the size of the EP, ensures the proper attachment and grounding of the DAC. Designing vias* into the land area and implementing large ground planes in the PC board design achieve optimal DAC performance. Use an array of 3 × 3 (or greater) vias (0.3mm diameter per via hole and 1.2mm pitch between via holes) for this 48-pin TQFP-EP package.

Dynamic Performance Parameter Definitions

Adjacent Channel Leakage Ratio (ACLR)

Commonly used in combination with wideband code-division multiple-access (WCDMA), ACLR reflects the leakage power ratio in dB between the measured power within a channel relative to its adjacent channel. ACLR provides a quantifiable method of determining out-of-band spectral energy and its influence on an adjacent channel when a bandwidth-limited RF signal passes through a nonlinear device.

Total Harmonic Distortion (THD)

THD is the ratio of the RMS sum of all essential harmonics (within a Nyquist window) of the input signal to the fundamental itself. This can be expressed as:

$$THD = 20 \times \log\left(\sqrt{\left(V_2^2 + V_3^2 + V_4^2 ... + ... V_N^2\right)} / V_1\right)$$

where V_1 is the fundamental amplitude, and V_2 through V_N are the amplitudes of the 2nd through Nth-order harmonics.

Spurious-Free Dynamic Range (SFDR)

SFDR is the ratio of RMS amplitude of the carrier frequency (maximum signal component) to the RMS value of the next-largest spectral component. SFDR is usually measured in dBc with respect to the carrier frequency amplitude or in dB FS with respect to the DAC's full-scale range. Depending on its test condition, SFDR is observed within a predefined window or to Nyquist.

Multitone Power Ratio (MTPR)

A series of equally spaced tones are applied to the DAC with one tone removed from the center of the range. MTPR is defined as the worst-case distortion (usually a 3rd-order harmonic product of the fundamental frequencies), which appears as the largest spur at the frequency of the missing tone in the sequence. This test can be performed with any number of input tones; however, four and eight tones are among the most common test conditions for CDMA- and GSM/EDGE-type applications.

Intermodulation Distortion (IMD)

The two-tone IMD is the ratio expressed in dBc of either output tone to the worst 3rd-order (or higher) IMD products.

Static Performance Parameter Definitions

Integral Nonlinearity (INL)

Integral nonlinearity (INL) is the deviation of the values on an actual transfer function from a line drawn between the end points of the transfer function, once offset and gain errors have been nullified. For a DAC, the deviations are measured at every individual step.

Differential Nonlinearity (DNL)

Differential nonlinearity (DNL) is the difference between an actual step height and the ideal value of 1 LSB. A DNL error specification no more negative than -1 LSB guarantees monotonic transfer function.

Offset Error

Offset error is the current flowing from positive DAC output when the digital input code is set to zero. Offset error is expressed in LSBs.

*Vias connect the land pattern to internal or external copper planes.

Dual, 10-Bit, 300Msps, DAC with 4x/2x/1x Interpolation Filters and PLL

Gain Error

A gain error is the difference between the ideal and the actual full-scale output current on the transfer curve, after nullifying the offset error. This error alters the slope of the transfer function and corresponds to the same percentage error in each step. The ideal current is defined by reference voltage at V_{REFO} / I_{REF} x 32.

Settling Time

The settling time is the amount of time required from the start of a transition until the DAC output settles to its new output value to within the converter's specified accuracy.

Glitch Impulse

A glitch is generated when a DAC switches between two codes. The largest glitch is usually generated around the midscale transition, when the input pattern transitions from 011…111 to 100…000. This occurs due to timing variations between the bits. The glitch impulse is found by integrating the voltage of the glitch at the midscale transition over time. The glitch impulse is usually specified in pV-s.

Chip Information

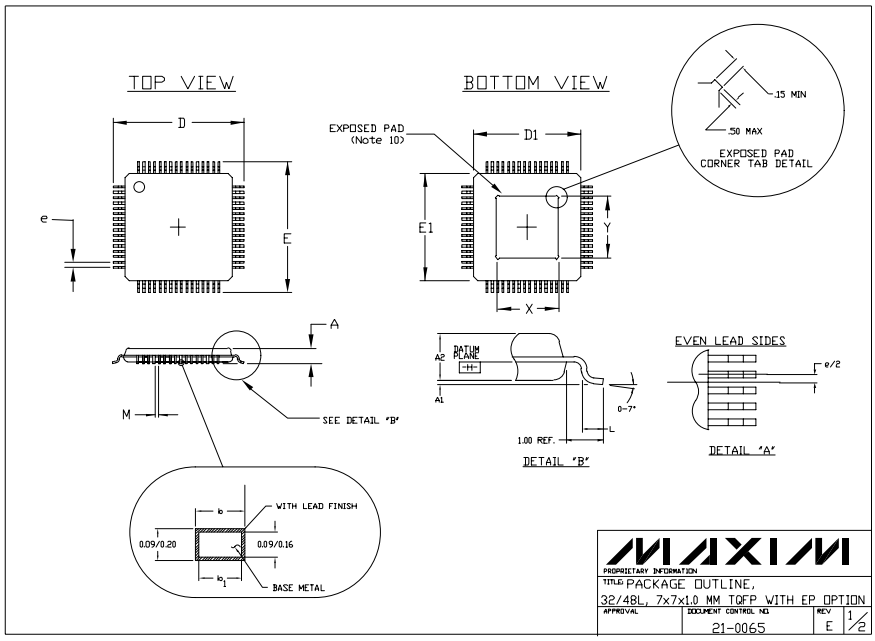
TRANSISTOR COUNT: 178,376

PROCESS: CMOS

Dual, 10-Bit, 300Msps, DAC with 4x/2x/1x Interpolation Filters and PLL

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



NOTES:
1. ALL DIMENSIONS AND TOLERANCING CONFORM TO ANSI Y14.5-1982.
2. DATUM PLANE -H- IS LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT BOTTOM OF PARTING LINE.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.254 MM ON D1 AND E1 DIMENSIONS.
4. THE TOP OF PACKAGE IS SMALLER THAN THE BOTTOM OF PACKAGE BY 0.15 MILLIMETERS.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. CONTROLLING DIMENSION: MILLIMETER.
7. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-136, VARIATIONS AC AND AE.
8. LEADS SHALL BE COPLANAR WITHIN .004 INCH.
9. EXPOSED DIE PAD SHALL BE COPLANAR WITH BOTTOM OF PACKAGE WITHIN 2 MILS (.05 MM).
10. DIMENSIONS X & Y APPLY TO EXPOSED PAD (EP) VERSIONS ONLY. SEE INDIVIDUAL PRODUCT DATASHEET TO DETERMINE IF A PRODUCT USES EXPOSED PAD PACKAGE.

SYMBOL	JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS					
	AC			AE		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A			1.20			1.20
A_1	0.05	0.10	0.15	0.05	0.10	0.15
A_2	0.95	1.00	1.05	0.95	1.00	1.05
D	9.00 BSC.			9.00 BSC.		
D_1	7.00 BSC.			7.00 BSC.		
E	9.00 BSC.			9.00 BSC.		
E_1	7.00 BSC.			7.00 BSC.		
L	0.45	0.60	0.75	0.45	0.60	0.75
M	0.15			0.14		
N	32			48		
e	0.80 BSC.			0.50 BSC.		
b	0.30	0.37	0.45	0.17	0.22	0.27
b1	0.30	0.35	0.40	0.17	0.20	0.23
*X	3.20	3.50	3.80	3.70	4.00	4.30
*Y	3.20	3.50	3.80	3.70	4.00	4.30

* EXPOSED PAD (Note 10)

MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE,
32/48L, 7x7x1.0 MM TQFP WITH EP OPTION
APPROVAL
DOCUMENT CONTROL NO.
21-0065
REV
E
2/2

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