PHC2300

Complementary enhancement mode MOS transistors

Rev. 05 — 24 February 2011 Product data sheet

1. Product profile

1.1 General description

One N-channel and one P-channel enhancement mode Field-Effect Transistor (FET) in a plastic package. This product is designed and qualified for use in computing, communications, consumer and industrial applications only.

1.2 Features and benefits

- Suitable for high frequency applications due to fast switching characteristics

1.3 Applications

- High-speed line drivers
- Line transformer drivers
- Relay drivers
- Universal line interface in telephone sets

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 150$ °C; N-channel		-	-	300	V
		$T_j \geq 25$ °C; $T_j \leq 150$ °C; P-channel		-	-	-300	V
I_D	drain current	T_{sp} = 80 °C; N-channel	[1]	-	-	340	mA
		T_{sp} = 80 °C; P-channel	[1]	-	-	-235	mA
P_{tot}	total power dissipation	T_{sp} = 80 °C	[2]	-	-	1.6	W
Static characteristics							
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 170 mA; T_j = 25 °C; N-channel		-	-	6	Ω
		V_{GS} = -10 V; I_D = -115 mA; T_j = 25 °C; P-channel		-	-	17	Ω

Table 1. Quick reference data *...continued*

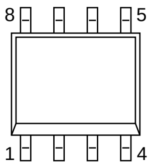
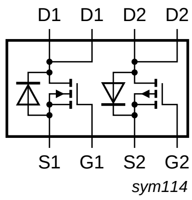
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Dynamic characteristics						
Q_{GD}	gate-drain charge	V_{GS} = -10 V; I_D = -115 mA; V_{DS} = -50 V; T_j = 25 °C; P-channel	-	674	-	pC
		V_{GS} = 10 V; I_D = 170 mA; V_{DS} = 50 V; T_j = 25 °C; N-channel	-	1385	-	pC

[1] Solder point temperature is the temperature at the soldering point of the drain leads.

[2] Maximum permissible dissipation per MOS transistor (both devices may thus be loaded up to 1.6 W at the same time).

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source1	 SOT96-1 (SO8)	
2	G1	gate1		
3	S2	source2		
4	G2	gate2		
5	D2	drain2		
6	D2	drain2		
7	D1	drain1		
8	D1	drain1		

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PHC2300	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

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4. Limiting values

Table 4. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 150$ °C; N-channel		-	300	V
		$T_j \geq 25$ °C; $T_j \leq 150$ °C; P-channel		-	-300	V
V_{GS}	gate-source voltage			-20	20	V
I_D	drain current	$T_{sp} = 80$ °C; N-channel	[1]	-	340	mA
		$T_{sp} = 80$ °C; P-channel	[1]	-	-235	mA
I_{DM}	peak drain current	$T_{sp} = 25$ °C; pulsed; N-channel	[2]	-	1.4	A
		$T_{sp} = 25$ °C; pulsed; P-channel	[2]	-	-0.9	A
P_{tot}	total power dissipation	$T_{sp} = 80$ °C	[3]	-	1.6	W
		$T_{amb} = 25$ °C	[4]	-	1.8	W
		$T_{amb} = 25$ °C	[5]	-	0.9	W
		$T_{amb} = 25$ °C	[6]	-	1.2	W
T_{stg}	storage temperature			-55	150	°C
T_j	junction temperature			-55	150	°C

[1] Solder point temperature is the temperature at the soldering point of the drain leads.

[2] Pulse width and duty cycle limited by maximum junction temperature.

[3] Maximum permissible dissipation per MOS transistor (both devices may thus be loaded up to 1.6 W at the same time).

[4] Maximum permissible dissipation per MOS transistor. Value based on a printed-circuit board with an $R_{th(a-tp)}$ (ambient to tie-point) of 27.5 K/W.

[5] Maximum permissible dissipation per MOS transistor. Value based on a printed-circuit board with an $R_{th(a-tp)}$ (ambient to tie-point) of 90 K/W.

[6] Maximum permissible dissipation if only one MOS transistor dissipates. Value based on a printed-circuit board with an $R_{th(a-tp)}$ (ambient to tie-point) of 90 K/W.

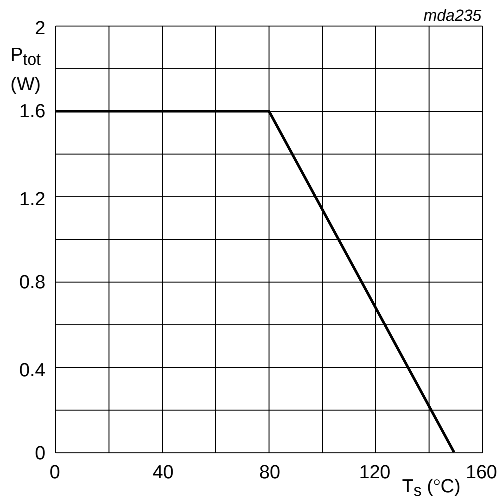
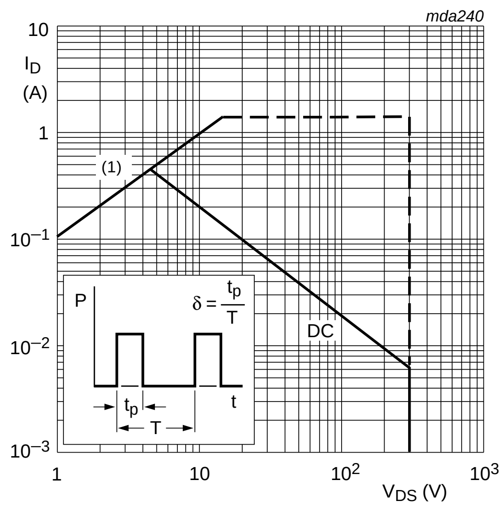


Fig 1. Power derating curve



δ = 0.01; $T_{sp} = 80$ °C.

(1) R_{DSon} limitation.

Fig 2. SOAR; N-channel

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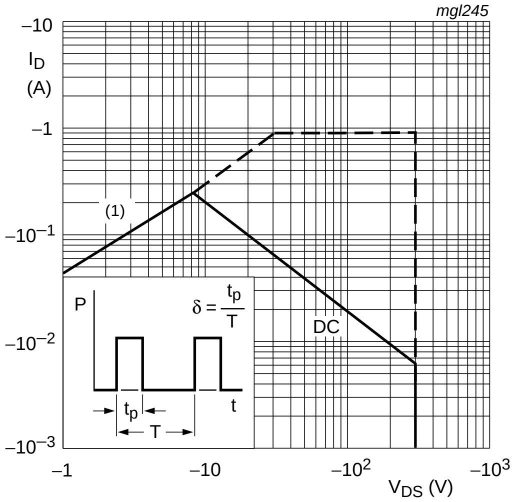


$\delta = 0.01$; $T_{sp} = 80$ °C.

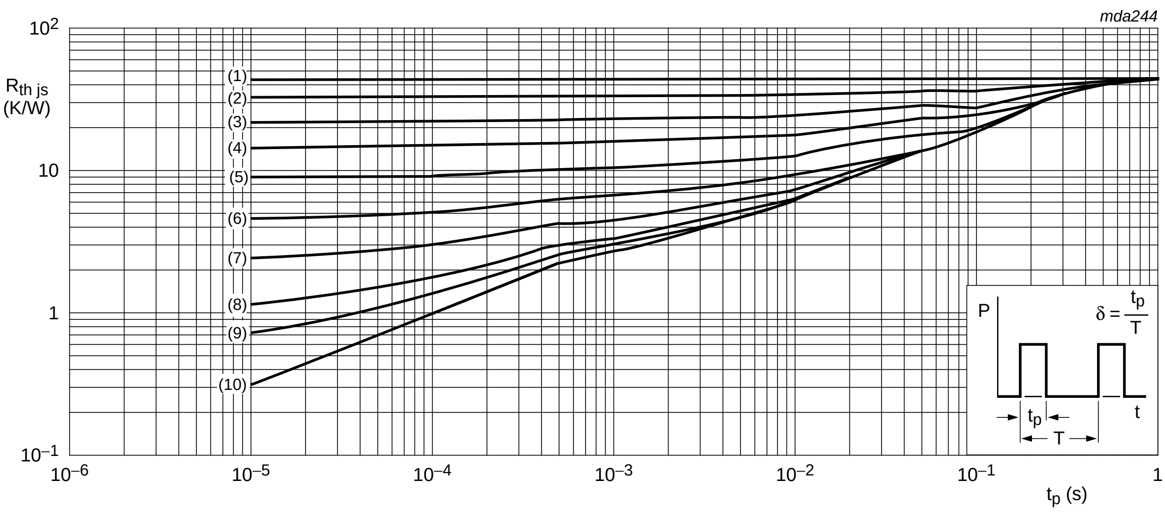
(1) R_{DSon} limitation.

Fig 3. SOAR; P-channel

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point		-	-	43	K/W



(1) $\delta = 1.00$. (2) $\delta = 0.75$. (3) $\delta = 0.5$. (4) $\delta = 0.33$. (5) $\delta = 0.2$.

(6) $\delta = 0.1$. (7) $\delta = 0.05$. (8) $\delta = 0.02$. (9) $\delta = 0.01$. (10) $\delta = 0$.

Fig 4. Transient thermal resistance from junction to soldering point as a function of pulse time for N- and P-channel; typical values

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6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = -10 µA; V_{GS} = 0 V; T_j = 25 °C; P-channel	-300	-	-	V
		I_D = 10 µA; V_{GS} = 0 V; T_j = 25 °C; N-channel	300	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; T_j = 25 °C; N-channel	0.8	-	2	V
		I_D = -1 mA; V_{DS} = V_{GS}; T_j = 25 °C; P-channel	-0.8	-	-2	V
I_{DSS}	drain leakage current	V_{DS} = -240 V; V_{GS} = 0 V; T_j = 25 °C; P-channel	-	-	-100	nA
		V_{DS} = 240 V; V_{GS} = 0 V; T_j = 25 °C; N-channel	-	-	100	nA
I_{GSS}	gate leakage current	V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 °C; N-channel	-	-	100	nA
		V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25 °C; N-channel	-	-	100	nA
		V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 °C; P-channel	-	-	100	nA
		V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25 °C; P-channel	-	-	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 170 mA; T_j = 25 °C; N-channel	-	-	6	Ω
		V_{GS} = -10 V; I_D = -115 mA; T_j = 25 °C; P-channel	-	-	17	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	I_D = 170 mA; V_{DS} = 50 V; V_{GS} = 10 V; T_j = 25 °C; N-channel	-	6240	-	pC
		I_D = -115 mA; V_{DS} = -50 V; V_{GS} = -10 V; T_j = 25 °C; P-channel	-	2137	-	pC
Q_{GS}	gate-source charge	I_D = 170 mA; V_{DS} = 50 V; V_{GS} = 10 V; T_j = 25 °C; N-channel	-	226	-	pC
		I_D = -115 mA; V_{DS} = -50 V; V_{GS} = -10 V; T_j = 25 °C; P-channel	-	68	-	pC
Q_{GD}	gate-drain charge	I_D = -115 mA; V_{DS} = -50 V; V_{GS} = -10 V; T_j = 25 °C; P-channel	-	674	-	pC
		I_D = 170 mA; V_{DS} = 50 V; V_{GS} = 10 V; T_j = 25 °C; N-channel	-	1385	-	pC
C_{iss}	input capacitance	V_{DS} = 50 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C; N-channel	-	102	-	pF
		V_{DS} = -50 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C; P-channel	-	45	-	pF
C_{oss}	output capacitance	V_{DS} = 50 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C; N-channel	-	15	-	pF
		V_{DS} = -50 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C; P-channel	-	15	-	pF

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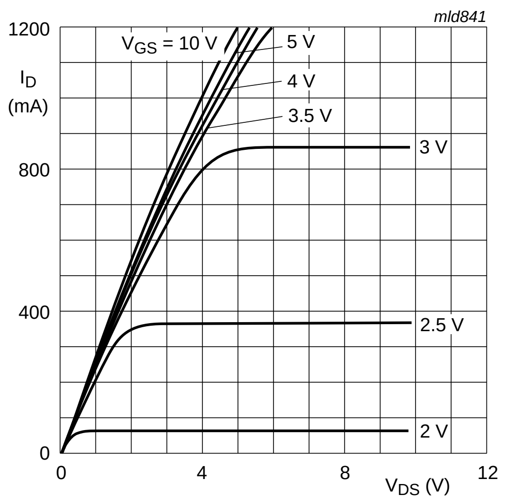
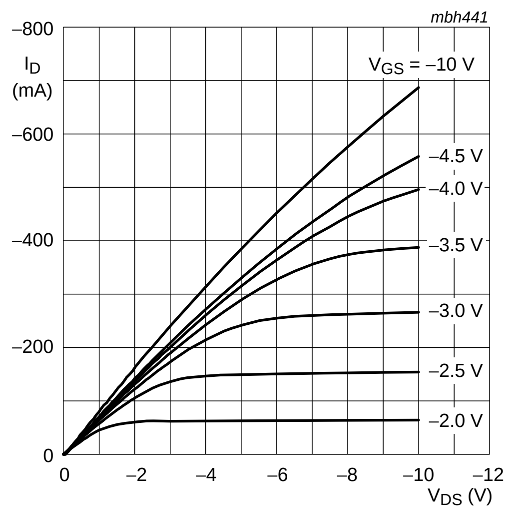
Table 6. Characteristics *...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{rss}	reverse transfer capacitance	V_{DS} = 50 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C; N-channel	-	7.3	-	pF
		V_{DS} = -50 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C; P-channel	-	3	-	pF
t_{on}	turn-on time	V_{DS} = 50 V; V_{GS} = 10 V; I_D = 170 mA; T_j = 25 °C; N-channel	-	7	12	ns
		V_{DS} = -50 V; V_{GS} = -10 V; I_D = -115 mA; T_j = 25 °C; P-channel	-	4	10	ns
t_{off}	turn-off time	V_{DS} = 50 V; V_{GS} = 10 V; T_j = 25 °C; I_D = 170 mA; N-channel	-	53	65	ns
		V_{DS} = -50 V; V_{GS} = -10 V; T_j = 25 °C; I_D = -115 mA; P-channel	-	25	35	ns



T_{amb} = 25 °C; t_p = 80 µs; δ = 0.

Fig 5. Output characteristics: drain current as a function of drain-source voltage; N-channel; typical values



T_{amb} = 25 °C; t_p = 80 µs; δ = 0.

Fig 6. Output characteristics: drain current as a function of drain-source voltage; P-channel; typical values

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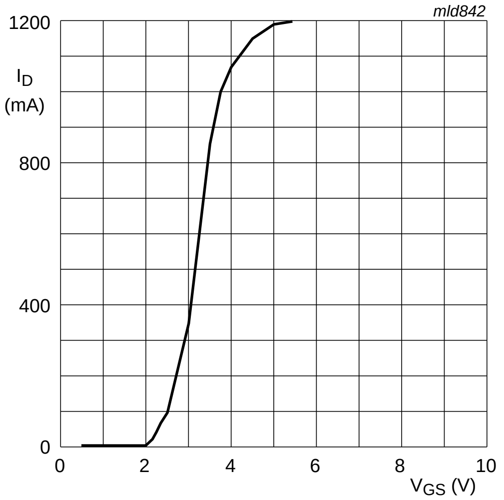
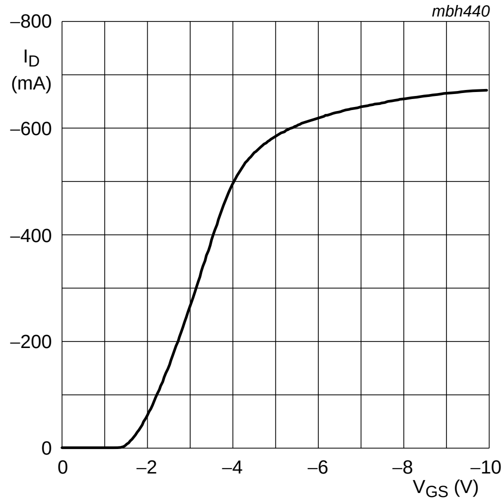


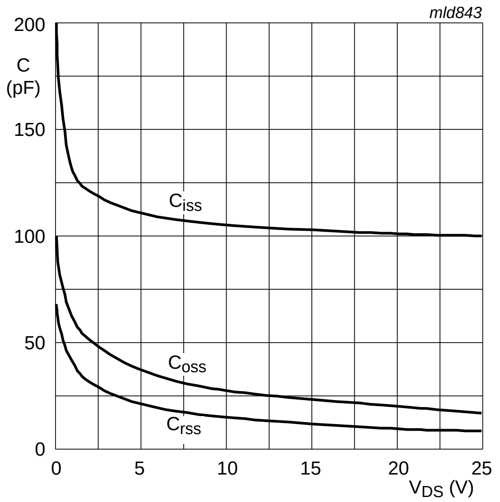
V_{DS} = 10 V; T_{amb} = 25 °C; t_p = 80 μs; δ = 0.

Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; N-channel; typical values



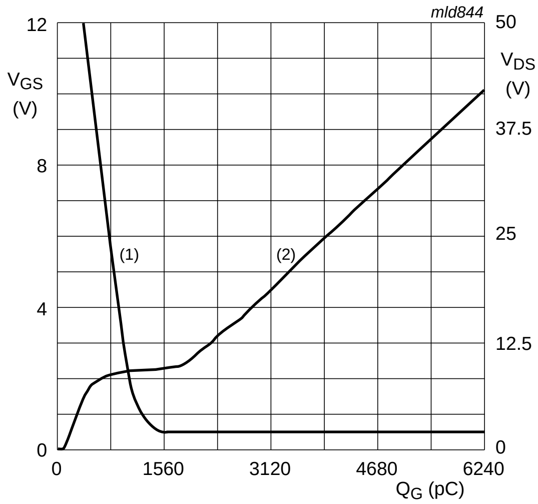
V_{DS} = -10 V; T_{amb} = 25 °C; t_p = 80 μs; δ = 0.

Fig 8. Transfer characteristics: drain current as a function of gate-source voltage; P-channel; typical values



$T_{amb} = 25°C; f = 1MHz$

Fig 9. Input, output and reverse transfer capacitances as a function of drain-source voltage; N-channel; typical values



V_{DS} = 50 V; I_D = 170 mA; T_{amb} = 25 °C.

(1) V_{DS}

(2) V_{GS}

Fig 10. Gate-source voltage and drain-source voltage as a function of gate charge; N-channel typical values

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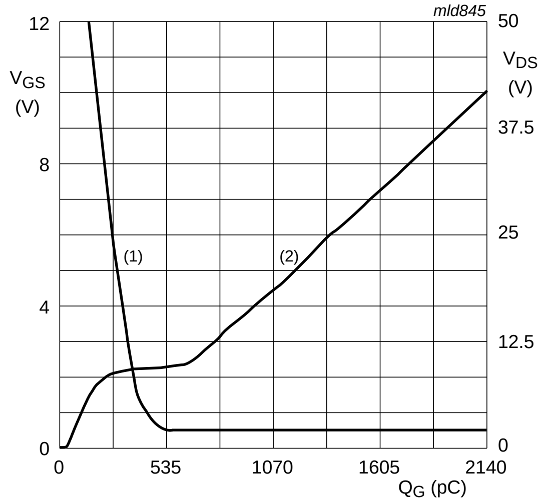
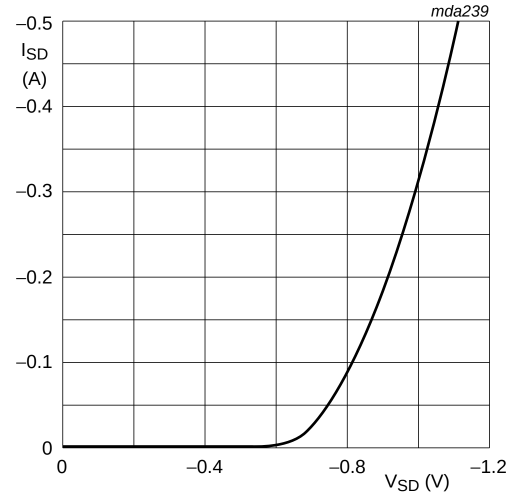


V_{DS} = -50 V; I_D = -115 mA; T_{amb} = 25 °C.

(1) V_{DS}

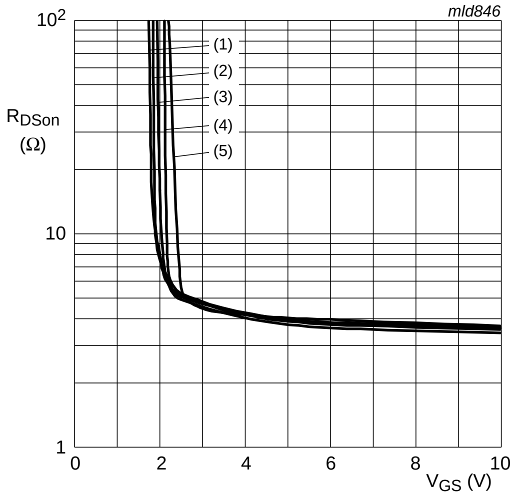
(2) V_{GS}

Fig 11. Gate-source voltage and drain-source voltage as a function of gate charge; P-channel typical values



$V_{GD} = 0V$

Fig 12. Source current as a function of source-drain voltage; P-channel typical values



$V_{DS} \geq I_D \times R_{DSon}$; T_{amb} = 25 °C; t_p = 300 μs; δ = 0.

(1) I_D = 10 mA.

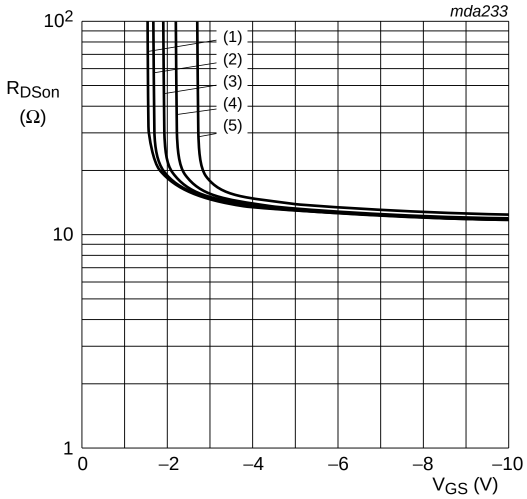
(2) I_D = 20 mA.

(3) I_D = 50 mA.

(4) I_D = 100 mA.

(5) I_D = 200 mA.

Fig 13. Drain-source on-state resistance as a function of gate-source voltage; N-channel typical values



$V_{DS} \geq I_D \times R_{DSon}$; T_{amb} = 25 °C; t_p = 300 μs; δ = 0.

(1) I_D = -10 mA.

(2) I_D = -20 mA.

(3) I_D = -50 mA.

(4) I_D = -100 mA.

(5) I_D = -200 mA.

Fig 14. Drain-source on-state resistance as a function of gate-source voltage; P-channel typical values

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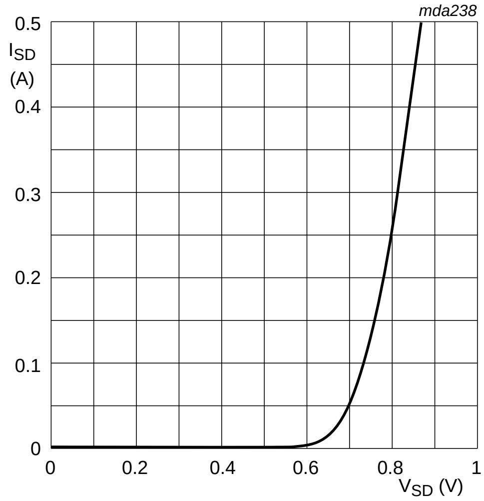
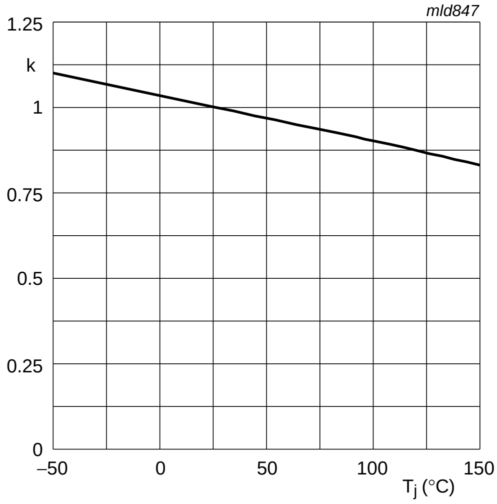


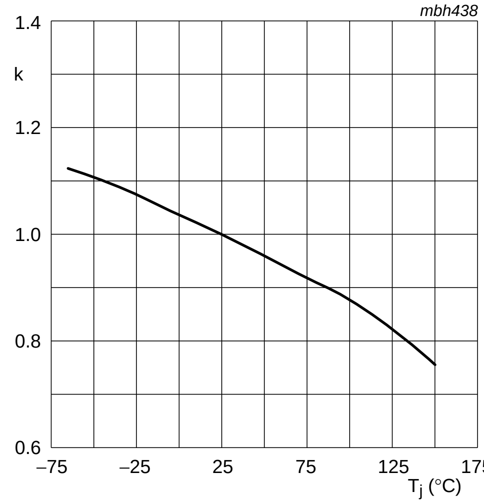
$V_{GD} = 0V$

Fig 15. Source-drain current as a function of source-drain diode voltage; N-channel; typical values



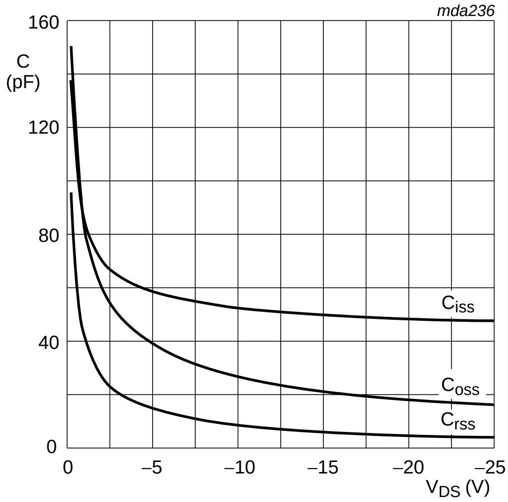
$V_{DS} = V_{GS}$; $I_D = 1$ mA.

Fig 16. Temperature coefficient of gate-source threshold voltage as a function temperature; N-channel; typical values



$V_{DS} = V_{GS}$; $I_D = -1$ mA.

Fig 17. Temperature coefficient of gate-source threshold voltage as a function temperature; P-channel; typical values



$T_{amb} = 25°C; f = 1MHz$

Fig 18. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

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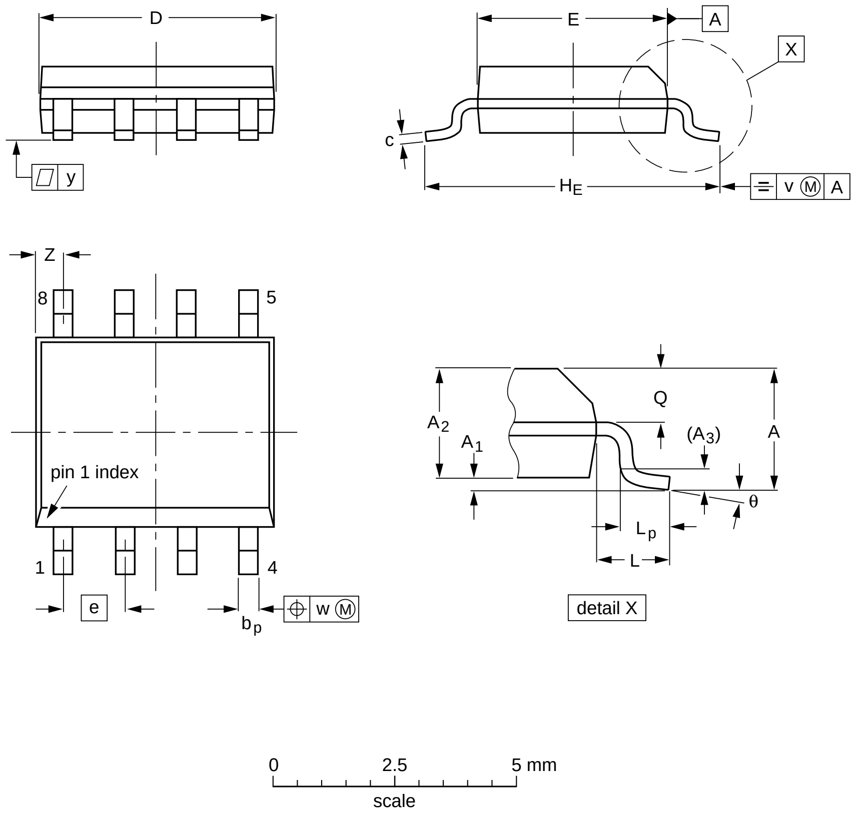
7. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D[1]	E[2]	e	H_E	L	L_p	Q	v	w	y	Z[1]	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT96-1	076E03	MS-012				~~99-12-27~~ 03-02-18

Fig 19. Package outline SOT96-1 (SO8)

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8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PHC2300 v.5	20110224	Product data sheet	-	PHC2300 v.4
Modifications:	• Various changes to content.			
PHC2300 v.4	20101216	Product data sheet	-	PHC2300 v.3

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9. Legal information

9.1 Data sheet status

Document status [1] [2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nexperia.com.

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For sales office addresses, please send an email to: salesaddresses@nexperia.com

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11. Contents

1 Product profile 1
1.1 General description 1
1.2 Features and benefits 1
1.3 Applications 1
1.4 Quick reference data 1
2 Pinning information 2
3 Ordering information 2
4 Limiting values 3
5 Thermal characteristics 4
6 Characteristics 5
7 Package outline 10
8 Revision history 11
9 Legal information 12
9.1 Data sheet status 12
9.2 Definitions 12
9.3 Disclaimers 12
9.4 Trademarks 13
10 Contact information 13

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