

Dominant Mode Multipoint Transceiver

Check for Samples: [DS36277](#)

FEATURES

- **FAILSAFE Receiver, RO = HIGH for:**
 - OPEN Inputs
 - Terminated Inputs
 - SHORTED Inputs
- **Optimal for Use in SAE J1708 Interfaces**
- **Compatible with Popular Interface Standards:**
 - TIA/EIA-485 and TIA/EIA-422-A
 - CCITT Recommendation V.11
- **Bi-Directional Transceiver**
 - Designed for Multipoint Transmission
- **Wide Bus Common Mode Range**
 - (–7V to +12V)
- **Available in PDIP and SOIC Packages**

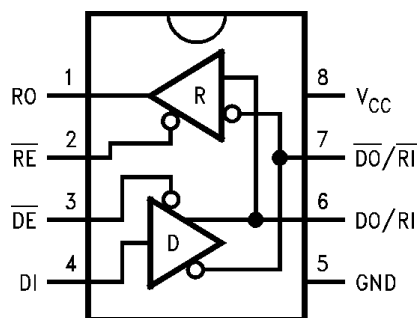
DESCRIPTION

The DS36277 Dominant Mode Multipoint Transceiver is designed for use on bi-directional differential busses. It is optimal for use on Interfaces that utilize Society of Automotive Engineers (SAE) J1708 Electrical Standard.

The device is similar to standard TIA/EIA-485 transceivers, but differs in enabling scheme. The Driver's Input is normally externally tied LOW, thus providing only two states: Active (LOW), or Disabled (OFF). When the driver is active, the dominant mode is LOW, conversely, when the driver is disabled, the bus is pulled HIGH by external bias resistors.

The receiver provides a FAILSAFE feature that ensures a known output state when the Interface is in the following conditions: Floating Line, Idle Line (no active drivers), and Line Fault Conditions (open or short). The receiver output is HIGH for the following conditions: Open Inputs, Terminated Inputs (50Ω), or Shorted Inputs. FAILSAFE is a highly desirable feature when the transceivers are used with Asynchronous Controllers such as UARTs.

Connection and Logic Diagram



See Package Number D (R-PDSO-G8)
or
P (R-PDIP-T8)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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Truth Table

Driver			
Inputs		Outputs	
\overline{DE}	DI	DO/RI	$\overline{DO} / \overline{RI}$
L	L	L	H
L	H	H	L
H	X	Z	Z
Receiver			
Inputs		Output	
\overline{RE}	DO/RI- $\overline{DO} / \overline{RI}$	RO	
L	≥ 0 mV	H	
L	≤ -500 mV	L	
L	SHORTED	H	
L	OPEN	H	
H	X	Z	



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings⁽¹⁾⁽²⁾

		Value	Unit
Supply Voltage (V_{CC})		7	V
Input Voltage (\overline{DE} , \overline{RE} , and DI)		5.5	V
Driver Output Voltage/Receiver Input Voltage		-10V to +15	V
Receiver Output Voltage (RO)		5.5	V
Maximum Package Power Dissipation @ +25°C	P Package (derate 9.3 mW/°C above +25°C)	1168	mW
	D Package (derate 5.8 mW/°C above +25°C)	726	mW
Storage Temperature Range		-65°C to +150	°C
Lead Temperature (Soldering 4 sec.)		260	°C
ESD Rating (HBM, 1.5 kΩ, 100 pF)		7.0	kV

- (1) "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be specified. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}	4.75	5.25	V
Bus Voltage	-7	+12	V
Operating Temperature (T_A) DS36277T	-40	+85	°C

Electrical Characteristics⁽¹⁾⁽²⁾

Over recommended Supply Voltage and Operating Temperature ranges, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units			
DRIVER CHARACTERISTICS									
V_{OD}	Differential Output Voltage	$I_O = 0$ mA (No Load)	1.5	3.6	6	V			
V_{oDO}	Output Voltage	$I_O = 0$ mA (Output to GND)	0		6	V			
$V_{o\overline{DO}}$	Output Voltage		0		6	V			
V_{T1}	Differential Output Voltage (Termination Load)	$R_L = 54\Omega$ (485)	(Figure 1)		1.3	2.2	5.0	V	
		$R_L = 100\Omega$ (422)			1.7	2.6	5.0	V	
ΔV_{T1}	Balance of V_{T1} $ V_{T1} - \overline{V_{T1}} $	$R_L = 54\Omega$	See ⁽³⁾		-0.2		0.2	V	
		$R_L = 100\Omega$			-0.2		0.2	V	
V_{OS}	Driver Common Mode Output Voltage	$R_L = 54\Omega$	(Figure 1)		0	2.5	3.0	V	
		$R_L = 100\Omega$			0	2.5	3.0	V	
ΔV_{OS}	Balance of V_{OS} $ V_{OS} - \overline{V_{OS}} $	$R_L = 54\Omega$	See ⁽³⁾		-0.2		0.2	V	
		$R_L = 100\Omega$			-0.2		0.2	V	
V_{OH}	Output Voltage High	$I_{OH} = -22$ mA	(Figure 2)		2.7	3.7		V	
V_{OL}	Output Voltage Low	$I_{OL} = +22$ mA			1.3	2		V	
I_{OSD}	Driver Short-Circuit Output Current	$V_O = +12$ V	(Figure 3)			92	290	mA	
		$V_O = -7$ V				-187	-290	mA	
RECEIVER CHARACTERISTICS									
V_{TH}	Differential Input High Threshold Voltage ⁽⁴⁾	$V_O = V_{OH}$, $I_O = -0.4$ mA $-7V \leq V_{CM} \leq +12V$			-0.150	0		V	
V_{TL}	Differential Input Low Threshold Voltage ⁽⁴⁾	$V_O = V_{OL}$, $I_O = 8.0$ mA $-7V \leq V_{CM} \leq +12V$	-0.5	-0.230				V	
V_{HST}	Hysteresis ⁽⁵⁾	$V_{CM} = 0$ V			80			mV	
I_{IN}	Line Input Current ($V_{CC} = 4.75$ V, 5.25V, 0V)	Other Input = 0V $\overline{DE} = V_{IH}$ ⁽⁶⁾	$V_I = +12$ V		0.5	1.5		mA	
			$V_I = -7$ V		-0.5	-1.5		mA	
I_{OSR}	Short Circuit Current	$V_O = 0$ V	RO		-15	-32	-85	mA	
I_{OZ}	TRI-STATE Leakage Current	$V_O = 0.4$ to 2.4V			-20	1.4	+20	μ A	
V_{OH}	Output High Voltage (Figure 12)	$V_{ID} = 0$ V, $I_{OH} = -0.4$ mA			2.3	3.7		V	
		$V_{ID} = OPEN$, $I_{OH} = -0.4$ mA			2.3	3.7		V	
V_{OL}	Output Low Voltage (Figure 12)	$V_{ID} = -0.5$ V, $I_{OL} = +8$ mA				0.3	0.7		V
		$V_{ID} = -0.5$ V, $I_{OL} = +16$ mA				0.3	0.8		V
R_{IN}	Input Resistance			10	20			k Ω	
DEVICE CHARACTERISTICS									
V_{IH}	High Level Input Voltage		\overline{DE} , \overline{RE} , or DI	2.0		V_{CC}		V	
V_{IL}	Low Level Input Voltage			GND		0.8			V
I_{IH}	High Level Input Current	$V_{IH} = 2.4$ V					20		μ A
I_{IL}	Low Level Input Current	$V_{IL} = 0.4$ V					-100		μ A
V_{CL}	Input Clamp Voltage	$I_{CL} = -18$ mA				-0.7	-1.5		V
I_{CC}	Output Low Voltage	$\overline{DE} = 0$ V, $\overline{RE} = 0$ V, DI = 0V				39	60		mA
I_{CCR}	Supply Current (No Load)	$\overline{DE} = 3$ V, $\overline{RE} = 0$ V, DI = 0V			24	50		mA	
		$\overline{DE} = 0$ V, $\overline{RE} = 3$ V, DI = 0V			40	75		mA	
		$\overline{DE} = 3$ V, $\overline{RE} = 3$ V, DI = 0V			27	45		mA	

(1) Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground unless otherwise specified.

(2) All typicals are given for $V_{CC} = 5.0$ V and $T_A = +25^\circ$ C.

(3) $\Delta |V_{T1}|$ and $\Delta |V_{OS}|$ are changes in magnitude of V_{T1} and V_{OS} , respectively, that occur when the input changes state.

(4) Threshold parameter limits specified as an algebraic value rather than by magnitude.

(5) Hysteresis defined as $V_{HST} = V_{TH} - V_{TL}$.

(6) I_{IN} includes the receiver input current and driver TRI-STATE leakage current.

Switching Characteristics⁽¹⁾

Over recommended Supply Voltage and Operating Temperature ranges, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRIVER CHARACTERISTICS						
t_{PLHD}	Diff. Prop. Delay Low to High	$R_L = 54\Omega$	8	17	60	ns
t_{PHLD}	Diff. Prop. Delay High to Low	$C_L = 50\text{ pF}$	8	19	60	ns
t_{SKD}	Diff. Skew ($ t_{PLHD} - t_{PHLD} $)	$C_D = 50\text{ pF}$		2	10	ns
t_r	Diff. Rise Time	(Figure 4 and Figure 5)		11	60	ns
t_f	Diff. Fall Time			11	60	ns
t_{PLH}	Prop. Delay Low to High	$R_L = 27\Omega, C_L = 15\text{ pF}$ (Figure 6 and Figure 7)		22	85	ns
t_{PHL}	Prop. Delay High to Low			25	85	ns
t_{PZH}	Enable Time Z to High	$R_L = 110\Omega$ $C_L = 50\text{ pF}$ (Figure 8 – Figure 11)		25	60	ns
t_{PZL}	Enable Time Z to Low			30	60	ns
t_{PHZ}	Disable Time High to Z			16	60	ns
t_{PLZ}	Disable Time Low to Z			11	60	ns
RECEIVER CHARACTERISTICS						
t_{PLH}	Prop. Delay Low to High	$V_{ID} = -1.5\text{V to } +1.5\text{V}$ $C_L = 15\text{ pF}$ (Figure 13 and Figure 14)	15	37	90	ns
t_{PHL}	Prop. Delay High to Low		15	43	90	ns
t_{SK}	Skew ($ t_{PLH} - t_{PHL} $)			6	15	ns
t_{PZH}	Enable Time Z to High	$C_L = 15\text{ pF}$ (Figure 15 and Figure 16)		12	60	ns
t_{PZL}	Enable Time Z to Low			28	60	ns
t_{PHZ}	Disable Time High to Z			20	60	ns
t_{PLZ}	Disable Time Low to Z			10	60	ns

(1) All typicals are given for $V_{CC} = 5.0\text{V}$ and $T_A = +25^\circ\text{C}$.

PARAMETER MEASUREMENT INFORMATION

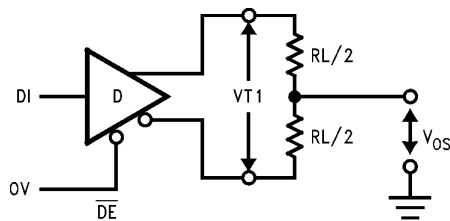


Figure 1. Driver V_{T1} and V_{OS} Test Circuit

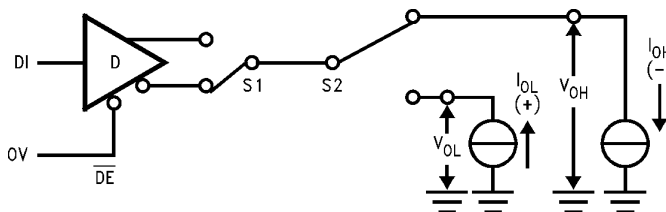


Figure 2. Driver V_{OH} and V_{OL} Test Circuit

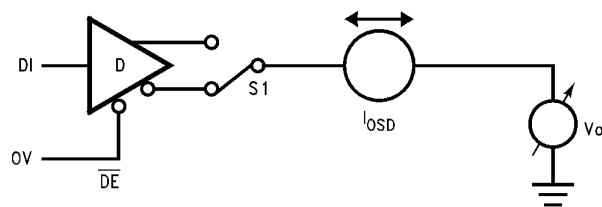
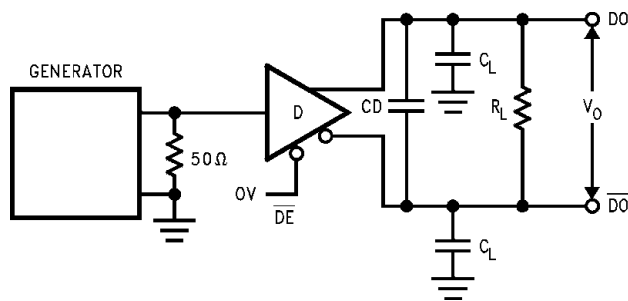


Figure 3. Driver Short Circuit Test Circuit



C_L includes probe and stray capacitance

The input pulse is supplied by a generator having the following characteristics: $f=1.0$ MHz, 50% duty cycle, T_r and $t_f < 6.0$ ns, $Z_o=50\Omega$

Figure 4. Driver Differential Propagation Delay and Transition Time Test Circuit

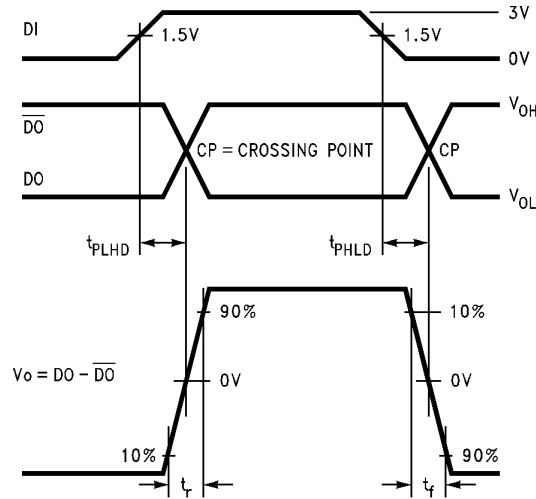
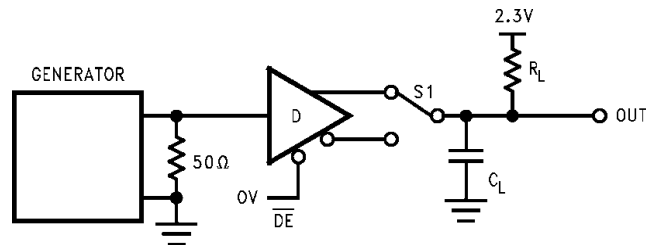


Figure 5. Driver Differential Propagation Delays and Transition Times



C_L includes probe and stray capacitance
 The input pulse is supplied by a generator having the following characteristics: $f=1.0$ MHz, 50% duty cycle, T_r and $t_f < 6.0$ ns, $Z_o=50\Omega$

Figure 6. Driver Propagation Delay Test Circuit

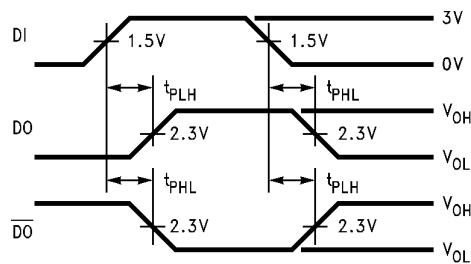
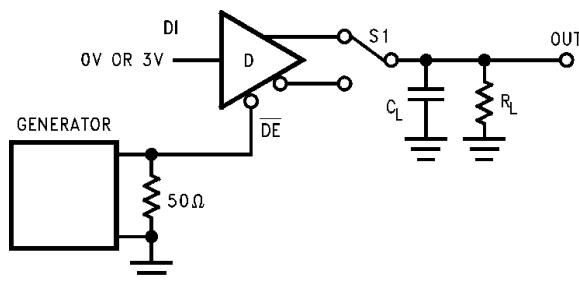


Figure 7. Driver Propagation Delays



S1 to \overline{DO} for DI = 3V
 S1 to \overline{DO} for DI = 0V
 C_L includes probe and stray capacitance
 The input pulse is supplied by a generator having the following characteristics: $f=1.0$ MHz, 50% duty cycle, T_r and $t_f < 6.0$ ns, $Z_o=50\Omega$

Figure 8. Driver TRI-STATE Test Circuit (t_{PZH} , t_{PHZ})

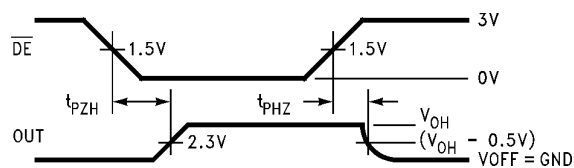
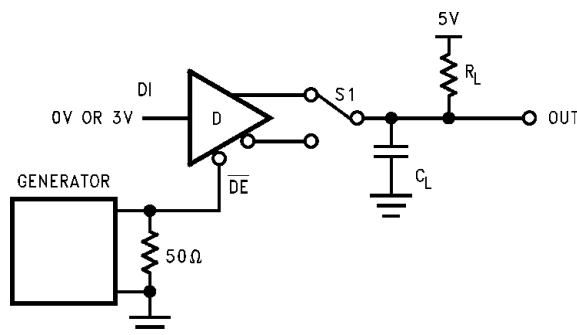


Figure 9. Driver TRI-STATE Delays (t_{PZH} , t_{PHZ})



S1 to \overline{DO} for DI = 0V
 S1 to \overline{DO} for DI = 3V
 C_L includes probe and stray capacitance
 The input pulse is supplied by a generator having the following characteristics: $f=1.0$ MHz, 50% duty cycle, T_r and $t_f < 6.0$ ns, $Z_o=50\Omega$

Figure 10. Driver TRI-STATE Test Circuit (t_{PZL} , t_{PLZ})

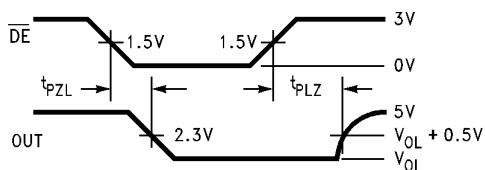


Figure 11. Driver TRI-STATE Delays (t_{PZL} , t_{PLZ})

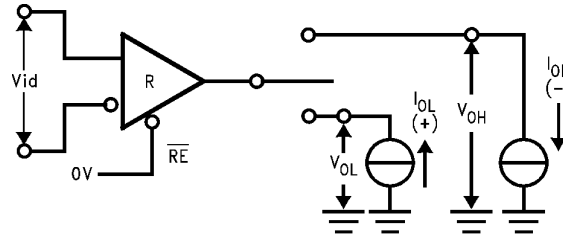
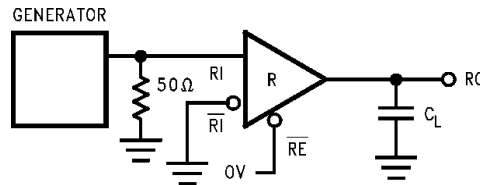


Figure 12. Receiver V_{OH} and V_{OL}



C_L includes probe and stray capacitance

The input pulse is supplied by a generator having the following characteristics: $f=1.0$ MHz, 50% duty cycle, T_r and $t_f < 6.0$ ns, $Z_o=50\Omega$

Figure 13. Receiver Propagation Delay Test Circuit

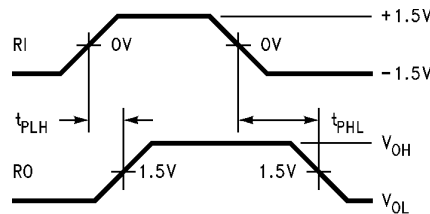
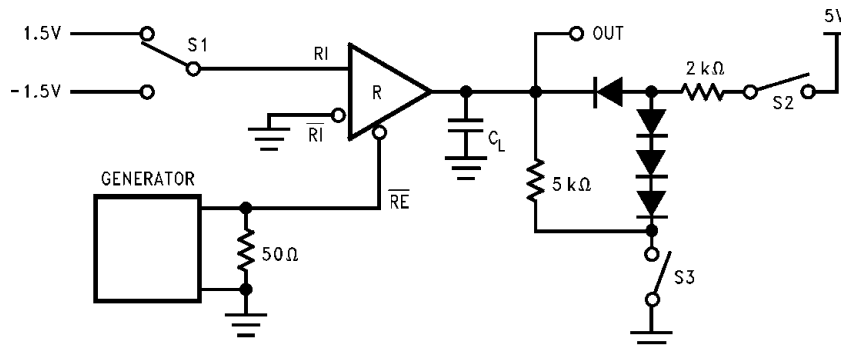


Figure 14. Receiver Propagation Delays



C_L includes probe and stray capacitance

The input pulse is supplied by a generator having the following characteristics: $f=1.0$ MHz, 50% duty cycle, T_r and $t_f < 6.0$ ns, $Z_o=50\Omega$

Diodes are 1N916 or equivalent.

Figure 15. Receiver TRI-STATE Delay Test Circuit

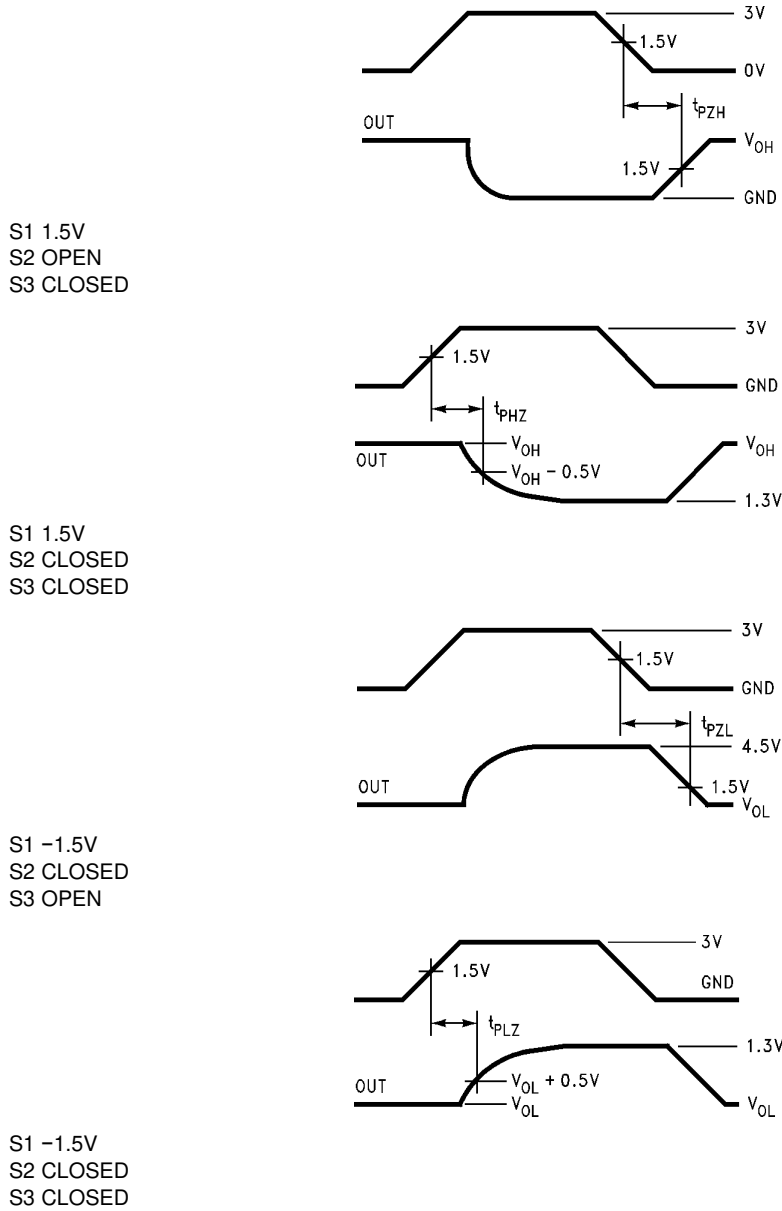


Figure 16. Receiver Enable and Disable Timing

Typical Performance Characteristics

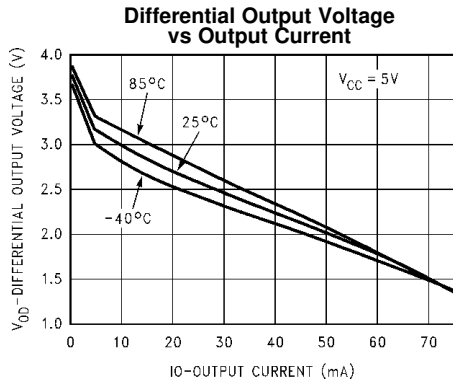


Figure 17.

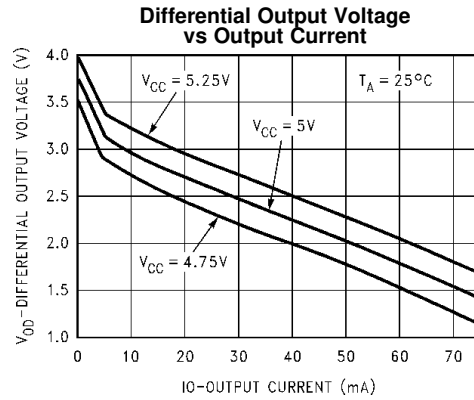


Figure 18.

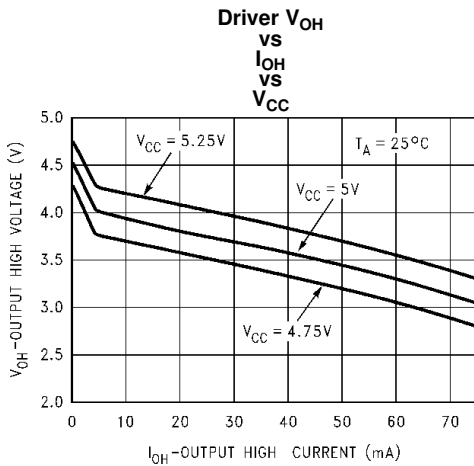


Figure 19.

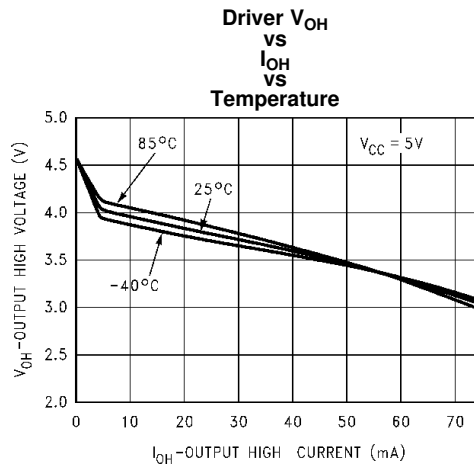


Figure 20.

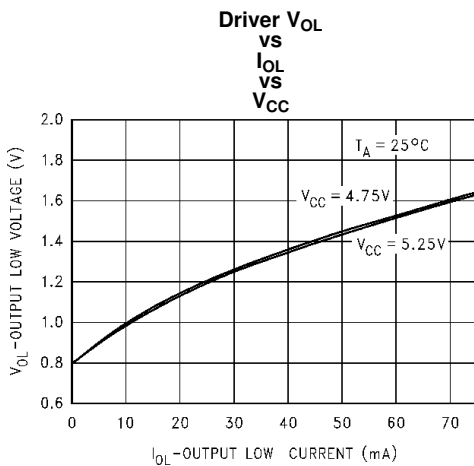


Figure 21.

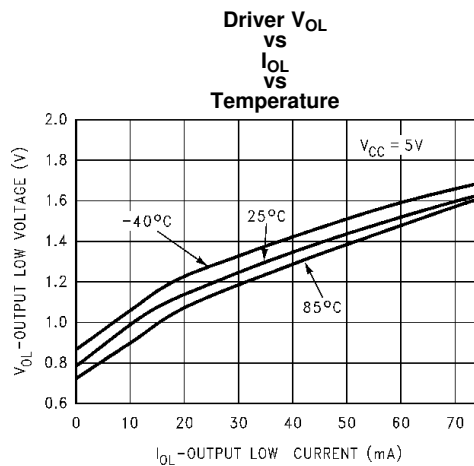
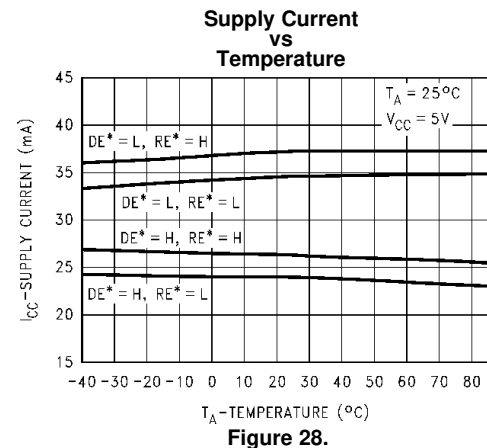
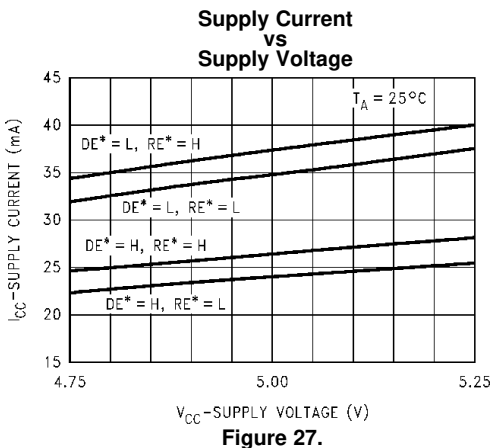
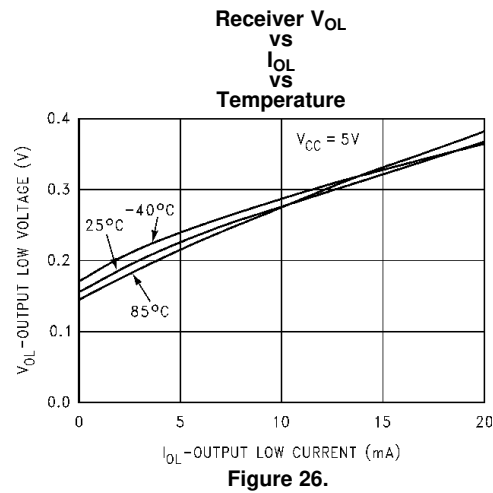
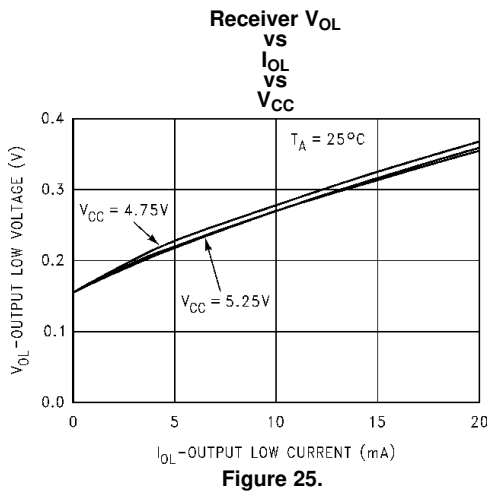
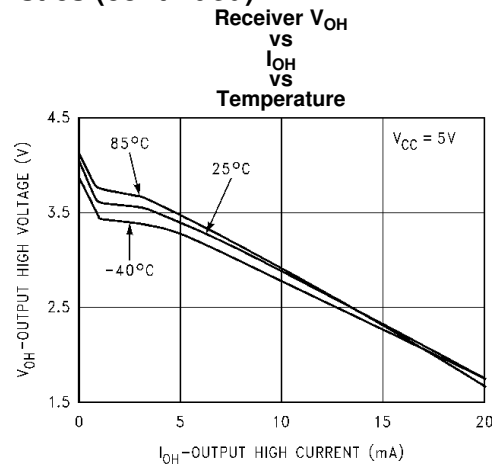
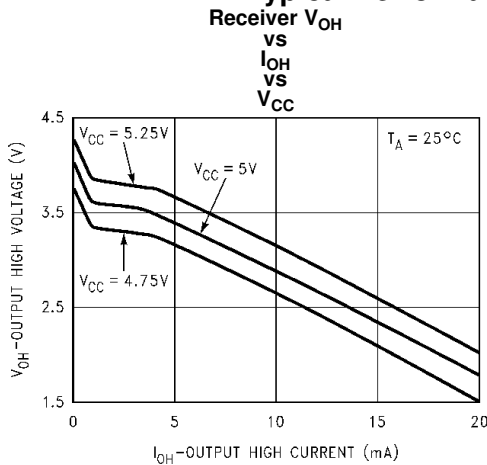


Figure 22.

Typical Performance Characteristics (continued)



Typical Performance Characteristics (continued)

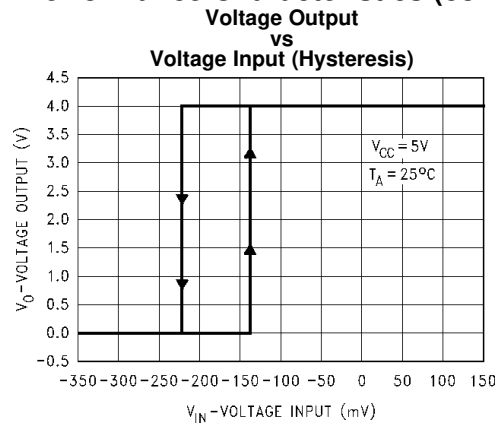


Figure 29.

TYPICAL APPLICATIONS INFORMATION

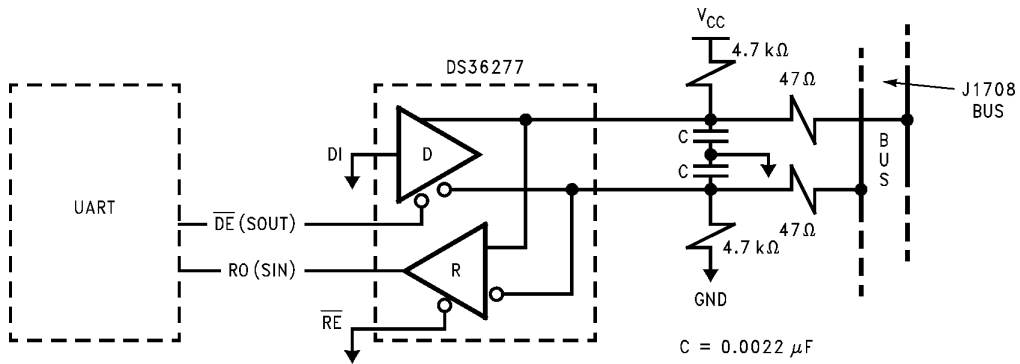


Figure 30. SAE J1708 Node with External Bias Resistors and Filters

REVISION HISTORY

Changes from Revision D (April 2013) to Revision E	Page
• Changed layout of National Data Sheet to TI format	12

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS36277TMX/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	DS362 77TM	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

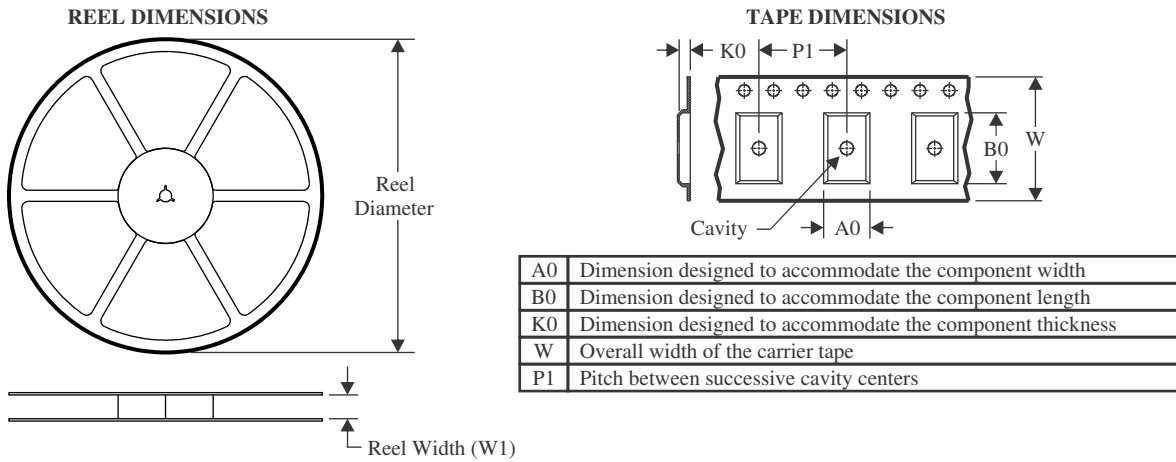
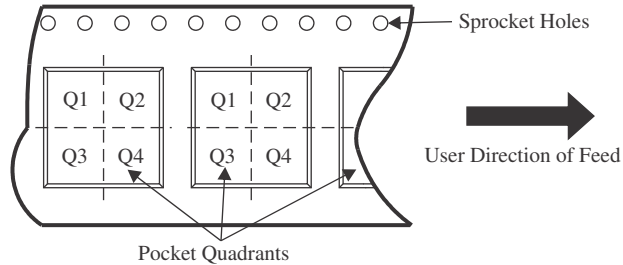
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

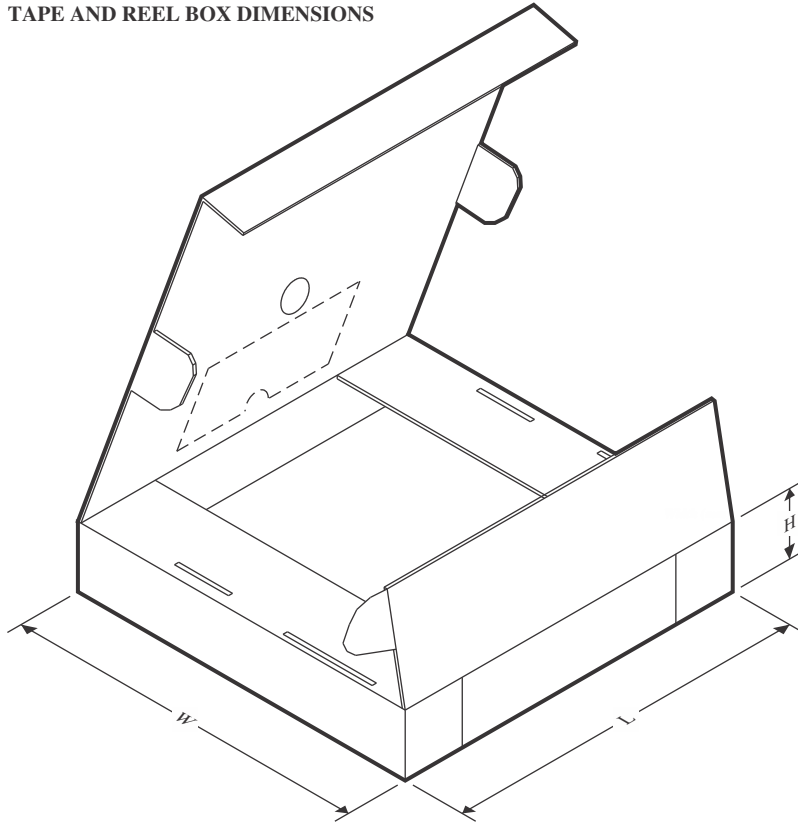
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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS36277TMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS36277TMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

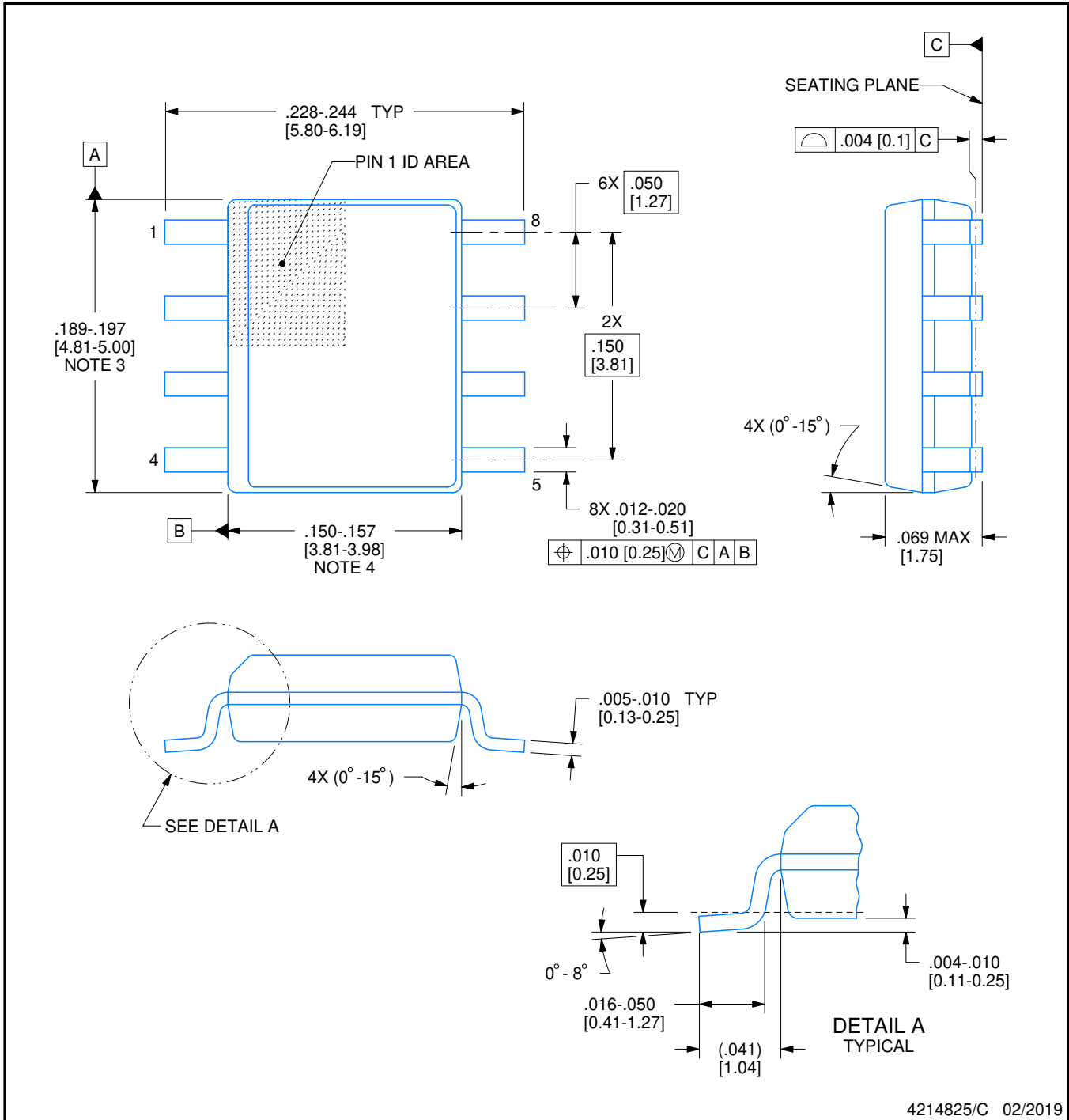


D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

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NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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