LB1946

Monolithic Digital IC

PWM Current Control Stepping Motor Driver

ON Semiconductor®

http://onsemi.com

Overview

The LB1946 is stepping motor drive IC that implements PWM current control bipolar drive with a fixed off time. This IC features 15-current setting levels using a fixed VREF voltage and supports for microstepping drive from 1-2 phase excitation to 4W1-2 phase excitation drive. This device is optimal for driving stepping motors such as those used for carriage drive and paper feed in printers.

Applications

• PWM current control stepping motor drivers

Features

• PWM current control with a fixed off time
• Logic input serial-parallel converter (allows 1-2, W1-2, 2W1-2, and 4W1-2 phase excitation drive)
• Current attenuation switching function (with slow decay, fast decay, and mixed decay modes)
• Built-in upper and lower side output diodes
• Simultaneous on state prevention function (through current prevention)
• Noise canceller function
• Thermal shutdown circuit
• Shutoff on low logic system voltage circuit
• Low-power mode control pin

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Motor supply voltage	VBB		50	V
Peak output current	I_O PEAK	tw≤20µs	1.75	A
Maximum continuous output current	I_O max		1.5	A
Logic system supply voltage	V_{CC}		7.0	V
Logic input voltage range	V_{IN}		-0.3 to V_{CC}	V
Emitter output voltage	VE		1.0	V
Operating temperature	Topr		-20 to +85	°C
Storage temperature	Tstg		-55 to +150	°C
Allowable power dissipation (IC internal)	Pd max	Ta=25°C, independent IC	3.0	W

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

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Allowable Operating Ranges at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Motor supply voltage	VBB		10 to 45	V
Logic supply voltage	V_{CC}		4.5 to 5.5	V
Reference voltage	VREF		0.0 to 3.0	V

Electrical Characteristics at Ta = 25°C, V_{CC} = 5V, VBB = 45V, VRES = 1.52V

Parameter	Symbol	Conditions	Ratings			unit
			min	typ	max	
Output Block						
Output stage supply current	IBB ON		1.6	2.4	3.5	mA
	IBB OFF		1.3	1.9	2.5	mA
Output saturation voltage 1	$V_O$sat1	I_O=+1.0A (sink)		1.2	1.6	V
Output saturation voltage 2	$V_O$sat2	I_O =+1.5 A (sink)		1.5	1.9	V
Output saturation voltage 3	$V_O$sat3	I_O=-1.0 A (source)		1.9	2.2	V
Output saturation voltage 4	$V_O$sat4	I_O=-1.5 A (source)		2.2	2.4	V
Output leakage current	I_O1 (leak)	V_O=VBB (sink)			50	μA
	I_O2 (leak)	V_O=0V (source)	-50			μA
Output sustain voltage	V_O sus	L=15mH I_O=1.5A *	45			V
Logic Block						
Logic system supply current	I_{CC} ON	D0=1,D1=1,D2=1,D3=1 When these data values are set	25.5	37	48.5	mA
	I_{CC} OFF1	D0=0,D1=0,D2=0,D3=0	18	26	34	mA
	I_{CC} OFF2	ST=LOW	0.01	0.05	0.1	mA
Input voltage	V_{IH}		2			V
	V_{IL}				0.8	V
Input current	I_{IH}	V_{IH}=2V			35	μA
	I_{IL}	V_{IL}=0.8V	6			μA
Sense voltages	VE	D0=1,D1=1,D2=1,D3=1 When these data values are set	0.470	0.50	0.525	V
		D0=1,D1=1,D2=1,D3=0	0.445	0.48	0.505	V
		D0=1,D1=1,D2=0,D3=1	0.425	0.46	0.485	V
		D0=1,D1=1,D2=0,D3=0	0.410	0.43	0.465	V
		D0=1,D1=0,D2=1,D3=1	0.385	0.41	0.435	V
		D0=1,D1=0,D2=1,D3=0	0.365	0.39	0.415	V
		D0=1,D1=0,D2=0,D3=1	0.345	0.37	0.385	V
		D0=1,D1=0,D2=0,D3=0	0.325	0.35	0.365	V
		D0=0,D1=1,D2=1,D3=1	0.280	0.30	0.325	V
		D0=0,D1=1,D2=1,D3=0	0.240	0.26	0.285	V
		D0=0,D1=1,D2=0,D3=1	0.195	0.22	0.235	V
		D0=0,D1=1,D2=0,D3=0	0.155	0.17	0.190	V
		D0=0,D1=0,D2=1,D3=1	0.115	0.13	0.145	V
		D0=0,D1=0,D2=1,D3=0	0.075	0.09	0.100	V
Reference current	IREF	VREF=1.5V	-0.5			μA
CR pin current	ICR	CR=1.0V	-1.7	-1.25	-0.9	mA
MD pin current	IMD	MD=1.0V, CR=4.0V	-5.0			μA
Logic system on voltage	VLSDON		2.6	2.8	3.0	V
Logic system off voltage	VLSDOFF		2.45	2.65	2.85	V
LVSD hysteresis	VLHIS		0.03	0.15	0.35	V
Thermal shutdown temperature	Ts			170		°C

*Design guaranteed value

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AC Electrical Characteristics at $V_{CC} = 5V$

Parameter	Symbol	Conditions	Ratings min	Ratings typ	Ratings max	unit
Clock frequency	f_{clk}	V_{CC}=5.0V		200	550	kHz
Data setup time	t_{DS}	V_{CC}=5.0V	0.9	2.5		µs
Data hold time	t_{DH}	V_{CC}=5.0V	0.9	2.5		µs
Minimum clock high-level pulse width	t_{SCH}	V_{CC}=5.0V	0.9	2.5		µs
Minimum clock low-level pulse width	t_{SCL}	V_{CC}=5.0V	0.9	2.5		µs
SET pin stipulated time	t_{lat}	V_{CC}=5.0V	0.9	2.5		µs
SET pin signal pulse width	t_{latw}	V_{CC}=5.0V	1.9	5.0		µs
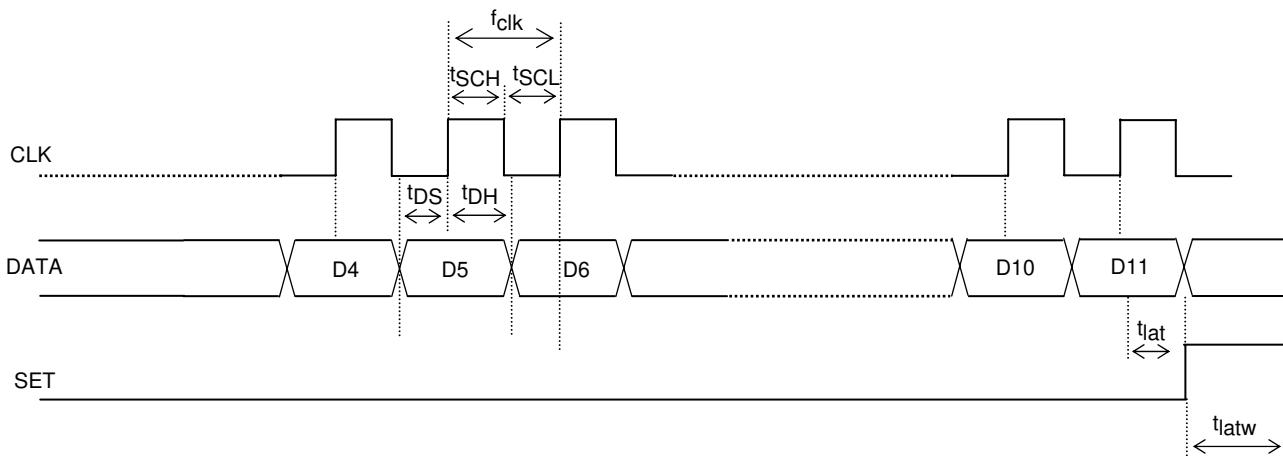
V_{CC}=3.3V Specification

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Ratings	Unit
Emitter output voltage	VE		0.5	V

Allowable Operating Ranges at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Motor system supply voltage	VBB		10 to 45	V
Logic system supply voltage	V_{CC}		3.0 to 3.6	V
Reference voltage	VREF		0.0 to 1.0	V

Electrical Characteristics at Ta = 25°C, V_{CC} = 3.3V, VBB = 45V, VREF = 1.0V

Parameter	Symbol	Conditions	Ratings min	Ratings typ	Ratings max	unit
Output Block						
Output stage supply current	IBB ON		1.6	2.4	3.5	mA
	IBB OFF		1.3	1.9	2.5	mA
Output saturation voltage 1	$V_O$sat1	I_O=+1.0A (sink)		1.3	1.7	V
Output saturation voltage 2	$V_O$sat2	I_O=+1.5 A (sink)		1.6	2.0	V
Output saturation voltage 3	$V_O$sat3	I_O=-1.0 A (source)		1.9	2.2	V
Output saturation voltage 4	$V_O$sat4	I_O=-1.5 A (source)		2.2	2.4	V
Output leakage current	I_O1 (leak)	V_O=VBB (sink)			50	µA
	I_O2 (leak)	V_O=0V (source)	-50			µA
Output sustain voltage	V_O sus	L=15mH I_O=-1.5A *	45			V

*Design guaranteed value

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Parameter	Symbol	Conditions	Ratings min	Ratings typ	Ratings max	unit
Logic Block						
Logic system supply current	I_{CC} ON	D0=1,D1=1,D2=1,D3=1 When these data values are set	23.5	34	44.5	mA
	I_{CC} OFF1	D0=0,D1=0,D2=0,D3=0	16	23	30	mA
	I_{CC} OFF2	ST=0.8V	0.005	0.03	0.1	mA
Input voltage	V_{IH}		2			V
	V_{IL}				0.8	V
Input current	I_{IH}	V_{IH}=2V			35	µA
	I_{IL}	V_{IL}=0.8V	6			µA
Sense voltages	VE	D0=1,D1=1,D2=1,D3=1 When these data values are set	0.303	0.330	0.356	V
		D0=1,D1=1,D2=1,D3=0	0.290	0.315	0.341	V
		D0=1,D1=1,D2=0,D3=1	0.276	0.300	0.324	V
		D0=1,D1=1,D2=0,D3=0	0.263	0.286	0.309	V
		D0=1,D1=0,D2=1,D3=1	0.250	0.272	0.294	V
		D0=1,D1=0,D2=1,D3=0	0.236	0.257	0.278	V
		D0=1,D1=0,D2=0,D3=1	0.223	0.243	0.263	V
		D0=1,D1=0,D2=0,D3=0	0.209	0.228	0.247	V
		D0=0,D1=1,D2=1,D3=1	0.183	0.200	0.217	V
		D0=0,D1=1,D2=1,D3=0	0.155	0.170	0.185	V
		D0=0,D1=1,D2=0,D3=1	0.128	0.143	0.158	V
		D0=0,D1=1,D2=0,D3=0	0.102	0.114	0.126	V
		D0=0,D1=0,D2=1,D3=1	0.074	0.085	0.096	V
		D0=0,D1=0,D2=1,D3=0	0.047	0.057	0.067	V
Reference current	IREF	VREF=1.5V	-0.5			µA
CR pin current	ICR	CR=1.0V	-0.91	-0.7	-0.49	mA
MD pin current	IMD	MD=1.0V, CR=4.0V	-5.0			µA
Logic system on voltage	VLSDON		2.6	2.8	3.0	V
Logic system off voltage	VLSDOFF		2.45	2.65	2.85	V
LVSD hysteresis	VLHIS		0.03	0.15	0.35	V
Thermal shutdown temperature	Ts			170		°C

AC Electrical Characteristics at $V_{CC} = 3.3V$

Parameter	Symbol	Conditions	Ratings min	Ratings typ	Ratings max	unit
Clock frequency	f_{clk}	V_{CC}=3.3V		200	550	kHz
Data setup time	t_{DS}	V_{CC}=3.3V	0.9	2.5		µs
Data hold time	t_{DH}	V_{CC}=3.3V	0.9	2.5		µs
Minimum clock high-level pulse width	t_{SCH}	V_{CC}=3.3V	0.9	2.5		µs
Minimum clock low-level pulse width	t_{SCL}	V_{CC}=3.3V	0.9	2.5		µs
SET pin stipulated time	t_{lat}	V_{CC}=3.3V	0.9	2.5		µs
SET pin signal pulse width	t_{latw}	V_{CC}=3.3V	1.9	5.0		µs
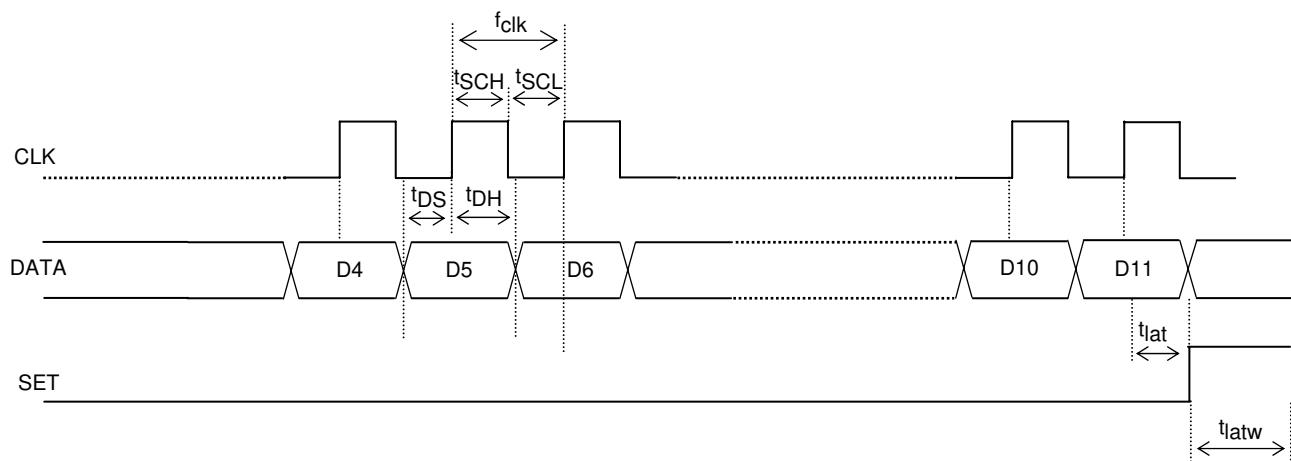
Package Dimensions

unit:mm (typ)

3147C

DIP28H(500mil)

Pd max - Ta
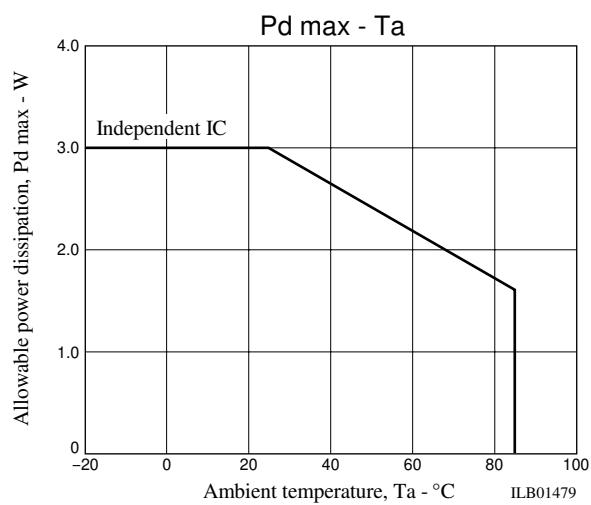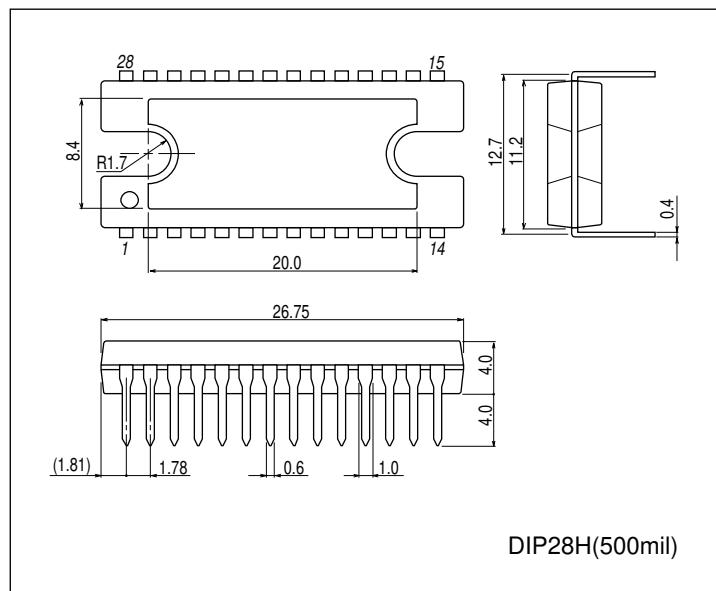
Block Diagram

Pin Assignment

Pin	Name
28	VCC
27	VREF1
26	NC
25	CR1
24	MD
23	CLK
22	DATA
21	SET
20	ST
19	NC
18	CR2
17	NC
16	VREF2
15	GND

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Pin	Name
1	VBB
2	NC
3	E1
4	NC
5	NC
6	OUTA-
7	OUTA
8	OUTB-
9	OUTB
10	NC
11	NC
12	E2
13	NC
14	VBB

Top view

Timing Chart

CLOCK   1μs
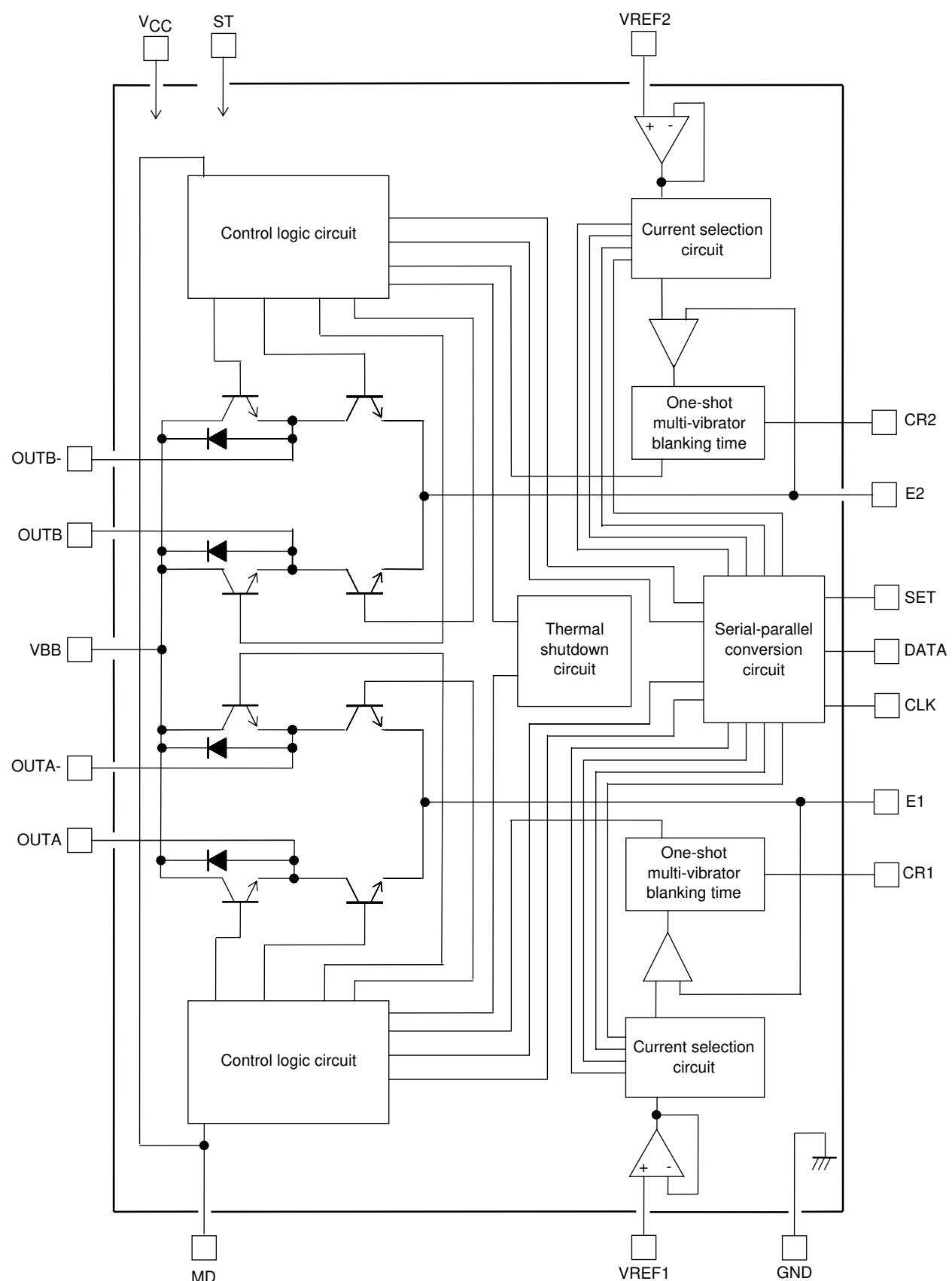
DATA   1μs   D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11
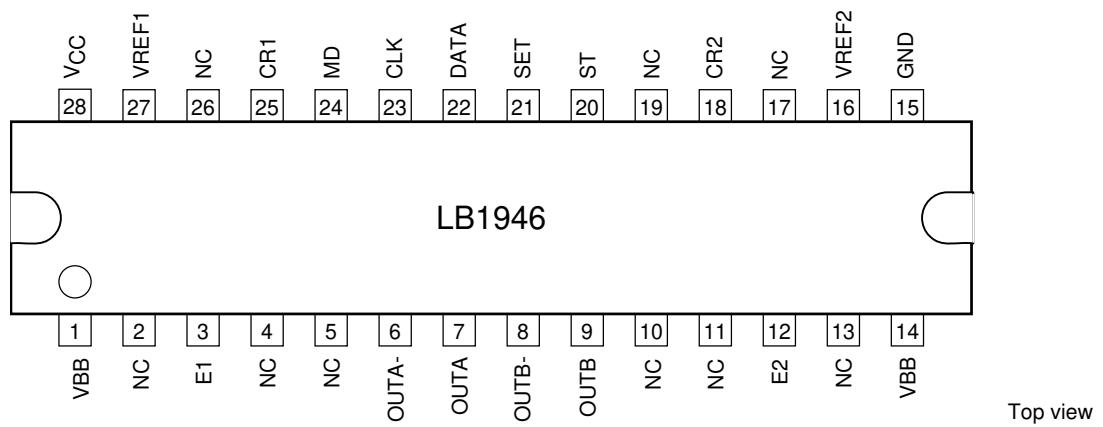
SET
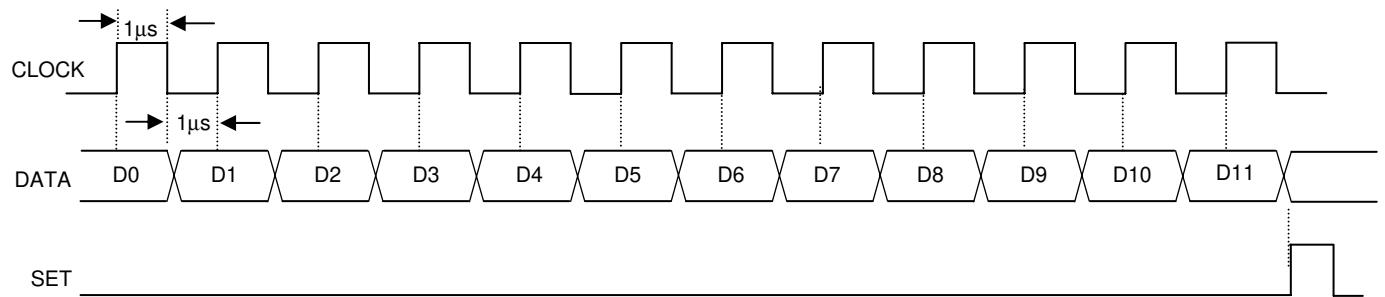
Serial Transmission Data Definitions

No.	IA4 D0	IA3 D1	IA2 D2	IA1 D3	DE1 D4	PH1 D5	IB4 D6	IB3 D7	IB2 D8	IB1 D9	DE2 D10	PH2 D11	Output mode OUTA	OUTA-	OUTB	OUTB-	I/O ratio	DEC MODE
0	1	1	1	1	1	1	1	1	1	1	1	1	H	L	H	L	100%	SLOW
1	1	1	1	0	1	1	1	1	1	0	1	1	H	L	H	L	96	SLOW
2	1	1	0	1	1	1	1	1	0	1	1	1	H	L	H	L	91	SLOW
3	1	1	0	0	1	1	1	1	0	0	1	1	H	L	H	L	87	SLOW
4	1	0	1	1	1	1	1	0	1	1	1	1	H	L	H	L	83	SLOW
5	1	0	1	0	1	1	1	0	1	0	1	1	H	L	H	L	78	SLOW
6	1	0	0	1	1	1	1	0	0	1	1	1	H	L	H	L	74	SLOW
7	1	0	0	0	1	1	1	0	0	0	1	1	H	L	H	L	70	SLOW
8	0	1	1	1	1	1	0	1	1	1	1	1	H	L	H	L	61	SLOW
9	0	1	1	0	1	1	0	1	1	0	1	1	H	L	H	L	52	SLOW
10	0	1	0	1	1	1	0	1	0	1	1	1	H	L	H	L	44	SLOW
11	0	1	0	0	1	1	0	1	0	0	1	1	H	L	H	L	35	SLOW
12	0	0	1	1	1	1	0	0	1	1	1	1	H	L	H	L	26	SLOW
13	0	0	1	0	1	1	0	0	1	0	1	1	H	L	H	L	17	SLOW
14	1	1	1	1	0	0	1	1	1	1	0	0	L	H	L	H	100	FAST
15	1	1	1	0	0	0	1	1	1	0	0	0	L	H	L	H	96	FAST
16	1	1	0	1	0	0	1	1	0	1	0	0	L	H	L	H	91	FAST
17	1	1	0	0	0	0	1	1	0	0	0	0	L	H	L	H	87	FAST
18	1	0	1	1	0	0	1	0	1	1	0	0	L	H	L	H	83	FAST
19	1	0	1	0	0	0	1	0	1	0	0	0	L	H	L	H	78	FAST
20	1	0	0	1	0	0	1	0	0	1	0	0	L	H	L	H	74	FAST
21	1	0	0	0	0	0	1	0	0	0	0	0	L	H	L	H	70	FAST
22	0	1	1	1	0	0	0	1	1	1	0	0	L	H	L	H	61	FAST
23	0	1	1	0	0	0	0	1	1	0	0	0	L	H	L	H	52	FAST
24	0	1	0	1	0	0	0	1	0	1	0	0	L	H	L	H	44	FAST
25	0	1	0	0	0	0	0	1	0	0	0	0	L	H	L	H	35	FAST
26	0	0	1	1	0	0	0	0	1	1	0	0	L	H	L	H	26	FAST
27	0	0	1	0	0	0	0	0	1	0	0	0	L	H	L	H	17	FAST
28	0	0	0	0	*	*	0	0	0	0	*	*	OFF	OFF	OFF	OFF	0	-

Note *: Don't care (0 or 1)

Note 1: In the mixed decay mode, set D4 and D10 to 0 and set the MD pin to a level shown below.

Programmable MD voltage range

V_{CC}=5V specifications: 1.6 to 3.9V

V_{CC}=3.3V specifications: 1.2 to 2.5V

Current Settings Truth Table

* Items in parentheses are defined by the serial data.

| IA4 (D0)	IA3 (D1)	IA2 (D2)	IA1 (D3)	Set Current I_{OUT}	Current Ratio (%)
1	1	1	1	11.5/11.5×VREF/3.04RE=I_{OUT}	100
1	1	1	0	11.0/11.5×VREF/3.04RE=I_{OUT}	95.65
1	1	0	1	10.5/11.5×VREF/3.04RE=I_{OUT}	91.30
1	1	0	0	10.0/11.5×VREF/3.04RE=I_{OUT}	86.95
1	0	1	1	9.5/11.5×VREF/3.04RE=I_{OUT}	82.61
1	0	1	0	9.0/11.5×VREF/3.04RE=I_{OUT}	78.26
1	0	0	1	8.5/11.5×VREF/3.04RE=I_{OUT}	73.91
1	0	0	0	8.0/11.5×VREF/3.04RE=I_{OUT}	69.56
0	1	1	1	7.0/11.5×VREF/3.04RE=I_{OUT}	60.87
0	1	1	0	6.0/11.5×VREF/3.04RE=I_{OUT}	52.17
0	1	0	1	5.0/11.5×VREF/3.04RE=I_{OUT}	43.48
0	1	0	0	4.0/11.5×VREF/3.04RE=I_{OUT}	34.78
0	0	1	1	3.0/11.5×VREF/3.04RE=I_{OUT}	26.08
0	0	1	0	2.0/11.5×VREF/3.04RE=I_{OUT}	17.39

Note 1: The current ratios shown are calculated values.

Sample Application Circuit at V_{CC}=5V

MD voltage setting
(1.6 to 3.9V)
Fast mode: GND
Slow mode: V_{CC}

Logic level inputs

28	27	26	25	24	23	22	21	20	19	18	17	16	15
V_{CC}	VREF1	NC	CR1	MD	CLK	DATA	SET	ST	NC	CR2	NC	VREF2	GND

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VBB	NC	E1	NC	NC	OUTA -	OUTA	OUTB -	OUTB	NC	NC	E2	NC	VBB
1	2	3	4	5	6	7	8	9	10	11	12	13	14

Top view

Sample Application Circuit at $V_{CC}=3.3V$

MD voltage setting
(1.2 to 2.5V)
Fast mode: GND
Slow mode: V_{CC}

Logic level inputs

28	27	26	25	24	23	22	21	20	19	18	17	16	15
V_{CC}	VREF1	NC	CR1	MD	CLK	DATA	SET	ST	NC	CR2	NC	VREF2	GND

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VBB	NC	E1	NC	NC	OUTA -	OUTA	OUTB -	OUTB	NC	NC	E2	NC	VBB
1	2	3	4	5	6	7	8	9	10	11	12	13	14

10μF 3.3V 30kΩ 680pF 30kΩ 680pF 1.0V 0.1μF

SBD SBD SBD SBD

L L

1Ω 1Ω 42V 47μF

Top view

Current Path in Slow Decay Mode

Regenerative current during upper-side transistor switching operation
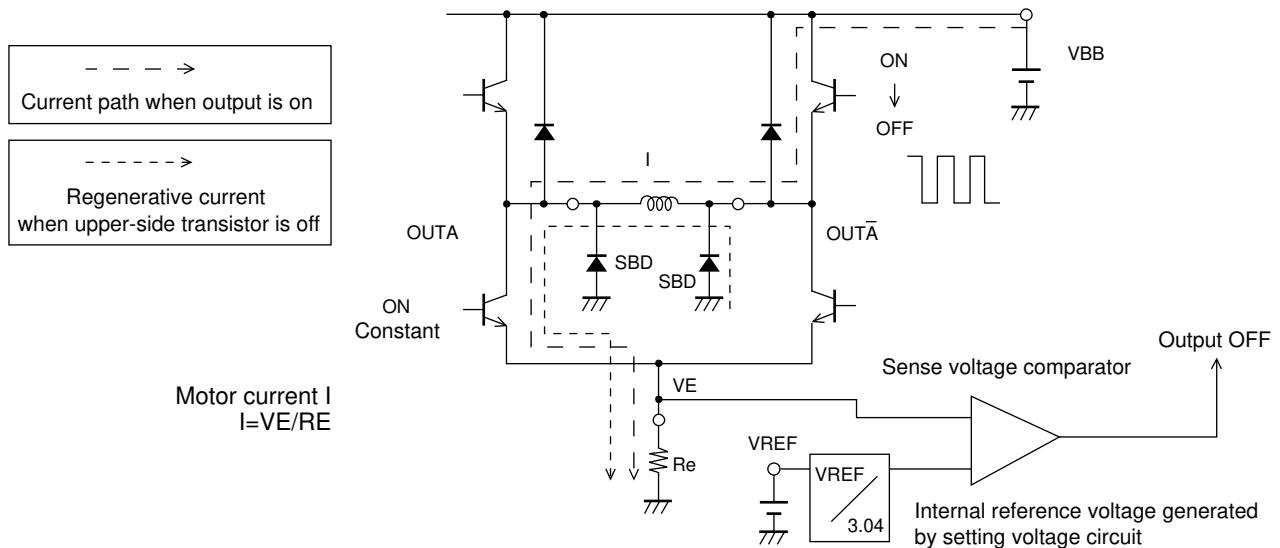
Figure 1

ILB01480

Current Path in Fast Decay Mode
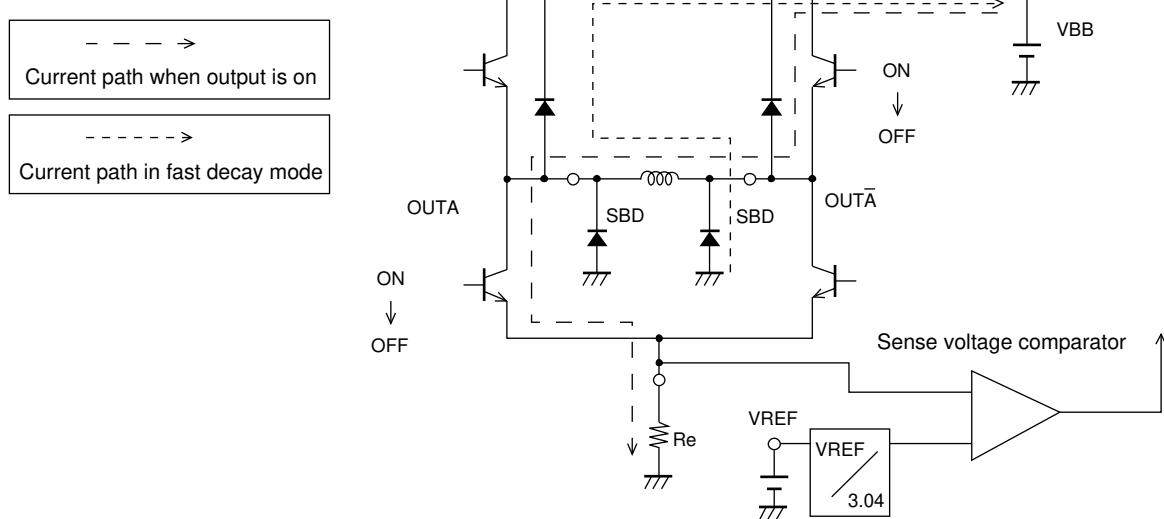
ILB01481

Switching Timing Chart During PWM Drive Mode

Slow decay (upper-side chopping)   Serial transmission data (D4, D10) = High   MD pin: Low

E pin

Output current

tn

CR pin

Output pin

Switching Waveform
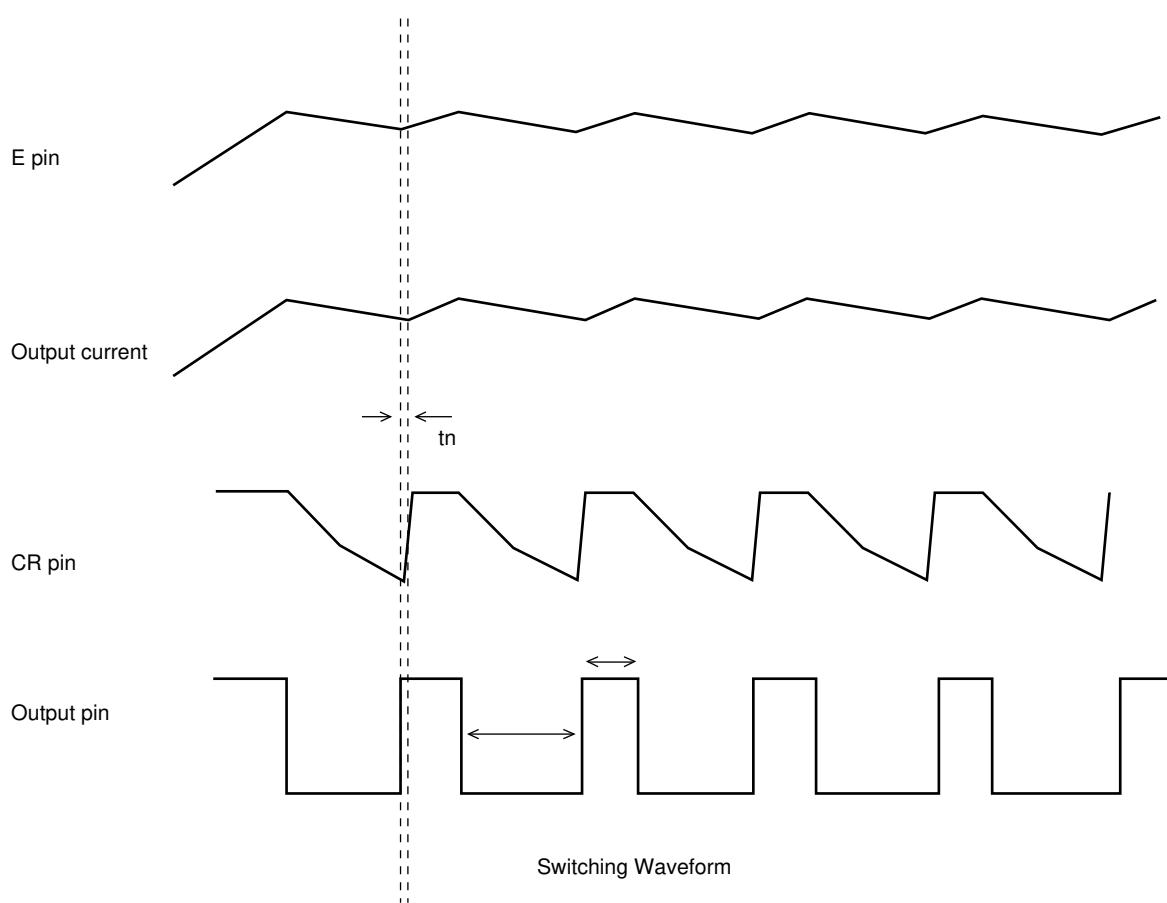
ILB01482

FAST DECAY   Serial transmission data (D4, D10) = Low   MD pin: Low

Noise spike

E pin

Output current

CR pin

Output pin

Switching Waveform

ILB01483

MIX DECAY

Switching Waveform
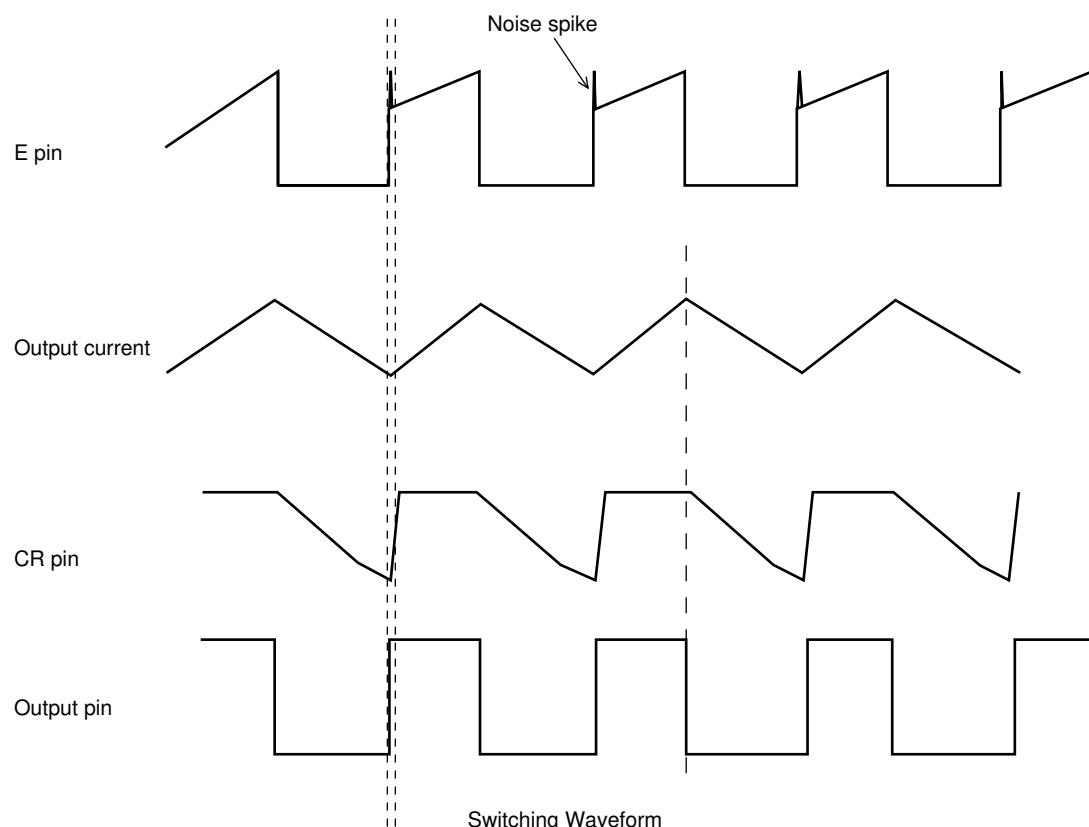
ILB01484
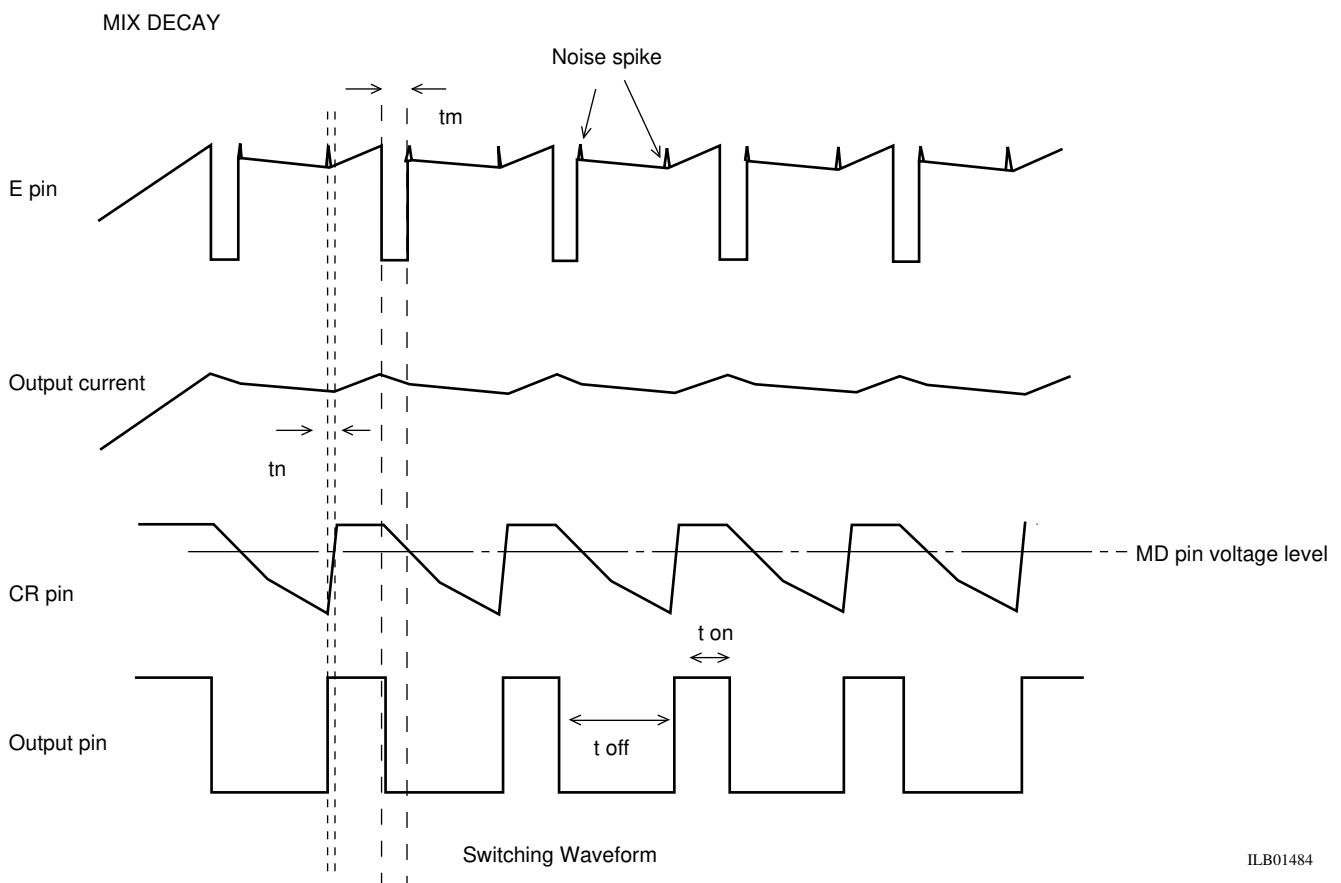
Mix decay logic setting

When serial transmission data (D4, D10) is Low

MD pin setting:

5V V_{CC} type: 1.6 to 3.9V

3.3V V_{CC} type: 1.2 to 2.5V

CR voltage and MD pin voltage are compared to select dual-side chopping or upper-side chopping.

CR voltage > MD pin voltage: dual-side chopping

CR voltage < MD pin voltage: upper-side chopping

t on: Output on time

t off: Output off time

tm: Fast decay time in mix decay mode

tn: Noise cancellation time

1. Switching OFF time and noise cancellation time calculations
   Notes on the CR pin setting (switching off time and noise canceller time)

The noise canceller time (Tn) and the switching off time (Toff) are set using the following formulas.

- When V_{CC}=5V
  Noise canceller time (Tn)

  $Tn \approx C \cdot R \cdot ln \{(1.5 - RI)/(4.0 - RI)\}$ [s]
  CR pin charge current: 1.25mA

  Switching off time (Toff)

  $Toff \approx -C \cdot R \cdot ln (1.5/4.8)$ [s]

  Component value ranges
  R: 5.6kΩ to 100kΩ
  C: 470pF to 2000pF

- When V_{CC}=3.3V
  Noise canceller time (Tn)

  $Tn \approx C \cdot R \cdot ln \{(1.06 - RI)/(2.66 - RI)\}$ [s]
  CR pin charge current: 0.7mA

  Switching off time (Toff)

  $Toff \approx -C \cdot R \cdot ln (1.06/3.1)$ [s]
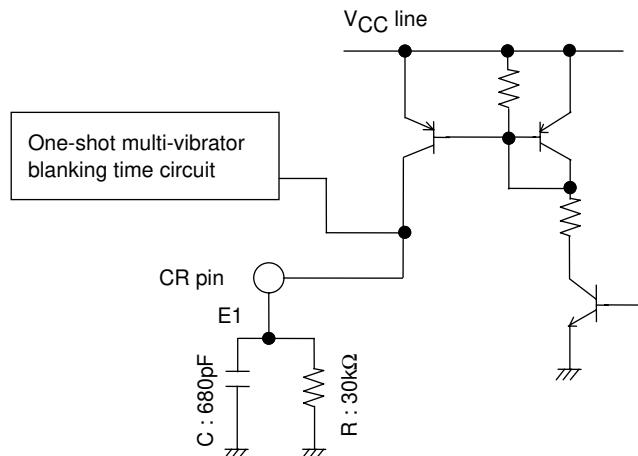
Figure 2 CR Pin Internal Circuit Structure

2. Notes on the MD pin

- If slow decay mode is set up by setting the D4 and D10 bits in the input serial data to 1, the MD pin must be shorted to GND.

- If the decay mode is set up by setting the D4 and D10 bits in the input serial data to 0, decay mode can be set with the MD pin.
  When the V_{CC}=5V specifications are used, the setting voltage range for mixed decay mode is 1.6 to 3.9V.
  When the V_{CC}=3.3V specifications are used, the setting voltage range for mixed decay mode is 1.2 to 2.5V.
  If mixed decay mode will not be used with the fast decay mode setting, either:
  Short the MD pin to GND to select fast decay mode, or
  Short the MD pin to V_{CC} to select slow decay mode.

3. Usage Notes

- Notes on the VREF pin
  Since the VREF pin inputs the reference voltage used to set the current, applications must be designed so that noise does not occur at this pin.

- Notes on the GND pins
  Since this IC switches large currents, care is required with respect to the GND pins.
  The PCB pattern in sections where large currents flow must be designed with low impedances and must be kept separate from the small-signal system.
  In particular, the GND terminals of the E pin sense resistor (RE) and external Schottky barrier diode GND terminals must be located as close as possible to the IC GND. The capacitor between V_{CC} and ground and between VBB and GND must be as close as possible to the corresponding V_{CC} and VBB pin in the pattern.

- Power on sequence
  When turning the power systems on
  $V_{CC}\rightarrow$logic level inputs (CLK, DATA, SET, and ST) $\rightarrow$VREF$\rightarrow$VBB

  When turning the power systems off
  VBB$\rightarrow$VREF$\rightarrow$logic level inputs (CLK, DATA, SET, and ST) $\rightarrow V_{CC}$

  Note that if the power supply for the logic level inputs is on when the V_{CC} power supply is off, a bias with an unstable state will be applied to the protection diodes at the V_{CC} pins, and this can cause incorrect operation.