



LVECL/LVPECL 1:15 Differential Divide-by-1/Divide-by-2 Clock Driver

MAX9322

General Description

The MAX9322 low-skew 1:15 differential clock driver reproduces or divides one of two differential input clocks at 15 differential outputs. An input multiplexer selects from one of two input clocks with input switching frequency in excess of 1.0GHz. The 15 outputs are arranged in four banks with 2, 3, 4, and 6 outputs, respectively. Each output bank is individually programmable to provide a divide-by-1 or divide-by-2 frequency function.

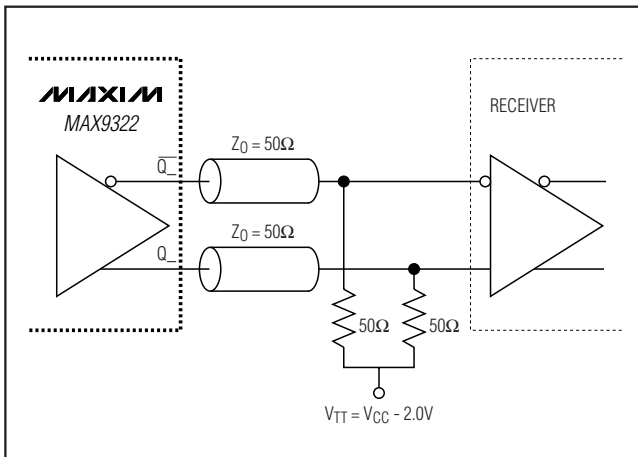
The MAX9322 operates in LVPECL systems with a +2.375V to +3.8V supply or in LVECL systems with a -2.375V to -3.8V supply. A V_{BB} reference output provides compatibility with single-ended clock input signals and a master reset input provides a simultaneous reset on all outputs.

The MAX9322 is available in 52-pin TQFP and 68-pin QFN packages and is specified for operation over -40°C to +85°C. For 1:10 clock drivers, refer to the MAX9311/MAX9313 data sheet. For 1:5 clock drivers, refer to the MAX9316 data sheet.

Applications

- Precision Clock Distribution
- Low-Jitter Data Repeaters
- Central-Office Backplane Clock Distribution
- DSLAM Backplane
- Base Stations
- ATE

Typical Operating Circuit



Features

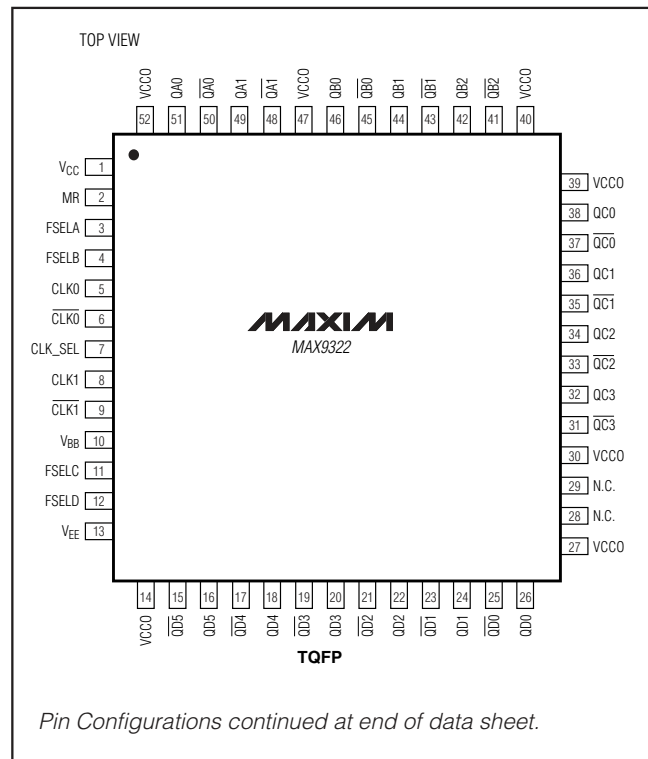
- ◆ 1.2ps (RMS) Maximum Random Jitter
- ◆ 300mV Differential Output at 1.0GHz
- ◆ 900ps Propagation Delay
- ◆ Selectable Divide-by-1 or Divide-by-2 Frequency Outputs
- ◆ Multiplexed 2:1 Input Function
- ◆ LVECL Operation from $V_{EE} = -2.375V$ to $-3.8V$
- ◆ LVPECL Operation from $V_{CC} = +2.375V$ to $+3.8V$
- ◆ ESD Protection: > 2kV Human Body Model

Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE |
|-------------|----------------|-------------|
| MAX9322ECY | -40°C to +85°C | 52 TQFP |
| MAX9322ETK* | -40°C to +85°C | 68 QFN |

*Future product—contact factory for availability.

Pin Configurations



Pin Configurations continued at end of data sheet.



For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

LVECL/LVPECL 1:15 Differential Divide-by-1/Divide-by-2 Clock Driver

ABSOLUTE MAXIMUM RATINGS

| | |
|---|--|
| V _{CC} to V _{EE} | 4.1V |
| Inputs and Outputs to V _{EE} | -0.3V to (V _{CC} + 0.3V) |
| Differential Input Magnitude..... | Lower of (V _{CC} - V _{EE}) and 3V |
| Continuous Output Current..... | 50mA |
| Surge Output Current..... | 100mA |
| V _{BB} Sink/Source Current..... | ±0.65mA |
| Continuous Power Dissipation (T _A = +70°C) | |
| Single-Layer PC Board | |
| 52-Pin TQFP (derate 15.4mW/°C above +70°C)..... | 1230.8mW |
| 68-Lead QFN (derate 27.8mW/°C above +70°C) ... | 2222.2mW |
| Multilayer PC Board | |
| 52-Pin TQFP (derate 19.1mW/°C above +70°C)..... | 1529.6mW |
| 68-Lead QFN (derate 38.5mW/°C above +70°C) ... | 3076.9mW |
| Junction-to-Ambient Thermal Resistance in Still Air | |
| Single-Layer PC Board | |
| 52-Pin TQFP..... | +65°C/W |
| 68-Lead QFN..... | +36°C/W |
| Multilayer PC Board | |
| 52-Pin TQFP..... | +52.3°C/W |
| 68-Lead QFN..... | +26°C/W |

| | |
|--|-----------------|
| Junction-to-Ambient Thermal Resistance with 500 LFPM Airflow | |
| Single-Layer PC Board | |
| 52-Pin TQFP..... | +50°C/W |
| 68-Lead QFN..... | +27°C/W |
| Multilayer PC Board | |
| 52-Pin TQFP..... | +40°C/W |
| 68-Lead QFN..... | +20°C/W |
| Junction-to-Case Thermal Resistance | |
| 52-Pin TQFP..... | +12.9°C/W |
| 68-Lead QFN..... | +2°C/W |
| Operating Temperature Range..... | -40°C to +85°C |
| Junction Temperature..... | +150°C |
| Storage Temperature Range..... | -65°C to +150°C |
| ESD Protection | |
| Human Body Model (Q ₁ _, Q ₂ _, CLK_SEL, FSEL_, CLK_, CLK_, MR, V _{BB})..... | ±2kV |
| Soldering Temperature (10s)..... | +300°C |

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} - V_{EE}) = 2.375V to 3.8V, outputs loaded with 50Ω ±1% to V_{CC} - 2V; CLK_SEL, FSEL_ = high or low; MR = low; |V_{IO}| = 0.095V to the lower of (V_{CC} - V_{EE}) and 3V. Typical values are at (V_{CC} - V_{EE}) = 3.3V, V_{IHD} = V_{CC} - 1V, V_{ILD} = V_{CC} - 1.5V.) (Notes 1-4)

| PARAMETER | SYMBOL | CONDITIONS | -40°C | | | +25°C | | | +85°C | | | UNITS |
|--|------------------|---|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|-----|-------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| SINGLE-ENDED INPUT (MR, FSEL_, CLK_SEL) | | | | | | | | | | | | |
| Input High Voltage | V _{IH1} | Figure 1 | V _{CC} - 1.155 | V _{CC} - 0.88 | V _{CC} - 1.155 | V _{CC} - 0.88 | V _{CC} - 1.155 | V _{CC} - 0.88 | V _{CC} - 1.155 | V _{CC} - 0.88 | V | |
| Input Low Voltage | V _{IL1} | Figure 1 | V _{CC} - 1.81 | V _{CC} - 1.505 | V _{CC} - 1.81 | V _{CC} - 1.505 | V _{CC} - 1.81 | V _{CC} - 1.505 | V _{CC} - 1.81 | V _{CC} - 1.505 | V | |
| Input Current | I _{IN1} | MR, FSEL_, CLK_SEL = V _{IL} or V _{IH} | -15 | +150 | -15 | +150 | -15 | +150 | -15 | +150 | μA | |
| DIFFERENTIAL INPUT (CLK_, CLK_) | | | | | | | | | | | | |
| Single-Ended Input High Voltage | V _{IH2} | Figure 1 | V _{CC} - 1.155 | V _{CC} - 0.88 | V _{CC} - 1.155 | V _{CC} - 0.88 | V _{CC} - 1.155 | V _{CC} - 0.88 | V _{CC} - 1.155 | V _{CC} - 0.88 | V | |
| Single-Ended Input Low Voltage | V _{IL2} | Figure 1 | V _{CC} - 1.81 | V _{CC} - 1.505 | V _{CC} - 1.81 | V _{CC} - 1.505 | V _{CC} - 1.81 | V _{CC} - 1.505 | V _{CC} - 1.81 | V _{CC} - 1.505 | V | |
| High Voltage of Differential Input | V _{IHD} | | V _{EE} + 1.2 | V _{CC} | V _{EE} + 1.2 | V _{CC} | V _{EE} + 1.2 | V _{CC} | V _{EE} + 1.2 | V _{CC} | V | |
| Low Voltage of Differential Input | V _{ILD} | | V _{EE} | V _{CC} - 0.095 | V _{EE} | V _{CC} - 0.095 | V _{EE} | V _{CC} - 0.095 | V _{EE} | V _{CC} - 0.095 | V | |

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DC ELECTRICAL CHARACTERISTICS (continued)

($V_{CC} - V_{EE}$) = 2.375V to 3.8V, outputs loaded with $50\Omega \pm 1\%$ to $V_{CC} - 2V$; CLK_SEL, FSEL_ = high or low; MR = low; $|V_{ID}| = 0.095V$ to the lower of ($V_{CC} - V_{EE}$) and 3V. Typical values are at ($V_{CC} - V_{EE}$) = 3.3V, $V_{IHD} = V_{CC} - 1V$, $V_{ILD} = V_{CC} - 1.5V$.) (Notes 1–4)

| PARAMETER | SYMBOL | CONDITIONS | -40°C | | | +25°C | | | +85°C | | | UNITS |
|--|---------------------|--|------------------|-----|-------------------|------------------|-----|-------------------|------------------|-----|-------------------|---------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| Differential Input Voltage | $V_{IHD} - V_{ILD}$ | For $V_{CC} - V_{EE} < 3.0V$ | 0.095 | | $V_{CC} - V_{EE}$ | 0.095 | | $V_{CC} - V_{EE}$ | 0.095 | | $V_{CC} - V_{EE}$ | V |
| | | For $V_{CC} - V_{EE} \geq 3.0V$ | 0.095 | | 3.0 | 0.095 | | 3.0 | 0.095 | | 3.0 | |
| Input Current | I_{IN2} | CLK_, $\overline{CLK}_$ = V_{IHD} or V_{ILD} | -150 | | +150 | -150 | | +150 | -150 | | +150 | μA |
| OUTPUTS ($Q_$, $\overline{Q}_$) | | | | | | | | | | | | |
| Single-Ended Output High Voltage | V_{OH} | Figure 1 | $V_{CC} - 1.085$ | | $V_{CC} - 0.880$ | $V_{CC} - 1.025$ | | $V_{CC} - 0.880$ | $V_{CC} - 1.025$ | | $V_{CC} - 0.880$ | V |
| Single-Ended Output Low Voltage | V_{OL} | Figure 1 | $V_{CC} - 1.810$ | | $V_{CC} - 1.52$ | $V_{CC} - 1.810$ | | $V_{CC} - 1.620$ | $V_{CC} - 1.810$ | | $V_{CC} - 1.620$ | V |
| Differential Output Voltage | $V_{OH} - V_{OL}$ | Figure 1 | 500 | | | 600 | | | 600 | | | mV |
| REFERENCE | | | | | | | | | | | | |
| Reference Voltage Output | V_{BB} | $I_{BB} = \pm 0.5mA$ (Note 5) | $V_{CC} - 1.41$ | | $V_{CC} - 1.25$ | $V_{CC} - 1.41$ | | $V_{CC} - 1.25$ | $V_{CC} - 1.41$ | | $V_{CC} - 1.25$ | V |
| SUPPLY | | | | | | | | | | | | |
| Supply Current | I_{EE} | (Note 6) | 50 | 85 | | 66 | 115 | | 80 | 130 | | mA |

LVECL/LVPECL 1:15 Differential Divide-by-1/Divide-by-2 Clock Driver

AC ELECTRICAL CHARACTERISTICS

($V_{CC} - V_{EE}$) = 2.375V to 3.8V; outputs loaded with $50\Omega \pm 1\%$ to $V_{CC} - 2V$; input frequency $\leq 1000\text{MHz}$; input transition time = 125ps (20% to 80%); CLK_SEL , FSEL_ = high or low, MR = low; V_{IH} = $V_{EE} + 1.2V$ to V_{CC} ; V_{ILD} = V_{EE} to $V_{CC} - 0.4V$; $V_{IH} - V_{ILD}$ = 0.4V to 1V. Typical values are at ($V_{CC} - V_{EE}$) = 3.3V, $V_{IH} = V_{CC} - 1V$, $V_{ILD} = V_{CC} - 1.5V$.) (Note 7)

| PARAMETER | SYMBOL | CONDITION | -40°C | | | +25°C | | | +85°C | | | UNITS |
|---|----------------------------|---|-------|-----|------|-------|-----|------|-------|-----|------|-------------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| Differential Input-to-Output Delay | t_{PLHD} , t_{PHLD} | Figure 2 | 700 | 900 | 1150 | 725 | 900 | 1180 | 750 | 950 | 1225 | ps |
| Single-Ended $\text{CLK_}/\overline{\text{CLK_}}$ to Output Delay | t_{PLHS} , t_{PLHS} | Figure 1 | 700 | 900 | 1170 | 700 | 900 | 1175 | 725 | 950 | 1250 | ps |
| MR to Output Delay | t_{PD} | Figure 3 | 450 | | 930 | 450 | | 930 | 450 | | 930 | ps |
| Output-to-Output Skew | t_{SKOO} | (Note 8) | | | 85 | | | 56 | | | 50 | ps |
| Added Random Jitter | t_{RJ} | $f_{IN} = 1.0\text{GHz}$ clock pattern (Note 9) | | | 1.2 | | | 1.2 | | | 1.2 | ps (RMS) |
| Added Deterministic Jitter | t_{DJ} | 1Gbps 223 - 1 PRBS pattern (Note 9) | | | 61 | | | 61 | | | 61 | pSP-P |
| Switching Frequency | f_{MAX} | $V_{OD} > 300\text{mV}$ | 1.0 | | | 1.0 | | | 1.0 | | | GHz |
| Differential Output Rise and Fall Time (20% to 80%) | t_R , t_F | Figure 2 | 200 | 260 | 400 | 200 | 260 | 400 | 200 | 240 | 400 | ps |

Note 1: Measurements are made with the device in thermal equilibrium.

Note 2: Current into a pin is defined as positive. Current out of a pin is defined as negative.

Note 3: Single-ended CLK_ , $\overline{\text{CLK_}}$ input operation is limited to $V_{CC} - V_{EE} = 3.0V$ to 3.8V.

Note 4: DC parameters are production tested at $T_A = +25^\circ\text{C}$ and guaranteed by design over the full operating temperature range.

Note 5: Use V_{BB} as a reference for inputs of the same device only.

Note 6: All pins open except V_{CC} and V_{EE} .

Note 7: Guaranteed by design and characterization. Limits are set at ± 6 sigma.

Note 8: Measured between outputs of the same parts at the signal crossing points under identical conditions for a same-edge transition.

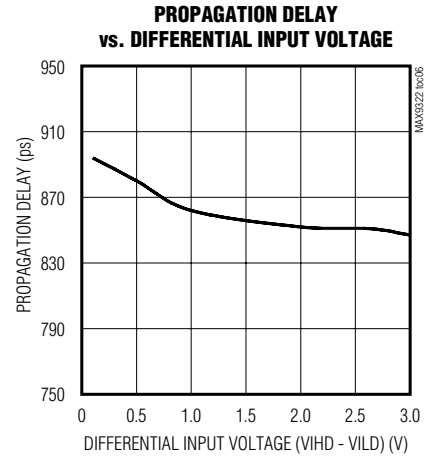
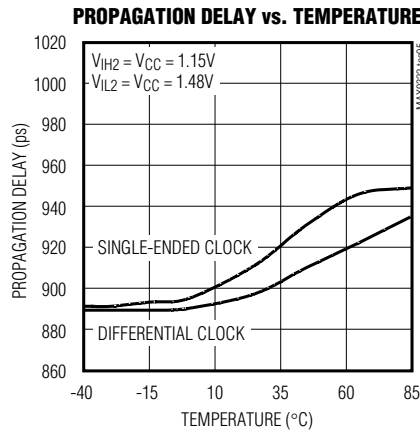
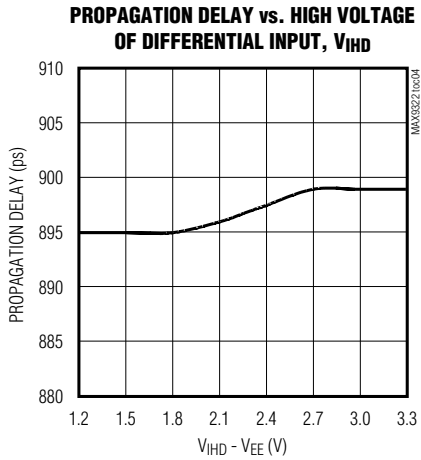
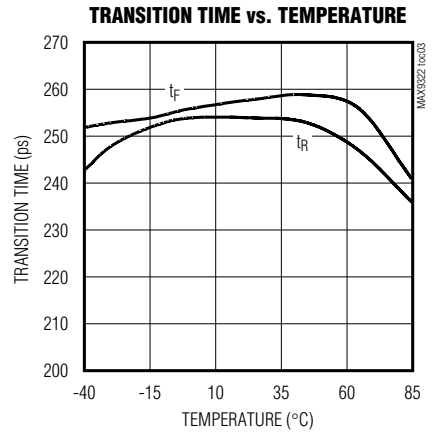
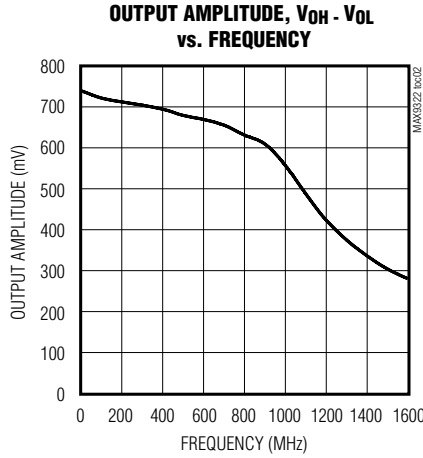
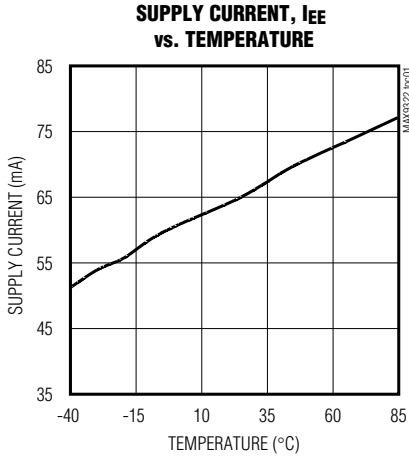
Note 9: Device jitter added to a jitter-free input signal.

LVECL/LVPECL 1:15 Differential Divide-by-1/Divide-by-2 Clock Driver

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Typical Operating Characteristics

($V_{CC} - V_{EE} = 3.3V$, $V_{IH2} = V_{CC} - 1V$, $V_{ILD} = V_{CC} - 1.5V$, $V_{ID} = 500mV$, $CLK_SEL = 0$, $FSEL_ = 0$, $f_{IN} = 600MHz$, $T_A = +25^{\circ}C$, unless otherwise noted.)



LVECL/LVPECL 1:15 Differential Divide-by-1/Divide-by-2 Clock Driver

Pin Description

| PIN | | NAME | FUNCTION |
|----------------------------|--|--------------------------|---|
| TQFP | QFN | | |
| 1 | 2, 3 | V _{CC} | Positive Power Supply. Powers input circuitry. Bypass each V _{CC} to V _{EE} with a 0.01μF and 0.1μF capacitor. Place the capacitors as close to the device as possible with the smaller value capacitor closest to the device. |
| 2 | 4 | MR | Single-Ended Master Reset. A high on MR sets all outputs to differential zero. A low on MR enables all outputs. MR is pulled to V _{EE} through a 75kΩ resistor. |
| 3 | 5 | FSELA | Single-Ended Frequency Select A. Selects the output frequency for bank A. Bank A consists of two differential outputs. A low on FSELA selects divide-by-1. A high on FSELA selects divide-by-2. FSELA is pulled to V _{EE} through a 75kΩ resistor. |
| 4 | 6 | FSELB | Single-Ended Frequency Select B. Selects the output frequency for bank B. Bank B consists of three differential outputs. A low on FSELB selects divide-by-1. A high on FSELB selects divide-by-2. FSELB is pulled to V _{EE} through a 75kΩ resistor. |
| 5 | 7 | CLK0 | Noninverting Clock 0 Input. $\overline{\text{CLK0}}$ is pulled to V _{EE} through 75kΩ resistors. |
| 6 | 8 | $\overline{\text{CLK0}}$ | Inverting Clock 0 Input. CLK0 is pulled to V _{CC} and to V _{EE} through a 75kΩ resistor. |
| 7 | 9 | CLK_SEL | Single-Ended Clock Selector Input. A low on CLK_SEL selects CLK0. A high on CLK_SEL selects CLK1. CLK_SEL is pulled to V _{EE} through a 75kΩ resistor. |
| 8 | 10 | CLK1 | Noninverting Clock 1 Input. CLK1 is pulled to V _{EE} through a 75kΩ resistor. |
| 9 | 11 | $\overline{\text{CLK1}}$ | Inverting Clock 1 Input. $\overline{\text{CLK1}}$ is pulled to V _{CC} and to V _{EE} through 75kΩ resistors. |
| 10 | 12 | V _{BB} | Reference Voltage Output. Connect V _{BB} to CLK_ or $\overline{\text{CLK}}$ to provide a reference for single-ended operation. When used, bypass with a 0.01μF ceramic capacitor to V _{CC} ; otherwise leave open. |
| 11 | 13 | FSELC | Single-Ended Frequency Select C. Selects the output frequency for bank C. Bank C consists of four differential outputs. A low on FSELC selects divide-by-1. A high on FSELC selects divide-by-2. FSELC is pulled to V _{EE} through a 75kΩ resistor. |
| 12 | 14 | FSELD | Single-Ended Frequency Select D. Selects the output frequency for bank D. Bank D consists of six differential outputs. A low on FSELD selects divide-by-1. A high on FSELD selects divide-by-2. FSELD is pulled to V _{EE} through a 75kΩ resistor. |
| 13 | 15, 16 | V _{EE} | Negative Power-Supply Input |
| 14, 27, 30, 39, 40, 47, 52 | 19, 20, 33, 36, 37, 40, 49, 50, 53, 54, 61, 66, 67 | V _{CCO} | Output Driver Positive Power Supply. Powers device output drivers. Bypass each V _{CCO} to V _{EE} with a 0.01μF and 0.1μF capacitor. Place the capacitors as close to the device as possible with the smaller value capacitor closest to the device. |
| 15 | 21 | $\overline{\text{QD5}}$ | Inverting QD5 Output. Typically terminate with 50Ω resistor to V _{CC} - 2V. |
| 16 | 22 | QD5 | Noninverting QD5 Output. Typically terminate with 50Ω resistor to V _{CC} - 2V. |
| 17 | 23 | $\overline{\text{QD4}}$ | Inverting QD4 Output. Typically terminate with 50Ω resistor to V _{CC} - 2V. |
| 18 | 24 | QD4 | Noninverting QD4 Output. Typically terminate with 50Ω resistor to V _{CC} - 2V. |

LVECL/LVPECL 1:15 Differential Divide-by-1/Divide-by-2 Clock Driver

Pin Description (continued)

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| PIN | | NAME | FUNCTION |
|--------|---|------------------|--|
| TQFP | QFN | | |
| 19 | 25 | $\overline{QD3}$ | Inverting QD3 Output. Typically terminate with 50Ω resistor to V _{CC} - 2V. |
| 20 | 26 | QD3 | Noninverting QD3 Output. Typically terminate with 50Ω resistor to V _{CC} - 2V. |
| 21 | 27 | $\overline{QD2}$ | Inverting QD2 Output. Typically terminate with 50Ω resistor to V _{CC} - 2V. |
| 22 | 28 | QD2 | Noninverting QD2 Output. Typically terminate with 50Ω resistor to V _{CC} - 2V. |
| 23 | 29 | $\overline{QD1}$ | Inverting QD1 Output. Typically terminate with 50Ω resistor to V _{CC} - 2V. |
| 24 | 30 | QD1 | Noninverting QD1 Output. Typically terminate with 50Ω resistor to V _{CC} - 2V. |
| 25 | 31 | $\overline{QD0}$ | Inverting QD0 Output. Typically terminate with 50Ω resistor to V _{CC} - 2V. |
| 26 | 32 | QD0 | Noninverting QD0 Output. Typically terminate with 50Ω resistor to V _{CC} - 2V. |
| 28, 29 | 1, 17, 18, 34, 35, 38, 39, 51, 52, 68 | N.C. | No Connection. Not internally connected. |
| 31 | 41 | $\overline{QC3}$ | Inverting QC3 Output. Typically terminate with 50Ω resistor to V _{CC} - 2V. |
| 32 | 42 | QC3 | Noninverting QC3 Output. Typically terminate with 50Ω resistor to V _{CC} - 2V. |
| 33 | 43 | $\overline{QC2}$ | Inverting QC2 Output. Typically terminate with 50Ω resistor to V _{CC} - 2V. |
| 34 | 44 | QC2 | Noninverting QC2 Output. Typically terminate with 50Ω resistor to V _{CC} - 2V. |
| 35 | 45 | $\overline{QC1}$ | Inverting QC1 Output. Typically terminate with 50Ω resistor to V _{CC} - 2V. |
| 36 | 46 | QC1 | Noninverting QC1 Output. Typically terminate with 50Ω resistor to V _{CC} - 2V. |
| 37 | 47 | $\overline{QC0}$ | Inverting QC0 Output. Typically terminate with 50Ω resistor to V _{CC} - 2V. |
| 38 | 48 | QC0 | Noninverting QC0 Output. Typically terminate with 50Ω resistor to V _{CC} - 2V. |
| 41 | 55 | $\overline{QB2}$ | Inverting QB2 Output. Typically terminate with 50Ω resistor to V _{CC} - 2V. |
| 42 | 56 | QB2 | Noninverting QB2 Output. Typically terminate with 50Ω resistor to V _{CC} - 2V. |
| 43 | 57 | $\overline{QB1}$ | Inverting QB1 Output. Typically terminate with 50Ω resistor to V _{CC} - 2V. |
| 44 | 58 | QB1 | Noninverting QB1 Output. Typically terminate with 50Ω resistor to V _{CC} - 2V. |
| 45 | 59 | $\overline{QB0}$ | Inverting QB0 Output. Typically terminate with 50Ω resistor to V _{CC} - 2V. |
| 46 | 60 | QB0 | Noninverting QB0 Output. Typically terminate with 50Ω resistor to V _{CC} - 2V. |
| 48 | 62 | $\overline{QA1}$ | Inverting QA1 Output. Typically terminate with 50Ω resistor to V _{CC} - 2V. |
| 49 | 63 | QA1 | Noninverting QA1 Output. Typically terminate with 50Ω resistor to V _{CC} - 2V. |
| 50 | 64 | $\overline{QA0}$ | Inverting QA0 Output. Typically terminate with 50Ω resistor to V _{CC} - 2V. |
| 51 | 65 | QA0 | Noninverting QA0 Output. Typically terminate with 50Ω resistor to V _{CC} - 2V. |
| — | EP | V _{EE} | The exposed pad of the QFN package is internally connected to V _{EE} . Refer to Application Note HFAN-08.1. |

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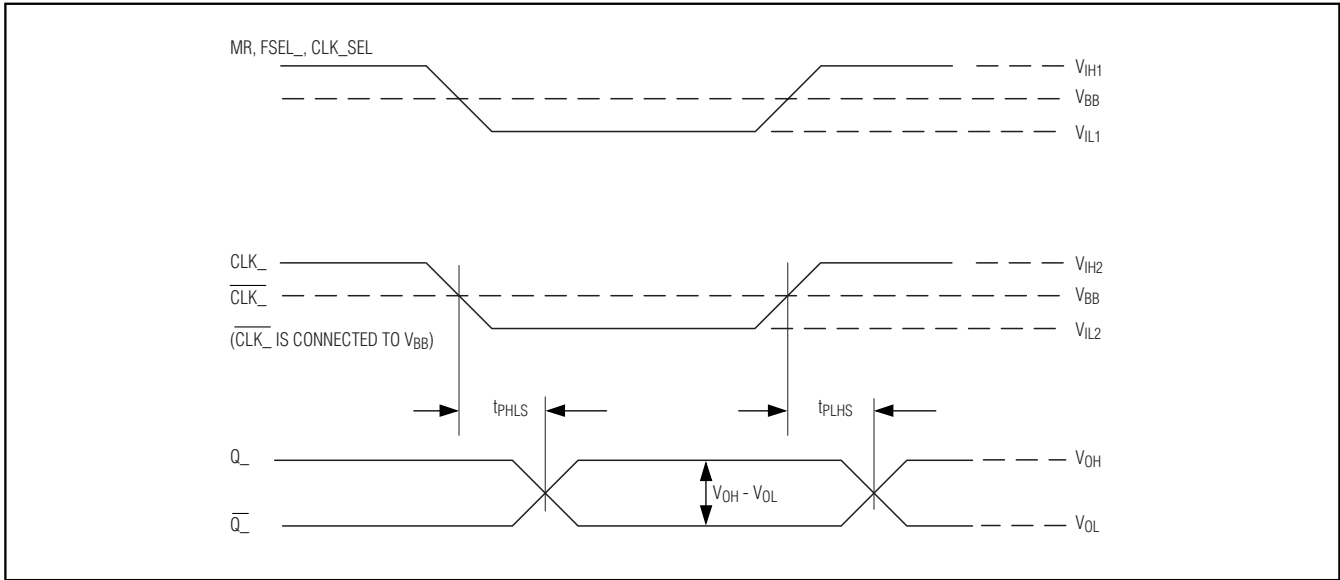


Figure 1. Timing Diagram for Single-Ended Inputs

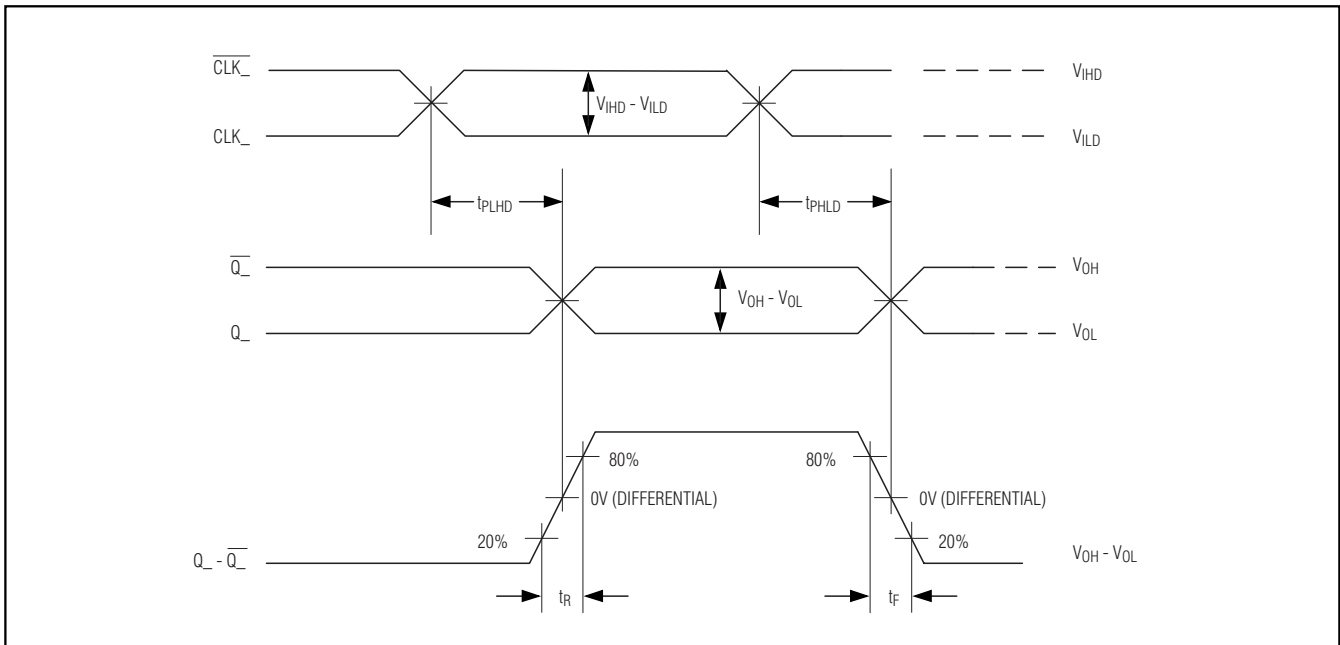


Figure 2. Timing Diagram for Differential Inputs

LVECL/LVPECL 1:15 Differential Divide-by-1/Divide-by-2 Clock Driver

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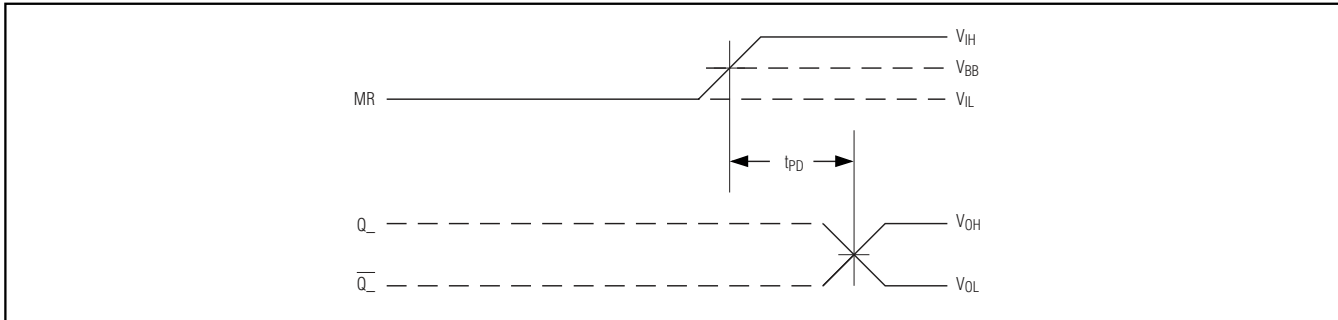


Figure 3. Timing Diagram for MR

Detailed Description

The MAX9322 low-skew 1:15 differential clock driver reproduces or divides one of two differential input clocks at 15 differential outputs. An input multiplexer selects from one of two input clocks with input frequency operation in excess of 1.0GHz. The 15 outputs are arranged into four banks with 2, 3, 4, and 6 outputs, respectively. Each output bank is individually programmable to provide a divide-by-1 or divide-by-2 frequency function.

LVECL/LVPECL Operation

Output levels are referenced to V_{CC} and are LVPECL or LVECL, depending on the level of the V_{CC} supply. With V_{CC} connected to a positive supply and V_{EE} connected to ground, the outputs are LVPECL. The outputs are LVECL when V_{CC} is connected to ground and V_{EE} is connected to a negative supply. When interfacing to differential LVPECL signals, the V_{CC} range is 2.375V to 3.8V (V_{EE} = 0), allowing high-performance clock distribution in systems with nominal 2.5V and 3.3V supplies. When interfacing to differential LVECL, the V_{EE} range is -2.375V to -3.8V (V_{CC} = 0).

Control Inputs (FSEL₋, CLK_SEL, MR)

The MAX9322 provides four output banks: A, B, C, and D. Bank A consists of two differential output pairs. Bank B consists of three differential output pairs. Bank C consists of four differential output pairs. Bank D consists of six differential output pairs. FSEL₋ selects the output clock frequency for a bank. A low on FSEL₋ selects divide-by-1 frequency operation while a high on FSEL₋ selects divide-by-2 operation. CLK_SEL selects CLK0 or CLK1 as the input signal. A low on CLK_SEL selects CLK0 while a high selects CLK1.

Master reset (MR) enables all outputs. CLK_SEL and FSEL₋ are asynchronous. Changes to the control inputs (CLK_SEL, FSEL₋) or on power-up cause indeterminate output states requiring a MR assertion to resynchronize any divide-by-2 outputs (Figure 4). A low on MR activates

all outputs for normal operation. A high on MR resets all outputs to differential low condition. See Table 1.

Input Termination Resistors

Differential inputs CLK₊ and CLK₋ are biased to guarantee a known state (differential low) if the inputs are left open. CLK₊ is internally pulled to V_{EE} through a 75kΩ resistor. CLK₋ is internally pulled to V_{CC} and to V_{EE} through 75kΩ resistors.

Single-ended inputs FSEL₋, MR, and CLK_SEL are internally pulled to V_{EE} through a 75kΩ resistor.

Differential Clock Input

The MAX9322 accepts two differential or single-ended clock inputs, CLK0/CLK0 and CLK1/CLK1. CLK_SEL selects between CLK0/CLK0 and CLK1/CLK1. A low on CLK_SEL selects CLK0/CLK0. A high on CLK_SEL selects CLK1/CLK1. See Table 1.

Differential CLK₊ inputs must be at least V_{BB} ±95mV to switch the outputs to the V_{OH} and V_{OL} levels specified in the DC Electrical Characteristics table. The maximum magnitude of the differential signal applied to the differential clock input is the lower of (V_{CC} - V_{EE}) and 3.0V. This limit also applies to the difference between any reference voltage input and a single-ended input. Specifications for the high and low voltages of a differential input (V_{IHD} and V_{ILD}) and the differential input voltage (V_{IHD} - V_{ILD}) apply simultaneously.

Table 1. Function Table

| PIN | FUNCTION | |
|-------------------|-------------|-------------|
| | LOW OR OPEN | HIGH |
| FSEL ₋ | Divide-by-1 | Divide-by-2 |
| CLK_SEL | CLK0 | CLK1 |
| MR* | Active | Reset |

*A master reset is required following power-up or changes to input functions to prevent indeterminate output states.

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Single-Ended Inputs and V_{BB}

The differential clock input can be configured to accept a single-ended input when operating at $V_{CC} - V_{EE} = 3.0V$ to $3.8V$. Connect V_{BB} to the inverting or noninverting input of the differential input as a reference for single-ended operation. The differential CLK_{-} input is converted to a noninverting, single-ended input by connecting V_{BB} to CLK_{-} and connecting the single-ended input signal to CLK . Similarly, an inverting configuration is obtained by connecting V_{BB} to CLK_{-} and connecting the single-ended input to CLK_{-} .

The single-ended inputs $FSEL_{-}$, CLK_{SEL} , and MR are internally referenced to V_{BB} . All single-ended inputs ($FSEL_{-}$, CLK_{SEL} , MR , and any CLK_{-} in single-ended mode) can be driven to V_{CC} and V_{EE} or with a single-ended LVPECL/LVECL signal. The single-ended input must be at least $V_{BB} \pm 95mV$ to switch the outputs to the V_{OH} and V_{OL} levels specified in the *DC Electrical Characteristics* table. When using the V_{BB} reference output, bypass V_{BB} with a $0.01\mu F$ ceramic capacitor to V_{CC} . Leave V_{BB} open when not used. The V_{BB} reference can source or sink $0.5mA$. Use V_{BB} as a reference for the same device only.

Applications Information

Supply Bypassing

Bypass each V_{CC} and V_{CCO} to V_{EE} with high-frequency surface-mount ceramic $0.01\mu F$ and $0.1\mu F$ capacitors in parallel as close to the device as possible, with the $0.01\mu F$ capacitor closest to the device. Use multiple parallel vias to minimize parasitic inductance. When using the V_{BB} reference output, bypass V_{BB} to V_{CC} with a $0.01\mu F$ ceramic capacitor.

Controlled-Impedance Traces

Input and output trace characteristics affect the performance of the MAX9322. Connect input and output signals with 50Ω characteristic impedance traces. Minimize the number of vias to prevent impedance discontinuities. Reduce reflections by maintaining the 50Ω characteristic impedance through cables and connectors. Reduce skew within a differential pair by matching the electrical length of the traces.

Output Termination

Terminate outputs with 50Ω to $V_{CC} - 2V$ or use an equivalent Thevenin termination. When a single-ended signal is taken from a differential output, terminate both outputs. For example, if $QA0$ is used as a single-ended output, terminate both $QA0$ and $QA0$.

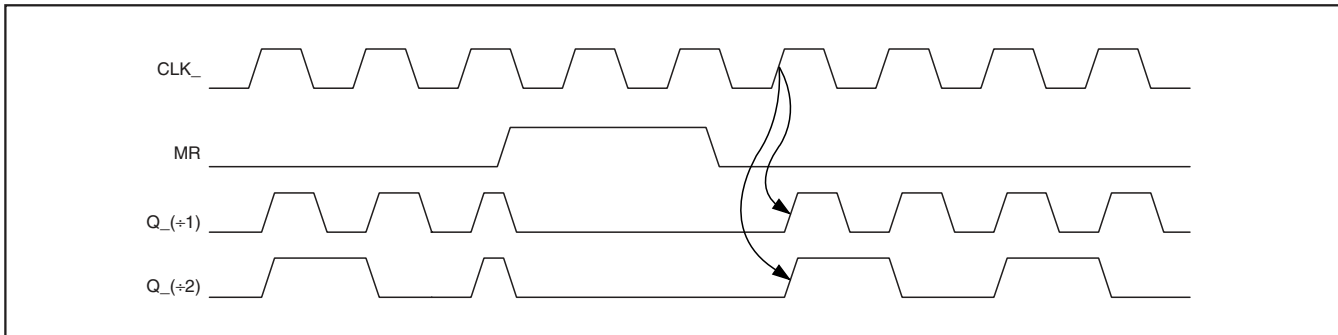
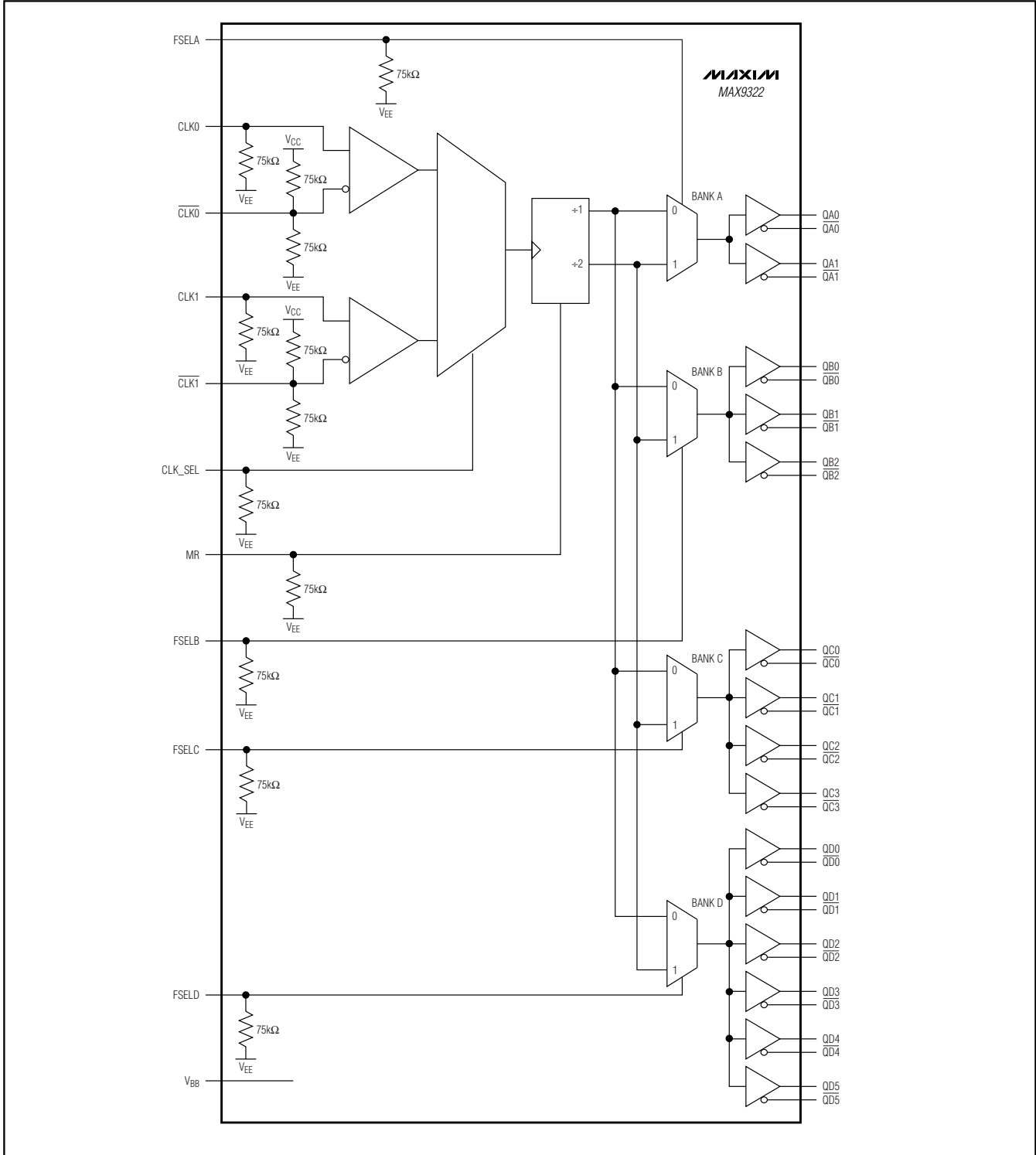


Figure 4. Timing Diagram for MR Resynchronization

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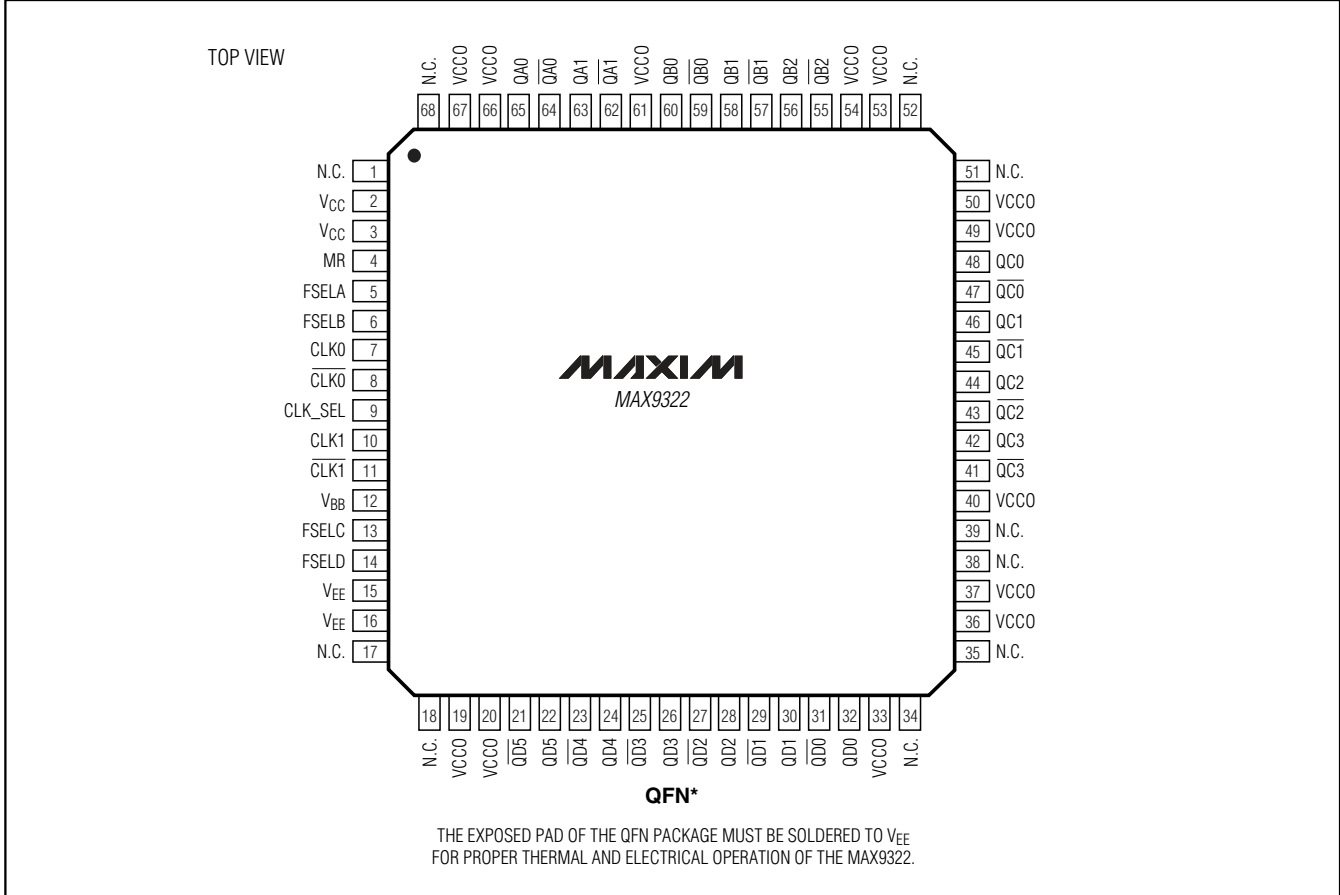
Functional Diagram

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LVECL/LVPECL 1:15 Differential Divide-by-1/Divide-by-2 Clock Driver

Pin Configurations (continued)



Chip Information

TRANSISTOR COUNT: 2063

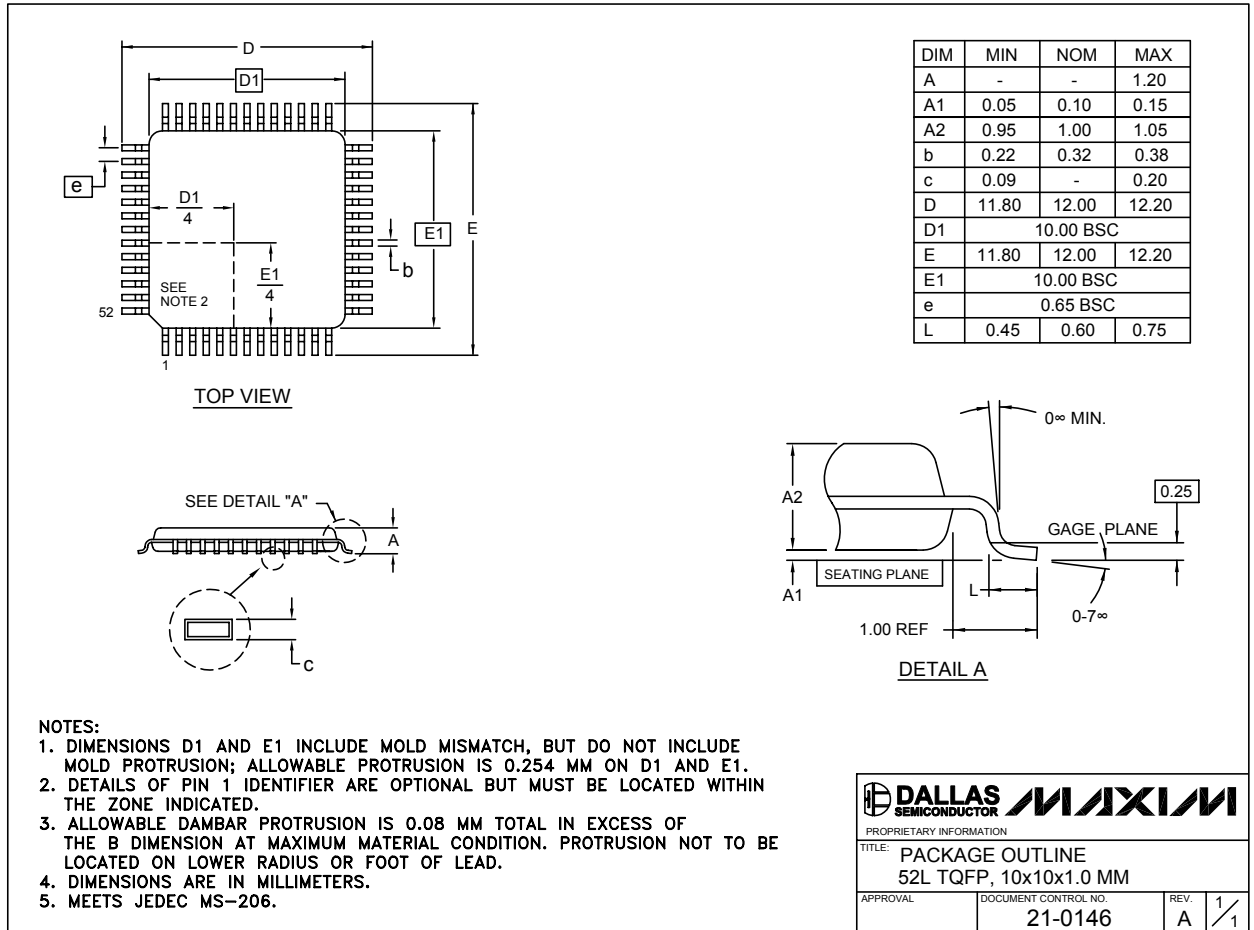
PROCESS: Bipolar

LVECL/LVPECL 1:15 Differential Divide-by-1/Divide-by-2 Clock Driver

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)

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Revision History

Pages changed at Rev 2: 1, 5, 13

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