TVP7002EVM

User's Guide

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Contents

1 Introduction 7
1.1 Functional Description 7
1.2 Overview 7
1.3 Board-Level Description 8
1.3.1 Analog Inputs 8
1.3.2 External Reference Clock and External Clock Input 8
1.3.3 Test Points and Jumpers 9
1.3.4 Common Board Interface 9
1.3.5 Component Analog Outputs 9
1.4 System Level Description 10

2 Hardware and Software Setup 11
2.1 Required Hardware and Equipment 11
2.2 Hardware Setup 11
2.3 Software Installation 12

3 WinVCC4 Quick Start 13

4 WinVCC4 in Depth 15
4.1 Starting WinVCC4 15
4.2 WinVCC4 Configuration Dialog Box 15
4.3 I^2C System Test 17
4.4 Main Menu 18
4.4.1 System Initialization 18
4.4.2 Register Editing 22
4.5 TVP7002 Property Sheets 25
4.5.1 Input Mux 25
4.5.2 Clamp 26
4.5.3 PLL 28
4.5.4 Gain and Offset - ALC 30
4.5.5 Output 31
4.5.6 Status 32

5 Troubleshooting 35
5.1 Troubleshooting Guide 35
5.2 Corrective Action Dialogs 37
5.2.1 Setting the PC Parallel Port Mode 38
5.2.2 General I^2C Error Report 38

6 TVP7002EVM Schematics 39

A Recommended PLL Settings 53

B Embedded Sync Setups 55

C Color Space Converter Coefficients 57

D Macrovision™ Support 59

List of Figures

1-1 TVP7002EVM Block Diagram 8
1-2 TVP7002EVM System Level Block Diagram 10
3-1 WinVCC4 – I²C Configuration Screen 13
3-2 WinVCC4 – Main Screen 14
3-3 WinVCC4 – System Initialization 14
4-1 WinVCC4 Multiple Occurrences Error Message 15
4-2 WinVCC4 I²C Address Configuration 16
4-3 I²C System Failure 17
4-4 WinVCC4 – Main Screen 18
4-5 System Initialization 19
4-6 TVP7002 Register Map 23
4-7 THS8200 Register Map 23
4-8 Generic I²C Register Editor 24
4-9 Input Mux Property Sheet 25
4-10 Clamp and ALC Placement 26
4-11 Clamp Control Property Sheet 28
4-12 PLL Property Sheet 29
4-13 Gain and Offset Property Sheet 30
4-14 Output Property Sheet 31
4-15 Status Property Sheet 33
5-1 I²C System Failure Dialog Box 36
5-2 Corrective Action Dialog Box 37
5-3 Corrective Action Required 37
5-4 Corrective Action Required 37
5-5 I²C Error Report 38
B-1 720p60 Example, Total Line Length = 1650 Pixels 55

List of Tables

1-1 Analog Inputs and Pin Terminals 8
1-2 I²C Address Selection Jumper (I2C ADDR) 9
1-3 Power Down Mode Selection Jumper (PWDN) 9
4-1 Main Menu Summary 18
4-2 Register Map Editor Controls 24
4-3 Recommended SOG LPF Settings 26
4-4 Typical Clamp Setup for RGB Graphics 27
4-5 Recommended Clamp LPF Settings 28
4-6 Recommended Coast Settings 30
4-7 Recommended ALC Settings 31
4-8 Use of Property Sheet Controls 34
4-9 Property Sheet Button Controls 34
5-1 TVP7002EVM Troubleshooting 35
5-2 I²C Troubleshooting 36
A-1 Recommended PLL Settings 53
B-1 Embedded Sync Setups 55
D-1 Recommended Reg 34h Macrovsion Stripper Width Settings (MAC_EN = 1) 59

Introduction

1.1 Functional Description

The TVP7002EVM is composed of the TVP7002 board and the THS8200 board when they are connected together. Both boards share a common interface via a 120-pin connector. This interface provides all data, clocks, I^2C communication, and 5-V power to each board.

The THS8200 is a Texas Instruments triple digital-to-analog converter (DAC) providing component analog RGB or YPbPr outputs. The THS8200 supports resolutions up to UXGA for PC graphics and up to 1080p for video. This triple DAC minimizes artifacts commonly associated with backend processing. Its purpose is only to convert the digital data from the TVP7002 triple analog-to-digital converter (ADC) back to analog. Use of a TV or display capable of supporting both component RGB and YPbPr analog inputs is recommended.

1.2 Overview

The TVP7002EVM is powered by a single 5-V universal supply. I^2C communication is emulated using a PC parallel port configured for the extended capability port (ECP) or bidirectional mode. The parallel port mode can be changed using the PC BIOS setup, available during the reboot process.

The TVP7002 triple ADC converts three channels of analog video input into digital component data. This digital data and the associated clocks from the TVP7002 are sent to the THS8200.

Control of the TVP7002EVM is provided by WinVCC4, a Windows™-based application developed by Texas Instruments and provided free of charge. This application uses the parallel port to provide I^2C communication to the TVP7002EVM. WinVCC4 provides a graphics user interface (GUI) and a register level interface to program and vary the controls available within the TVP7002 triple ADC and the THS8200.

1.3 Board-Level Description

The following sections describe the various features available on the TVP7002EVM. Figure 1-1 shows the TVP7002EVM block diagram.

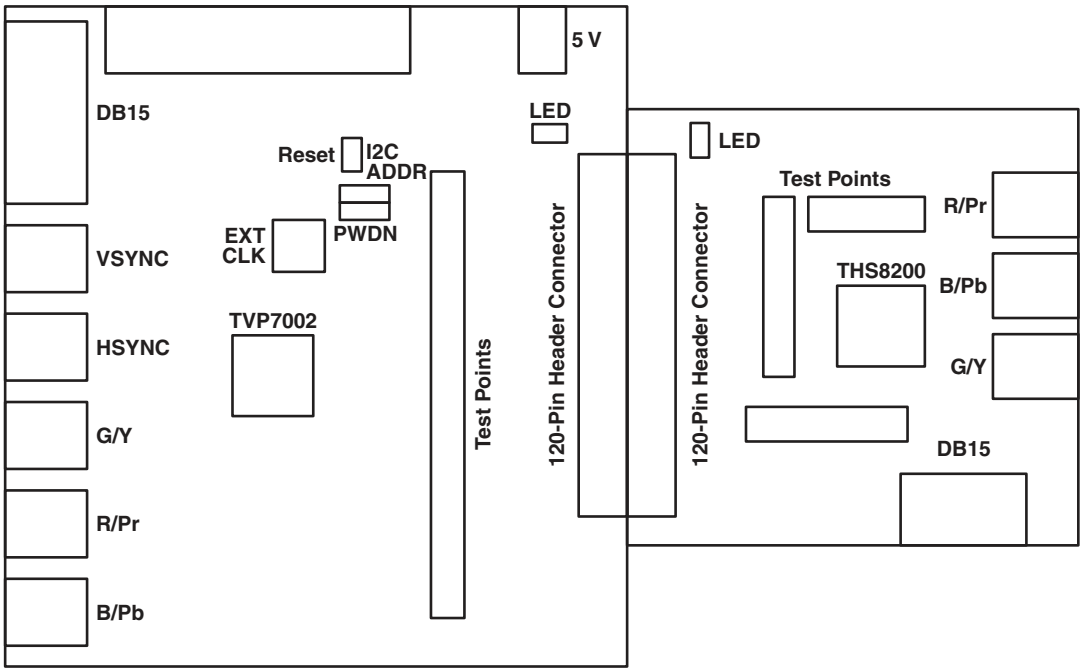


Figure 1-1. TVP7002EVM Block Diagram

1.3.1 Analog Inputs

The TVP7002EVM uses all the available inputs on the TVP7002 triple ADC. The following inputs are available for use:

- Five BNC connectors (Y/G, Pb/B, Pr/R, HSYNC, and VSYNC)
- One DB15 graphics connector (Y/G, Pb/B, Pr/R, HSYNC, and VSYNC)

Table 1-1 shows the pins used for the inputs described above.

Table 1-1. Analog Inputs and Pin Terminals

Input Type	TVP7002 Pins
5-BNC	RIN_1, GIN_1, BIN_1, VSYNC_B, HSYNC_B
DB15	RIN_3, GIN_3, BIN_3, VSYNC_A, HSYNC_A

Note: Both the TVP7002 and THS8200 EVMs include PCB footprints for passive (LC) anti-alias and reconstruction filters. Due to the wide variety of formats that are supported, both boards are shipped from the factory with these filters bypassed and unpopulated.

1.3.2 External Reference Clock and External Clock Input

The EVM is shipped with a 27-MHz crystal oscillator that can be used as a stable reference clock (REFCLK) for input format detection. The REFCLK output is connected to pin 80 of the TVP7002 and is used by the TVP7002 to report line length and HSYNC width status for input detection (see Section 4.5.6 for more detail).

An SMA connector (EXTCLK) for use with an external ADC sample clock is also provided. This input is end-terminated with a 50-Ω resistor for use with a lab clock generator and can be routed to pin 80 (EXTCLK) of the TVP7002 with a slight jumper configuration change. An external ADC sample clock can be used by setting the PCLK SEL bit in I²C register 1Ah to 0. Removal of the termination resistor may be required for some clock sources incapable of driving the 50-Ω load.

Note: The EVM is shipped from the factory with the 27-MHz oscillator connected to pin 80 of the TVP7002. To use the EXTCLK, the 0-Ω resistor installed at J3 can be moved from the OSC position to the EXT position.

1.3.3 Test Points and Jumpers

Various test points are available on the TVP7002EVM. This includes DCLK (DATACLK), HS (HSOUT), VS (VSOUT), DE_FID, SOG_OUT, SDA, SCL, power, and GND. Each test point is clearly labeled on the TVP7002EVM silkscreen. The primary test-point headers for the TVP7002 are H2, H3, and H4, which provide access to the red, green, and blue data, respectively.

There are two jumpers on the TVP7002 board that configure the power-down mode and I²C address select. Each jumper is set by default in its preferred state for the TVP7002EVM. Near each jumper on the TVP7002 board is a silkscreen that describes the two states of the jumper configuration.

Table 1-2. I²C Address Selection Jumper (I2C ADDR)

I2C ADDR Jumper	I²C Address
1 - 2	0xB8
2 - 3	0xBA

Table 1-3. Power Down Mode Selection Jumper (PWDN)

PWDN Jumper	Operation
1 - 2	Normal operation
2 - 3	Power down

Note: If the I²C address is changed on either the TVP7002 board or the THS8200 board while the TVP7002EVM is powered up, then that device does not recognize the new I²C address. The reset button on the TVP7002EVM must be pressed, and WinVCC4 must be reconfigured for the new I²C address.

1.3.4 Common Board Interface

The TVP7002EVM uses a 120-pin connector to connect the TVP7002 board (P3) to the THS8200 board (P2). This interface shares all common signals including the I²C and the 5-V supply. This modularizes the TVP7002 board and allows users to interface it to a variety of other Texas Instruments products including DVI transmitters, video encoders, or to any other platform that shares the same interface.

This connector shares all digital video data (R[9:0], G[9:0], and B[9:0]), all video clocks (DCLK_OUT, VSYNC, and HSYNC), RESET, I²C, and 5 V as mentioned above.

1.3.5 Component Analog Outputs

The THS8200 board provides component analog outputs to a display RGB or YPbPr formats. The configuration settings for the TVP7002EVM use the RGB color space for PC graphics and the YPbPr color space for video (480i to 1080p).

1.4 System Level Description

The system block diagram in Figure 1-2 gives an example of how the TVP7002EVM may be used for evaluation. Typically, an RGB or YPbPr component analog input is provided by a graphics/video source such as a pattern generator or a DVD player.

The TVP7002EVM is configured with the provided 5-V supply and the parallel port cable. The output is provided by the THS8200 triple DAC to convert the digital data from the TVP7002 back to analog. This analog output is then fed into a display monitor.

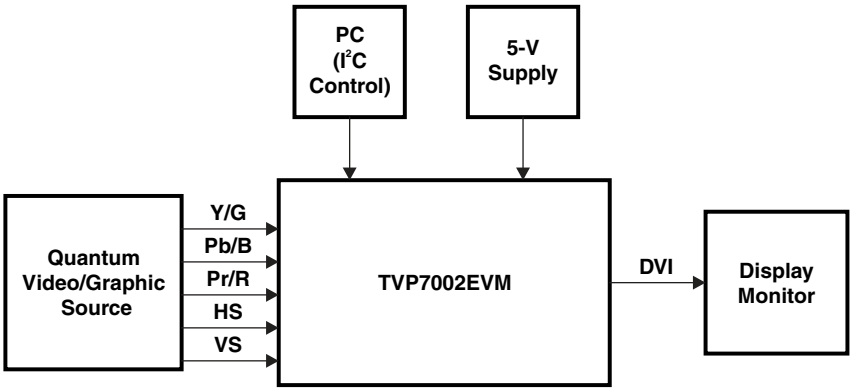


Figure 1-2. TVP7002EVM System Level Block Diagram

Hardware and Software Setup

2.1 Required Hardware and Equipment

The required hardware and equipment necessary to use the TVP7002EVM are:

- TVP7002EVM (provided)
- Universal 5-V power supply (provided)
- Parallel cable (provided)
- Windows-based PC
- One cable with five BNC connectors (RGB, HS, VS)
- One cable with three BNC connectors (RGB or YPbPr)
- Two DB15 PC cables
- Video source (multiformat video/graphics signal generator or DVD player)
- Display monitor that supports PC graphics and video up to 1080p

2.2 Hardware Setup

Perform the following steps to set up the hardware for the TVP7002EVM:

1. Connect the TVP7002 board and the THS8200 board using the 120-pin board connector. The two boards connected together are called the TVP7002EVM.
2. Connect a video or graphics source to the DB15 input connector or the RGB, HSYNC, and VSYNC input connectors of the TVP7002 EVM. The HSYNC and VSYNC input connections are not required if component video sources with sync-on-y are used.
3. Depending on the desired output format, connect either a graphics DB15 cable or video BNC cable to the output of the THS8200 board.
4. Connect the parallel port cable from the TVP7002EVM to the PC.

Note: There are footprints for a dc jack on the THS8200 board, but the default power is provided by the TVP7002 board via the 120-pin connector, P3.

5. Connect the 5-V power supply to the dc jack on the TVP7002 board. A green LED on each board should light.

2.3 Software Installation

WinVCC4 is a Windows application that uses the PC parallel port to emulate I^2C, providing access to each device on the I^2C bus. WinVCC4 makes use of CMD files, a text editable file that allows preset video setups to be programmed easily.

This feature allows the user to easily set multiple I^2C registers with the press of a button. WinVCC4 also has property sheets for the TVP7002, which allows the user to control the I^2C registers with a graphical user interface (GUI).

All necessary software for the TVP7002EVM is provided on the enclosed CD. Perform the following steps to install WinVCC4:

1. Explore the provided TVP7002EVM software CD.
2. Run Port95NT.exe to install the parallel port driver used by WinVCC4.
   This driver must be installed, and the PC must be rebooted before WinVCC4 can operate correctly.
3. Run Setup.exe to install WinVCC4.
   Click Next at all prompts and click Finish to complete the installation process. No reboot is required.
4. Run WinVCC4.exe

Note: A shortcut to WinVCC4 should now be available on the desktop. Another shortcut to WinVCC4 and additional TVP7002 related documentation can be found at Start>Programs>TVP7002EVM Software.

Perform the following steps to enable video output from the TVP7002EVM.

1. Run WinVCC4. When the WinVCC4 Configuration screen appears, use it to configure the I²C bus.
2. Next to TVP7002, select the TVP7002 and ensure the I²C address is set to 0xB8. The address selected here must match the address selected by the I2C ADDR jumper on the TVP7002 board.
3. Next to THS8200, select the THS8200 and ensure the I²C address is set to 0x40. The address selected here must match the address selected by the I2C ADDR jumper on the THS8200 board.

Note: If WinVCC4 is running and the TVP7002 or THS8200 board I²C address is changed, then power must be cycled on the EVM to enable the EVM to use the new address.

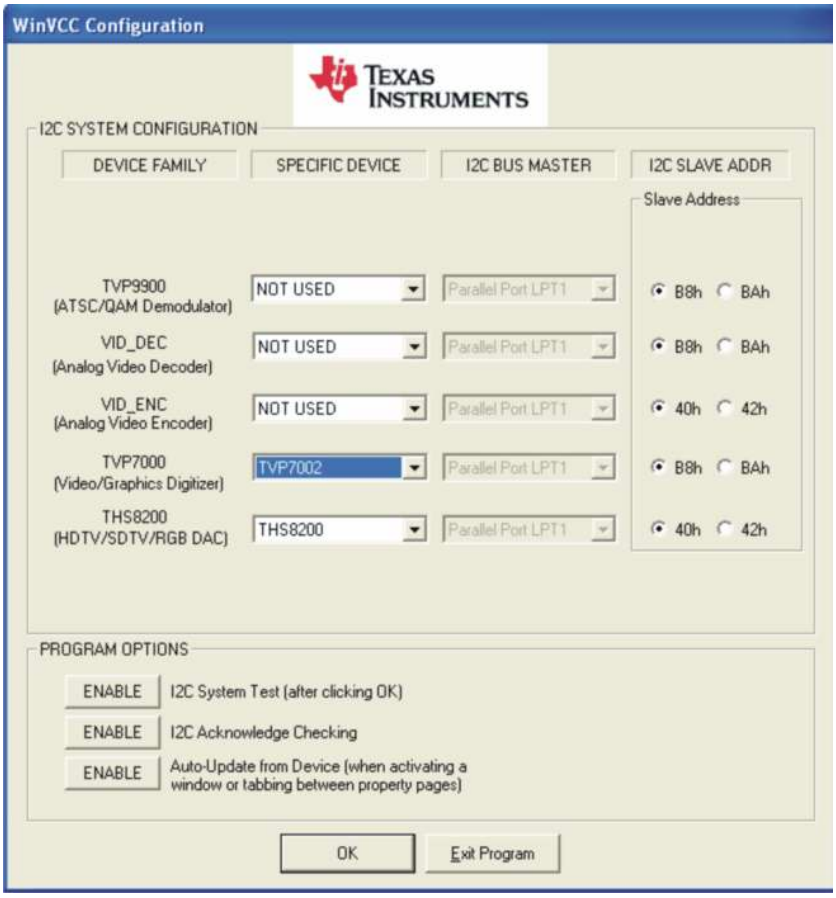


Figure 3-1. WinVCC4 – I²C Configuration Screen

4. Ensure that all other boxes are selected as "Not Used" and that all program options buttons are set to ENABLE. Click OK.
5. If there are no I²C communication problems, then the Main Screen window displays next. If there are I²C problems, then an I²C Test Report box displays. Completely exit out of WinVCC4, double-check the parallel port cable connections, cycle power on the TVP7002EVM, and run WinVCC4 again.

6. Load the provided TVP7002EVM.CMD file into WinVCC4 by clicking on Tools>System Initialization>Browse. The default directory is c:\Program Files\Texas Instruments\TVP7002EVM\Initialization.

Figure 3-2. WinVCC4 – Main Screen

7. Click the desired "TVP7002 + THS8200_..." dataset in the window, and then click the Program Dataset button to initialize the TVP7002EVM.

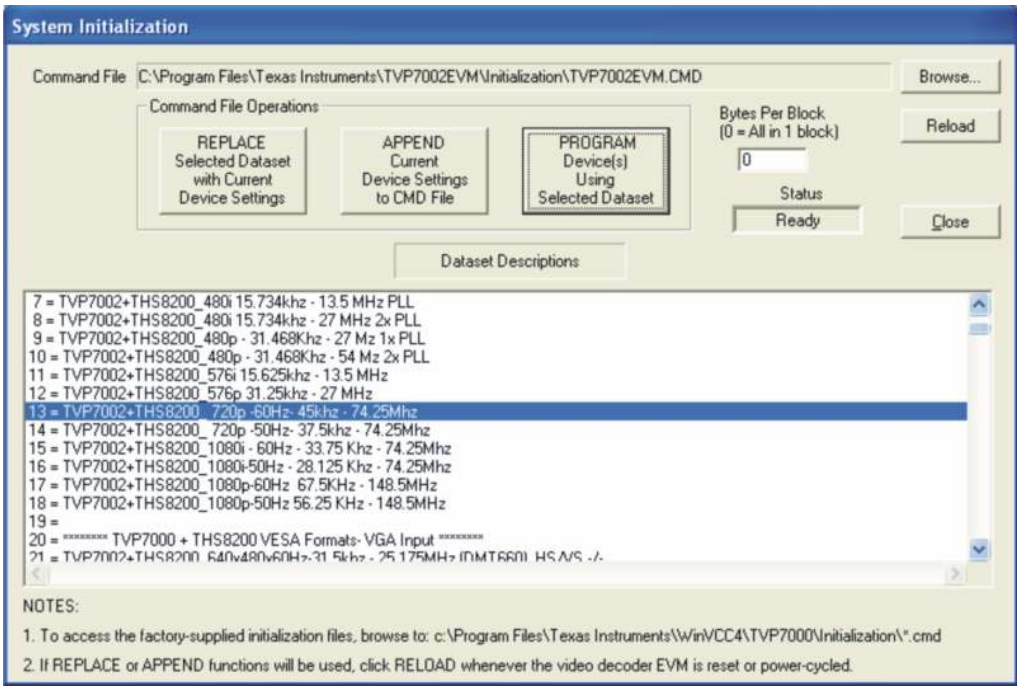


Figure 3-3. WinVCC4 – System Initialization

8. With a graphics/video source provided at the BNC or DB15 connectors and with the proper resolution configured, video or graphics should be viewable on the display monitor.

Note: To ensure that the TVP7002 is working properly, go to Status and check the HSYNC and VSYNC detection status. If using the YPbPr inputs with sync-on-y, then the SOG status should indicate "DETECTED", and the HSYNC and VSYNC input status should indicate "FROM SOG" and "FROM SYNC SEP", respectively.

WinVCC4 in Depth

This chapter describes in depth how to use WinVCC4. The various features and screens that the user may encounter while evaluating the TVP7002EVM are described.

4.1 Starting WinVCC4

The Port95NT parallel port driver must be installed before using WinVCC4. WinVCC4 may be started by clicking on Start>All Programs>TVP7002EVM Software>WinVCC4.

If the dialog box shown in Figure 4-1 is displayed, one of two things is indicated:

1. WinVCC4 did not run to completion the last time it ran. In this case, click OK to exit the program and restart WinVCC4.
2. There is more than one instance of WinVCC4 running at the same time. In this case:
   a. Click OK to exit the program.
   b. Press CTRL-ALT-DELETE to open the Task Manager.
   c. Select and click End Task for all occurrences of WinVCC4 or WinVCC4 CONFIGURATION.
   d. Restart WinVCC4.

Figure 4-1. WinVCC4 Multiple Occurrences Error Message

4.2 WinVCC4 Configuration Dialog Box

The WinVCC4 Configuration dialog box (see Figure 4-2) should now be visible. This dialog box configures the I^2C bus on the TVP7002EVM. All settings from this dialog box are stored in the Windows registry and are restored the next time the program is started. After initial installation, TVP7000 Video and Graphics Digitizer drop down box is set to TVP7002.

The I^2C slave address for each device must match the I^2C slave address selected by jumpers on the TVP7002EVM. These jumpers are set by the factory to use 0xB8 for the TVP7002 and 0x40 for the THS8200 transmitter.

It is also important to ensure that only the TVP7002 is selected when using the TVP7002EVM. All Program Options must be enabled. Disabling these options is required only if debugging a problem with the I^2C bus.

Click OK to begin I^2C communication with the selected devices.

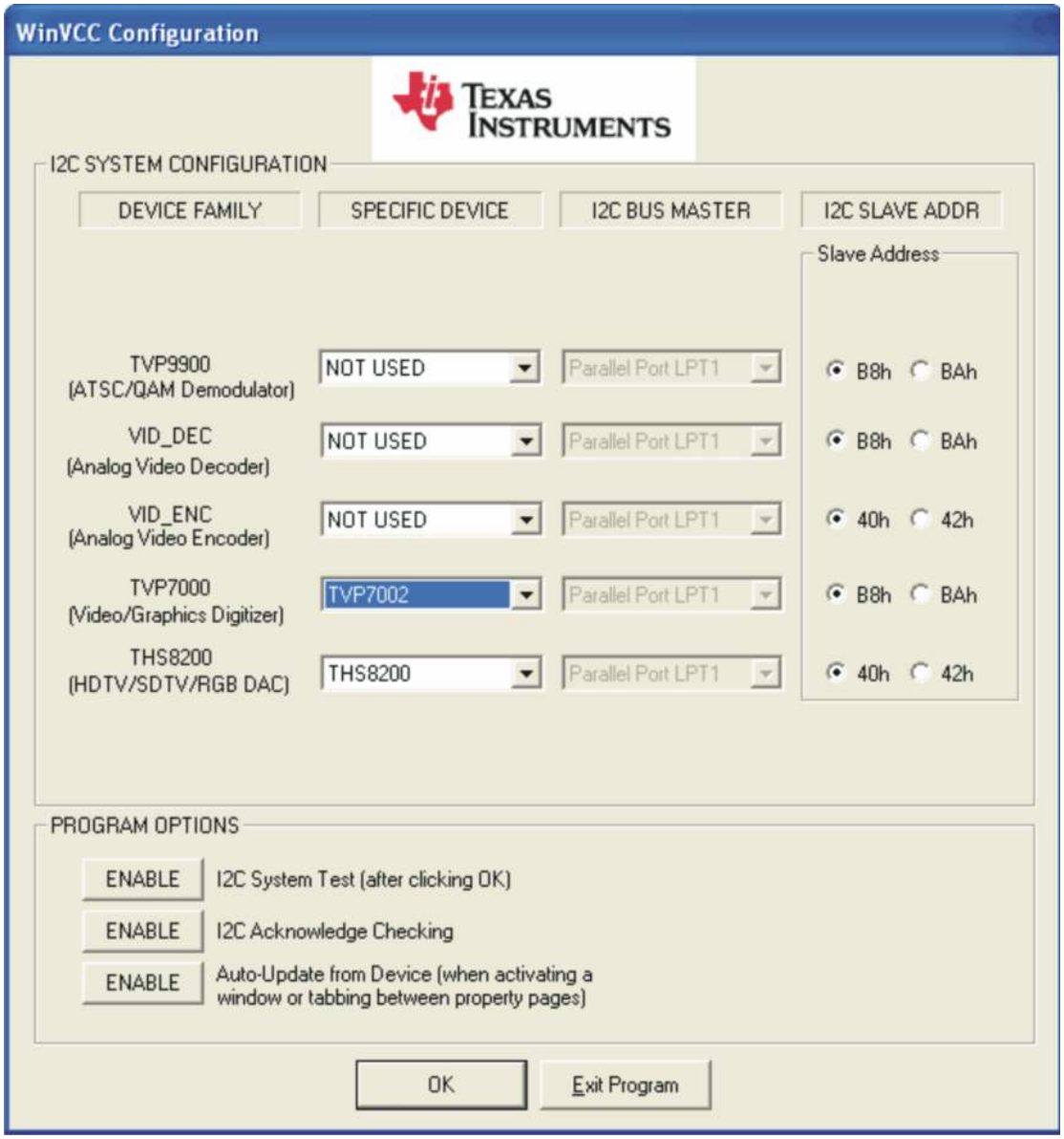


Figure 4-2. WinVCC4 I²C Address Configuration

4.3 I²C System Test

The I²C system test of selected registers runs immediately after closing the WinVCC4 Configuration dialog box by clicking OK (unless the I²C system test program options button was disabled).

If the I²C system test passes, then only a PASS message appears. If the test failed, then a dialog box appears (see Figure 4-3). See Chapter 5 for details on how to resolve this issue.

The I²C system test can be run at anytime by clicking Run System I²C Test in the Tools menu.

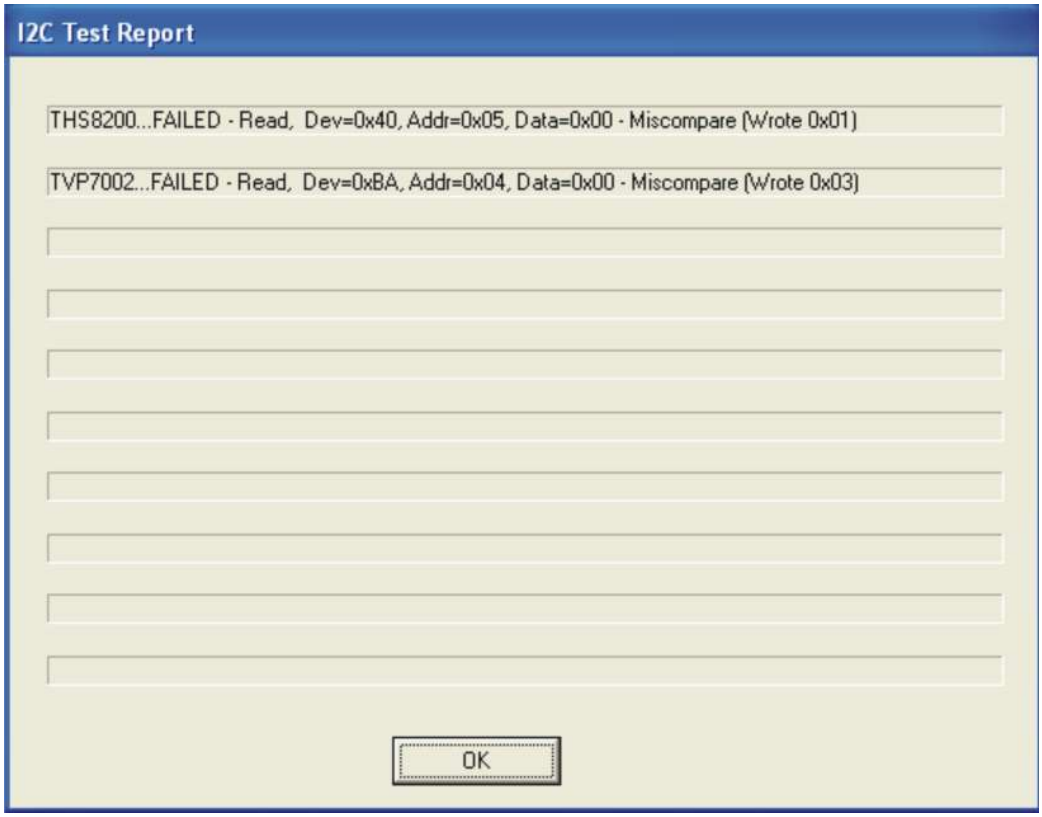


Figure 4-3. I²C System Failure

4.4 Main Menu

After configuring the I²C, the main menu is displayed as shown in Figure 4-4. The menus that are used to operate WinVCC4 are File, Edit, Tools, Window, and Help. The File menu's only function is Exit, which terminates the program. Table 4-1 summarizes the main menu contents.

Figure 4-4. WinVCC4 – Main Screen

Table 4-1. Main Menu Summary

Menu	Contents
File	Exit
Edit	Register Map TVP7002PNP Generic I²C Editor Property Sheets TVP7002PNP
Tools	System Initialization Real-time Polling TV Tuner Control (FQ12xx series only) Multiple-Byte I²C Transfers Set I²C Bit Rate Run System I²C Test Run Continuous I²C Test Read VBI FIFO Capture Live VBI Data
Window	Allows selection of the active window. Multiple windows can be open at the same time.
Help	Displays program version

4.4.1 System Initialization

Click System Initialization in the Tools menu to display the dialog box shown in Figure 4-5. This dialog box provides the means for initializing the TVP7002 triple ADC and/or THS8200 for a particular video mode. The details of the initialization are contained in the command file (with a CMD file extension).

The command file is loaded using the Browse… button. Once the command file is opened, a text list displays descriptions of the individual datasets contained within the command file.

Click once on the desired dataset description to select it. Click the Program Device(s) Using Selected Dataset button to run the selected dataset, which loads the devices via the I²C bus. When the device initialization has completed, the status indicator displays Ready.

Note: If Ready does not display, then the devices are not initialized and the I²C bus is not communicating. See Chapter 5 for possible solutions.

Click the OK button to close the dialog box. Each time the System Initialization dialog box is closed, the initialization file pathname and the dataset selection number are saved in the Windows registry to allow these settings to be retained for the next time WinVCC4 runs.

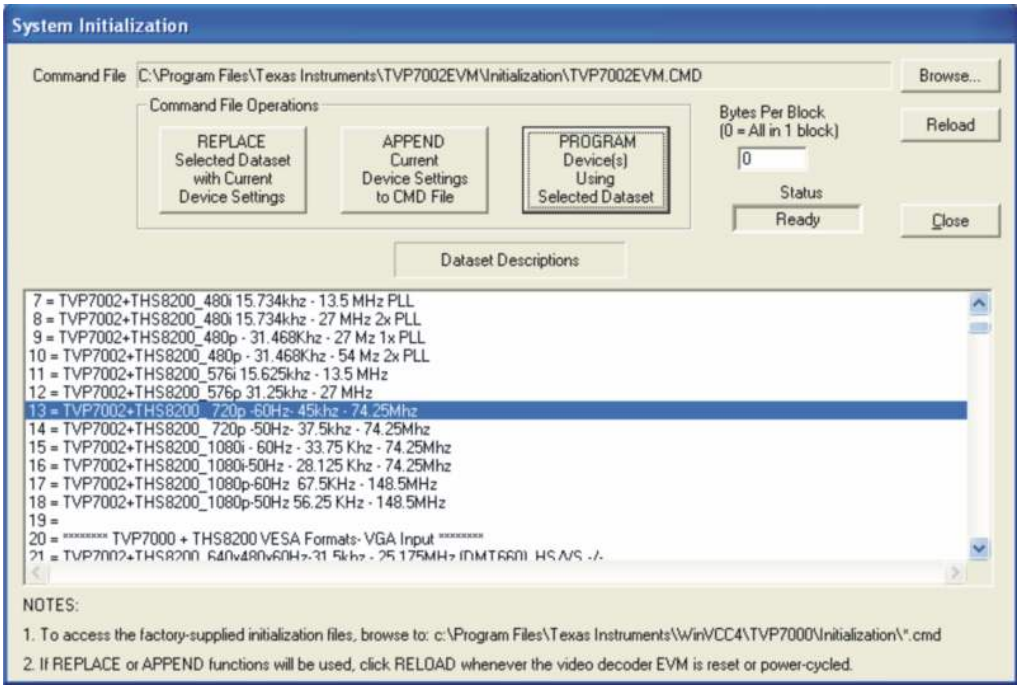


Figure 4-5. System Initialization

4.4.1.1 Adding a Custom Dataset

After programming the EVM via the System Initialization tool using the factory-supplied command file through the Property Sheets tool, the device register settings can be customized. Perform the following steps to save the custom settings:

1. Reopen the System Initialization dialog box via the Tools menu.
2. Click the Append Current Device Settings to Command File button. A dialog box requesting a description of the new dataset appears.
3. Optionally, click the dropdown box and select one of the existing descriptions.
4. Modify the description text or type a description.
5. Click OK. All nondefault register values from the TVP7002 and THS8200 are appended to the current command file as an additional dataset.

Select the custom dataset and send it by pressing the Program… button.

Note: The command file (.CMD) must be saved as plain text.

4.4.1.2 Command Files

The command file is a text file that can be generated using any common editor; however, it must be saved as plain text. Command files are especially useful for quickly switching between the various system configurations. These .CMD files are unrelated to the typical Windows .CMD files.

A default command file has been provided on the CD. This command file contains most of the desired setups. This command file is located at:

c:\Program Files\Texas Instruments\TVP7002EVM\Initialization\TVP7002EVM.cmd

A command file can contain up to 250 datasets. A dataset is a set of register settings to initialize the TVP7002 triple ADC and/or THS8200 for a particular video mode. Each dataset includes a description that is displayed in one row of the dataset descriptions list. The register settings may be located in the command file itself and/or may be stored in separate include file(s) (with an .INC file extension) and be included into the command file using the INCLUDE statement.

4.4.1.3 Example Command File

The following is an example of one dataset within a command file.

```
////////////////////////////////////////////////////////////////////////////

BEGIN_DATASET  //

DATASET_NAME,"TVP7002+THS8200_720p-60Hz- 45khz - 74.25Mhz"

//TVP7002
WR_REG,TVP7000,0x01,0x01,0x67 // PLL DIVMSB  1650
WR_REG,TVP7000,0x01,0x02,0x20 // PLL DIVLSB
WR_REG,TVP7000,0x01,0x03,0xA0 // VCO2_CP3_RR_CP_R
WR_REG,TVP7000,0x01,0x04,0x80 // PHASE SEL(5) CKDI CKDI DIV2
WR_REG,TVP7000,0x01,0x05,0x32 // CLAMP START
WR_REG,TVP7000,0x01,0x06,0x20 // CLAMP WIDTH
WR_REG,TVP7000,0x01,0x07,0x28 // HSYNC OUTPUT WIDTH - 40
WR_REG,TVP7000,0x01,0x08,0x3C // Blue Fine Gain
WR_REG,TVP7000,0x01,0x09,0x3C // Green Fine Gain
WR_REG,TVP7000,0x01,0x0A,0x3C // Red Fine Gain
WR_REG,TVP7000,0x01,0x0B,0x80 // Blue Fine Offset
WR_REG,TVP7000,0x01,0x0C,0x80 // Green Fine Offset
WR_REG,TVP7000,0x01,0x0D,0x80 // Red Fine Offset
WR_REG,TVP7000,0x01,0x0E,0x24 // SYNC CONTROL    HSout+ VSout+
WR_REG,TVP7000,0x01,0x0F,0x2E // PLL and CLAMP CONTROL
WR_REG,TVP7000,0x01,0x10,0x5D // SOG Threshold-(YPbPr Clamp)
WR_REG,TVP7000,0x01,0x11,0x40 // SYNC SEPERATOR THRESHOLD
WR_REG,TVP7000,0x01,0x12,0x01 // PRE_COAST
WR_REG,TVP7000,0x01,0x13,0x00 // POST_COAST
WR_REG,TVP7000,0x01,0x15,0x04 // Output Formatter
WR_REG,TVP7000,0x01,0x17,0x00 // MISC Control 2  FID out, Enable Outputs
WR_REG,TVP7000,0x01,0x18,0x01 // MISC Control 3 Clock polarity
WR_REG,TVP7000,0x01,0x19,0x00 // INPUT MUX SELECT CH1 selected (BNC )
WR_REG,TVP7000,0x01,0x1A,0xC7 // INPUT MUX SELECT2,SOG/Clamp filter, HSYNC_B and
VSYNC_B
WR_REG,TVP7000,0x01,0x1B,0x77 // Default Blue and Green coarse analog gain
WR_REG,TVP7000,0x01,0x1C,0x07 // Default Red coarse analog gain
WR_REG,TVP7000,0x01,0x21,0x35 // HSOUT START (13+40)
WR_REG,TVP7000,0x01,0x22,0x00 // MACEN=0
WR_REG,TVP7000,0x01,0x26,0x80 // ALC Enable
WR_REG,TVP7000,0x01,0x28,0x53 // Default ALC FILTER Control
WR_REG,TVP7000,0x01,0x2A,0x87 // CM Offset, Enable FINE CLAMP CONTROL
WR_REG,TVP7000,0x01,0x2B,0x00 // POWER CONTROL-SOG ON
WR_REG,TVP7000,0x01,0x2C,0x50 // ADC Setup
WR_REG,TVP7000,0x01,0x2D,0x00 // Coarse Clamp OFF
WR_REG,TVP7000,0x01,0x2E,0x80 // SOG Clamp ON
WR_REG,TVP7000,0x01,0x31,0x5A // ALC PLACEMENT
WR_REG,TVP7000,0x01,0x34,0x07 // Macrovision Stripper Width
WR_REG,TVP7000,0x01,0x35,0x00 // VSout Align
WR_REG,TVP7000,0x01,0x36,0x00 // Sync Bypass
WR_REG,TVP7000,0x01,0x3D,0x06 // Line Length Tolerance
WR_REG,TVP7000,0x01,0x3F,0x0F //Video B/W control
WR_REG,TVP7000,0x01,0x40,0x39 // AVID Start  313 (300+13)
WR_REG,TVP7000,0x01,0x41,0x01 // AVID Start
```

```
WR_REG,TVP7000,0x01,0x42,0x39 // AVID Stop  1593 (313 + 1280)
WR_REG,TVP7000,0x01,0x43,0x06 // AVID Stop
WR_REG,TVP7000,0x01,0x44,0x05 // VBLK F0 Offset
WR_REG,TVP7000,0x01,0x45,0x05 // VBLK F1 Offset
WR_REG,TVP7000,0x01,0x46,0x1E // VBLK F0 Duration 30 lines
WR_REG,TVP7000,0x01,0x47,0x1E // VBLK F1 Duration

//THS8200 720p-60Hz

WR_REG,THS8200,0x01,0x03,0x01 // chip_ctl
// CSC not used
WR_REG,THS8200,0x01,0x19,0x03 // csc_offset3  - CSC bypassed
WR_REG,THS8200,0x01,0x1C,0x60 // dman_cntl  - 30 bit input format

// composite sync amplitude control
WR_REG,THS8200,0x01,0x1D,0x00 // dtg_y_sync1
WR_REG,THS8200,0x01,0x1E,0x49 // dtg_y_sync2
WR_REG,THS8200,0x01,0x1F,0xB6 // dtg_y_sync3
WR_REG,THS8200,0x01,0x20,0x00 // dtg_cbcr_sync1
WR_REG,THS8200,0x01,0x21,0x00 // dtg_cbcr_sync2
WR_REG,THS8200,0x01,0x22,0x00 // dtg_cbcr_sync3
WR_REG,THS8200,0x01,0x23,0x23 // dtg_y_sync_upper
WR_REG,THS8200,0x01,0x24,0x2A // dtg_cbcr_sync_upper
// horizontal timing setup
WR_REG,THS8200,0x01,0x25,0x28 // dtg_spec_a
WR_REG,THS8200,0x01,0x26,0x6E // dtg_spec_b
WR_REG,THS8200,0x01,0x27,0x28 // dtg_spec_c
WR_REG,THS8200,0x01,0x28,0x04 // dtg_spec_d
WR_REG,THS8200,0x01,0x29,0x00 // dtg_spec_d1
WR_REG,THS8200,0x01,0x2A,0x04 // dtg_spec_e
WR_REG,THS8200,0x01,0x2B,0xC0 // dtg_spec_h_msb
WR_REG,THS8200,0x01,0x2C,0x00 // dtg_spec_h_lsb
WR_REG,THS8200,0x01,0x2D,0x00 // dtg_spec_i_msb
WR_REG,THS8200,0x01,0x2E,0x00 // dtg_spec_i_lsb
WR_REG,THS8200,0x01,0x2F,0x6E // dtg_spec_k_lsb
WR_REG,THS8200,0x01,0x30,0x00 // dtg_spec_k_msb
WR_REG,THS8200,0x01,0x31,0x00 // dtg_spec_k1
WR_REG,THS8200,0x01,0x32,0x00 // dtg_speg_g_lsb
WR_REG,THS8200,0x01,0x33,0x00 // dtg_speg_g_msb
WR_REG,THS8200,0x01,0x34,0x06 // dtg_total_pixel_msb
WR_REG,THS8200,0x01,0x35,0x72 // dtg_total_pixel_lsb
WR_REG,THS8200,0x01,0x36,0x80 // dtg_linecnt_msb
WR_REG,THS8200,0x01,0x37,0x02 // dtg_linecnt_lsb
WR_REG,THS8200,0x01,0x38,0x82 // dtg_mode  - 720p
WR_REG,THS8200,0x01,0x39,0x27 // dtg_frame_field_msb
WR_REG,THS8200,0x01,0x3A,0xEE // dtg_frame_size_lsb
WR_REG,THS8200,0x01,0x3B,0xFF // dtg_field_size_lsb
// CSM setup not required if full-scale range is used
WR_REG,THS8200,0x01,0x4F,0x00 // csm_mode disabled
//discrete output sync control
WR_REG,THS8200,0x01,0x70,0x18 // dtg_hlength_lsb
WR_REG,THS8200,0x01,0x71,0x06 // dtg_hdly_msb
WR_REG,THS8200,0x01,0x72,0x49 // dtg_hdly_lsb
WR_REG,THS8200,0x01,0x73,0x1A // dtg_vlength_lsb
WR_REG,THS8200,0x01,0x74,0x00 // dtg_vdly_msb
WR_REG,THS8200,0x01,0x75,0x01 // dtg_vdly_lsb
WR_REG,THS8200,0x01,0x76,0x00 // dtg_vlength2_lsb
WR_REG,THS8200,0x01,0x77,0xC7 // dtg_vdly2_msb
WR_REG,THS8200,0x01,0x78,0x07 // dtg_vdly2_lsb
// discrete input sync control - use to align picture
```

```
WR_REG,THS8200,0x01,0x79,0x00 // dtg_hs_in_dly_msb
WR_REG,THS8200,0x01,0x7A,0x0F // dtg_hs_in_dly_lsb   - adjust horizontal position
WR_REG,THS8200,0x01,0x7B,0x00 // dtg_vs_in_dly_msb
WR_REG,THS8200,0x01,0x7C,0x01 // dtg_vs_in_dly_lsb  - adjust vertical position
WR_REG,THS8200,0x01,0x82,0x1B // pol_cntl,external FID

END_DATASET
////////////////////////////////////////////////////////////////////////////
```

Each command file may contain individual write-to-register (WR_REG) commands.

1. The comment indicator is the double-slash //.
2. The command file is not case-sensitive and ignores all white-space characters.
3. All numbers can be entered as hexadecimal (beginning with 0x) or as decimal.
4. Every dataset in a command file begins with BEGIN_DATASET and ends with END_DATASET. The maximum number of datasets is 250.
5. The dataset text description is entered between double quotes using the DATASET_NAME command. The enclosed text can be up to 128 characters in length. This text appears in the System Initialization dialog box when the command file is opened.
6. The INCLUDE command inserts the contents of an include file (with an .INC file extension) in-line in place of the INCLUDE command. Therefore, the include file must not contain the BEGIN_DATASET, END_DATASET, and DATASET_NAME commands.

   Note: All included files must be located in the same directory as the command (CMD) file.

7. The write-to-register command is written as follows:

   WR_REG, <DeviceFamily>, <Number of data bytes (N)>, <subaddress>, <Data1>,…, <DataN>

   or

   WR_REG, <Literal slave address>, <Number of data bytes (N)>, <subaddress>, <Data1>,…, <DataN>

   The valid device family mnemonics are:

   VID_DEC for the video decoders
   VID_ENC for the video encoders
   THS8200 for the THS8200 device

   WinVCC4 translates the device family mnemonic to the slave address that was selected in the WinVCC4 Configuration dialog box upon program startup. This eliminates having to edit command files if the alternate slave address must be used.

   If the literal slave address method is used, then the slave address entered is used directly. This method is normally used for programming the video encoder.
8. A delay may be inserted between commands using the WAIT command, which is written as follows:

   WAIT,<# milliseconds>

4.4.2 Register Editing

The following sections describe the available modes of register editing: Register Map Editor, Encoder Module Editor, Generic I^2C Register Editor, and Property Sheets. Each of these functions can be selected from the Edit menu.

4.4.2.1 Register Map Editor

The register map editor (see Figure 4-6 and Figure 4-7) allows the display and editing of the entire used register space of the device within a simple scrolling text box. To open this window, click on Edit Register Map in the Edit menu, and click on the device type to edit. If the intended device type is not shown, then use the Windows menu to activate the existing window.

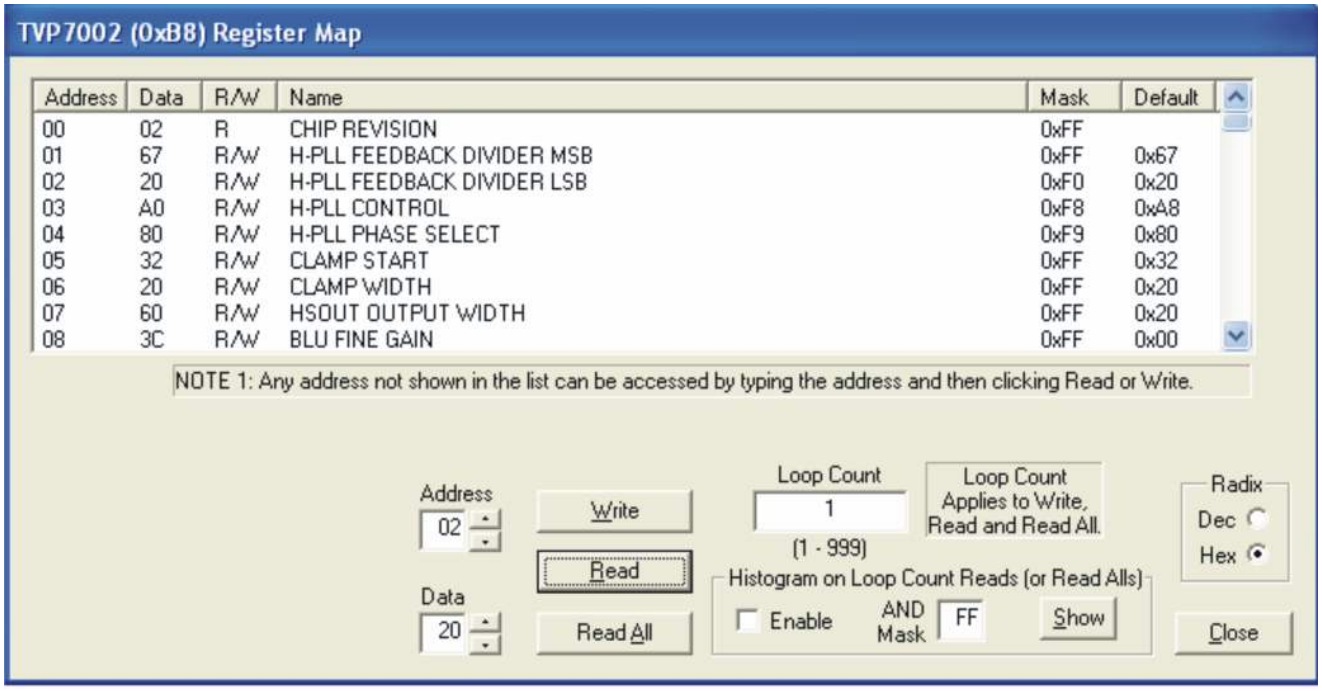


Figure 4-6. TVP7002 Register Map

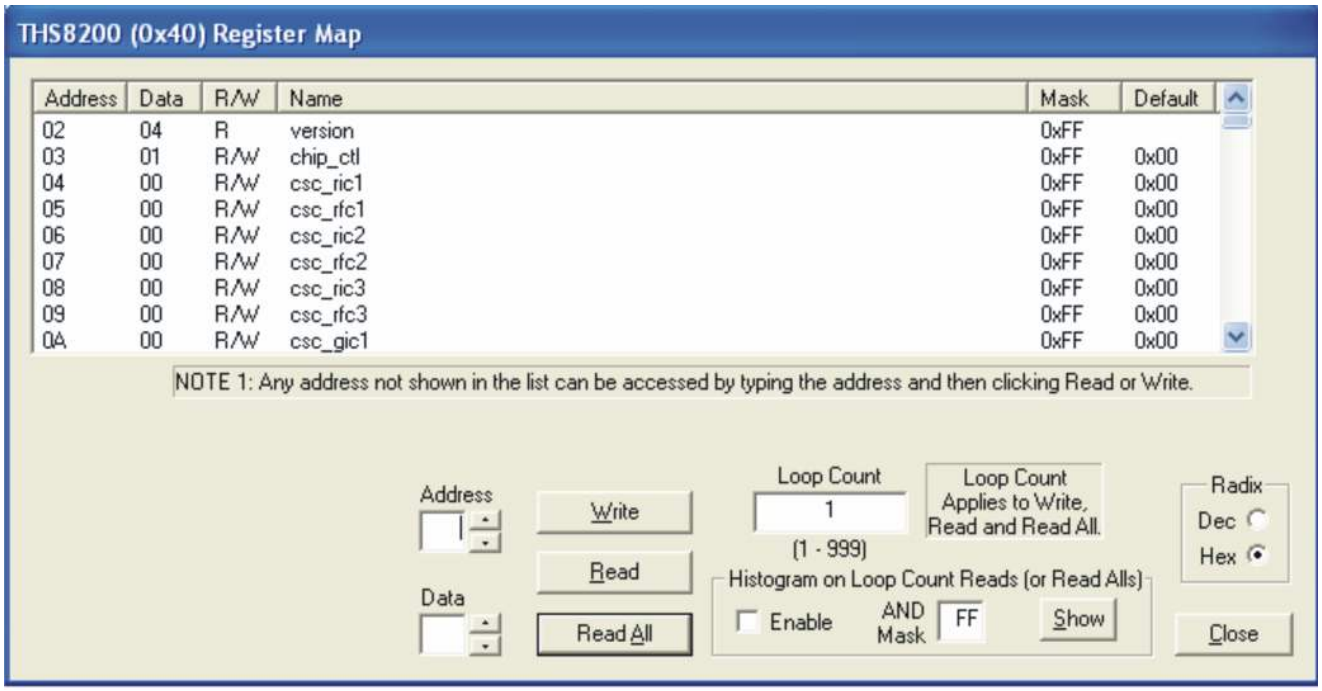


Figure 4-7. THS8200 Register Map

Table 4-2. Register Map Editor Controls

Control	Definition
Register Window	Scrolling text box that displays the address and data for the I²C registers that are defined for the device.
Address Field	This contains the I²C subaddress that is accessed using the Write and Read buttons. Clicking on a row selects an address, which then appears in the address field. Note: After clicking on a row, the Data field contains the data that was in the register window. The device has not yet been read. The address up/down arrows are used to jump to the next/previous subaddress that is defined for the device. If an address is not defined for the device, then it can still be accessed by typing the subaddress in the Address field.
Data Field	This contains the data that is written to or was read from the I²C subaddress. The data up/down arrows increment/decrement the data value by 1.
Write Button	Writes the byte in the Data field to the address in the Address field.
	The I²C register is written to whether or not the data is different from the last time the register was read.
Read Button	Reads the data from the address in the Address field into the Data field and the register window.
Read All Button	Reads all defined readable registers from the device and updates the register window.
Hex Button	Converts all values in the register window and address and data fields to hexadecimal.
Dec Button	Converts all values in the register window and address and data fields to decimal.
Close Button	Closes the dialog. Note: Multiple edit register map windows can be open at the same time (one for each device). Use the Window menu to navigate.
Loop Count	Causes subsequent write or read operations to be performed N times. N is entered as a decimal number from 1 to 999.
Edit Indirect Registers	Opens the indirect register editor of the TVP7002.

4.4.2.2 Generic I²C Register Editor

The Generic I²C Register Editor (see Figure 4-8) allows the display and editing of any device on the I²C bus. This editor works like the Register Map Editor, except that the I²C slave address must be entered and the Read All button is disabled.

To open this window, click on Edit Register Map in the Edit menu and then click on Generic I²C.

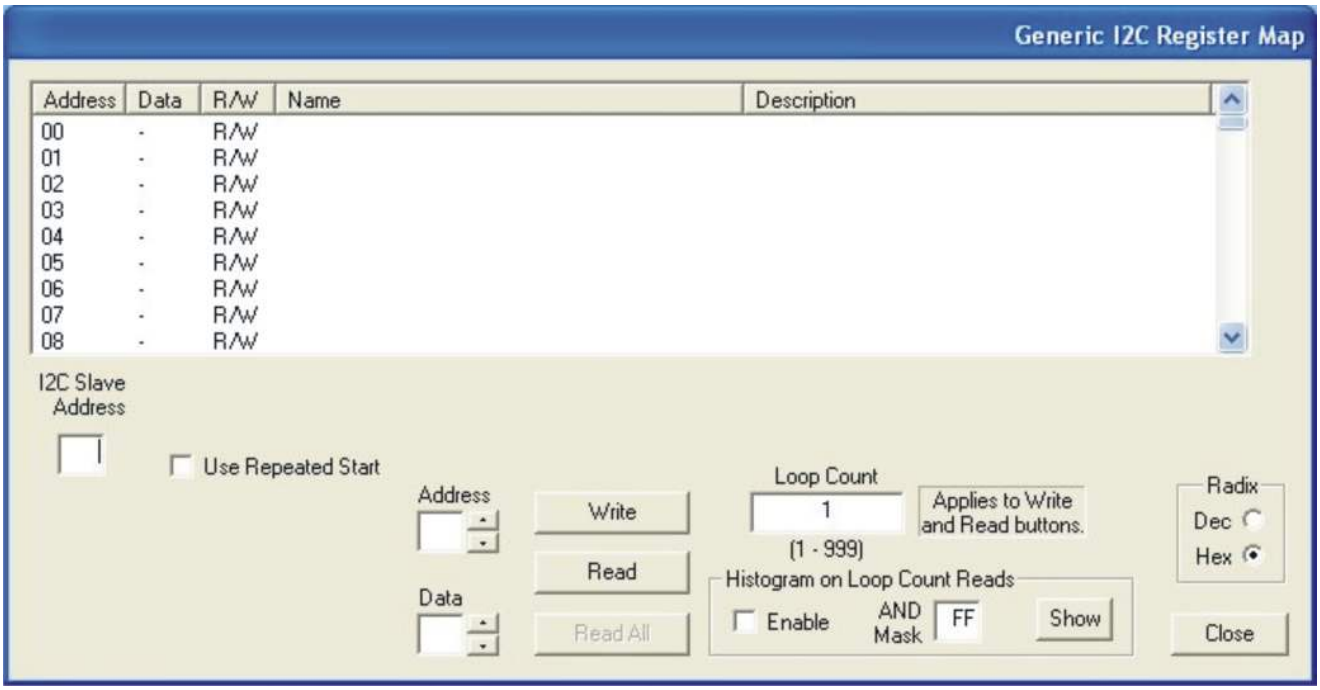


Figure 4-8. Generic I²C Register Editor

4.5 TVP7002 Property Sheets

The property sheets represent the register data in a user-friendly format. The data is organized by function, with each function having its own page and being selectable via tabs at the top.

To open a property sheet, click Edit Property Sheets in the Edit menu and select the device type to edit.

When the property sheet function is started or when tabbing to a different page, all readable registers in the device are read from hardware to initialize the dialog pages. Values on the page are changed by manipulating the various dialog controls.

There are OK, Cancel, and Apply buttons at the bottom of each property page.

With the TVP7002, there are six different tabs available within its property sheets. The tabs are organized by the TVP7002 functions. The following sections describe the additional details and recommendations of the controls within each tab.

4.5.1 Input Mux

The Input Mux Property Sheet provides controls for configuring the input connections and sync options. For most applications, auto detect is recommended for HSYNC/VSYNC selection and HSYNC input polarity. The TVP7002 automatically senses the presence of SOG and discrete HSYNC/VSYNC inputs. If SOG and discrete syncs are both present, then the TVP7002 automatically selects and uses the discrete syncs. Input sync status is available in the sync detect status I^2C register (14h) and can be viewed using the status property sheet. The BNC connectors on the TVP7002 EVM inputs must be used for sync-on-green (SOG) or sync-on-y operation.

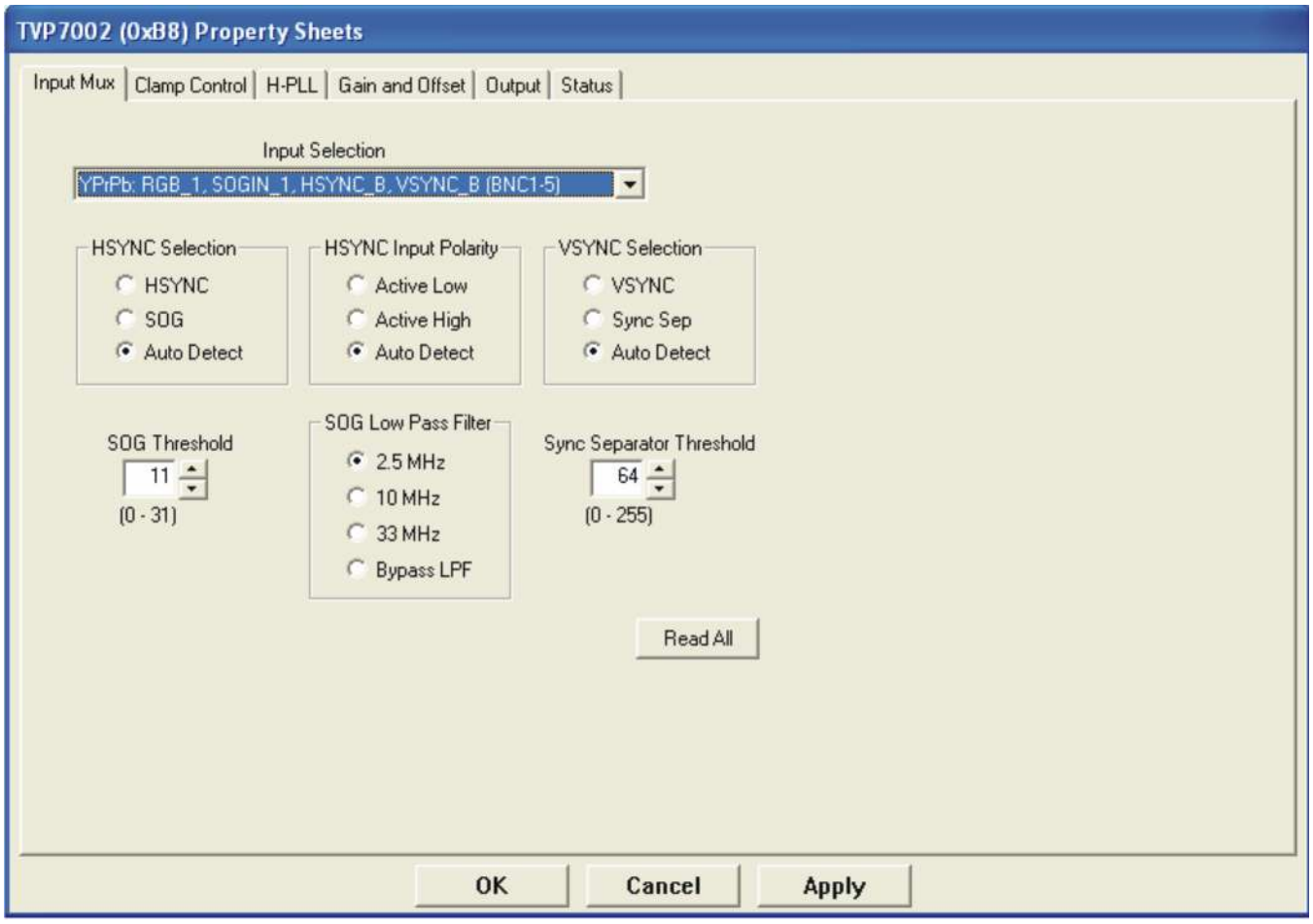


Figure 4-9. Input Mux Property Sheet

The SOG threshold (I^2C register 10h[7:3]) sets the voltage level threshold of the SOG comparator/slicer. Each step represents an 11-mV change in slice level. The default setting of 0Bh can be used for most applications.

The Sync Separator Threshold setting defines the sync separator count interval in internal REFCLK cycles and is used for VSYNC high/low detection and generation. A setting of 64 (40h) should be suitable for all nominal input formats.

A programmable SOG low-pass filter (I^2C register 1Ah[7:6]) is provided to filter glitches or noise that could be present on the SOG input. Recommended settings are shown in Table 4-3.

Table 4-3. Recommended SOG LPF Settings

SDTV Formats	10 MHz
HDTV and PC Graphics	33 MHz or Bypass

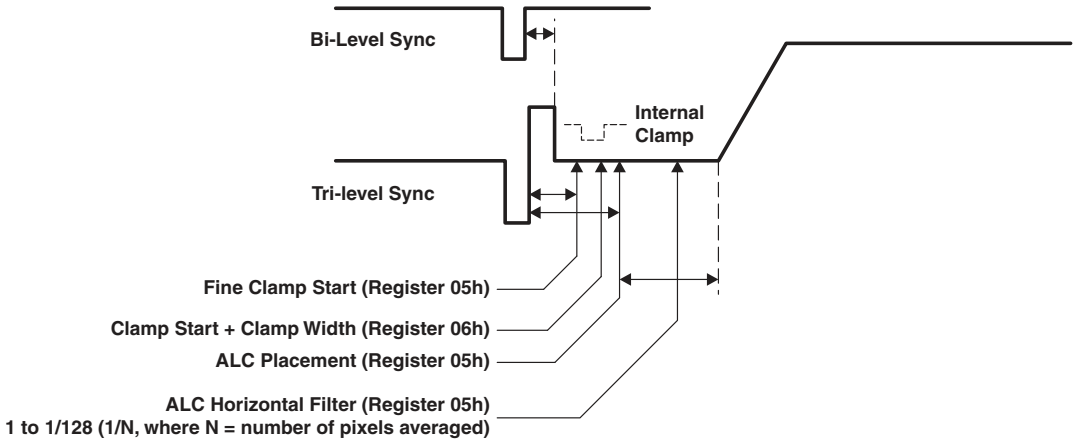
Note: Excessive filtering of high frequency SOG inputs can result in sync tip attenuation and sync processing issues.

Note: SOG filter settings affect SOG analog delay resulting in a slight HSOUT alignment shift. When discrete output syncs are used, the HSOUT start setting on the Output Property Sheet can be used to compensate for this horizontal alignment shift.

4.5.2 Clamp

Most ac-coupled video applications use the internally generated clamp pulse for dc restoration prior to the ADCs. The fine clamp start (I^2C register 05h) is relative to HSYNC trailing or leading edge depending on the Clamp REF bit setting in I^2C register 15h. In most cases, the trailing edge of the negative sync tip is used to avoid clamping during the sync pulse.

The fine clamps must be enabled in I^2C Register 2Ah and correctly positioned during the horizontal blanking interval. See Figure 4-10 for recommended clamp placement settings for various input formats. HDTV formats having tri-level syncs require additional delay to avoid clamping during the tri-level sync interval.



Typical Settings	Clamp Start	Clamp Width	ALC Placement
HDTV (tri-level)	50 (32h)	32 (20h)	90 (5Ah)
SDTV (bi-level)	6 (06h)	16 (10h)	24 (18h)
PC graphics	6 (06h)	16 (10h)	24 (18h)

Figure 4-10. Clamp and ALC Placement

Both clamp and auto-level control (ALC) placement are relative on the HSYNC reference edge selected by the clamp REF bit in I^2C register 15h. Most applications set up the TVP7002 to use the trailing edge of the negative sync tip for placement of the fine clamp and ALC. The maximum ALC horizontal filter setting may be limited by the back porch duration for some formats.

Either bottom-level or middle-level clamping can be selected. These must be set according to the video input format. Bottom-level clamping must be used for Y and RGB inputs. Middle-level clamping must be used for Pb and Pr inputs. Coarse clamp must be left disabled for most applications. A typical clamp setup for RGB graphics is shown in Table 4-4 and Figure 4-11.

Most applications use the internal fine clamp pulse that is automatically generated from the HSYNC input. Clamp polarity is only effective when an external clamp is used.

Note: The maximum ALC horizontal filter setting that can be used with some formats may be limited by the back porch duration.

Table 4-4. Typical Clamp Setup for RGB Graphics

I^2C Address	Setting	Description
05h	06h	Clamp start
06h	10h	Clamp width
0Fh	0Eh	Internal clamp enabled
10h	80h	Bottom-level clamping for RGB
15h	00h	Clamp pulse relative to HSYN trailing edge
2Ah	87h	Enable fine clamps
2Dh	00h	Coarse clamp disabled

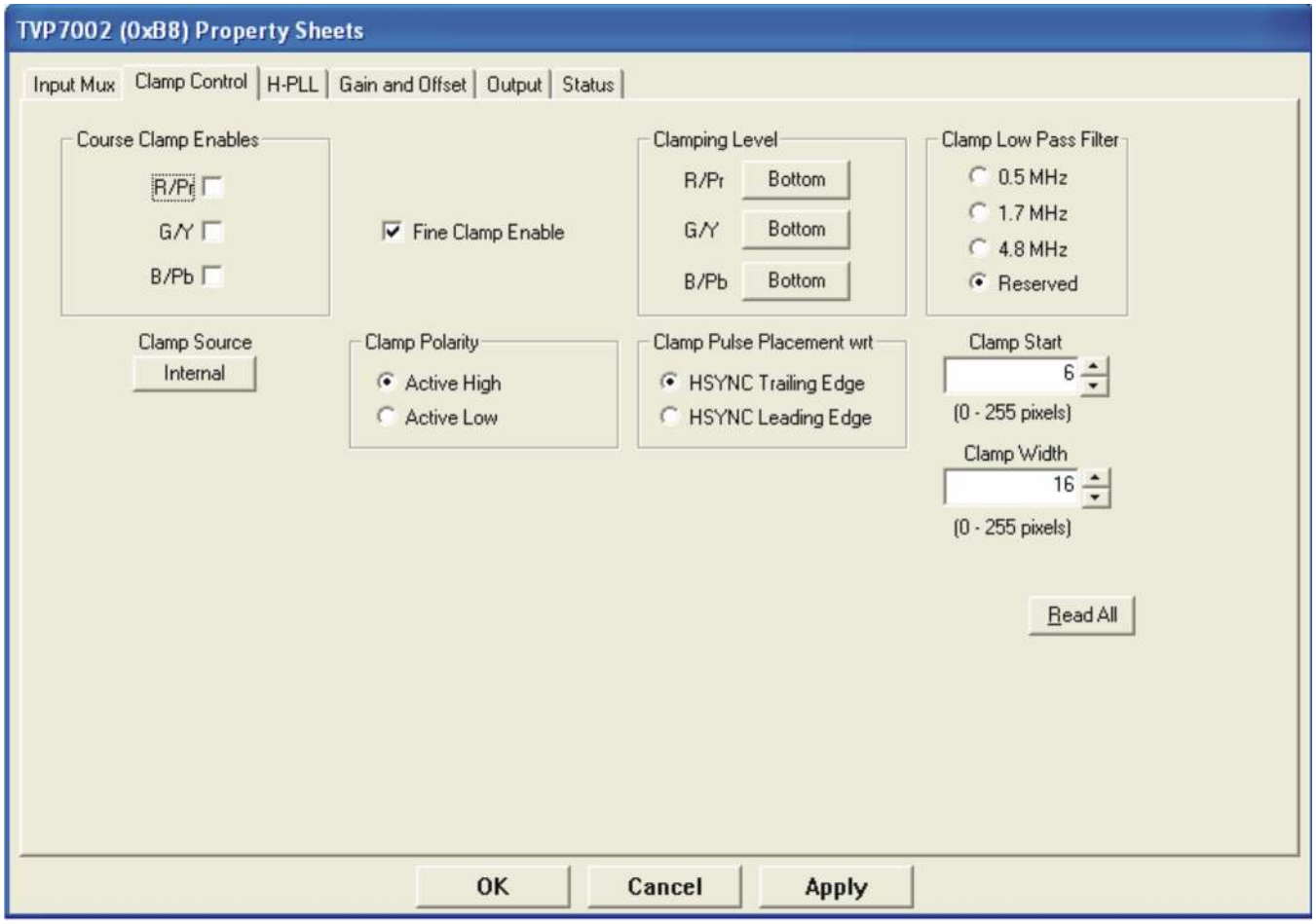


Figure 4-11. Clamp Control Property Sheet

Note: Bottom-level clamping is required for YGBR inputs, while middle-level clamping is required for PbPr inputs.

A programmable coarse clamp low-pass filter is provided (see I^2C register 1Ah) primarily for use with the SOG inputs that utilize a coarse bottom level sync tip clamp only. Recommended filter settings are shown in Table 4-5.

Table 4-5. Recommended Clamp LPF Settings

SDTV Formats	0.5 MHz
HDTV and PC Graphics	4.8 MHz

Note: Excessive clamp filtering can lead to SOG clamp level and sync processing issues.

4.5.3 PLL

A PLL setup calculator is integrated into the H-PLL Property Sheet. The H-PLL Feedback Divider, VCO range, and Charge Pump settings can be automatically calculated by entering the HSYNC and Pixel frequencies and pressing the Calculate>> button. The new settings are not written to the TVP7002 until the Program>> button is pressed.

Typically the Preferred Post Divider will be set to 1, and the feedback divider will be set to the total number of pixels per line. For lower frequency SDTV video formats, a 2x feedback divider value can be used with a Post Divider of 2 to improve jitter performance. In this case, the PLL operates at twice the desired frequency, but the output pixel rate will be at the PLL frequency divided by 2.

Note: When a Post Divider of 2 is used, only 16 of the 32 ADC clock phase control settings are available for use in the H-PLL Phase Select Register. ADC clock phase adjustments are typically required for PC graphics for precise alignment of the sample clock with the input pixel.

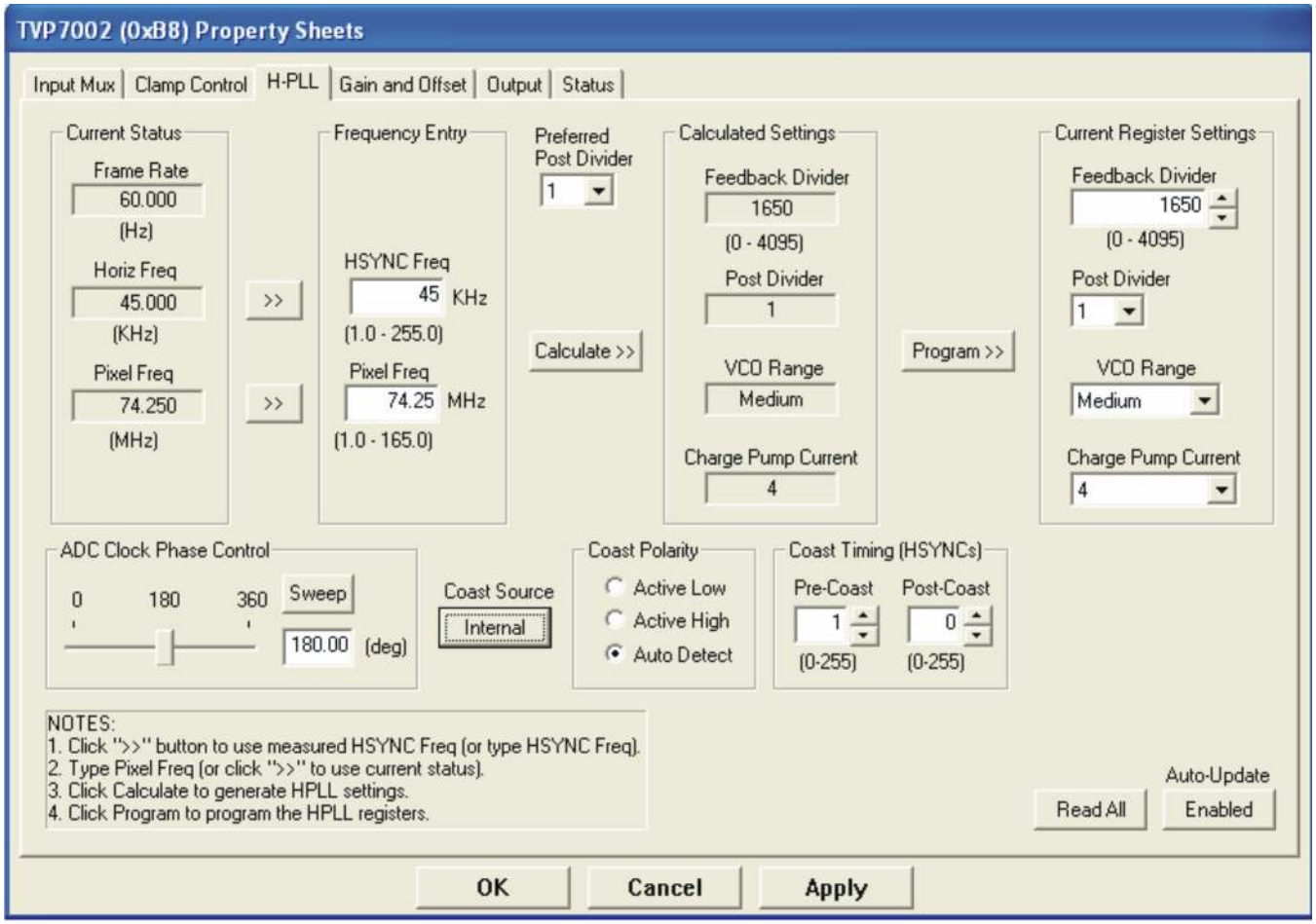


Figure 4-12. PLL Property Sheet

The Frame Rate, Horiz Freq, and Pixel Freq information reported in the Current Status frame are calculated values based on the current H-PLL Feedback Divider and the Lines/Frame and Clocks/Line Status read from the TVP7002 registers. The precision of these calculated values will depend on whether the internal reference clock or the 27-MHz external reference clock is selected. Current settings and status can be read at any time by pressing the Read All button.

An internally or externally generated coast signal can be used to put the PLL in coast or free-run mode to avoid disruptions in HSYNC during vertical blanking. When the internal coast is in use, the pre-coast and post-coast settings specify the coast interval range relative to the internally-detected VSYNC. Pre-coast specifies the number of lines before detecting VSYNC, and post-coast specifies the number of lines after VSYNC that are used for the coast interval.

Table 4-6. Recommended Coast Settings

Format	Pre-Coast	Post-Coast
480i/p	03h	03h
576i/p	03h	03h
1080i	01h	00h
1080p	01h	00h
720p	01h	00h
PC graphics with SOG	01h	00h

4.5.4 Gain and Offset - ALC

The Gain and Offset property sheet provides controls for both analog and digital gain/offset adjustment. The coarse gain and offset are analog in nature and are applied prior to the ADCs. Fine gain, fine offset, and automatic level correction (ALC) are applied in the digital domain after the ADCs. Coarse gain provides an analog gain range of 0.5 to 2.0, while Fine gain provides a digital gain range of 1 to 2.

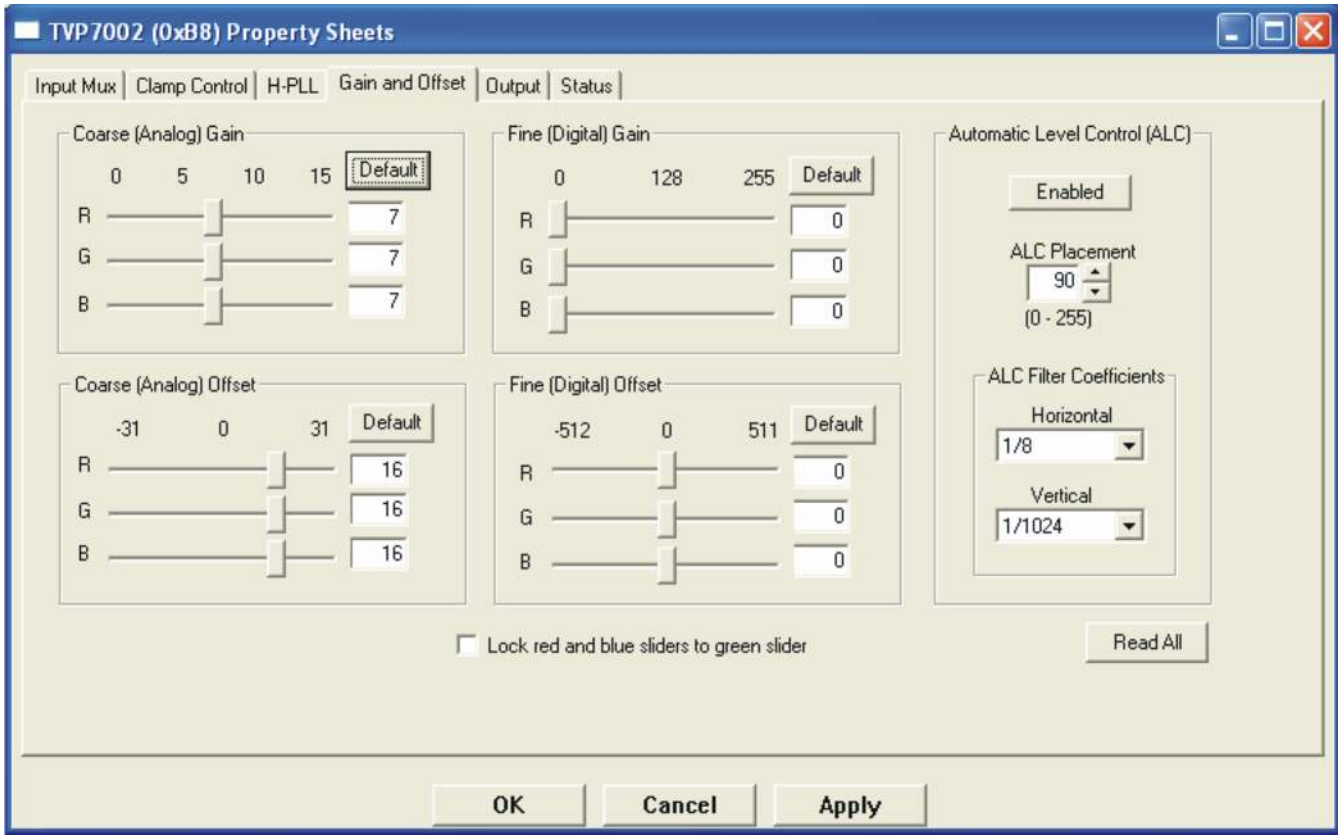


Figure 4-13. Gain and Offset Property Sheet

Stable output offset levels are maintained by use of the ALC feedback level control in the TVP7002. Two sets of filter coefficients are available that define the level of filtering applied on each line (horizontal) and the amount of feedback correction that is applied per line update (vertical). The horizontal coefficient (I^2C register 28h, NSH[2:0]) specifies the number of pixels that are used in the horizontal filter. The ALC filter must be applied during the horizontal blank interval following the clamp pulse, so it must be correctly positioned using the ALC placement register (register 31h). The amount of horizontal filtering that can used depends on the ALC placement and the horizontal blanking interval of the input video format. See Table 4-7 for recommended ALC placement settings.

The vertical coefficient (I^2C register 28h, NSV[3:0]) specifies the amount of feedback error correction derived from the horizontal filter that is applied to each line update. The NSV coefficient can range from 1 (maximum error applied) to 1/1024 (minimum error applied). The TVP7002 default filter coefficients should be adequate for most applications.

In the ALC operating mode, the fine offset registers are used to position the final digital output levels. To prevent bottom-level clipping at the ADCs, a coarse offset setting of 16 (10h) is recommended. Any clipping that occurs at the ADC input cannot be recovered by the ALC.

Table 4-7. Recommended ALC Settings

Format	Register 31h ALC Placement	Register 28h ALC Filter
SDTV and PC graphics	24 (18h)	53h
HDTV	90 (5Ah)	53h

4.5.5 Output

The Output property sheet provides controls for enabling outputs, selecting the output format, setting HSOUT polarity/position/width, and specifying embedded sync or Data Enable (DE) output timing. At power-up, the RGB data, DATACLK, and syncs are in a high-impedance state until enabled in I^2C register 17h or until programming the TVP7002EVM with one of the datasets include in the initialization file. The DATACLK output polarity is selectable in I^2C register 18h.

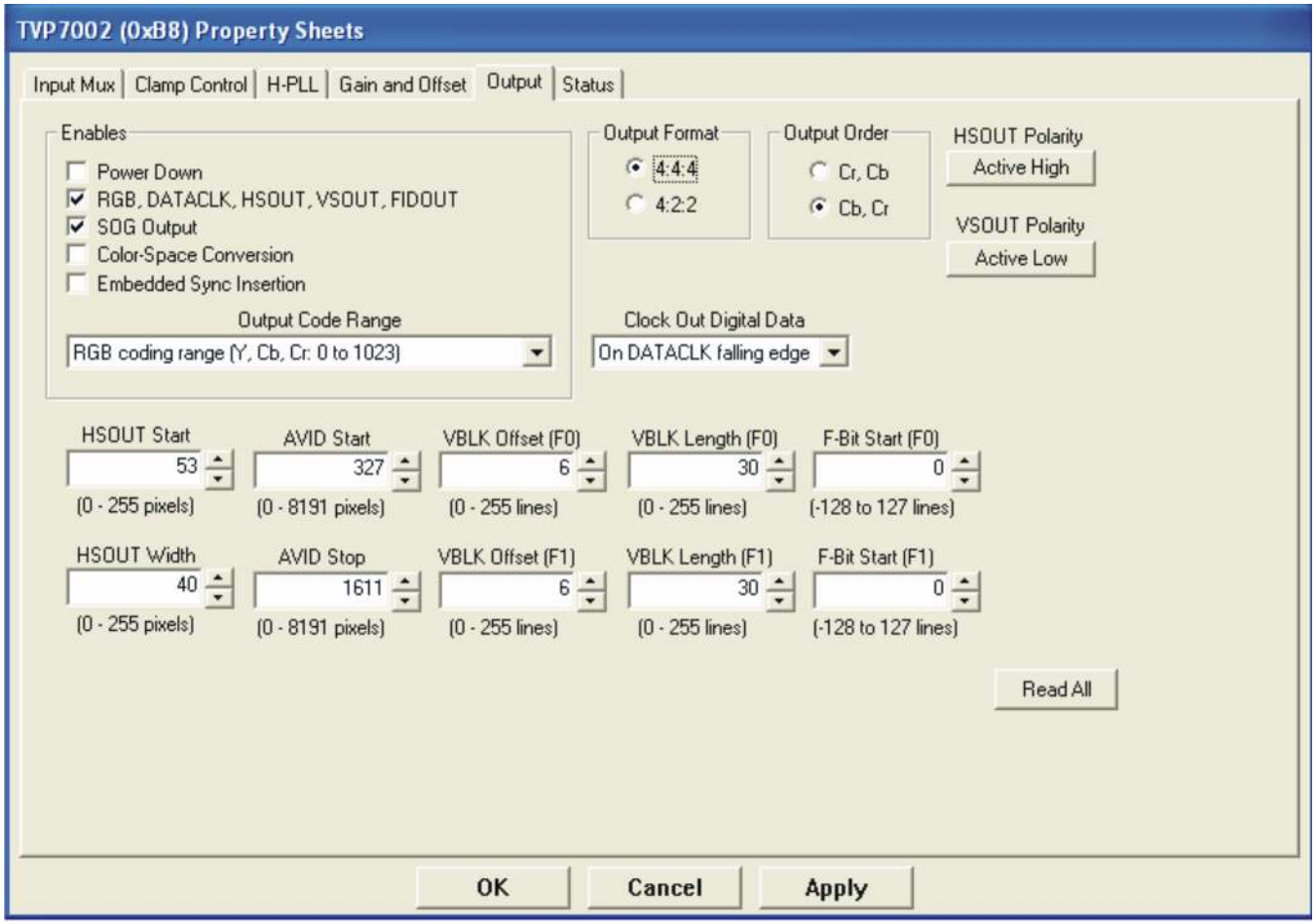


Figure 4-14. Output Property Sheet

The TVP7002 provides support for a 30-bit 4:4:4 or a 20-bit 4:2:2 output format. The 20-bit 4:2:2 output

format must be used when either the color space converter or embedded digital syncs are used. Additionally, when embedded syncs are used, the ITU-R BT.601 or the extended (4-1019) output code range must be used instead of the full (0 to 1023) RGB output code range. When the ITU-R BT.601 reduced code range (YRGB range = 64-940) is used, the YRGB fine digital offset settings should be set to 64 to avoid clipping of active video below code 64.

The AVID Start/Stop, VBLNK Offset/Length, and F-Bit Start settings define the position of the embedded sync code transitions and also the position of the Field ID (FID) and Data Enable (DE) when these outputs are used. When embedded syncs are enabled, the SAV embedded sync position can be adjusted with the AVID Start setting, and the EAV code can be adjusted with the AVID Stop setting. The lines where the embedded V-bit and F-bit transitions occur can be adjusted with the VBLK and F-Bit settings. See Appendix B for more information on embedded sync settings.

The TVP7002 color space converter (CSC) can be used to convert an RGB input to 20-bit YCbCr. The TVP7002 should default to CSC coefficients required for conversion of RGB to HDTV YCbCr. The CSC coefficients are fully programmable in I^2C registers 4Ah to 5Bh. See Appendix C for coefficients required for conversion to both HDTV and SDTV YCbCr color spaces.

Note: FID and DE output support is provided through use of the multi-function FIDOUT pin 22. See I^2C register 17h for more information.

4.5.6 Status

The Status property sheet reports input sync status from I^2C register 14h and line and frame rate information available in I^2C registers 37h to 39h. Lines per Frame and REFCLKs per Line are read directly from the I^2C registers, while the calculated status is derived from the measured values and the current H-PLL feedback divider.

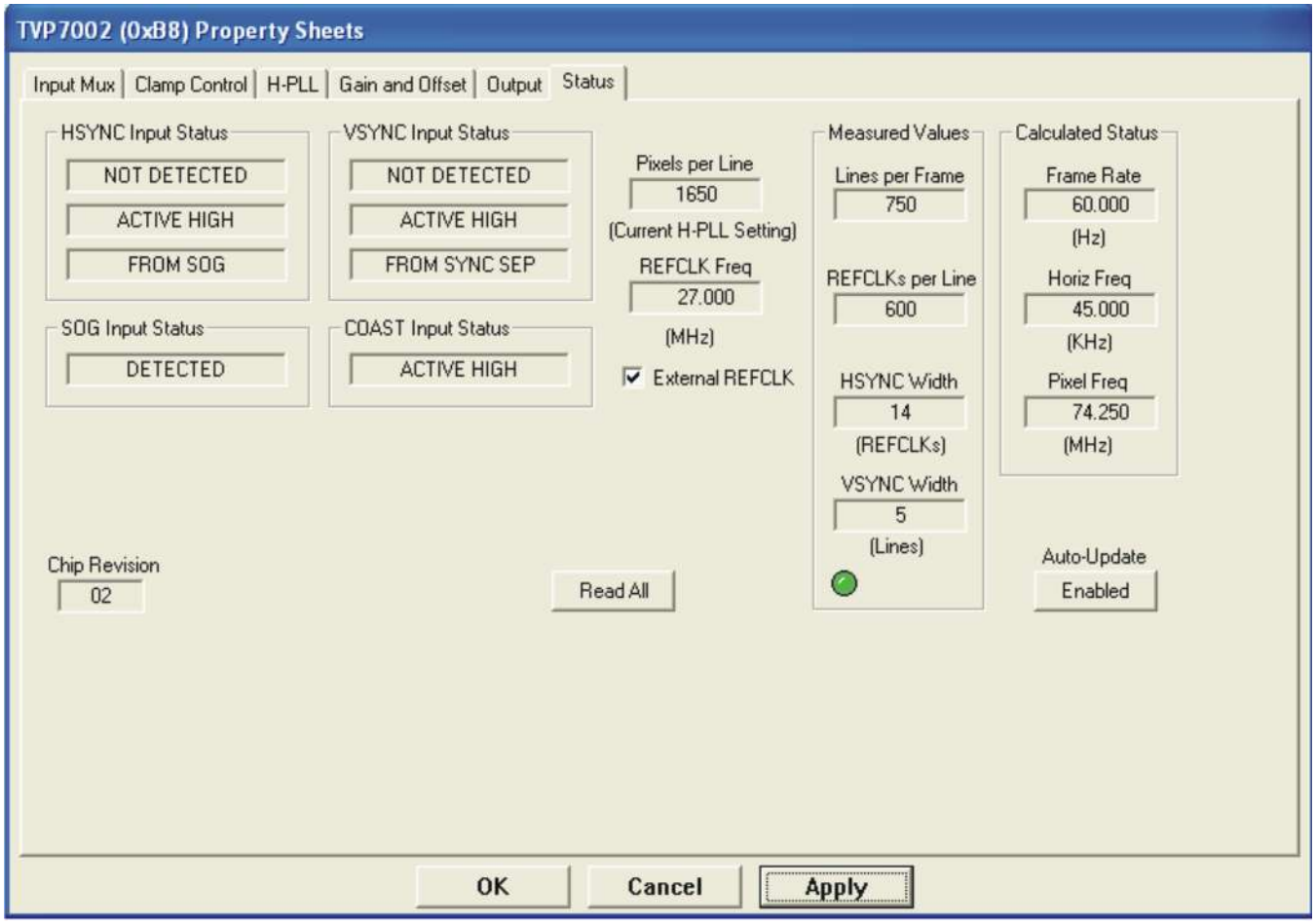


Figure 4-15. Status Property Sheet

Either an internal REFCLK (~6.5 MHz) or an external 27-MHz REFCLK can be used for REFCLKS per Line and HSYNC Width detection. The external 27-MHz REFCLK is recommended for a more stable and precise read back. The TVP7002 EVM is shipped with a 27-MHz oscillator connected to the EXTCLK input (pin 80).

Note: The internal REFCLK is not a precise clock source. Some part to part variation in clock frequency and status read back should be expected.

4.5.6.1 Reading the Register Map

The property sheets were designed so that the data displayed is always current. Certain actions cause the entire register map to be read from the device and to update the property sheets. This happens when:

1. Property sheets are initially opened.
2. Tabbing from one page to another.
3. Read All is clicked.
4. Making the Property Sheets window the active window (by clicking on it).
5. Making a Register Map Editor window the active window (by clicking on it).

4.5.6.2 Auto-Update from Device

Items 4 and 5 above are referred to as the Auto-Update feature. Auto-Update can be disabled by setting its program option button to DISABLED. This button is located on the initial dialog box (WinVCC4 Configuration).

With Auto-Update enabled (default), the user can open both the Property Sheets and the Register Map Editor at the same time. Changes made to the Property Sheets (and applied) are updated in the register map window as soon as the Register Map window is clicked on. It also works the other way; changes made in the Register Map Editor are updated in the Property Sheets as soon as the Property Sheets window is clicked on.

Table 4-8. Use of Property Sheet Controls

Property Sheet Dialog Control	What Do I Do With It?	When is Hardware Updated?
Read-only field	Read status information	N/A
Check box	Toggle a single bit	After Apply
Drop-down list	Select from a text list	After Apply
Edit box	Type a number	After Apply
Edit box with up/down arrows	Use up/down arrows or type a number	Up/down arrows: Immediately Type a number: After Apply
Slider	Slide a lever	Immediately
Pushbutton	Initiate an action	Immediately

Table 4-9. Property Sheet Button Controls

Button Control	Definition
OK	Writes to all writeable registers whose data has changed. A register is flagged as changed if the value to be written is different from the value last read from that address. Closes the dialog.
Cancel	Causes all changes made to the property page since the last Apply to be discarded. Changes made to dialog controls with 'immediate hardware update' are not discarded, because they have already been changed in hardware. Does not write to hardware. Closes the dialog.
Apply	Writes to all writeable registers whose data has changed. A register is flagged as changed if the value to be written is different from the value last read from that address.

Troubleshooting

This chapter describes ways to troubleshoot the TVP7002EVM.

5.1 Troubleshooting Guide

If there are problems with the TVP7002EVM hardware or the WinVCC4 software, see Table 5-1 and Table 5-2 for possible solutions.

Table 5-1. TVP7002EVM Troubleshooting

Symptom	Cause	Solution
At startup, the error message "Cannot find DLL file DLPORTIO.DLL" appears.	The parallel port driver supplied with the EVM has not been installed.	Run Port95NT.EXE on the CD to install the driver.
Blank screen	Wrong analog input is selected.	Go to Edit->Property Sheets->TVP7002, Analog Video page, select the correct video input(s) and click Apply. The Composite Video 1 input is default.
	Source is connected to the wrong input connector.	Connect source to the correct input connector.
Vertical stability or flashing display	Mode detect issue due to HSYNC/VSYNC alignment	Adjust HSYNC output delay
Line noise present with high-frequency vertical line input pattern	PLL phase setting is not set correctly for the input source	Adjust PLL phase setting
Line noise present with flat field	Excessive noise on the input source	Filter the inputs or try a different source
Picture too dark	Clamp or ALC not set correctly	Reposition Clamp or ALC. Reduce ALC horizontal filter coefficient
SOG/Y does not work	SOG clamp disabled	Set SOG_CE bit in register 2Eh to 1.
SOG does not work when using the VGA connector	The VGA input is not connected to an SOG input pin	The BNC connectors must be used for SOG operation

Table 5-2. I²C Troubleshooting

Symptom	Cause	Solution
No I²C communication	I²C slave address is wrong.	Close and restart WinVCC4. Choose the alternate slave address in the WinVCC4 Configuration dialog.
	Parallel cable is not connected from PC parallel port to the EVM DB25 connector.	Connect cable.
	EVM is not powered on.	The power supply must be plugged into a 100-V to 240-V/ 47-Hz to 63-Hz power source and the cord must be plugged into the power connector on the EVM.
	Wrong type of parallel cable	Some parallel cables are not wired straight through pin-for-pin. Use the cable supplied with the EVM.
	PC parallel port mode is not set correctly.	Reboot PC, enter BIOS setup program, set parallel port LPT1 mode (address 378h) to ECP mode or bidirectional mode (sometimes called PS/2 mode or byte mode). If already set to one of these two modes, switch to the other setting (see Section 5.2.1).
	Device was placed in power-down mode.	Press the reset button on the TVP7002EVM.
	EVM was configured for an external I²C master.	Reinstall 0-Ω resistors R5 and R6. Control EVM using the PC parallel port.
	Still no I²C communication	The PC may not be capable of operating in the required parallel port mode. This is true of some laptop computers. Use a different computer, preferably a desktop PC.

When WinVCC4 is started and the WinVCC4 Configuration dialog box is closed with OK, the I²C system test is performed (unless the I²C System Test program options button was disabled).

If the I²C system test fails, a dialog box appears. Figure 5-1 reports that a read from TVP7002 failed, using slave address 0xB8, subaddress 0x05. The data read was 0x00.

After noting which device had a problem, click OK to continue. Next, the Corrective Action Dialog box appears to help fix the problem.

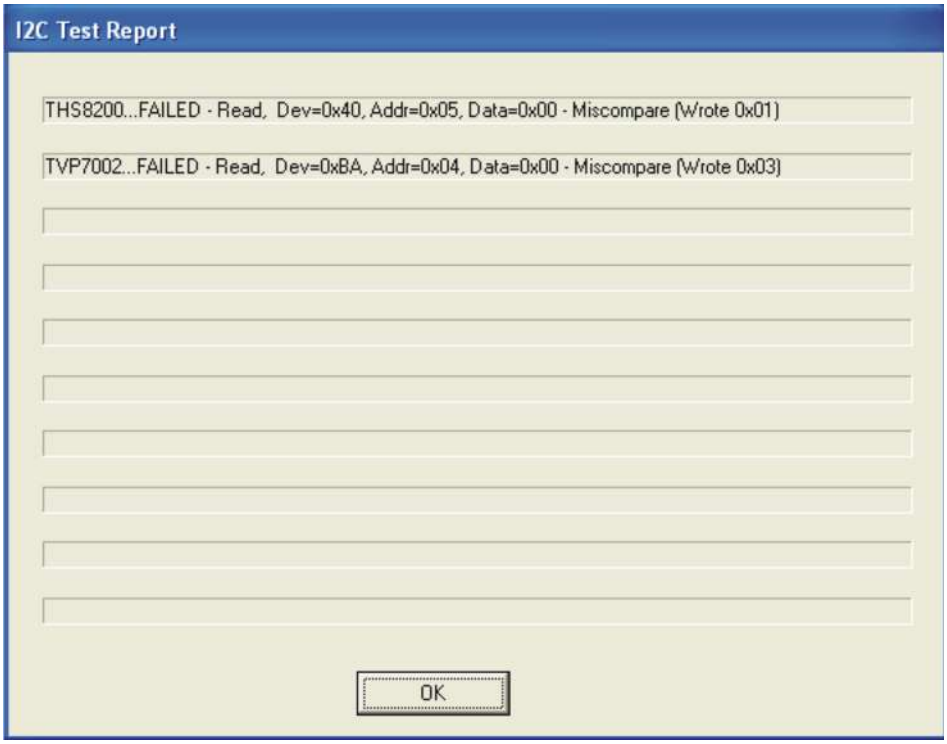


Figure 5-1. I²C System Failure Dialog Box

5.2 Corrective Action Dialogs

After closing the I²C system test report dialog box, the dialog box in Figure 5-2 appears.

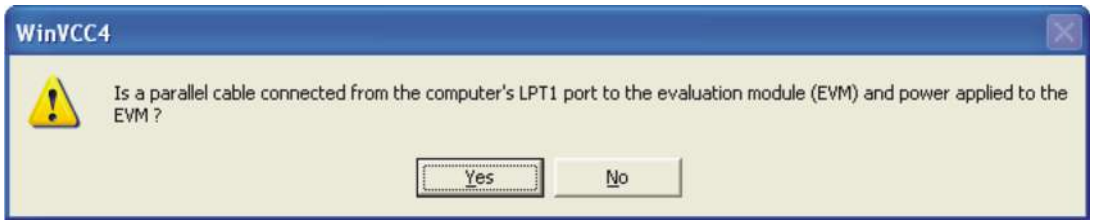


Figure 5-2. Corrective Action Dialog Box

1. If the parallel port cable is NOT connected between to PC and the TVP7002EVM or if the EVM power is not on, then:
   a. Click NO.
   b. The dialog box shown in Figure 5-3 appears with instructions on how to correct the problem.
   c. Correct the problem.
   d. Click OK to continue

Figure 5-3. Corrective Action Required

2. If the cable is connected from the PC parallel port to the TVP7002EVM and the EVM power is on:
   a. Click Yes.
   b. The dialog box shown in Figure 5-4 appears. This dialog box appears if the PC parallel port mode setting may need to be changed.

Note: Run the PC BIOS setup program only if the I²C communication problem cannot be resolved in another way (correct slave address settings, reset or power cycle the EVM, and/or check that the device type selected was TVP7002).

   c. Click OK to continue.
   d. Click OK to close it and get to the main menu.
   e. Click Exit in the File menu to exit the program.
   f. See troubleshooting guide above.

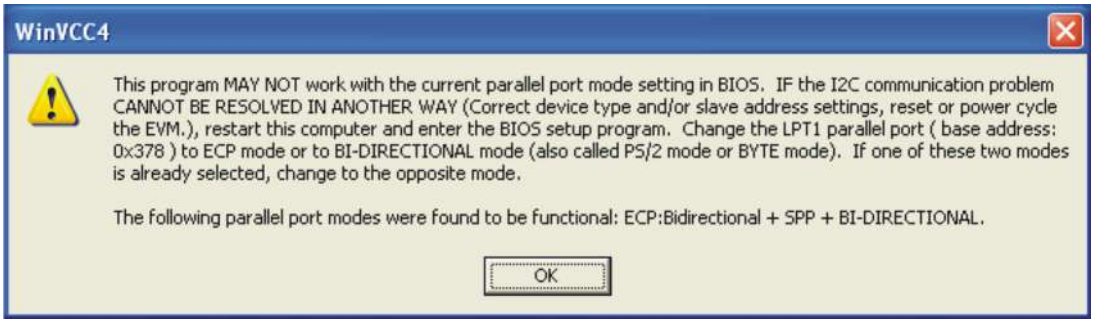


Figure 5-4. Corrective Action Required

5.2.1 Setting the PC Parallel Port Mode

Note: Run the PC BIOS setup program only if the I²C communication problem cannot be resolved in another way (correct slave address settings, reset or power cycle the EVM, and/or check that the device type selected was TVP7002).

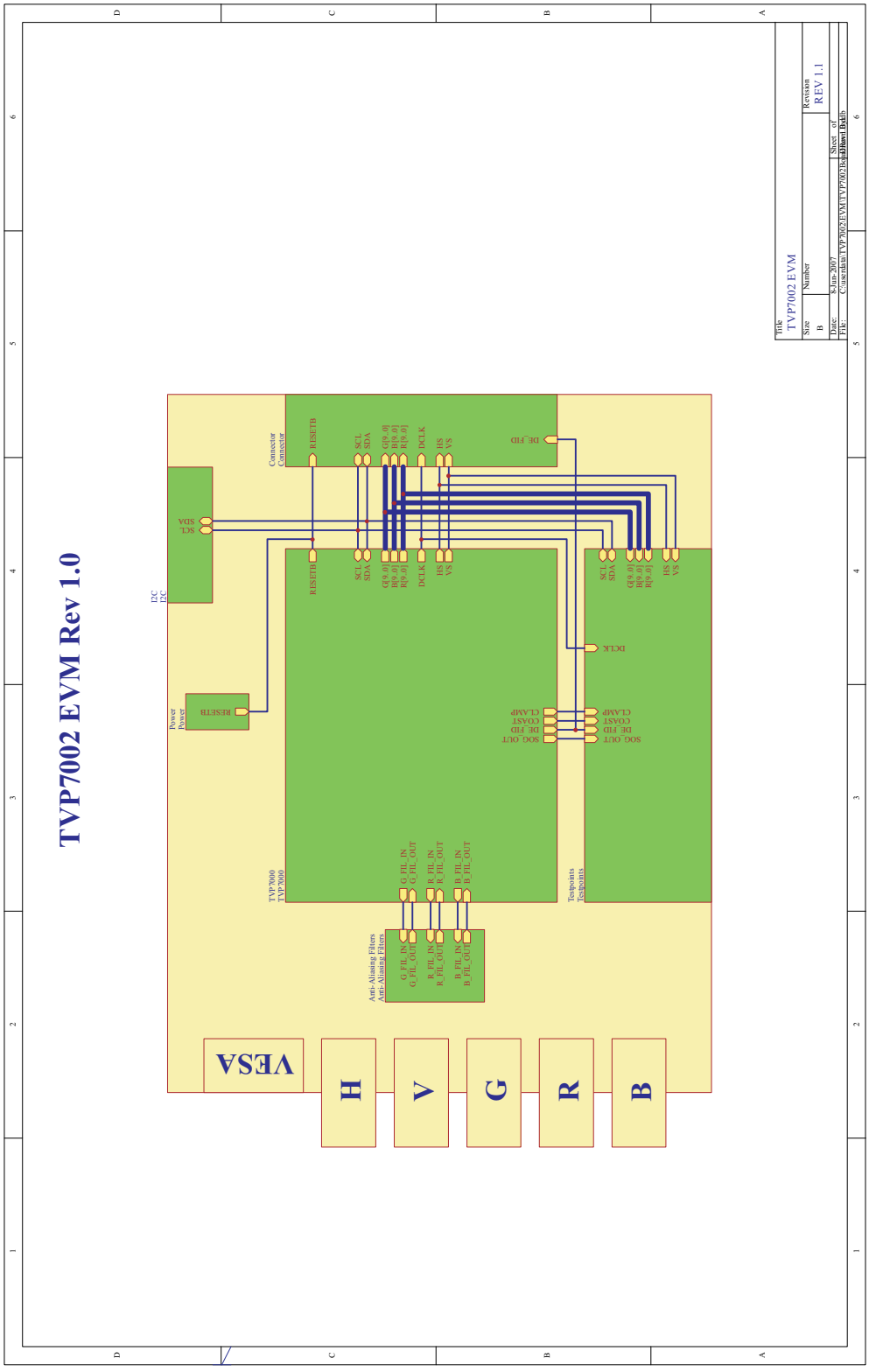
1. Restart the PC.
2. During the boot process, enter the BIOS setup program by pressing the required key (the initial text screen usually indicates which key to press).
3. Find where the parallel port settings are made.
4. Set the parallel port LPT1 at address 378h to ECP mode or bidirectional mode (sometimes called PS/2 mode or byte mode). If one of these two modes is already selected, then change to the opposite mode.
5. Exit and save changes.

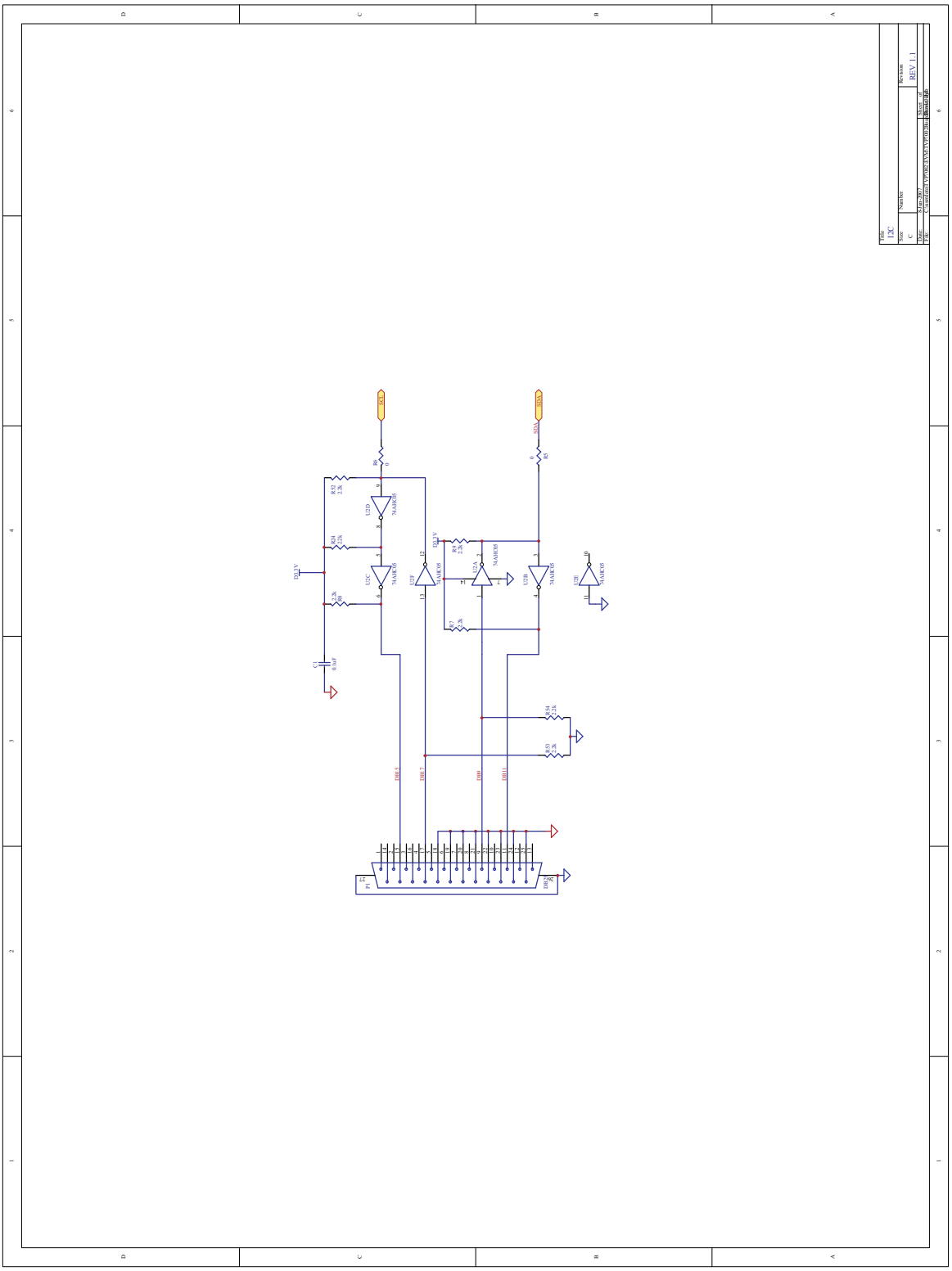
5.2.2 General I²C Error Report

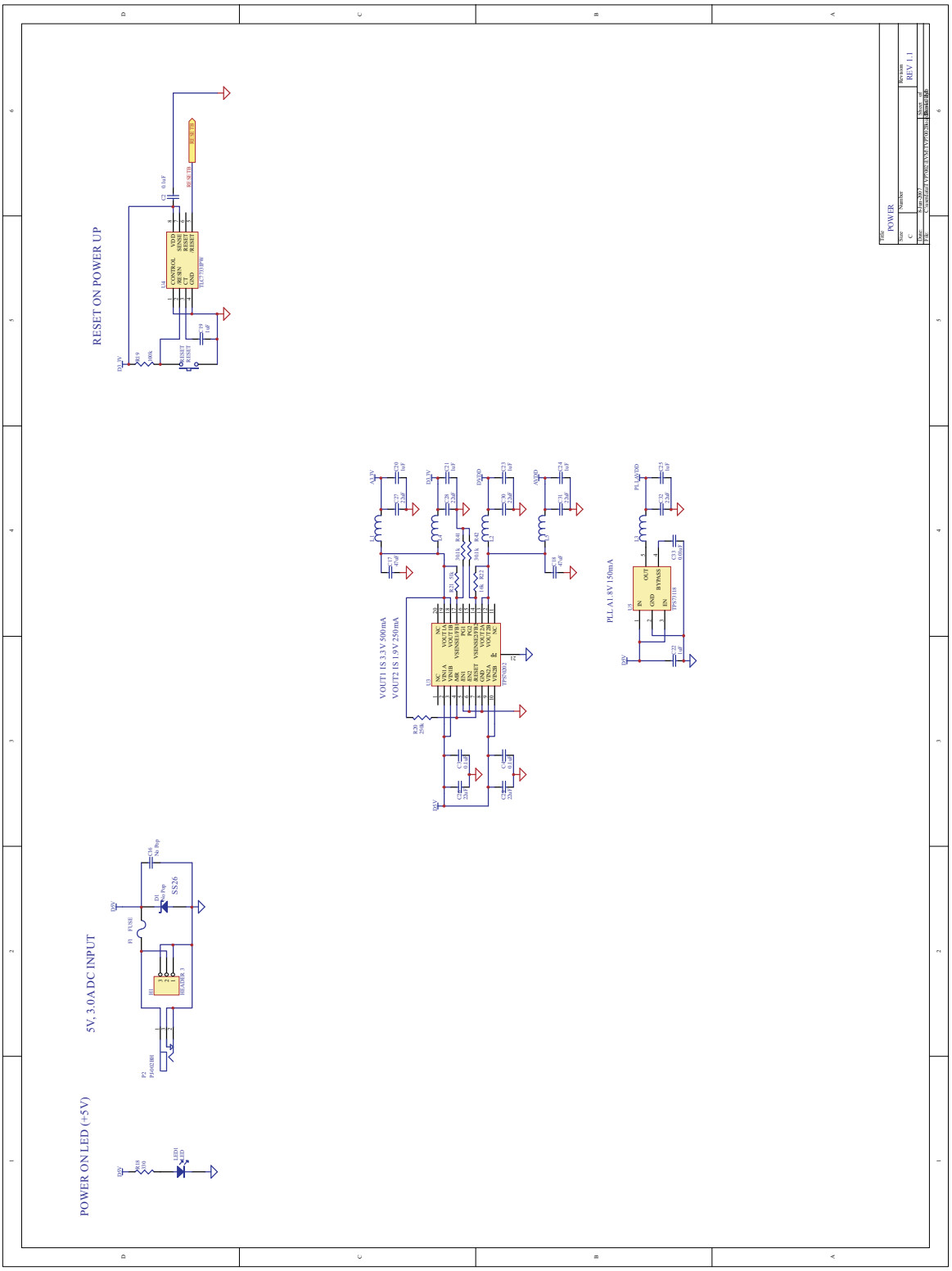
The error report shown in Figure 5-5 appears when an I²C error occurs at any time other than after the I²C system test. In this example, there was an acknowledge error at slave address 0x54 (the video triple ADC module). The error occurred on Read Cycle Phase 1 on the device (slave) address byte.

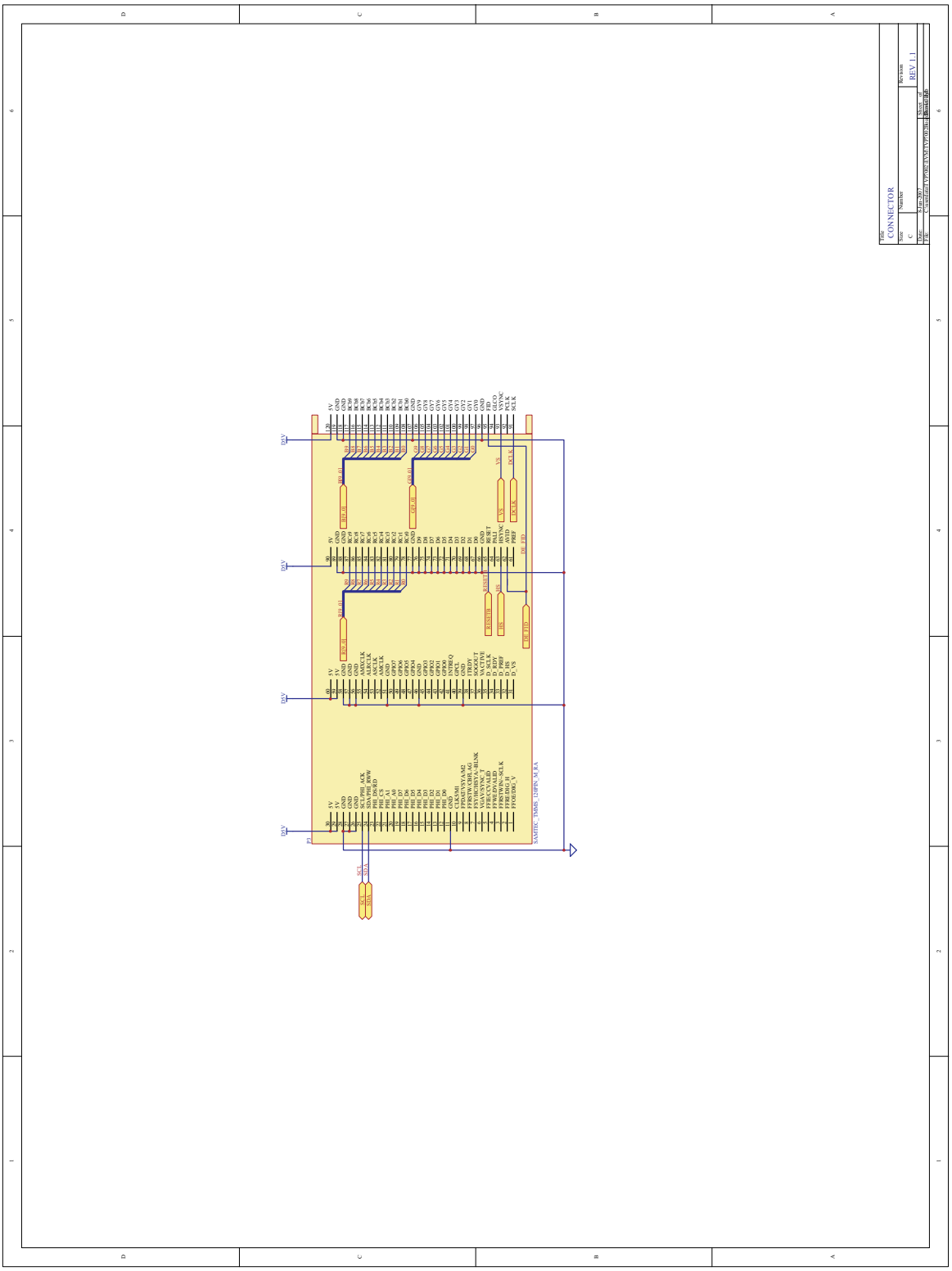
Figure 5-5. I²C Error Report

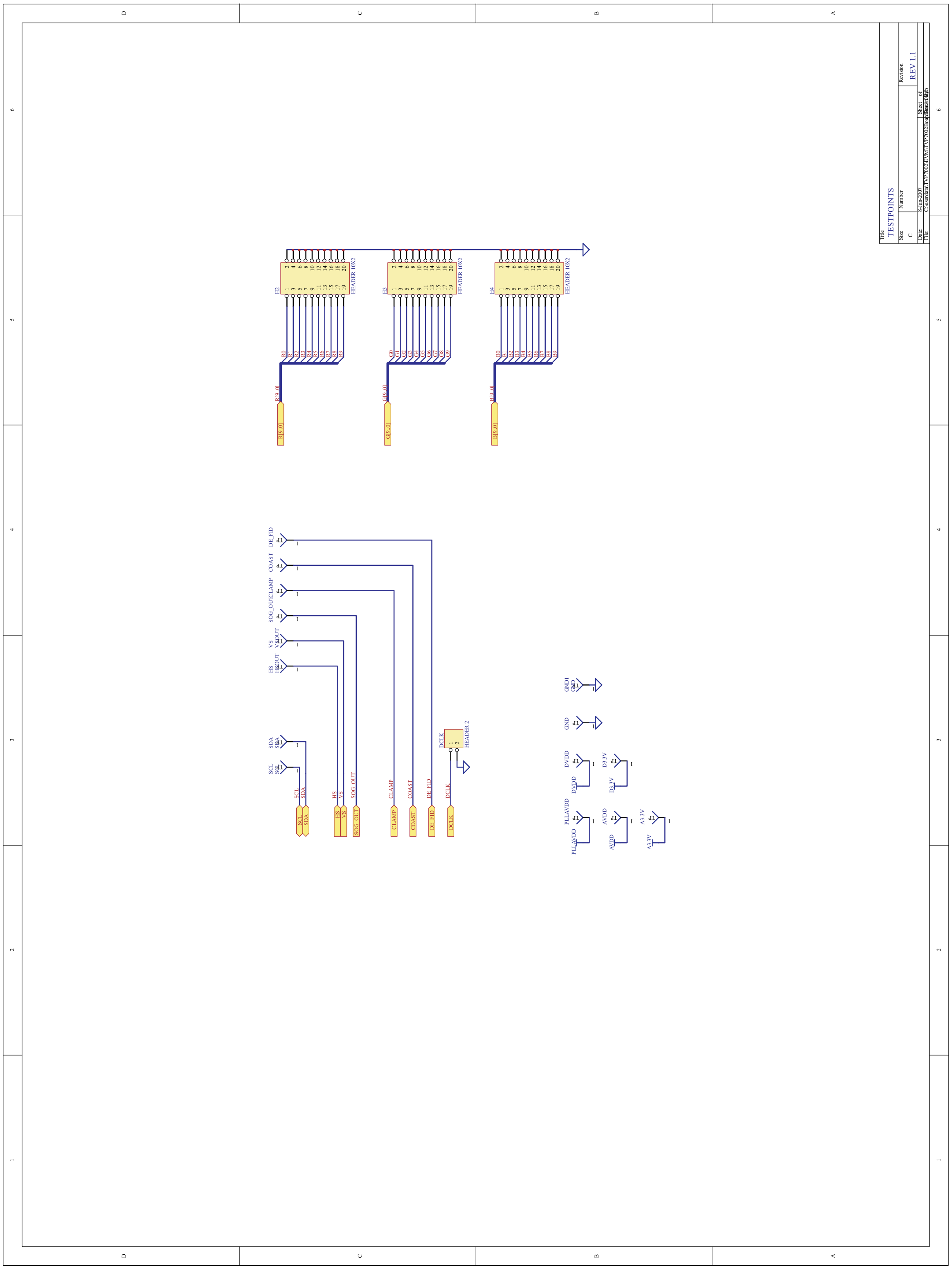
TVP7002EVM Schematics

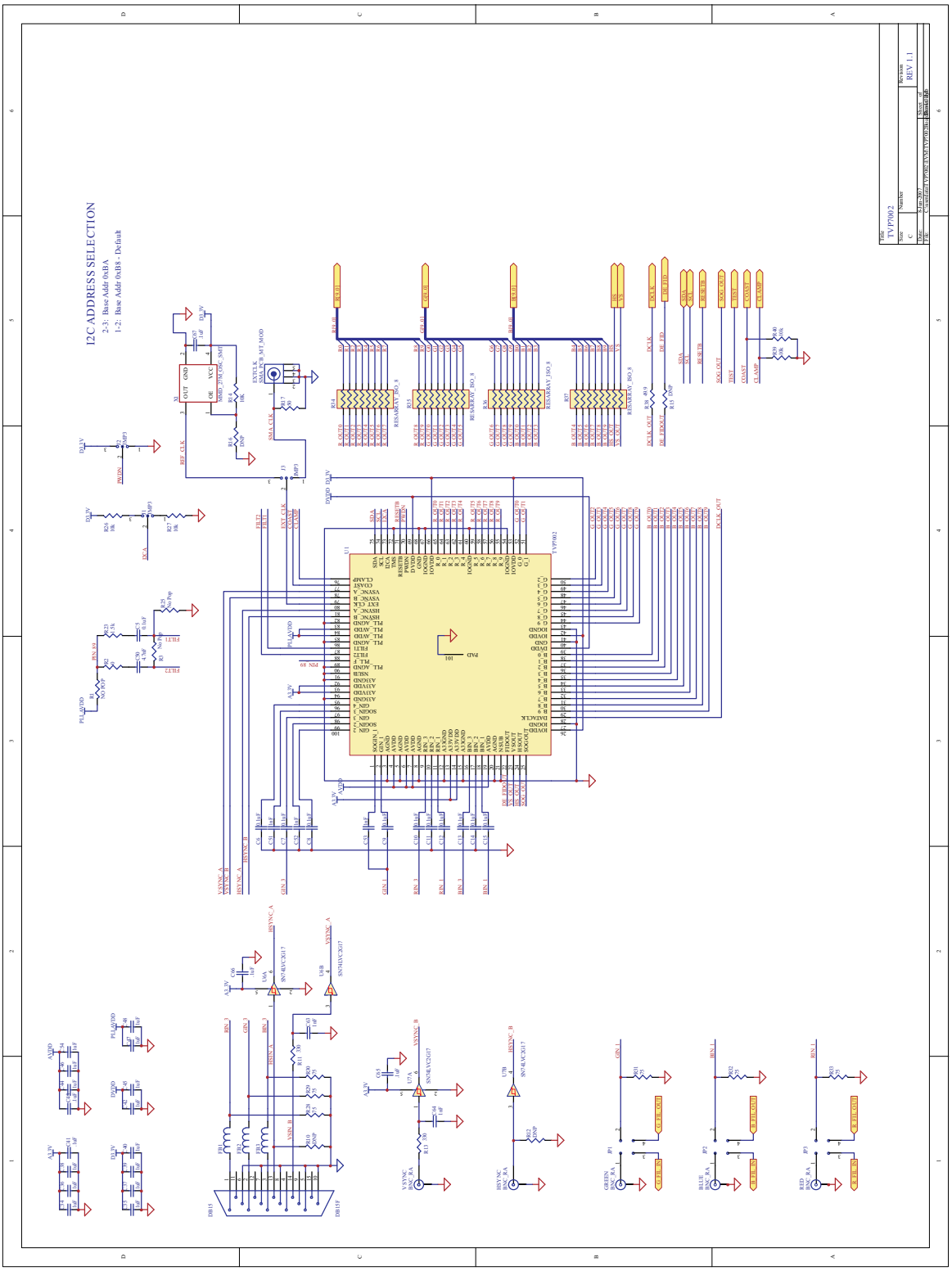

TVP7002 EVM Rev 1.0
Title
TVP7002 EVM
Size
B
Number
Revision
REV 1.1
Date:
8-June-2007
Sheet of
File:
C:\cases\ths\TVP7002\EVM\TVP7002b1.ddb
Drawn By:
Connector
Connector
RESETB
SCL
SDA
Q[9:0]
R[9:0]
G[9:0]
B[9:0]
DCLK
HS
VS
DE_FID
I2C
I2C
Power
Power
SOG_OUT
CLAMP
COAST
TVP7000
TVP7000
Testpoints
Testpoints
Anti-Aliasing Filters
Anti-Aliasing Filters
G_FIL_IN
G_FIL_OUT
R_FIL_IN
R_FIL_OUT
B_FIL_IN
B_FIL_OUT
VESA
H
V
G
R
B

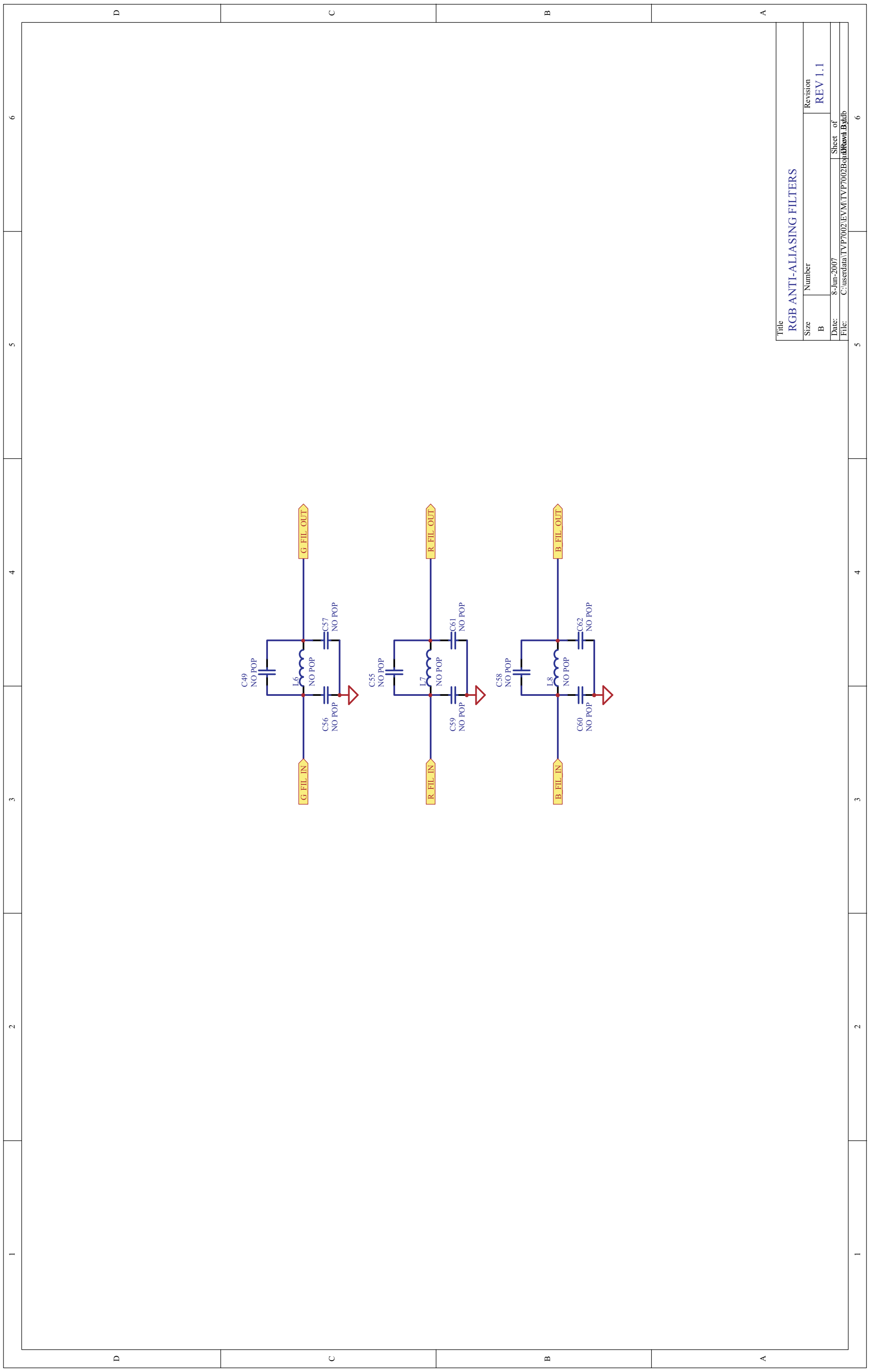


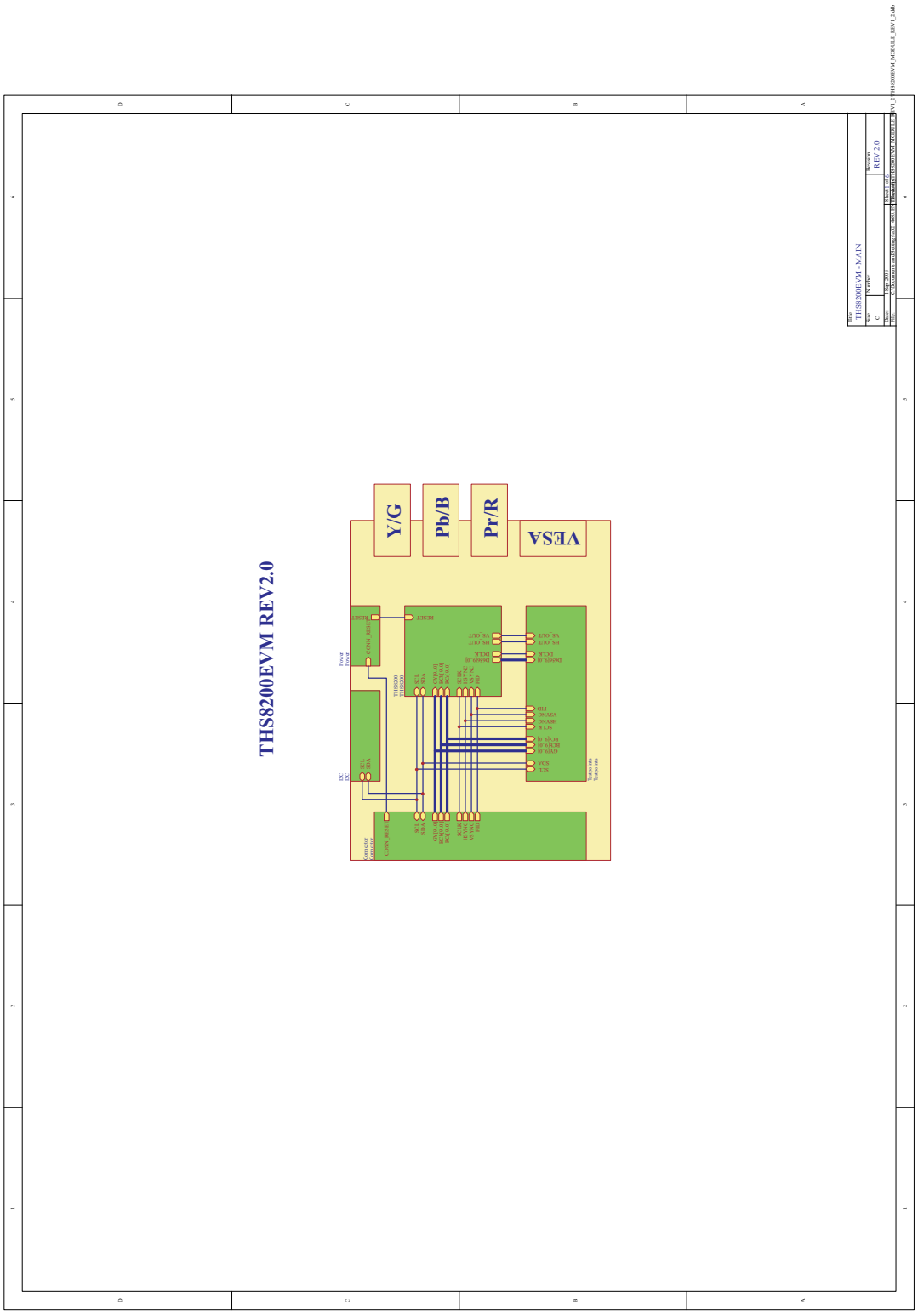

RESET ON POWER UP
VOUT1 IS 3.3V 500mA
VOUT2 IS 1.9V 250mA
PLL A1.8V 150mA
5V, 3.0A DC INPUT
POWER ON LED (+5V)
POWER

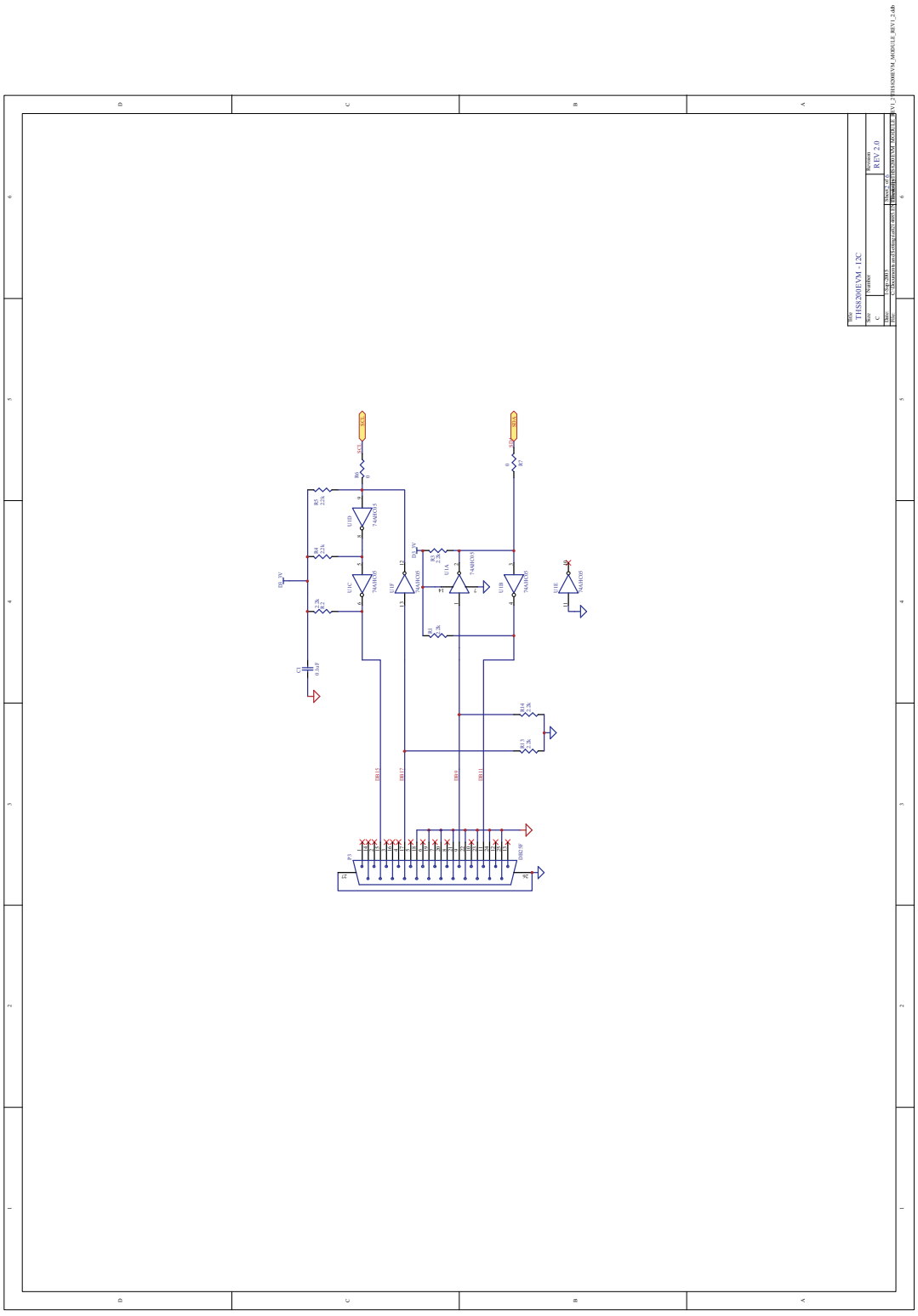

CONNECTOR
REV 1.1

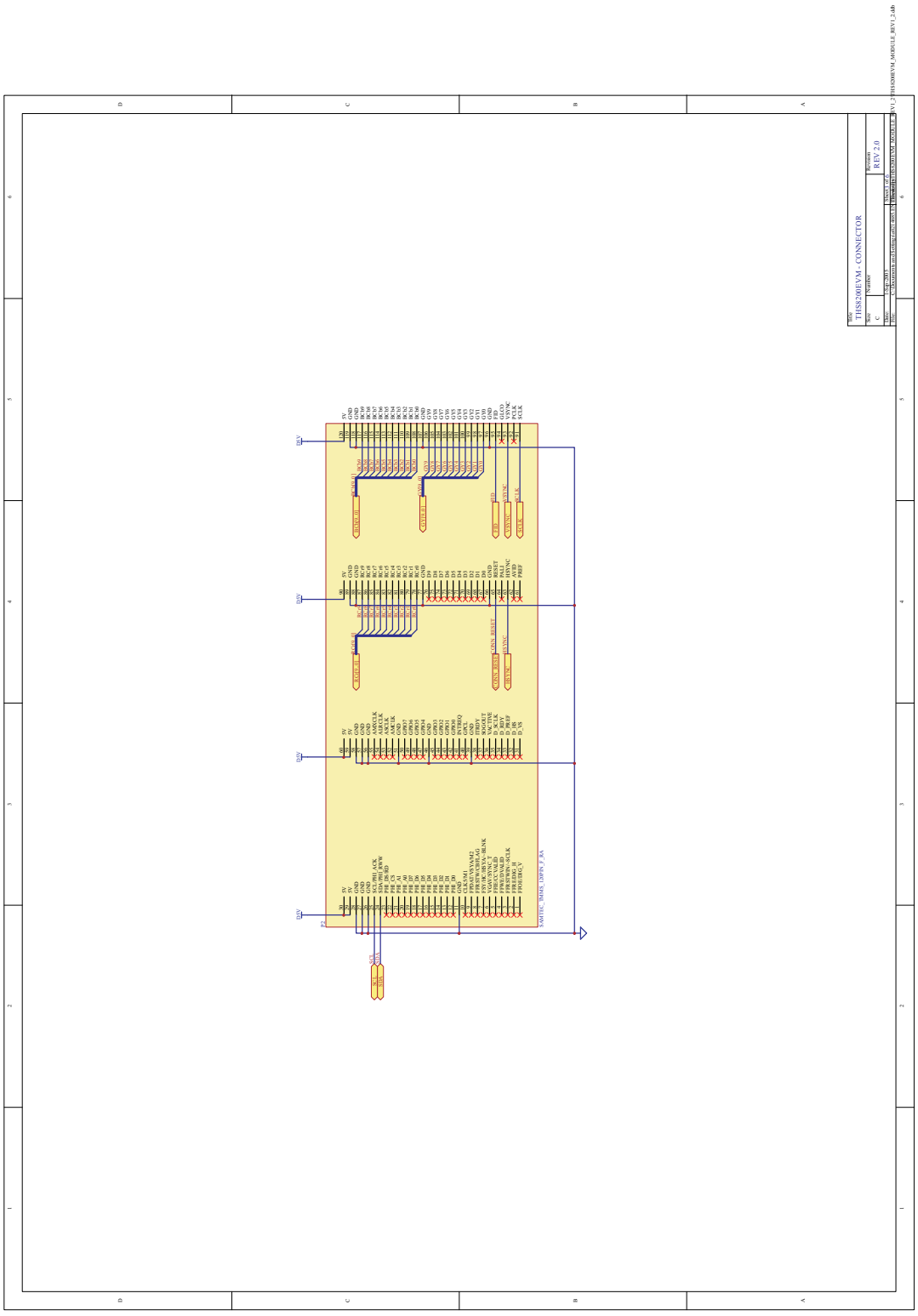

TESTPOINTS
REV 1.1
HEADER 10X2
HEADER 2

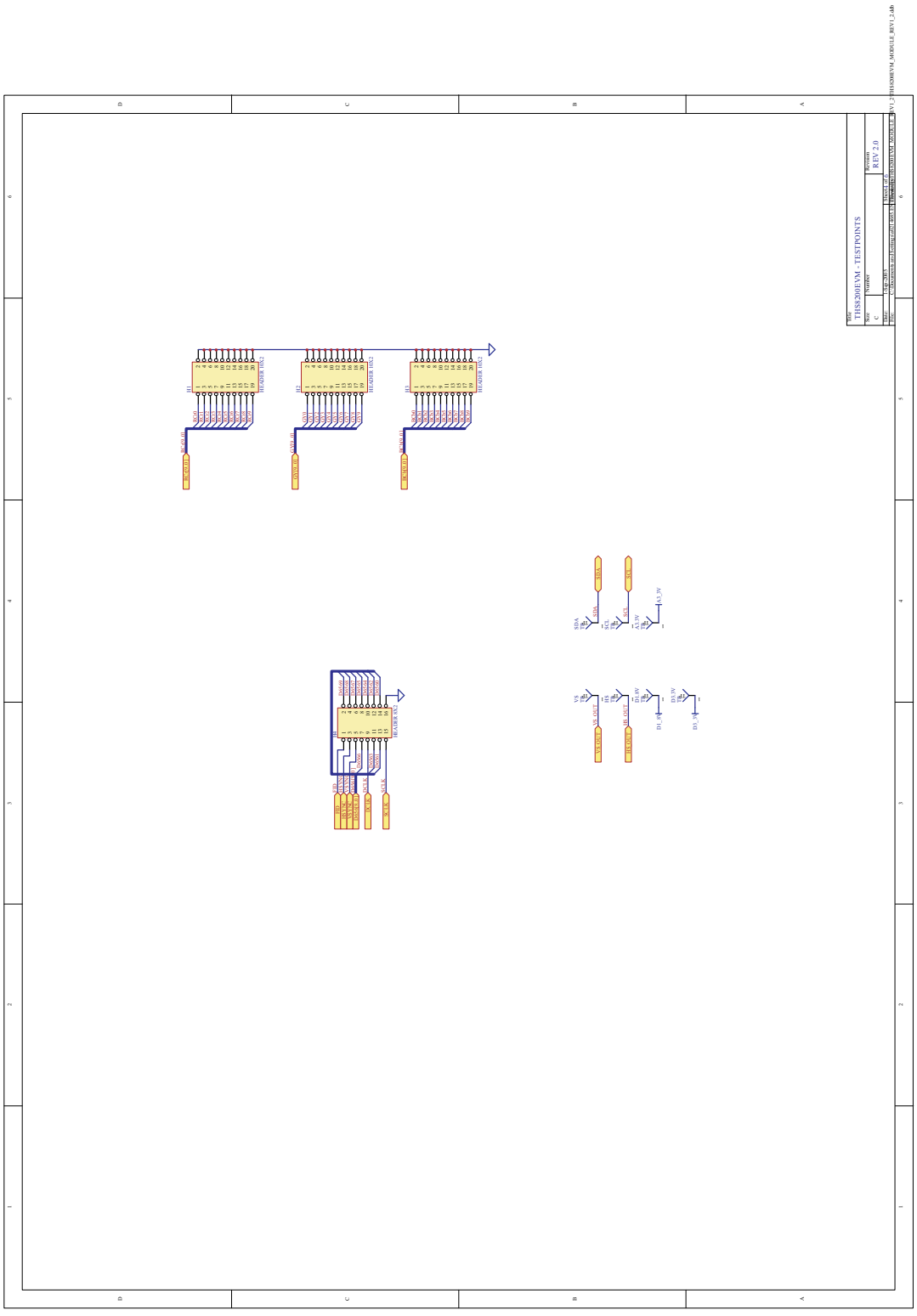

I2C ADDRESS SELECTION
2-3: Base Addr 0xBA
1-2: Base Addr 0xB8 - Default
TVP7002
REV 1.1

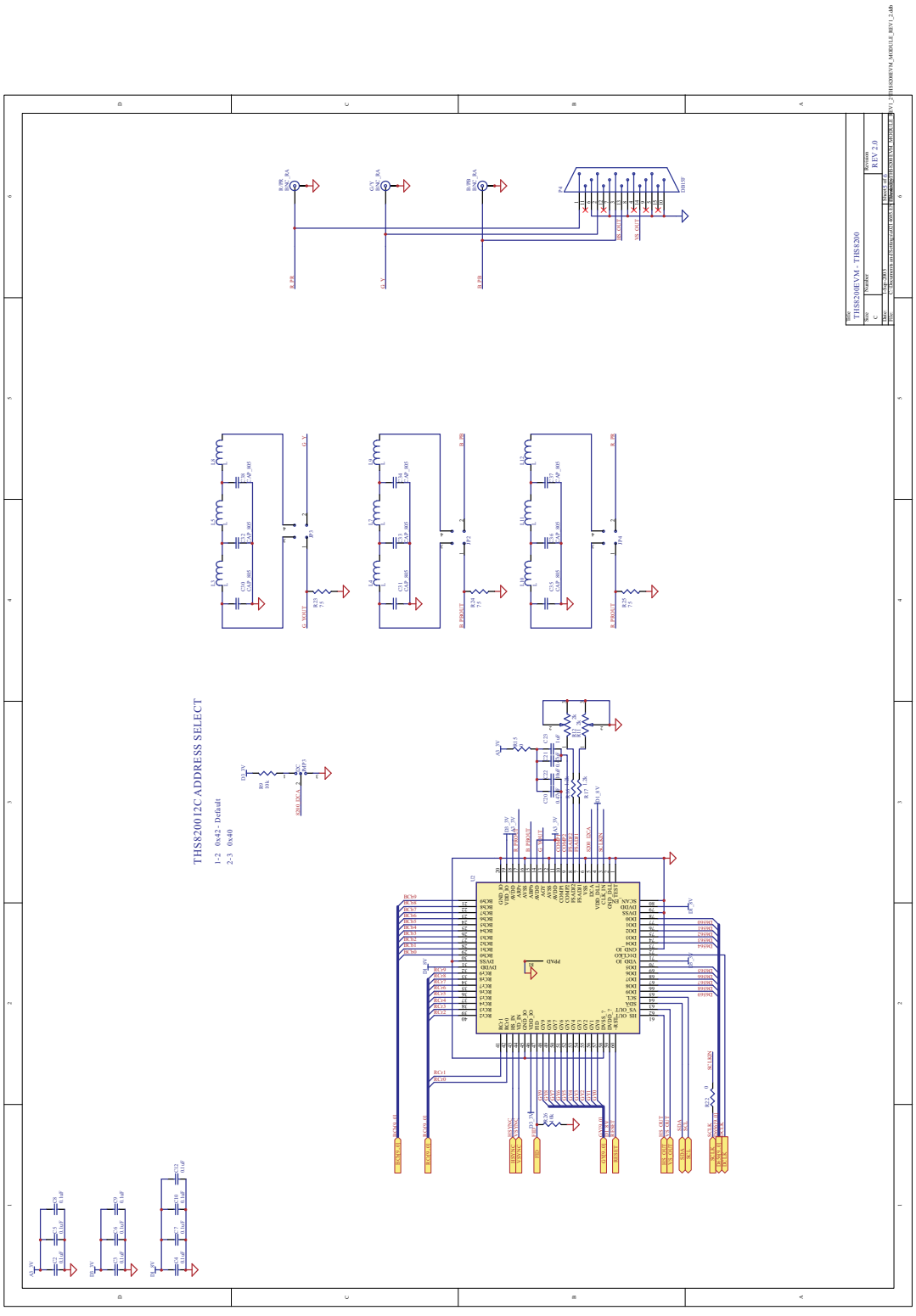

G_FIL_OUT
R_FIL_OUT
B_FIL_OUT
G_FIL_IN
R_FIL_IN
B_FIL_IN
C49
NO POP
L6
NO POP
C57
NO POP
C56
NO POP
C55
NO POP
L7
NO POP
C61
NO POP
C59
NO POP
C58
NO POP
L8
NO POP
C62
NO POP
C60
NO POP
Title
RGB ANTI-ALIASING FILTERS
Size
B
Number
Revision
REV 1.1
Date:
8-Jun-2007
File:
Sheet of

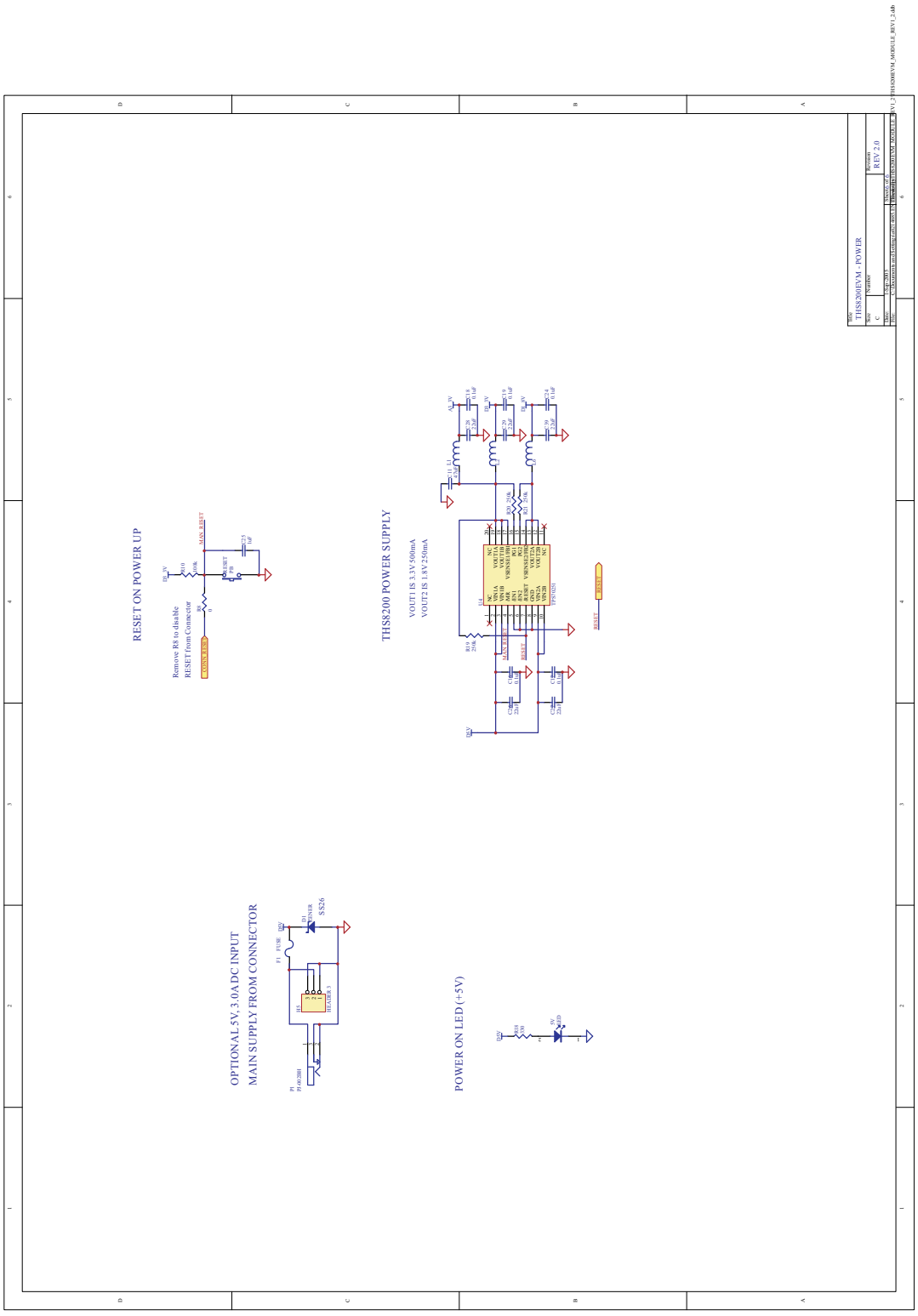

THS8200EVM REV2.0
Y/G
Pb/B
Pr/R
VESA
THS8200EVM - MAIN
REV 2.0




THS7002EVM - CONNECTOR
Revision
REV 2.0


THS230EVM - TESTPOINTS
Revision
REV 2.0


THS8200 I2C ADDRESS SELECT
1-2 0x42 - Default
2-3 0x40


RESET ON POWER UP
Remove R8 to disable
RESET from Connector
THS8200 POWER SUPPLY
VOUT1 3S 3.3V 500mA
VOUT2 2S 1.8V 250mA
OPTIONAL 5V, 3.0A DC INPUT
MAIN SUPPLY FROM CONNECTOR
POWER ON LED (+5V)
THS8200EVM - POWER
TVP7002EVM, THS8200EVM MODULE, REV1.2.sch

Recommended PLL Settings

Table A-1. Recommended PLL Settings

Standard	Resolution	Frame Rate (Hz)	Line Rate (kHz)	Pixel Rate (MHz)	PLL Divider (Total pix/line)	PLLDIV [11:4] Reg 01h [7:0]	PLLDIV [3:0] Reg 02h [7:4]	Reg 03h	Output Divider Reg 04h [0]	VCO Range Reg 03h [7:6]	CP Current Reg 03h [5:3]
VGA	640 x 480	59.94	31.469	25.175	800	32h	00h	20h	0	ULow (00b)	100b
	640 x 480	72.809	37.861	31.5	832	34h	00h	20h	0	ULow (00b)	100b
	640 x 480	75	37.5	31.5	840	34h	80h	20h	0	ULow (00b)	100b
	640 x 480	85.008	43.269	36	832	34h	00h	60h	0	Low (01b)	100b
SVGA	800 x 600	56.25	35.156	36	1024	40h	00h	58h	0	Low (01b)	011b
	800 x 600	60.317	37.879	40	1056	42h	00h	58h	0	Low (01b)	011b
	800 x 600	72.188	48.077	50	1040	41h	00h	58h	0	Low (01b)	011b
	800 x 600	75	46.875	49.5	1056	42h	00h	58h	0	Low (01b)	011b
	800 x 600	85.061	53.674	56.25	1048	41h	80h	58h	0	Low (01b)	011b
XGA	1024 x 768	60.004	48.363	65	1344	54h	00h	58h	0	Low (01b)	011b
	1024 x 768	70.069	56.476	75	1328	53h	00h	A8h	0	Med (10b)	101b
	1024 x 768	75.029	60.023	78.75	1312	52h	00h	A8h	0	Med (10b)	101b
	1024 x 768	84.997	68.677	94.5	1376	56h	00h	A0h	0	Med (10b)	100b
WXGA (I)	1280 x 768	59.995	47.396	68.25	1440	5Ah	00h	50h	0	Low (01b)	010b
	1280 x 768	59.87	47.776	79.5	1664	68h	00h	A0h	0	Med (10b)	100b
	1280 x 768	74.893	60.289	102.25	1696	6Ah	00h	A0h	0	Med (10b)	100b
	1280 x 768	84.837	68.633	117.5	1712	6Bh	00h	A0h	0	Med (10b)	100b
SXGA	1280 x 1024	60.02	63.981	108	1688	69h	80h	A0h	0	Med (10b)	100b
	1280 x 1024	75.025	79.976	135	1688	69h	80h	E8h	0	High (11b)	101b
	1280 x 1024	85.024	91.146	157.5	1728	6Ch	00h	E8h	0	High (11b)	101b
SXGA+	1400 x 1050	59.948	64.744	101	1560	61h	80h	A0h	0	Med (10b)	100b
	1400 x 1050	59.978	65.317	121.75	1864	74h	80h	98h	0	Med (10b)	011b
	1400 x 1050	74.867	82.278	156	1896	76h	80h	E0h	0	High (11b)	100b
WXGA (II)	1440 x 900	59.901	55.469	88.75	1600	64h	00h	A0h	0	Med (10b)	100b
	1440 x 900	59.887	55.935	106.5	1904	77h	00h	98h	0	Med (10b)	011b
	1440 x 900	74.984	70.635	136.75	1936	79h	00h	E0h	0	High (11b)	100b
	1440 x 900	84.842	80.43	157	1952	7Ah	00h	E0h	0	High (11b)	100b
UXGA	1600 x 1200	60	75	162	2160	87h	00h	E0h	0	High (11b)	100b

Table A-1. Recommended PLL Settings (continued)

Standard	Resolution	Frame Rate (Hz)	Line Rate (kHz)	Pixel Rate (MHz)	PLL Divider (Total pix/line)	PLLDIV [11:4] Reg 01h [7:0]	PLLDIV [3:0] Reg 02h [7:4]	Reg 03h	Output Divider Reg 04h [0]	VCO Range Reg 03h [7:6]	CP Current Reg 03h [5:3]
Video	720 x 480i	29.97	15.734	13.5	858	35h	A0h	18h	0	ULow (00b)	011b
	720 x 576i	25	15.625	13.5	864	36h	00h	18h	0	ULow (00b)	011b
	720 x 480p	59.94	31.469	27	858	35h	A0h	18h	0	ULow (00b)	011b
	720 x 576p	50	31.25	27	864	36h	00h	18h	0	ULow (00b)	011b
	1280 x 720p	60	45	74.25	1650	67h	20h	A0h	0	Med (10b)	100b
	1280 x 720p	50	37.5	74.25	1980	7Bh	C0h	98h	0	Med (10b)	011b
	1920 x 1080i	60	33.75	74.25	2200	89h	80h	98h	0	Med (10b)	011b
	1920 x 1080i	50	28.125	74.25	2640	A5h	00h	90h	0	Med (10b)	010b
	1920 x 1080p	60	67.5	148.5	2200	89h	80h	E0h	0	High (11b)	100b
	1920 x 1080p	50	56.25	148.5	2640	A5h	00h	D8h	0	High (11b)	011b

Embedded Sync Setups

Table B-1. Embedded Sync Setups

I²C Register	SA	480i60	480p60	720p60	1080i60	1080p60	XGA60
Output Format	15h	47h	47h	47h	47h	47h	47h
AVID Start LSB	40h	91h	93h	47h	06h	43h	43h
AVID Start MSB	41h	00h	00h	01h	01h	01h	01h
AVID Stop LSB	42h	0Bh	0Dh	4Bh	8Ah	8Ah	07h
AVID Stop MSB	43h	00h	00h	06h	08h	08h	00h
VBLK F0 Offset	44h	01h	05h	06h	02h	06h	02h
VBLK F1 Offset	45h	01h	05h	06h	02h	06h	00h
VBLK F0 DUR	46h	26h	2Ah	1Eh	16h	2Dh	26h
VBLK F1 DUR	47h	26h	2Ah	1Eh	17h	2Dh	26h
F0 F-bit	48h	02h	00h	00h	00h	00h	00h
F1 F-bit	49h	01h	00h	00h	00h	00h	00h

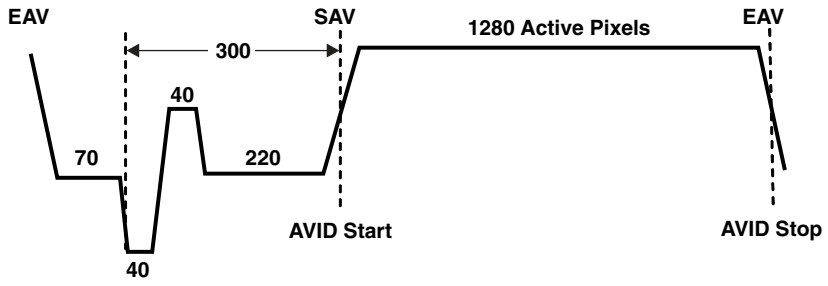


Figure B-1. 720p60 Example, Total Line Length = 1650 Pixels

AVID Start = Delay Factor + tri-level sync width + back-porch = 27 + 300 = 327 (147h)

AVID Stop = AVID Start + Active Pixels +4 = 327 + 1280 +4 = 1611

AVID Stop = 1611 (64Bh)

The horizontal reference point is the leading edge of the negative sync tip. The delay factor is a TVP7002 internal delay factor and can change slightly with SOG LPF settings. If AVID Stop exceeds the total line length, then subtract the total line length from the AVID Stop sum. An additional four pixels must be added to the active video interval.

Color Space Converter Coefficients

```
BEGIN_DATASET  //

DATASET_NAME,"CSC RGB to BT.709 HDTV YCbCr "

WR_REG,TVP7000,0x01,0x18,0x11  // CSC Enabled
WR_REG,TVP7000,0x01,0x4A,0xE3
WR_REG,TVP7000,0x01,0x4B,0x16
WR_REG,TVP7000,0x01,0x4C,0x4F
WR_REG,TVP7000,0x01,0x4D,0x02
WR_REG,TVP7000,0x01,0x4E,0xCE
WR_REG,TVP7000,0x01,0x4F,0x06
WR_REG,TVP7000,0x01,0x50,0xAB
WR_REG,TVP7000,0x01,0x51,0xF3
WR_REG,TVP7000,0x01,0x52,0x00
WR_REG,TVP7000,0x01,0x53,0x10
WR_REG,TVP7000,0x01,0x54,0x55
WR_REG,TVP7000,0x01,0x55,0xFC
WR_REG,TVP7000,0x01,0x56,0x78
WR_REG,TVP7000,0x01,0x57,0xF1
WR_REG,TVP7000,0x01,0x58,0x88
WR_REG,TVP7000,0x01,0x59,0xFE
WR_REG,TVP7000,0x01,0x5a,0x00
WR_REG,TVP7000,0x01,0x5b,0x10
END_DATASET
////////////////////////////////////////////////////////////////////////////////////////////////
//////////////
BEGIN_DATASET  //

DATASET_NAME,"CSC RGB to BT.601 SDTV YCbCr "

WR_REG,TVP7000,0x01,0x18,0x11  // CSC Enabled
WR_REG,TVP7000,0x01,0x4A,0xC9
WR_REG,TVP7000,0x01,0x4B,0x12
WR_REG,TVP7000,0x01,0x4C,0xA6
WR_REG,TVP7000,0x01,0x4D,0x03
WR_REG,TVP7000,0x01,0x4E,0x91
WR_REG,TVP7000,0x01,0x4F,0x09
WR_REG,TVP7000,0x01,0x50,0x66
WR_REG,TVP7000,0x01,0x51,0xF5
WR_REG,TVP7000,0x01,0x52,0x00
WR_REG,TVP7000,0x01,0x53,0x10
WR_REG,TVP7000,0x01,0x54,0x9A
WR_REG,TVP7000,0x01,0x55,0xFA
WR_REG,TVP7000,0x01,0x56,0x9A
WR_REG,TVP7000,0x01,0x57,0xF2
WR_REG,TVP7000,0x01,0x58,0x66
WR_REG,TVP7000,0x01,0x59,0xFD
WR_REG,TVP7000,0x01,0x5a,0x00
WR_REG,TVP7000,0x01,0x5b,0x10
END_DATASET
////////////////////////////////////////////////////////////////////////////////////////////////
//////////
```

Macrovision Support

Macrovision support is provided through use of the MAC_EN bit in I^2C register 22h and the Macrovision Stripper Width setting in I^2C register 34h. The Macrovision Stripper Width setting defines a window that masks undesired signals outside the HSYNC interval to avoid disturbance of the H-PLL. The stripper window is derived from REFCLK cycles, so the settings required depend on which REFCLK is used.

Table D-1. Recommended Reg 34h Macrovsion Stripper Width Settings (MAC_EN = 1)

Video Standard	REG 34h (Internal REFCLK Used)	REG 34h (External 27-Mhz REFCLK Used)
480i and 576i	24h	83h
480p and 576p	12h	43h
720p	07h	12h
1080i	07h	13h
1080p	03h	09h

Note: Settings less than those recommenced above can result in clamp and ALC placement issues. The stripper width setting has no effect when MAC_EN is set to 0.

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