Video Accessory ICs

High Performance VCOs for Image Sampling

BU2373FV,BU2374FV

No.11069EBT07

●Description

General-purpose VCO Series ICs (BU2373FV and BU2374FV) have a built-in VCO and phase comparator and facilitate the configuration of a PLL system through the external connection of a LPF and frequency divider.
Furthermore, in order to facilitate the loop constant settings of the PLL system, the application manual has been enhanced to ensure studies on the application.

●Features

1) The VCO enables midpoint settings within the range of oscillation through the external resistance.
2) The rising edge trigger type of phase comparator is built in.
3) Power-down mode setting can be made independently with the VCO and the phase comparator.
4) The VCO output frequency division can be selected on the SELECT pin.
5) Compact SSOP-B14 Package is adopted.

●Applications

CRT, LCD monitor, and CD-RW

●Line up matrix

		BU2373FV	BU2374FV
Supply voltage	VDD=3.0V	○	−
	VDD=3.3V	○	○
	VDD=5.0V	○	−
Frequency range	VDD=3.0V	37～60MHz	−
	VDD=3.3V	37～65MHz	37～60MHz
	VDD=5.0V	43～100MHz	−
VCO-Frequency dividing mode		1/2	1/4
Operating temperature range		-20～75℃	-20～75℃
Package		SSOP-B14	SSOP-B14

●Absolute maximum ratings (Ta=25℃)

	Symbol	Ratings	Unit
Supply voltage	VDD	-0.5～7.0	V
Input voltage	VIN	-0.5～VDD+0.5	V
Storage temperature range	Tstg	-30～125	℃
Power dissipation	Pd	400	mW

*1 Operating is not guaranteed.
*2 In the case of exceeding Ta = 25℃, 4.0mW should be reduced per 1℃.
*3 The radiation-resistance design is not carried out.
*4 Power dissipation is measured when the IC is mounted to the printed circuit board.

●Electrical characteristics

◎BU2373FV(Ta=25℃, VDD=3.0V, unless otherwise specified.)

Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
(VCO)						
VCO_IN input impedance	Zi	-	10	-	MΩ	
Consumption current (while in normal mode)	Idd(VCO)	-	15	-	mA	With 60 MHz output
Consumption current (while in standby mode)	Idd_st(VCO)	-	-	1	μA	VCO_INHIBIT=”H”, VCOIN=”L”
Control voltage	VI	0.5	-	VDD-0.5	V	
Oscillation range	frange	37	-	60	MHz	
Bias resistor range	Rbias	1.5	-	2.0	KΩ	*1
Frequency sensitivity	β1	-	23	-	MHz/V	*2
Output duty	Duty	45	50	55	%	Measured at a voltage of 1/2 of VDD
(PFD)						
Consumption current (while in normal mode)	Idd(PFD)	-	0.5	-	mA	When 1 MHz is input to the FIN_A and B
Consumption current (while in standby mode)	Idd_st(PFD)	-	-	1	μA	PFD_INHIBIT=”H”, FIN_A,B=”L”

*1 Design guaranteed figures 37 MHz to 45 MHz when Rbias = 2.0 kΩ
50 MHz to 60 MHz when Rbias = 1.5 kΩ
*2 Frequency sensitivity { f1 (VCOIN=2.0V) – f2 (VCOIN = 1.0V) } / 1.0V
*3 If the SELECT pin is set to “H” and the output frequency is reduced to 1/2, the frequency range and the frequency sensitivity will be all reduced to 1/2.

BU2373FV(Ta=25℃, VDD=5.0V, unless otherwise specified.)

Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
(VCO)						
VCO_IN input impedance	Zi	-	10	-	MΩ	
Consumption current (while in normal mode)	Idd(VCO)	-	25	-	mA	With 60 MHz output
Consumption current (while in standby mode)	Idd_st(VCO)	-	-	1	μA	VCO_INHIBIT=”H”, VCOIN=”L”
Control voltage	VI	0.5	-	VDD-0.5	V	
Oscillation range	frange	43	-	100	MHz	
Bias resistor range	Rbias	1.6	-	2.5	KΩ	*1
Frequency sensitivity	β1	-	25	-	MHz/V	*2
Output duty	Duty	45	50	55	%	Measured at a voltage of 1/2 of VDD
(PFD)						
Consumption current (while in normal mode)	Idd(PFD)	-	1	-	mA	When 1 MHz is input to the FIN_A and B
Consumption current (while in standby mode)	Idd_st(PFD)	-	-	1	μA	PFD_INHIBIT=”H”, FIN_A&B=”L”

*1 Design guaranteed figures 43 MHz to 77 MHz when Rbias = 2.5 kΩ
75 MHz to 100 MHz when Rbias = 1.6 kΩ
*2 Frequency sensitivity { f1 (VCOIN = 3.5V) – f2 (VCOIN=1.5 V) } / 2.0V
*3 If the SELECT pin is set to “H” and the output frequency is reduced to 1/2, the frequency range and the frequency sensitivity will be all reduced to 1/2.

◎BU2374FV(Ta=25℃, VDD=3.3V, unless otherwise specified.)

Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
(VCO)						
VCO_IN input impedance	Zi	-	10	-	MΩ	
Consumption current (while in normal mode)	Idd(VCO)	-	12.5	-	mA	With 50 MHz output
Consumption current (while in standby mode)	Idd_st(VCO)	-	-	1	μA	VCO_INHIBIT="H", VCOIN="L"
Control voltage	VI	0.5	-	VDD-0.5	V	
Oscillation range	frange	37	-	60	MHz	
Bias resistor range	Rbias	2.0	-	3.0	KΩ	*1
Frequency sensitivity	β 1	-	23	-	MHz/V	*2
Output duty	Duty	45	50	55	%	Measured at a voltage of 1/2 of VDD
(PFD)						
Consumption current (while in normal mode)	Idd(PFD)	-	0.5	-	mA	When 1 MHz is input to the FIN_A and B
Consumption current (while in standby mode)	Idd_st(PFD)	-	-	1	μA	PFD_INHIBIT="H", FIN_A, B="L"

*1 Design guaranteed figures 37 MHz to 54 MHz when Rbias =2 .0 kΩ
53 MHz to 60 MHz when Rbias = 3.0 kΩ

*2 Frequency sensitivity { f1 (VCOIN = 2.0V) – f2 (VCOIN = 1.0 V) } / 1.0V

*3 If the SELECT pin is set to "H" and the output frequency is reduced to 1/4, the frequency range and the frequency sensitivity will be all reduced to 1/4.

●Reference data

(BU2373FV－Power Voltage Fluctuation Data)

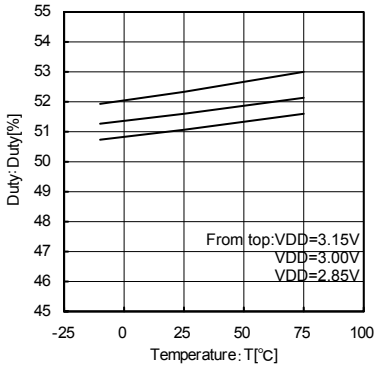


Fig.1 Control Vole – Output Frequency
(VDD=3.0V,Rbias=1.5KΩ,Ta=25℃)

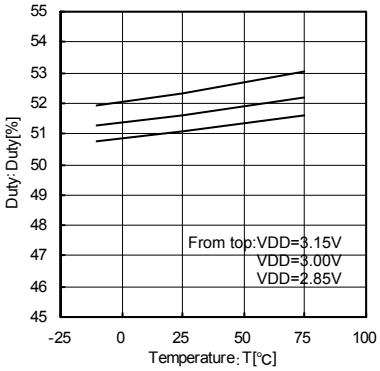


Fig.2 Control Voltage – Output Frequency
(VDD=3.0V,Rbias=1.8KΩ,Ta=25℃)

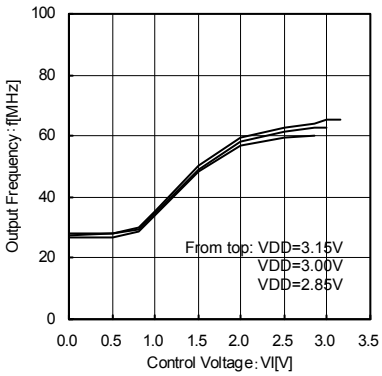


Fig.3 Control Voltage – Output Frequency
(VDD=3.0V,Rbias=2.0KΩ,Ta=25℃)

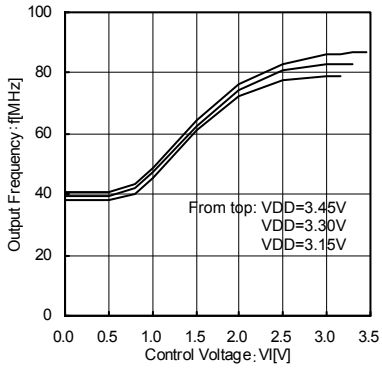


Fig.4 Control Voltage – Output Frequency
(VDD=3.3V,Rbias=1.6KΩ,Ta=25℃)

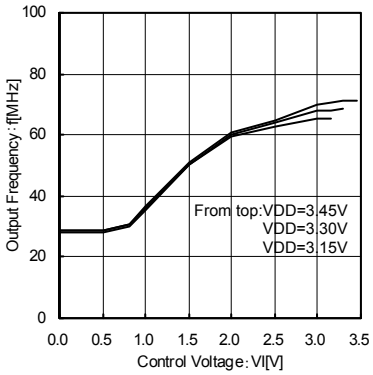


Fig.5 Control Voltage – Output Frequency
(VDD=3.3V,Rbias=2.0 KΩ,Ta=25℃)

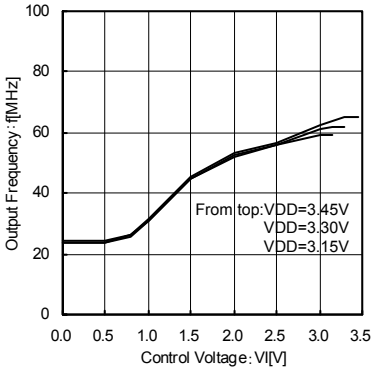


Fig.6 Control Voltage – Output Frequency
(VDD=3.3V,Rbias=2.2 KΩ,Ta=25℃)

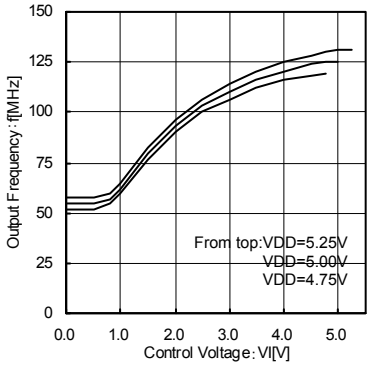


Fig.7 Control Voltage – Output Frequency
(VDD=5.0V,Rbias=1.6KΩ,Ta=25℃)

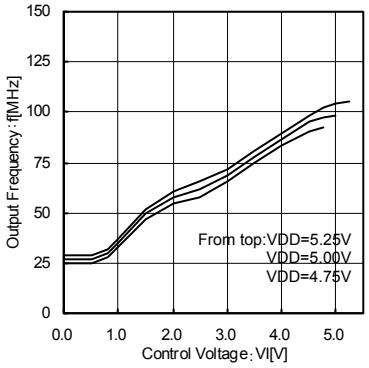


Fig.8 Control Voltage – Output Frequency
(VDD=5.0V,Rbias=2.4KΩ,Ta=25℃)

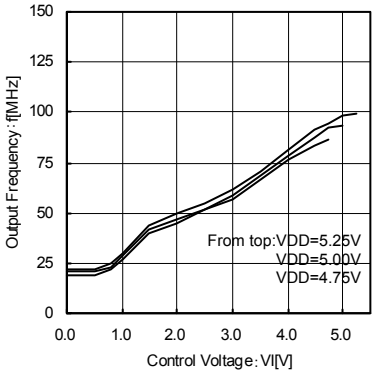


Fig.9 Control Voltage – Output Frequency
(VDD=5.0V,Rbias=2.7KΩ,Ta=25℃)

●**Reference data**

(BU2373FV－Temperature Fluctuation Data)

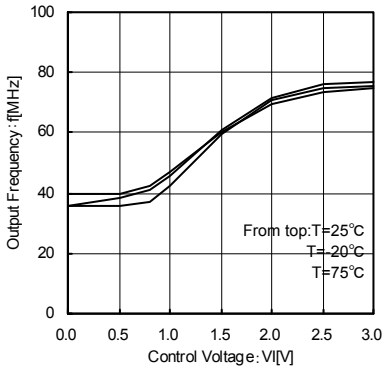


Fig.10 Control Voltage – Output Frequency
(VDD=3.0V,Rbias=1.5KΩ)

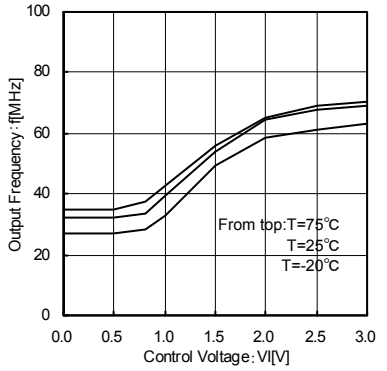


Fig.11 Control Voltage – Output Frequency
(VDD=3.0V,Rbias=1.8KΩ)

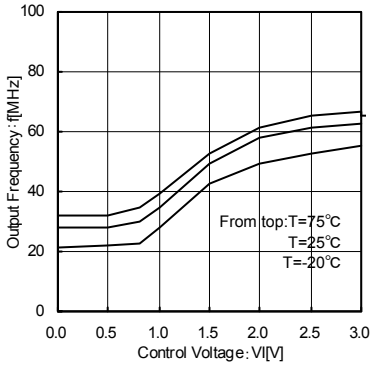


Fig.12 Control Voltage – Output Frequency
(VDD=3.0V,Rbias=2.0 KΩ)

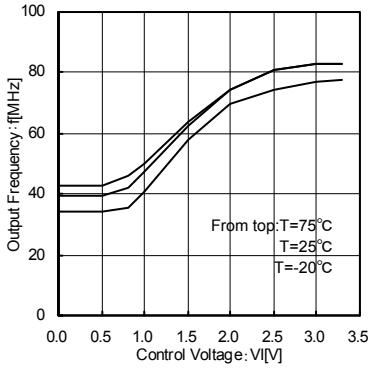


Fig.13 Control Voltage – Output Frequency
(VDD=3.3V,Rbias=1.6KΩ)

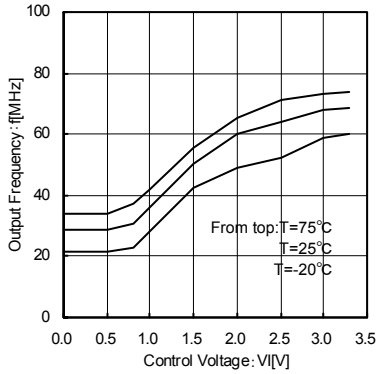


Fig.14 Control Voltage – Output Frequency
(VDD=3.3V,Rbias=2.0KΩ)

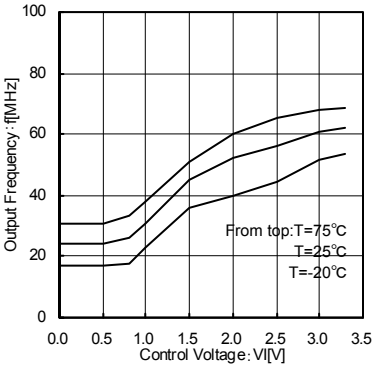


Fig.15 Control Voltage – Output Frequency
(VDD=3.3V,Rbias=2.2KΩ)

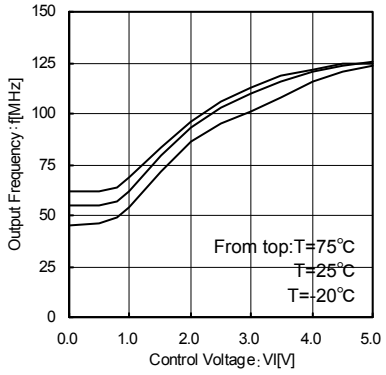


Fig.16 Control Voltage – Output Frequency
(VDD=5.0V,Rbias=1.6KΩ)

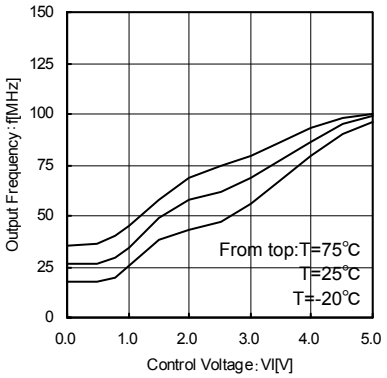


Fig.17 Control Voltage– Output Frequency
(VDD=5.0V,Rbias=2.4KΩ)

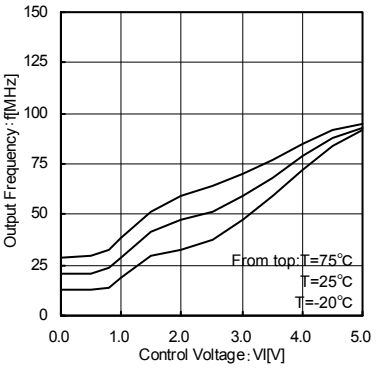


Fig.18 Control Voltage – Output Frequency
(VDD=5.0V,Rbias=2.7KΩ)

●Reference data

(BU2373FV－Recommended Oscillation Range, Frequency - Frequency Sensitivity)

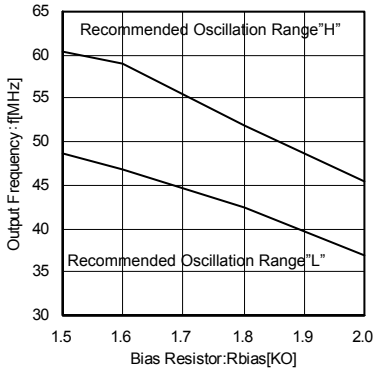


Fig.19 Bias Resistance
- Recommended Oscillation Range
(VDD=3.0V, Select="L")

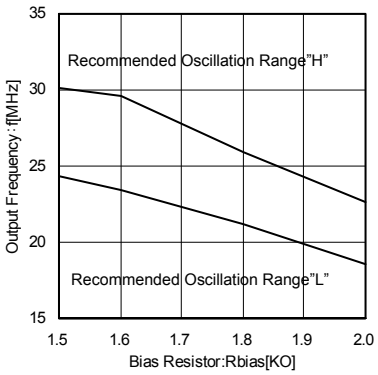


Fig.20 Bias Resistance
- Recommended Oscillation Range
(VDD=3.0V, Select="H")

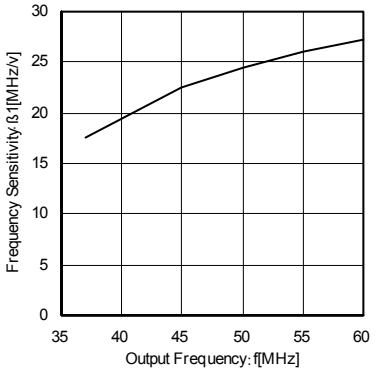


Fig.21 Output Frequency
- Frequency Sensitivity
(VDD=3.0V, Select="L")

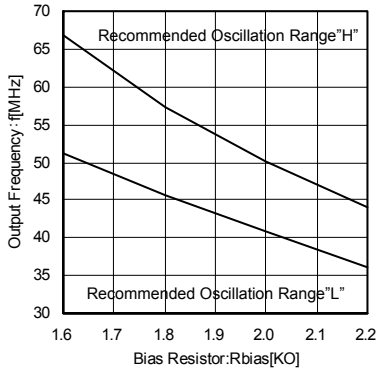


Fig.22 Bias Resistance
- Recommended Oscillation Range
(VDD=3.3V, Select="L")

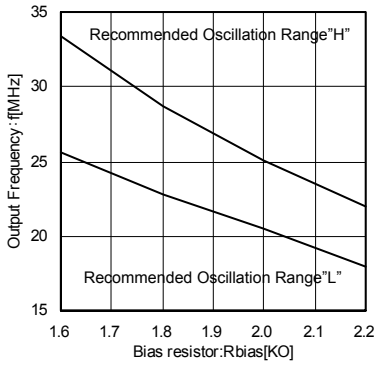


Fig.23 Bias Resistance -
Recommended Oscillation Range
(VDD=3.3V, Select="H")

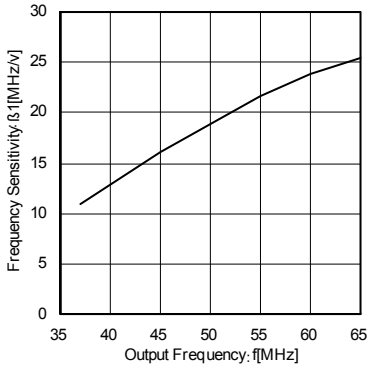


Fig.24 Output Frequency
- Frequency Sensitivity
(VDD=3.3V, Select="L")

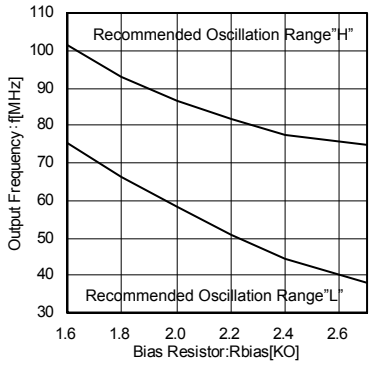


Fig.25 Bias Resistance –
Recommended Oscillation Range
(VDD=5.0V, Select="L")

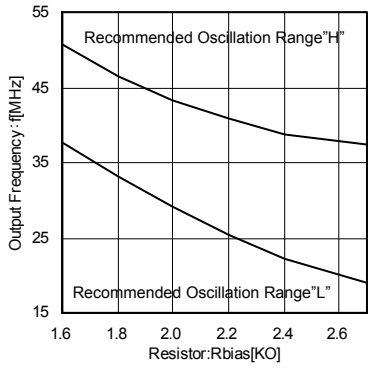


Fig.26 Bias Resistance –
Recommended Oscillation Range
(VDD=5.0V, Select="H")

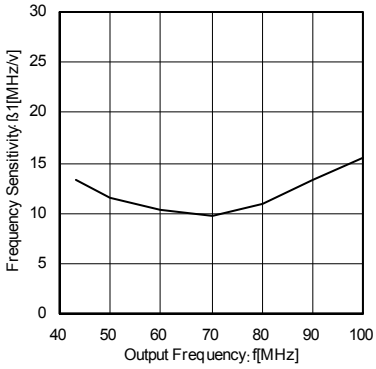


Fig.27 Output Frequency
- Frequency Sensitivity
(VDD=5.0V, Select="L")

●**Reference data**

(BU2374FV－Power Voltage Fluctuation Data)

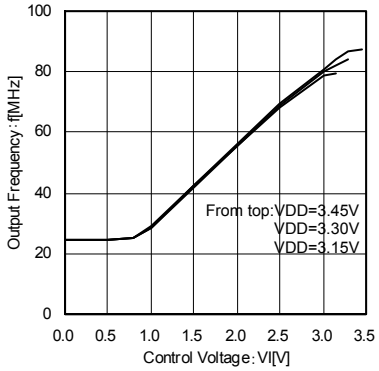


Fig.28 Control Voltage – Output Frequency
(VDD=3.3V,Rbias=2.0KΩ,Ta=25℃)

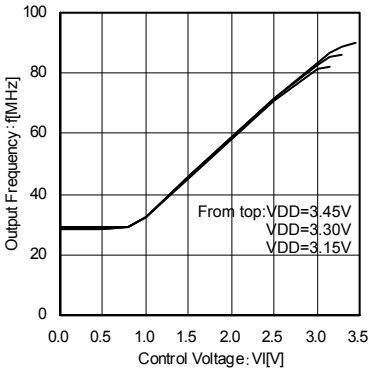


Fig.29 Control Voltage – Output Frequency
(VDD=3.3V,Rbias=2.4 KΩ,Ta=25℃)

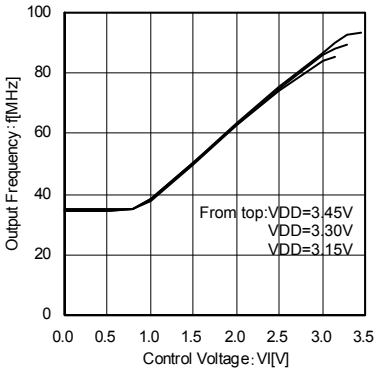


Fig.30Control Voltage – Output Frequency
(VDD=3.3V,Rbias=3.0KΩ,Ta=25℃)

●**Reference data**

(BU2374FV－Temperature Fluctuation Data)

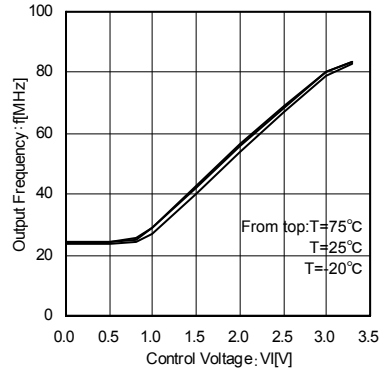


Fig.31 Control Voltage – Output Frequency
(VDD=3.3V,Rbias=2.0KΩ)

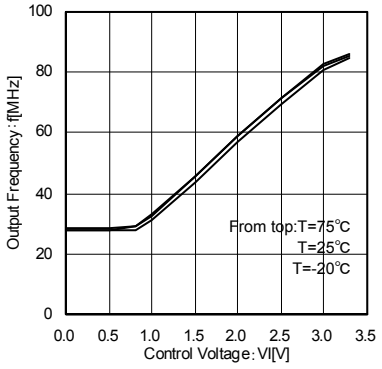


Fig.32 Control Voltage – Output Frequency
(VDD=3.3V,Rbias=2.4KΩ)

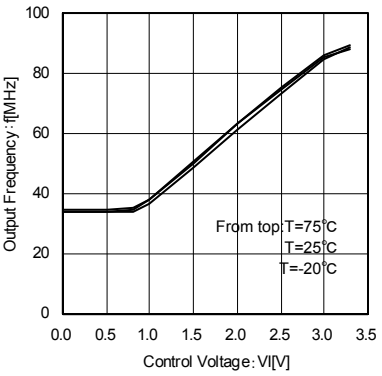


Fig.33 Control Voltage – Output Frequency
(VDD=3.3V,Rbias=3.0KΩ)

●**Reference data**

(BU2374FV－Recommended Oscillation Range, Frequency - Frequency Sensitivity)

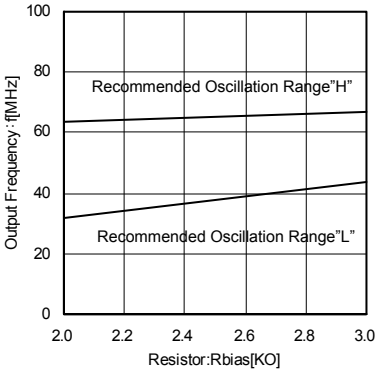


Fig.34 Bias Resistance
– Recommended Oscillation Range
(VDD=3.3V, Select="L")

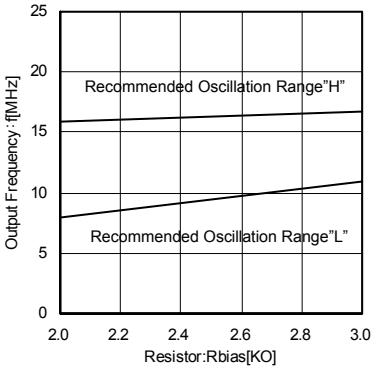


Fig.35 Bias Resistance
– Recommended Oscillation Range
(VDD=3.3V, Select="H")

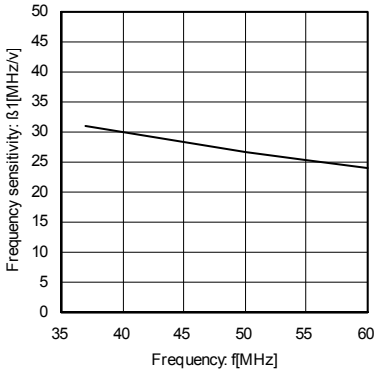


Fig.36 Output Frequency
- Frequency Sensitivity
(VDD=3.3V, Select="L")

●Reference data

(BU2373FV－VCO Free-run Output Characteristics)

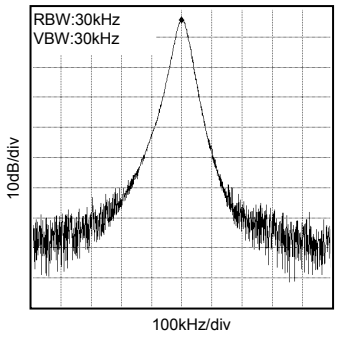


Fig.37 Spectrum Waveform
(VDD=3.0V,Select="L",Output=50MHz)

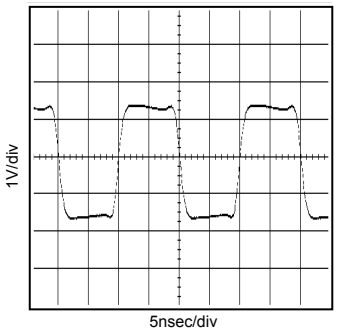


Fig.38 Output Waveform
(VDD=3.0V,Select="L",Output=50MHz)

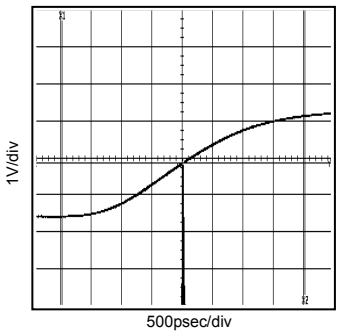


Fig.39 Period-Jitter Waveform
(VDD=3.0V,Select="L",Output=50MHz)

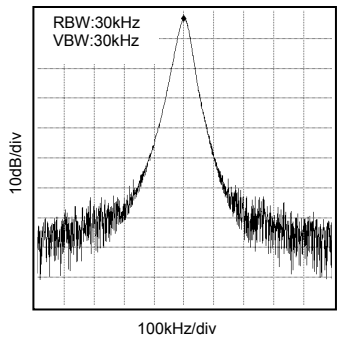


Fig40 Spectrum Waveform
(VDD=3.3V,Select="L",Output=50MHz)

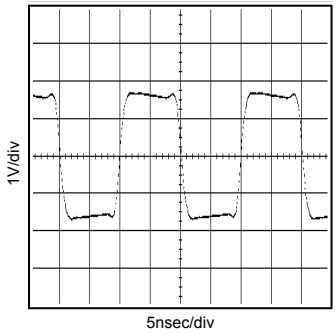


Fig.41 Output Waveform
(VDD=3.3V, Select="L", Output=50MHz)

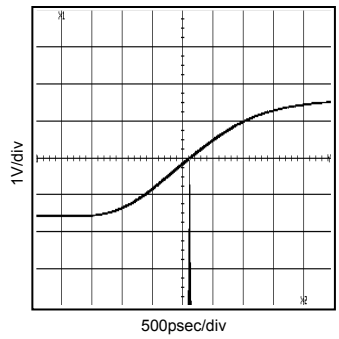


Fig.42 Period-Jitter Waveform
(VDD=3.3V,Select ="L", Output=50MHz)

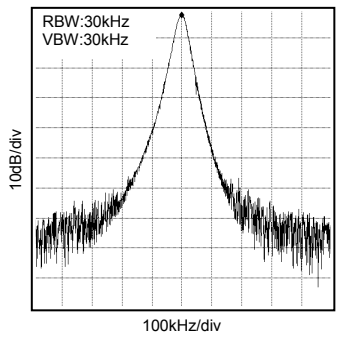


Fig.43 Spectrum Waveform
(VDD=5.0V,Select="L",Output=75MHz)

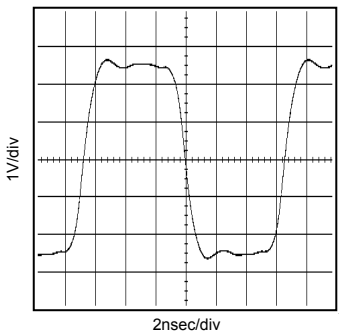


Fig.44 Output Waveform
(VDD=5.0V,Select="L",Output=75MHz)

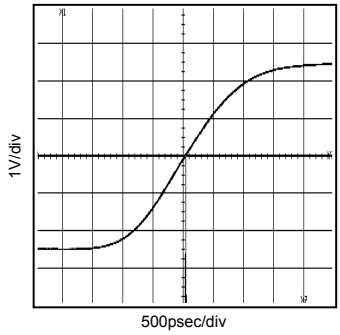


Fig.45 Period-Jitter Waveform
(VDD=5.0V,Select="L",Output=75MHz)

●Reference data

(BU2374FV－VCO Free-run Output Characteristics)

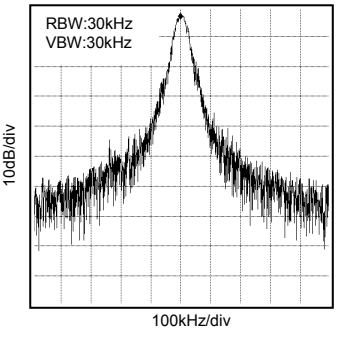


Fig.46 Spectrum Waveform
(VDD=3.3V,Select="L",Output=50MHz)

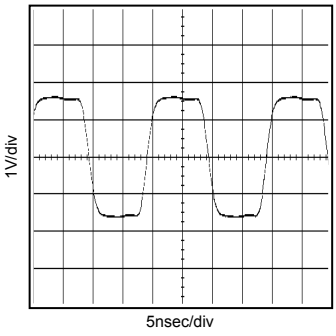


Fig.47 Output Waveform
(VDD=3.3V,Select="L",Output=50MHz)

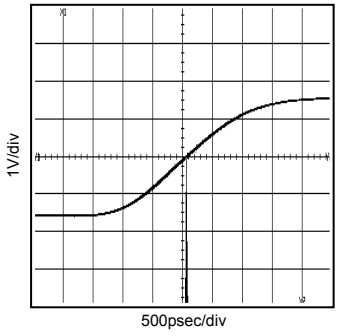
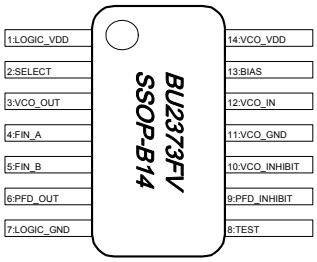


Fig.48 Period-Jitter Waveform
(VDD=3.3V,Select="L",Output=50MHz)

●Block diagram

(BU2373FV)



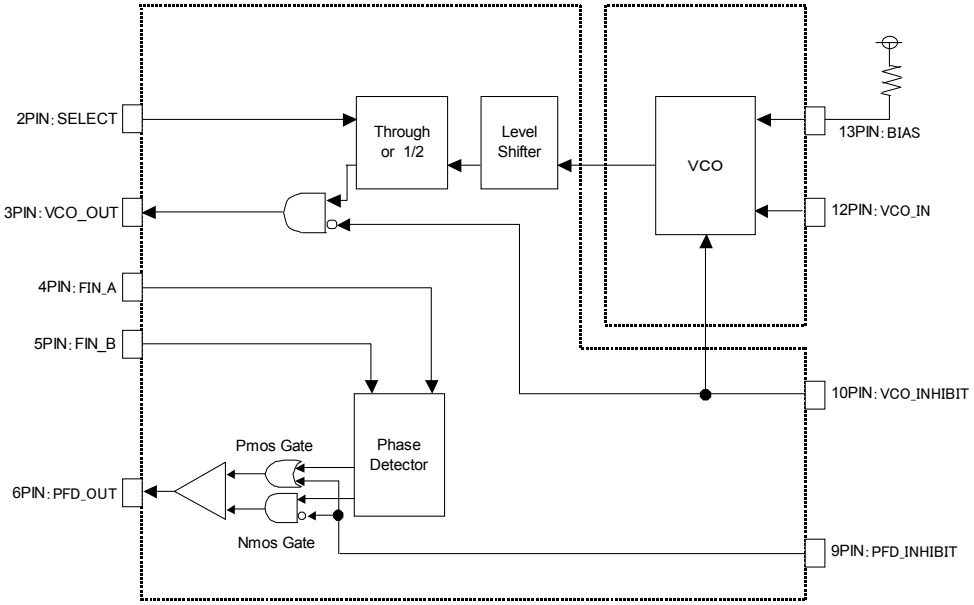
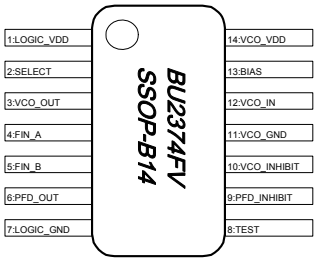


Fig.49

(BU2374FV)



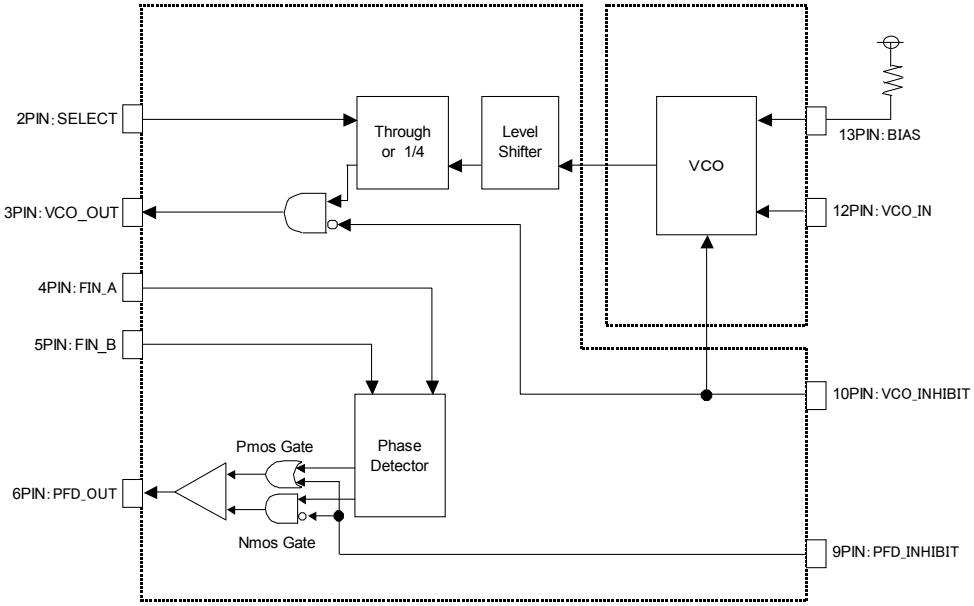


Fig.50

●Pin assignment function

PIN NO.	PIN name	Function
1	LOGIC_VDD	Power supply for the internal Logic and the VCO output, which should be separated from power supply for the VCO_VDD (analog block).
2	SELECT	VCO output frequency dividing mode selection pin. H: Frequency dividing output, L: Through output
3	VCO_OUT	VCO output pin. If the VCO_INHIBIT is set to “H”, the VCO_OUT will be fixed to L.
4	FIN-A	Reference frequency input pin
5	FIN-B	VCO block frequency dividing input pin, which inputs after the VCO output frequency is divided through the external counter.
6	PFD_OUT	Phase comparator output pin. If the PFD_INHIBIT is set to “H”, the PFD_OUT will be set to Hi-Z output.
7	LOGIC_GND	GND for the internal Logic and the VCO output
8	TEST	Test mode pin, which is normally used with set to OPEN or fixed to L. Equipped with Pull-down resistor.
9	PFD_INHIBIT	Phase comparator inhibit control pin. If the PFD_INHIBIT is set to “H”, the PFD_OUT will be set to Hi-Z output.
10	VCO_INHIBIT	VCO inhibit control pin. If the VCO_INHIBIT is set to “H”, the VCO_OUT will be fixed to L output.
11	VCO_GND	GND for VCO (Analog block GND)
12	VCO_IN	VCO control pin, to which loop filter output for the PLL system is connected due to frequency control on normal system.
13	BIAS	Bias current setting pin for the shift of VCO oscillation range. A resistor is connected to the VCO_VDD for the control of bias current.
14	VCO_VDD	VDD for VCO (power supply for analog block)

●Example of application circuit

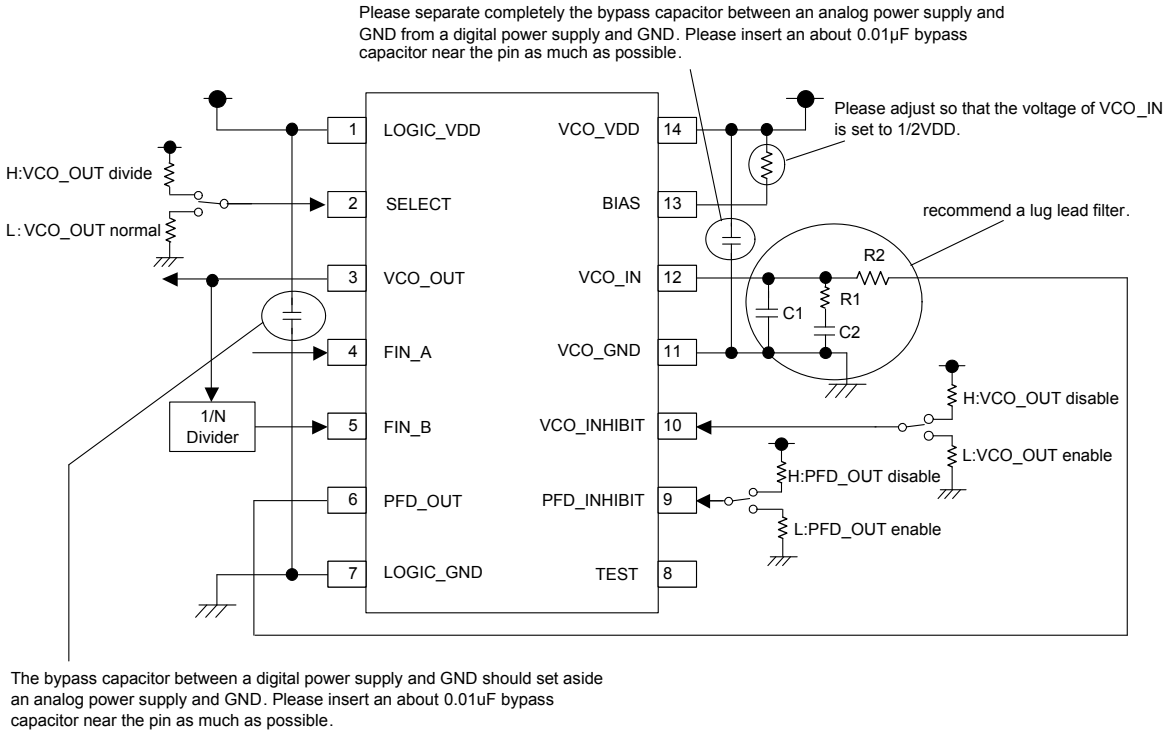


Fig.51

* It is recommended to use bypass capacitors of good high-frequency characteristics.
* It is recommended to apply power supply in the LOGIC_VDD and LOGIC_GND circuits for the SELECT. PFD_INHIBIT, and VCO_INHIBIT control pins.

●Description of operations

<VCO Block>

Our VCO block consists of ring oscillators using 5-step reverse Amp. Setting the 2PIN: SELECT to “H” makes it possible to set the system to output frequency dividing mode. (The frequency is divided to 1/2 on the BU2373FV, while 1/4 on the BU2374FV.) 50% of the frequency is guaranteed even to the duty at this time.

Furthermore, setting the 10Pin: VCO_INHIBIT to “H” makes it possible to set the system to power-down mode. While in power-down mode, the VCO_OUT output is fixed to “L”, thus achieving reduction in Analog consumption current approximately by 80%.

In addition, through the adjustment of external resistance value for the BIAS terminal on 13Pin, the fine adjustment of output frequency can be made.

(VCO I/O Characteristics)

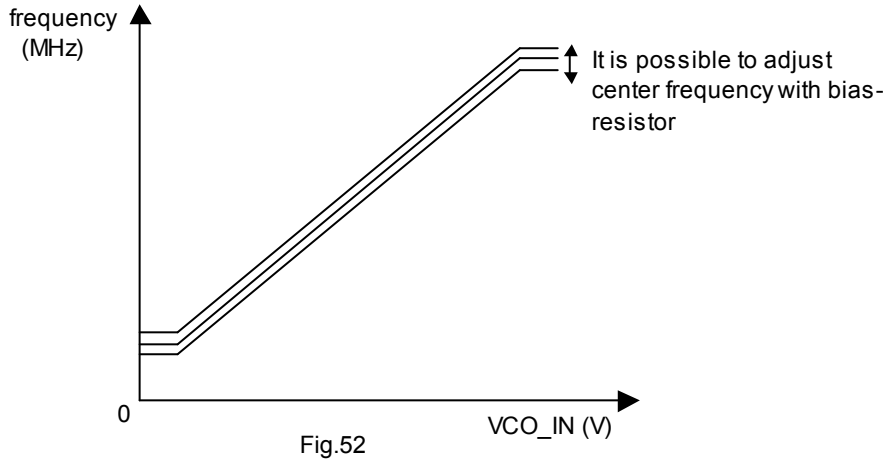


Fig.52

* The VCO built in the BU2373FV has been designed to provide the lowest frequency sensitivity when using the VCO_IN at about VDD/2. To make use of the VCO, it is recommended to adjust the BIAS resistance so that the voltage of the VCO_IN will reach VDD/2.

(Configuration of VCO Block)

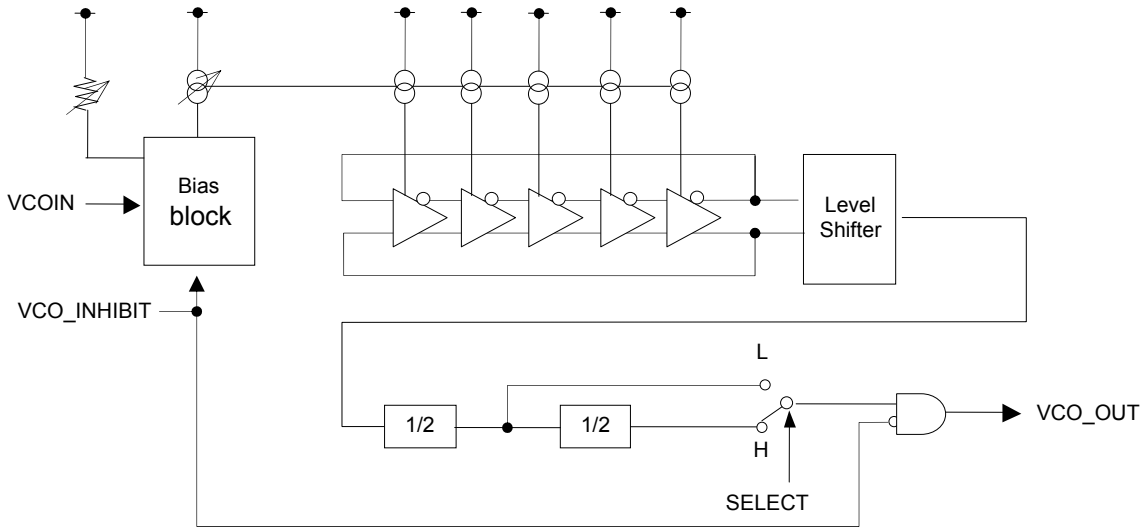


Fig.53

<Phase Comparator>

Our phase comparator is of rising edge detection type. This phase comparator shows the characteristics shown below.

(1) The phase comparator outputs an error pulse (UP signal) after the rising edge is detected at the FIN-A until the rising edge is detected at the FIN-B, and then it is reset.
(2) The phase comparator outputs an error pulse (DOWN signal) after the rising edge is detected at the FIN-B until the rising edge is detected at the FIN-A, and then it is reset.

Furthermore, setting the 9Pin: PFD_INHIBIT to “H” makes it possible to set the system to power-down mode. While in power-down mode, the PFD_OUT outputs high impedance. In other words, it is brought to reset state with the Logic power supply. (A leak current of 1 μA or less is guaranteed.)

(I/O Characteristics of Phase Comparator)

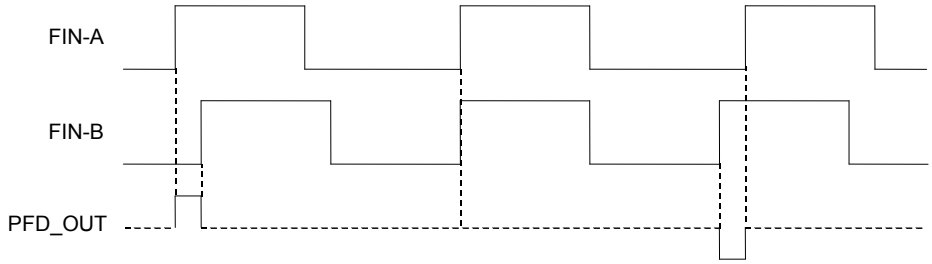


Fig.54

●Reference data

(Common to BU2373FV & BU2374FV – Phase Comparator I/O Waveform)

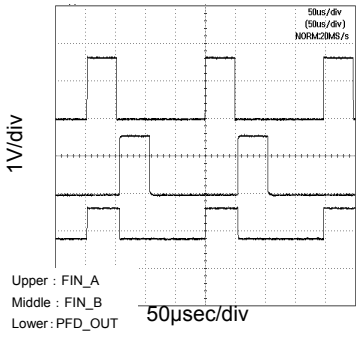


Fig.55 UP Signal Output
(VDD=3.3V, FIN_A > FIN_B)

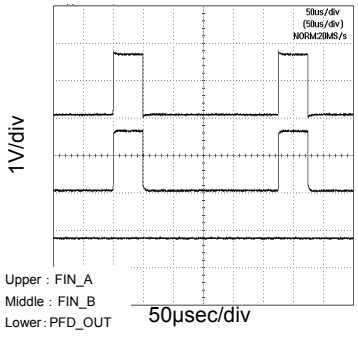


Fig.56 No Error Signal Output
(VDD=3.3V, FIN_A = FIN_B)

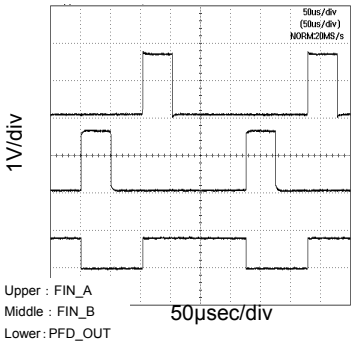


Fig.57 DOWN Signal Output
(VDD=3.3V, FIN_A < FIN_B)

(Functioning of PLL System)

In order to configure the stable PLL system, the following section describes the functional principle, open loop characteristics, and closed loop characteristics by block shown in the Block Diagram below.

<PLL System Block Diagram>

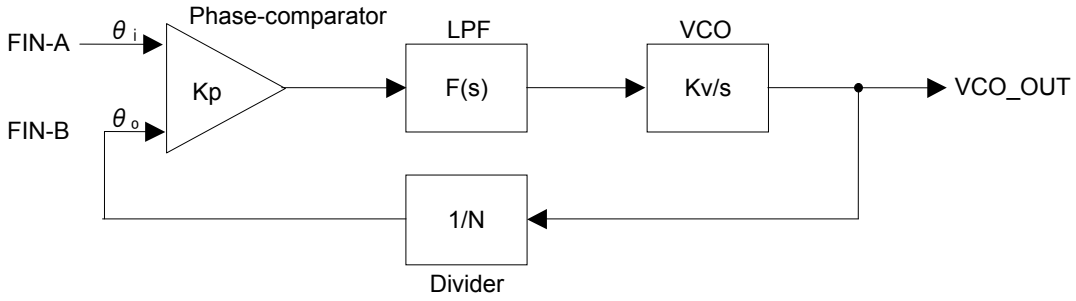


Fig.58

① Phase Comparator

The phase comparator shows the characteristics shown in figure below. Assuming that the Gain is Kp, Kp=(VOH−VOL)/4π(V/rad)

② VCO (Voltage Controlled Oscillator)

The VCO shows the characteristics shown in figure below.
Assuming that the Gain is Kv, Kv=2× π × (fmax-fmin)/(Vmax-Vmin)(rad/s/V)

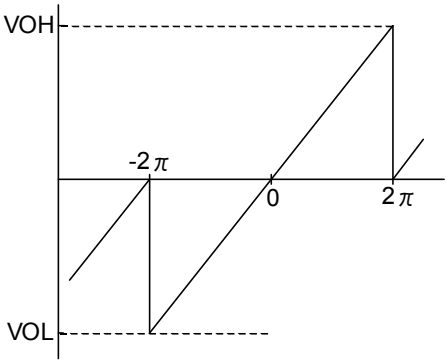


Fig.59 Phase Comparator Characteristics

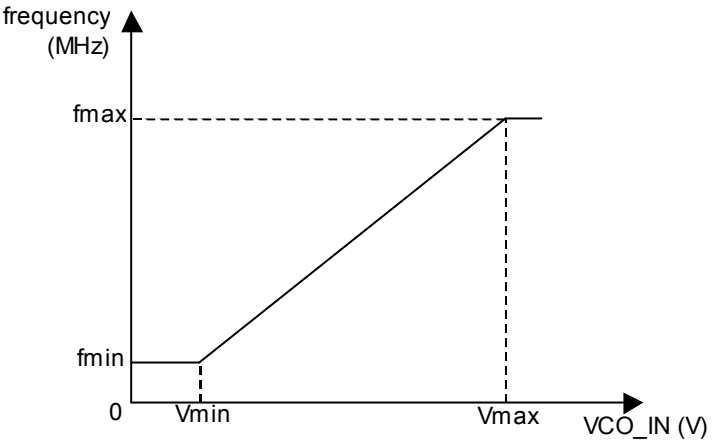


Fig.60 VCO Characteristics

③ LPF (Lag-Lead Filter)

Calculate the Gain of the lag-lead filter. It is recommended to use the filter having the pattern shown below.

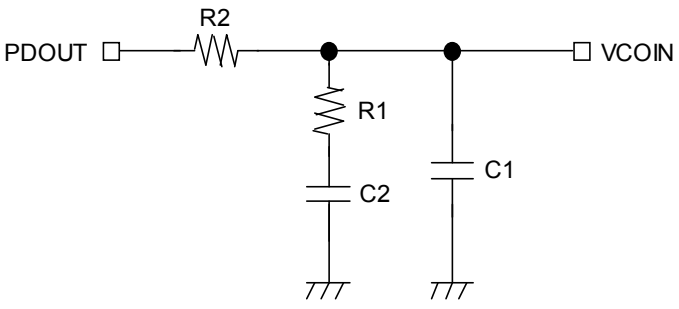


Fig.61

For the lag-lead filter afore-mentioned, assuming that C1 << C2 (C2 is used at a value approx. 10 times as high as C1), break this filter into two portions as shown below to facilitate the calculation, thus proceeding with the calculation.

(1)

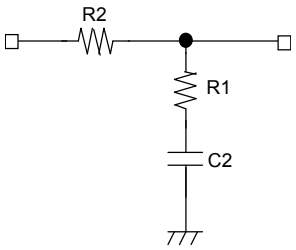


Fig.62 LPF Portion ①

(2)

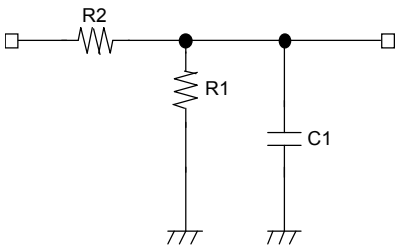


Fig.63 LPF Portion ②

In the case of (1) above,

$$F(s) = \frac{VOUT}{VIN} = \frac{R1+\dfrac{1}{S\cdot C2}}{R1+R2+\dfrac{1}{S\cdot C2}} = \frac{S\cdot C2\cdot R1+1}{S\cdot C2\cdot(R1+R2)+1} \qquad (S=j\omega)$$

$$|F(j\omega)| = \sqrt{\frac{1+\omega^2\cdot C2^2\cdot R1^2}{1+\{\omega\cdot C2\cdot(R1+R2)\}^2}} \qquad (\omega=2\pi f)$$

$$\phi(\omega) = \tan^{-1}(\omega\cdot C2\cdot R1)-\tan^{-1}\{\omega\cdot C2\cdot(R1+R2)\}$$

・By the expression above, the Gain and the Phase are given as shown in graphs below.

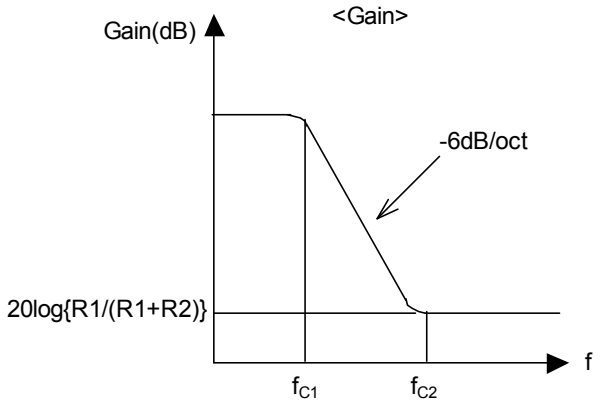


Fig.64 (Fig.62) Frequency – Gain Characteristics

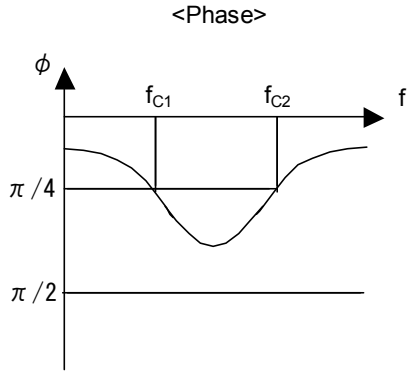


Fig.65 (Fig.62) Frequency – Phase Characteristics

$$\left(f_{C1} = \frac{1}{2\pi}\times\frac{1}{C2\cdot(R1+R2)}, \quad fc2 = \frac{1}{2\pi}\times\frac{1}{C2\cdot R1} \right)$$

In the case of (2) above,

$$F(s) = \frac{VOUT}{VIN} = \frac{\dfrac{R1}{1+S\cdot C1\cdot R1}}{R2+\dfrac{R1}{1+S\cdot C1\cdot R1}} = \frac{\dfrac{R1}{R1+R2}}{S\cdot C1\cdot\dfrac{R1\cdot R2}{R1+R2}+1} \qquad (S=j\omega)$$

$$|F(j\omega)| = \sqrt{\frac{\dfrac{R1^2}{(R1+R2)^2}}{1+\omega^2\cdot C1^2\cdot\dfrac{R1^2\cdot R2^2}{(R1+R2)^2}}} \qquad (\omega=2\pi f)$$

$$\phi(\omega) = -\tan^{-1}\{\omega\cdot C1\cdot\frac{R1\cdot R2}{(R1+R2)}\}$$

・By the expression aforementioned, the Gain and the Phase are given as shown in graphs below.

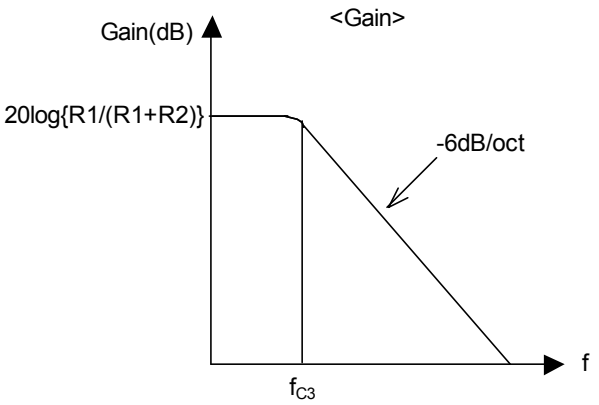


Fig.66 (Fig.63) Frequency – Gain Characteristics

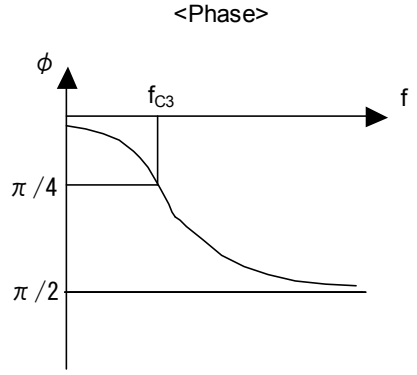


Fig.67 (Fig.63) Frequency – Phase Characteristics

$$\left(f_{C3} = \frac{1}{2\pi} \times \frac{R1+R2}{C1 \cdot R1 \cdot R2} \right)$$

By combining (1) and (2), finding the Gain and the Phase of the lag-lead filter,

$$F(s) = \frac{VOUT}{VIN} = \frac{1+S \cdot C2 \cdot R1}{\{1+S \cdot C2 \cdot (R1+R2)\} \times \{1+ S \cdot C1 \cdot \frac{R1 \cdot R2}{R1+R2}\}} \quad (S=j\omega)$$

The gain and the Phase are given as shown below, respectively.

$$Gain=20 \cdot \log\{\frac{G2}{G1 \times G3}\}, \quad Phase=\theta 2-\theta 1-\theta 3$$

$$\begin{cases} G1=\sqrt{1+C2^2 \cdot (R1+R2)^2 \cdot (2\pi f)^2}, & \theta 1= -\tan^{-1}\{2\pi f \cdot C2 \cdot (R1+R2)\} \\ G2=\sqrt{1+C2^2 \cdot R1^2 \cdot (2\pi f)^2}, & \theta 2= \tan^{-1}(2\pi f \cdot C2 \cdot R1) \\ G3=\sqrt{1+C1^2 \cdot R1^2 \cdot \frac{1}{(R1+R2)^2} \cdot (2\pi f)^2}, & \theta 3= -\tan^{-1}\{2\pi f \cdot C1 \cdot \frac{R1 \cdot R2}{(R1+R2)}\} \end{cases}$$

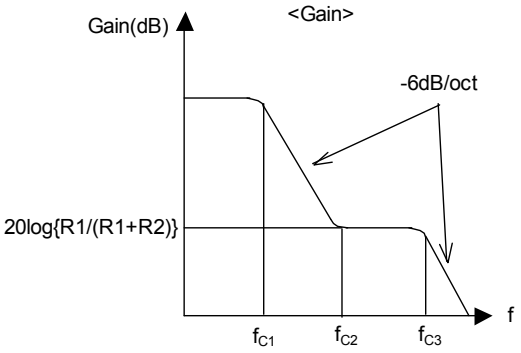


Fig.68 (Fig.61) Frequency – Gain Characteristics

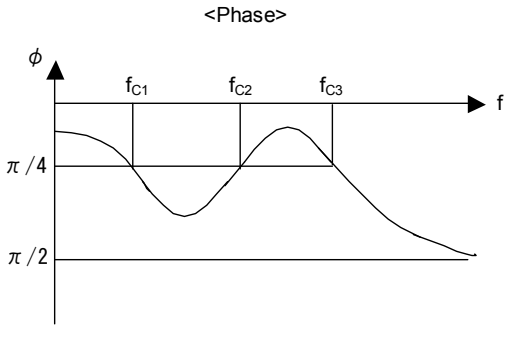


Fig.69 (Fig.61) Frequency – Phase Characteristics

・Where, find the Gain for the open loop of PLL system. Assuming that the transfer function is H(s),

$$H(s)= Kp\times F(s)\times \frac{Kv}{S}\times\frac{1}{N}$$

$$\begin{cases} Kp\times\dfrac{Kv}{S}\times\dfrac{1}{N}=\dfrac{1}{S\times\dfrac{N}{Kp\times Kv}} \\ G0=\sqrt{\left(\dfrac{2\pi f\times N}{Kp\times Kv}\right)^2}\ , \quad \theta 0=-\tan^{-1}\left(2\pi f\cdot\dfrac{N}{Kp\times Kv}\right)=\dfrac{\pi}{2} \end{cases}$$

$$PLL\text{-}Gain=20\cdot\log\left\{\frac{G2}{G1\times G3\times G0}\right\}\ , \quad Phase=-\theta 0+\theta 2-\theta 1-\theta 3$$

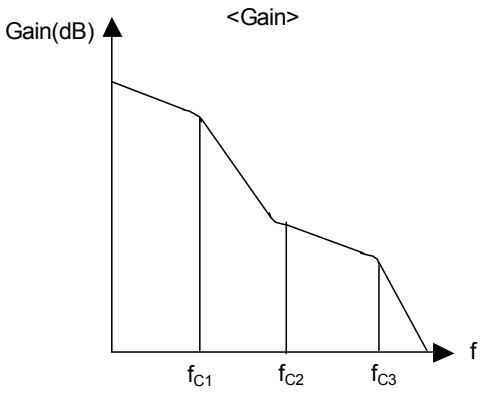


Fig.70 (Fig.58) Frequency – Gain Characteristics

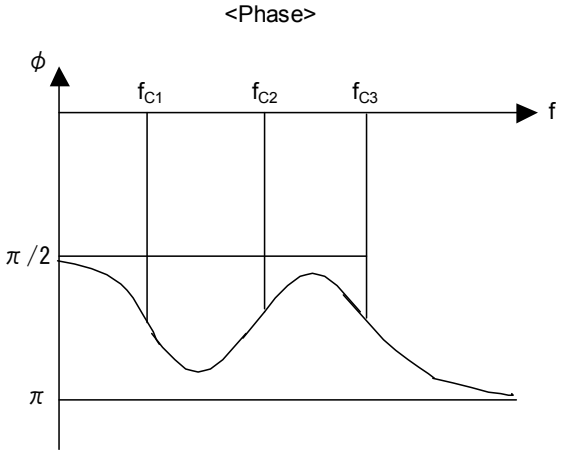


Fig.71 (Fig.58) Frequency – Phase Characteristics

If, by the expression above, the LPF constant is selected so that a phase margin of 45° or more is secured when the Gain for the open loop becomes 0 dB, the PLL system will stably function.

Note)

・As to the jitters, the TYP values vary with the substrate, power supply, output loads, noises, and others. Besides, for the use of the BU2373FV or the BU2374FV, the operating margin should be thoroughly checked.
・The Analog power supply and the Logic power supply should be separated from each other so that noises generated with the Logic power supply have no adverse influences on the Analog power one.
・Bypass capacitors between the power supply and GND should be mounted as close as possible.
・Power to control pins (i.e., VCO_INHIBIT, PFD_INHIBIT and SELECT) should be supplied from the logic power supply.
・In order to configure the PLL system, the LPF GND should be connected to the Analog GND and mounted in the proximity of the VCO_IN.

●Notes for use

(1) Absolute Maximum Ratings
An excess in the absolute maximum ratings, such as applied voltage (VDD or VIN), operating temperature range (Topr), etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

(2) Recommended operating conditions
These conditions represent a range within which characteristics can be provided approximately as expected. The electrical characteristics are guaranteed under the conditions of each parameter.

(3) Reverse connection of power supply connector
The reverse connection of power supply connector can break down ICs. Take protective measures against the breakdown due to the reverse connection, such as mounting an external diode between the power supply and the IC's power supply terminal.

(4) Power supply line
Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines.
In this regard, for the digital block power supply and the analog block power supply, even though these power supplies has the same level of potential, separate the power supply pattern for the digital block from that for the analog block, thus suppressing the diffraction of digital noises to the analog block power supply resulting from impedance common to the wiring patterns. For the GND line, give consideration to design the patterns in a similar manner.
Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use an electrolytic capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

(5) GND voltage
Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.

(6) Short circuit between terminals and erroneous mounting
In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.

(7) Operation in strong electromagnetic field
Be noted that using ICs in the strong electromagnetic field can malfunction them.

(8) Inspection with set PCB
On the inspection with the set PCB, if a capacitor is connected to a low-impedance IC terminal, the IC can suffer stress. Therefore, be sure to discharge from the set PCB by each process. Furthermore, in order to mount or dismount the set PCB to/from the jig for the inspection process, be sure to turn OFF the power supply and then mount the set PCB to the jig. After the completion of the inspection, be sure to turn OFF the power supply and then dismount it from the jig. In addition, for protection against static electricity, establish a ground for the assembly process and pay thorough attention to the transportation and the storage of the set PCB.

(9) Input terminals
In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

(10) Ground wiring pattern
If small-signal GND and large-current GND are provided, It will be recommended to separate the large-current GND pattern from the small-signal GND pattern and establish a single ground at the reference point of the set PCB so that resistance to the wiring pattern and voltage fluctuations due to a large current will cause no fluctuations in voltages of the small-signal GND. Pay attention not to cause fluctuations in the GND wiring pattern of external parts as well.

(11) External capacitor
In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

●Ordering part number

B	U	2	3	7	3	F	V	-	E	2

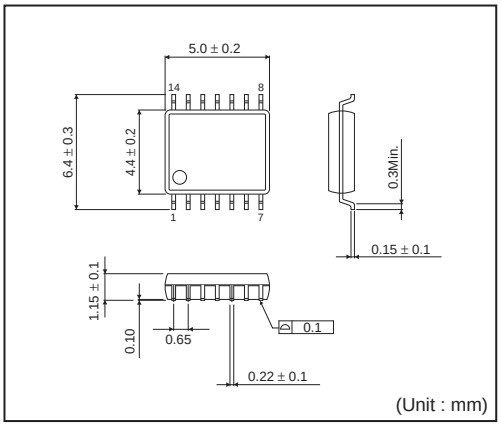
Part No.

Part No.
2373
2374

Package
F: SSOP-B14

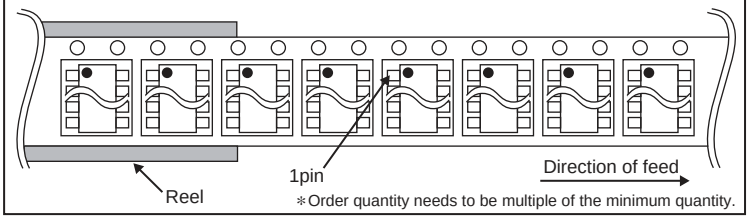
Packaging and forming specification
E2: Embossed tape and reel

SSOP-B14



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

Notes

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