

NUP4302MR6

Schottky Diode Array for Four Data Line ESD Protection

The NUP4302MR6 is designed to protect high speed data line interface from ESD, EFT and lightning.

Features

- Very Low Forward Voltage Drop
- Fast Switching
- PN Junction Guard Ring for Transient and ESD Protection
- ESD Rating of Class 3B (Exceeding 16 kV) per Human Body Model and Class C (Exceeding 400 V) per Machine Model
- IEC 61000-4-2 Level 4 ESD Protection
- Flammability Rating: UL 94 V-0
- Pb-Free Package is Available

Applications

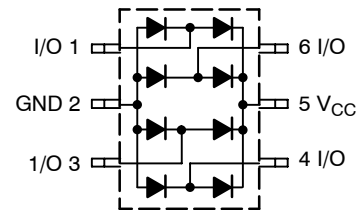
- Ultra High-Speed Switching
- USB 1.1 and 2.0 Power and Data Line Protection
- Digital Video Interface (DVI)
- Monitors and Flat Panel Displays



ON Semiconductor®

<http://onsemi.com>

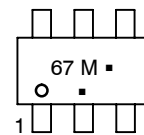
PIN CONFIGURATION AND SCHEMATIC



MARKING DIAGRAM



TSOP-6
CASE 318G
STYLE 12



- 67 = Specific Device Code
- M = Date Code
- = Pb-Free Package

(Note: Microdot may be in either location)

*Date Code orientation may vary depending upon manufacturing location.

ORDERING INFORMATION

Device	Package	Shipping†
NUP4302MR6T1	TSOP-6	3000/Tape & Reel
NUP4302MR6T1G	TSOP-6 (Pb-Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NUP4302MR6

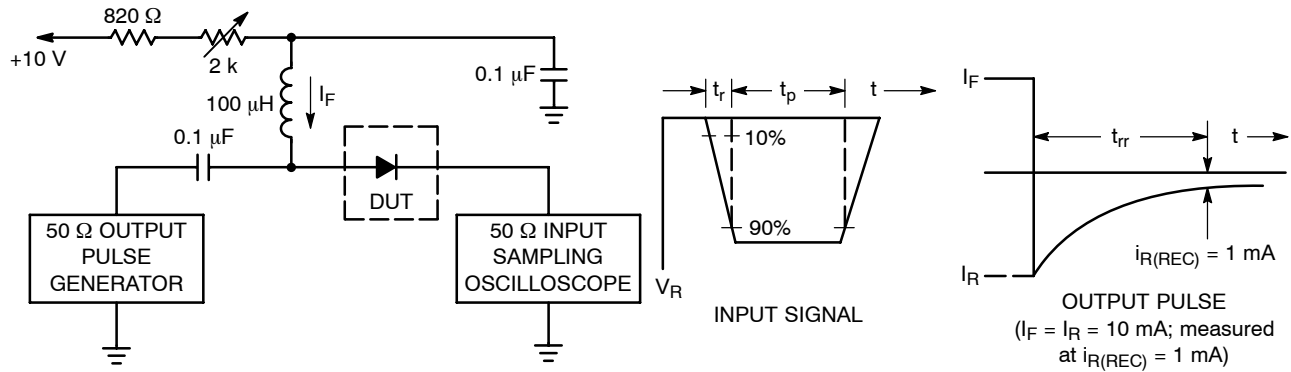
MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Peak Reverse Breakdown Voltage	V_{BR}	30	V
Forward Power Dissipation ($T_A = 25^\circ\text{C}$)	P_F	225	mW
Forward Continuous Current	I_F	200	mA
Junction Operating Temperature	T_J	-55 to +125	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-55 to +150	$^\circ\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reverse Breakdown Voltage	V_{BR}	$I_R = 100 \mu\text{A}$	30			V
Reverse Leakage	I_R	$V_R = 25 \text{ V}$			30	μA
Forward Voltage	V_F	$I_F = 0.1 \text{ mAdc}$			0.28	V
Forward Voltage	V_F	$I_F = 1.0 \text{ mAdc}$			0.35	V
Forward Voltage	V_F	$I_F = 10 \text{ mAdc}$			0.45	V
Forward Voltage	V_F	$I_F = 100 \text{ mAdc}$			1.00	V
Total Capacitance	C_T	$V_R = 0 \text{ V}, f = 1.0 \text{ MHz}, \text{I/O to Ground}$ $V_R = 0 \text{ V}, f = 1.0 \text{ MHz}, \text{I/O to I/O}$			28 18	pF
Reverse Recovery Time	t_{rr}	$I_F = I_R = 10 \text{ mA}, I_{R(\text{REC})} = 1.0 \text{ mA}$ (Figure 1)			5.0	ns



- Notes: 1. A 2.0 k Ω variable resistor adjusted for a Forward Current (I_F) of 10 mA.
 2. Input pulse is adjusted so $I_{R(\text{peak})}$ is equal to 10 mA.
 3. $t_p \gg t_{rr}$

Figure 1. Recovery Time Equivalent Test Circuit

NUP4302MR6

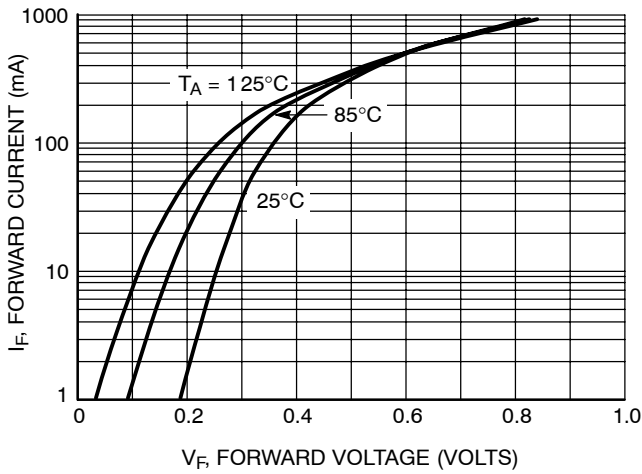


Figure 2. Forward Current as a Function of Forward Voltage; Typical Values

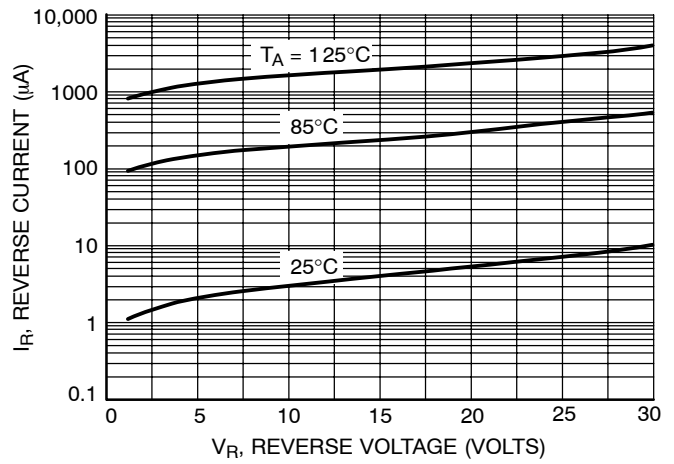


Figure 3. Reverse Current as a Function of Reverse Voltage; Typical Values

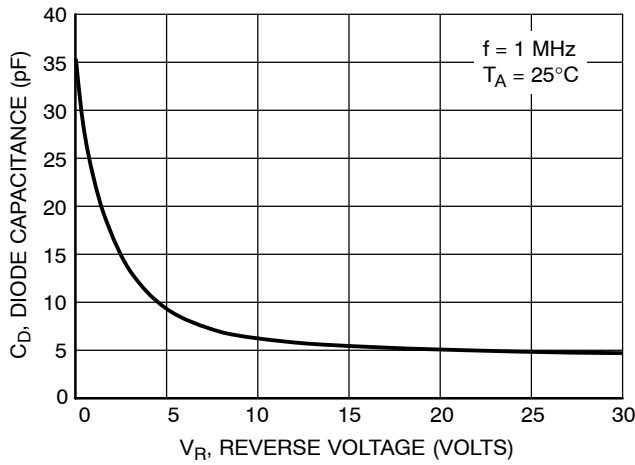


Figure 4. Diode Capacitance as a Function of Reverse Voltage; Typical Values

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS



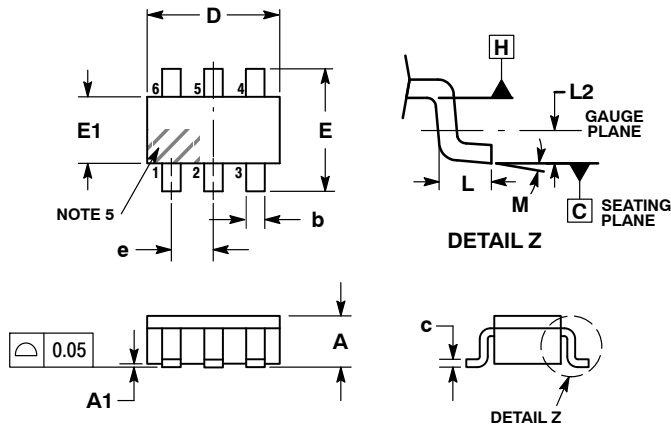
SCALE 2:1

TSOP-6

CASE 318G-02

ISSUE V

DATE 12 JUN 2012



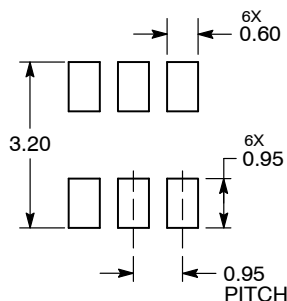
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
5. PIN ONE INDICATOR MUST BE LOCATED IN THE INDICATED ZONE.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.01	0.06	0.10
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.90	3.00	3.10
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e	0.85	0.95	1.05
L	0.20	0.40	0.60
L2	0.25 BSC		
M	0°	-	10°

- | | | | | | |
|--|--|---|---|---|--|
| <p>STYLE 1:</p> <p>PIN 1. DRAIN</p> <p>2. DRAIN</p> <p>3. GATE</p> <p>4. SOURCE</p> <p>5. DRAIN</p> <p>6. DRAIN</p> | <p>STYLE 2:</p> <p>PIN 1. EMITTER 2</p> <p>2. BASE 1</p> <p>3. COLLECTOR 1</p> <p>4. EMITTER 1</p> <p>5. BASE 2</p> <p>6. COLLECTOR 2</p> | <p>STYLE 3:</p> <p>PIN 1. ENABLE</p> <p>2. N/C</p> <p>3. R BOOST</p> <p>4. Vz</p> <p>5. V in</p> <p>6. V out</p> | <p>STYLE 4:</p> <p>PIN 1. N/C</p> <p>2. V in</p> <p>3. NOT USED</p> <p>4. GROUND</p> <p>5. ENABLE</p> <p>6. LOAD</p> | <p>STYLE 5:</p> <p>PIN 1. EMITTER 2</p> <p>2. BASE 2</p> <p>3. COLLECTOR 1</p> <p>4. EMITTER 1</p> <p>5. BASE 1</p> <p>6. COLLECTOR 2</p> | <p>STYLE 6:</p> <p>PIN 1. COLLECTOR</p> <p>2. COLLECTOR</p> <p>3. BASE</p> <p>4. EMITTER</p> <p>5. COLLECTOR</p> <p>6. COLLECTOR</p> |
| <p>STYLE 7:</p> <p>PIN 1. COLLECTOR</p> <p>2. COLLECTOR</p> <p>3. BASE</p> <p>4. N/C</p> <p>5. COLLECTOR</p> <p>6. EMITTER</p> | <p>STYLE 8:</p> <p>PIN 1. Vbus</p> <p>2. D(in)</p> <p>3. D(in)+</p> <p>4. D(out)+</p> <p>5. D(out)</p> <p>6. GND</p> | <p>STYLE 9:</p> <p>PIN 1. LOW VOLTAGE GATE</p> <p>2. DRAIN</p> <p>3. SOURCE</p> <p>4. DRAIN</p> <p>5. DRAIN</p> <p>6. HIGH VOLTAGE GATE</p> | <p>STYLE 10:</p> <p>PIN 1. D(OUT)+</p> <p>2. GND</p> <p>3. D(OUT)-</p> <p>4. D(IN)-</p> <p>5. VBUS</p> <p>6. D(IN)+</p> | <p>STYLE 11:</p> <p>PIN 1. SOURCE 1</p> <p>2. DRAIN 2</p> <p>3. DRAIN 2</p> <p>4. SOURCE 2</p> <p>5. GATE 1</p> <p>6. DRAIN 1/GATE 2</p> | <p>STYLE 12:</p> <p>PIN 1. I/O</p> <p>2. GROUND</p> <p>3. I/O</p> <p>4. I/O</p> <p>5. VCC</p> <p>6. I/O</p> |
| <p>STYLE 13:</p> <p>PIN 1. GATE 1</p> <p>2. SOURCE 2</p> <p>3. GATE 2</p> <p>4. DRAIN 2</p> <p>5. SOURCE 1</p> <p>6. DRAIN 1</p> | <p>STYLE 14:</p> <p>PIN 1. ANODE</p> <p>2. SOURCE</p> <p>3. GATE</p> <p>4. CATHODE/DRAIN</p> <p>5. CATHODE/DRAIN</p> <p>6. CATHODE/DRAIN</p> | <p>STYLE 15:</p> <p>PIN 1. ANODE</p> <p>2. SOURCE</p> <p>3. GATE</p> <p>4. DRAIN</p> <p>5. N/C</p> <p>6. CATHODE</p> | <p>STYLE 16:</p> <p>PIN 1. ANODE/CATHODE</p> <p>2. BASE</p> <p>3. EMITTER</p> <p>4. COLLECTOR</p> <p>5. ANODE</p> <p>6. CATHODE</p> | <p>STYLE 17:</p> <p>PIN 1. EMITTER</p> <p>2. BASE</p> <p>3. ANODE/CATHODE</p> <p>4. ANODE</p> <p>5. CATHODE</p> <p>6. COLLECTOR</p> | |

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

GENERIC MARKING DIAGRAM*



IC

STANDARD

- | | |
|----------------------------|----------------------------|
| XXX = Specific Device Code | XXX = Specific Device Code |
| A = Assembly Location | M = Date Code |
| Y = Year | ▪ = Pb-Free Package |
| W = Work Week | |
| ▪ = Pb-Free Package | |

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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