Uni-directional Ultra Low Capacitance ESD Protection Diode

DESCRIPTIONS

The TESDH5V0U04P2Q1 is an ultra-low capacitance ESD protection diode which includes two uni-directional ESD rated clamping cells to protect high speed data interfaces. It has been specifically designed to protect sensitive electronic components which are connected to data and transmission lines from over-stress caused by ESD (Electrostatic Discharge).

TESDH5V0U04P2Q1 is a unique design which includes proprietary clamping cells in a small package. During transient conditions, the proprietary clamping cells prevent over-voltage on the control/data/power lines, protecting any downstream components.

The TESDH5V0U04P2Q1 may be used to provide ESD protection up to ±20kV (contact and air discharge) according to IEC61000-4-2, and withstand peak pulse current up to 4A (8/20μs) according to IEC61000-4-5.

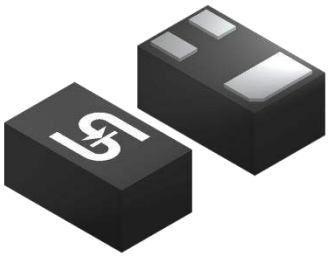
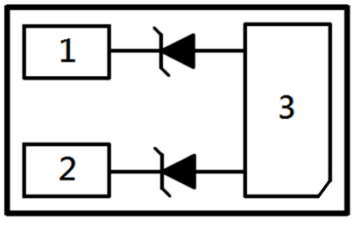
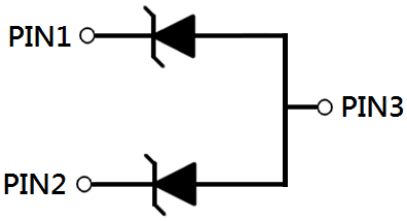
FEATURES

- ESD Protect for 2 high-speed I/O channels
- Provide ESD protection for each channel to IEC 61000-4-2 (ESD) ±20kV (air), ±20kV (contact) IEC 61000-4-5 (Lightning) 4A (8/20us)
- Low clamping voltage : V_{CL} = 22.2V @ I_{TLP} = 16A
- Ultra-low capacitance: 0.65pF
- Ultra-small DFN1006-3L package
- Fast turn-on and Low clamping voltage
- Moisture sensitivity level: level 1, per J-STD-020
- RoHS Compliant
- Halogen-Free according to IEC 61249-2-21

APPLICATION

- IEEE 1394
- PCI Express
- USB 2.0 and 3.0
- SATA and eSATA
- HDMI 1.3, 1.4 and 2.0 version
- Portable Electronics and Notebooks

Pb-Free RoHS COMPLIANT HALOGEN FREE

PACKAGE: DFN1006-3L	PIN CONFIGURATION		CIRCUIT DIAGRAM
			
	PIN 1	Cathode 1	
	PIN 2	Cathode 2	
	PIN 3	Anode	

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETER	SYMBOL	VALUE	UNIT
Peak pulse power (tp = 8/20us)	P_{PK}	60	W
Peak pulse current (tp = 8/20us)	I_{PP}	4	A
ESD according to IEC61000-4-2 air discharge	V_{ESD}	±20	kV
ESD according to IEC61000-4-2 contact discharge		±20	kV
Operating junction temperature range	T_J	-55 to +125	°C
Storage temperature range	T_{STG}	-55 to +150	°C

ELECTRICAL SPECIFICATIONS (T_A = 25°C unless otherwise noted)

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Reverse working voltage		V_{RWM}	-	-	5	V
Reverse breakdown voltage	I_R = 1mA, T_J = 25°C	V_{BR}	7	-	9	V
Forward voltage	I_F = 10mA, T_J = 25°C	V_F	0.6	-	1.2	V
Reverse leakage current	V_{RWM} = 5V	I_R	-	-	100	nA
Clamping voltage[1]	I_{PP} = 1A, tp = 8/20us	V_C	-	-	11	V
	I_{PP} = 4A, tp = 8/20us		-	-	15	V
Clamping voltage[2]	I_{TLP} = 16A, tp = 100ns	V_{CL}	-	22.2	-	V
Junction capacitance	1MHz, V_R = 0V Pin1 or 2 to Pin3	C_J	-	0.57	0.65	pF
	1MHz, V_R = 0V Between Pin1 and Pin2		-	0.25	0.40	pF
Dynamic resistance[2]		R_{DYN}	-	0.85	-	Ω

Notes:

1. Non-repetitive current pulse, according to IEC61000-4-5.
2. TLP parameter: Z_0 = 50 Ω, tp = 100ns, tr = 2ns, averaging window from 60ns to 80ns. RDYN is calculated from 4A to 16A.

ORDERING INFORMATION

ORDERING CODE	PACKAGE	PACKING
TESDH5V0U04P2Q1 RNG	DFN1006-3L	10,000 / 7" Reel

CHARACTERISTICS CURVES

(T_A = 25°C unless otherwise noted)

Fig.1 Peak Pulse Power vs. Junction Temperature

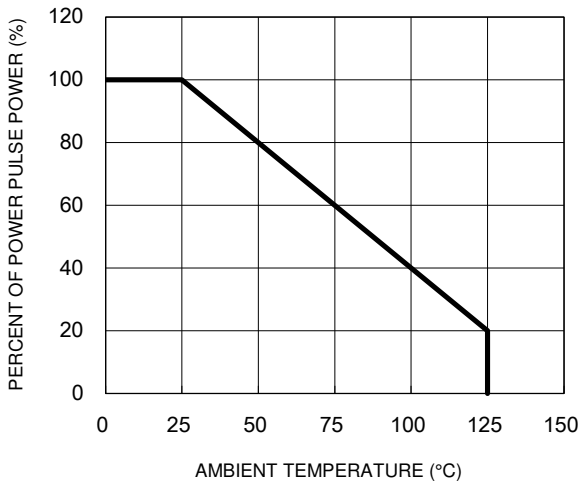


Fig.2 Non-Repetitive Peak Pulse Power vs. Pulse Time

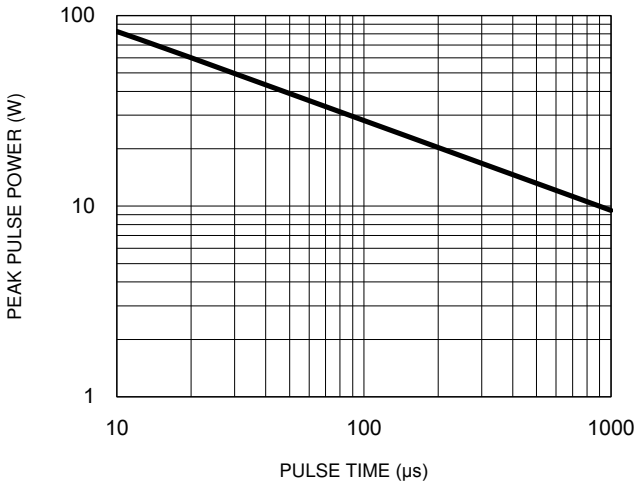


Fig.3 Clamping Voltage vs. Peak Pulse Current

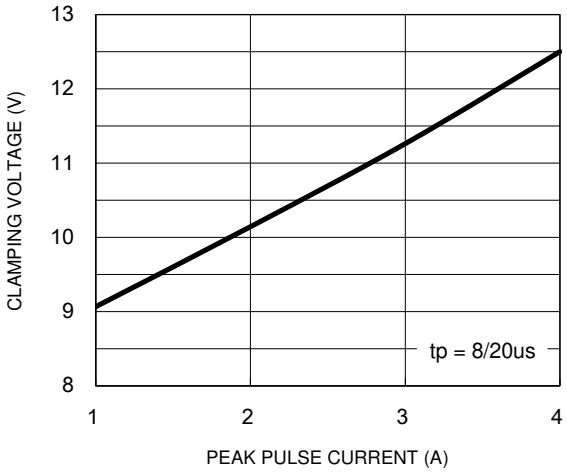


Fig.4 Capacitance vs. Reverse Voltage

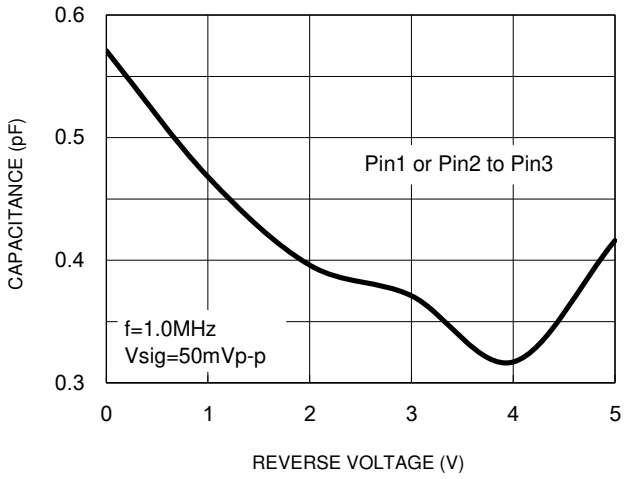
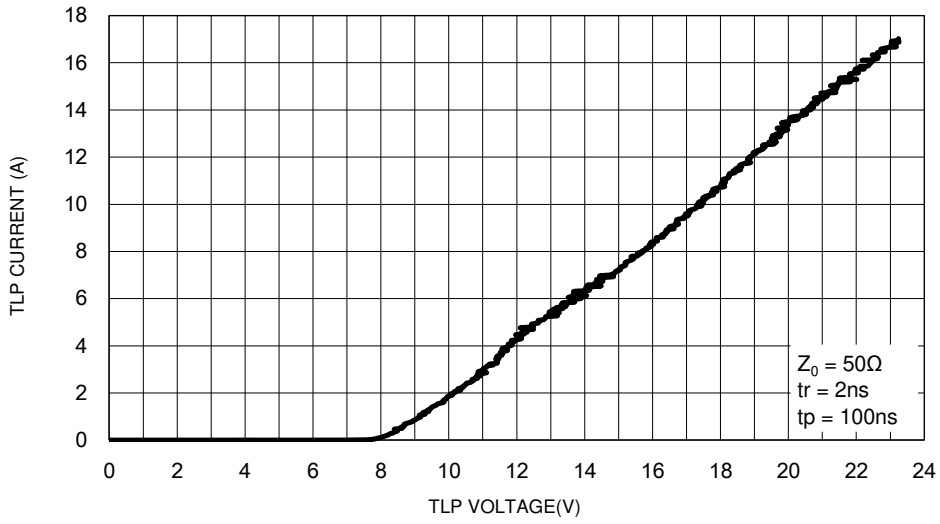


Fig.5 TLP Curve



CHARACTERISTICS CURVES

(T_A = 25°C unless otherwise noted)

Fig.6 8/20μs pulse waveform per IEC61000-4-5

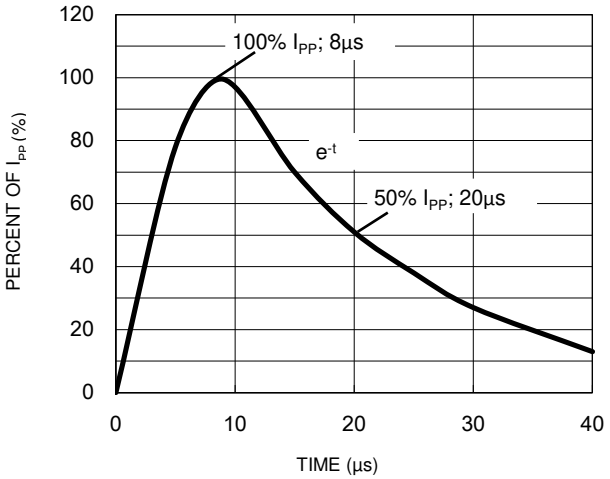
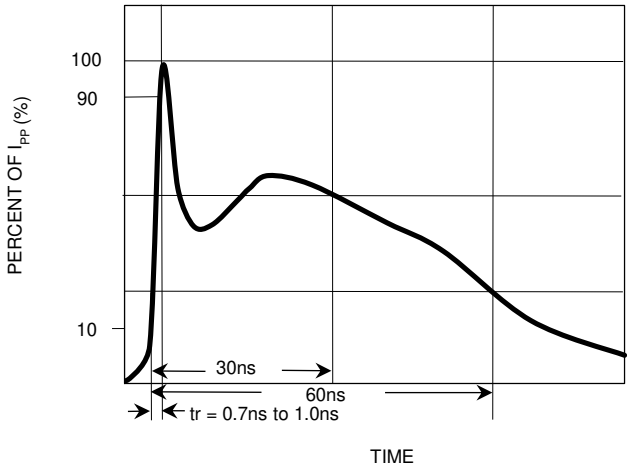


Fig.7 ESD pulse waveform per IEC61000-4-2



APPLICATION INFORMATION

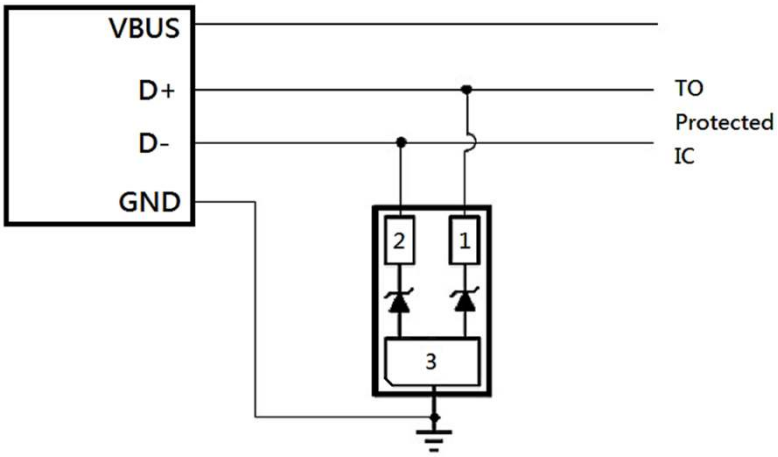
Device Connection

The TESDH5V0U04P2Q1 is designed to protect two data lines from transient over-voltage (such as ESD stress pulse). The device connection of TESDH5V0U04P2Q1 is shown in the Fig. 1. In Fig. 1, the two protected data lines are connected to the ESD protection pins (pin1, pin2) of TESDH5V0U04P2Q1. The ground pin (pin3) of TESDH5V0U04P2Q1 is a negative reference pin. This pin should be directly connected to the GND rail of PCB (Printed Circuit Board). To get minimum parasitic inductance, the path length should keep as shortas possible.

TESDH5V0U04P2Q1 can provide protection for 2 I/O signal lines simultaneously. If the number of I/O signal lines is less than 2, the unused I/O pin canbe simply left as NC pin.

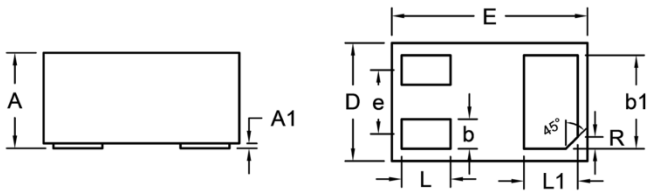
The TESDH5V0U04P2Q1 is designed to protect two high speed line against ESD. The Fig.1 below shown the onnection for USB interface ESD protection

Fig.1 Data lines connection of TESDH5V0U04P2Q1



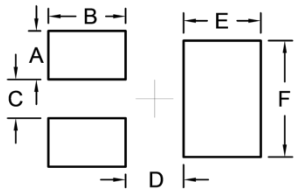
PACKAGE OUTLINE DIMENSIONS

DFN1006-3L



DIM.	Unit (mm)		Unit (inch)	
	Min.	Max.	Min.	Max.
A	0.46	0.51	0.018	0.020
A1	0.00	0.05	0.000	0.002
b	0.10	0.20	0.004	0.008
b1	0.40	0.55	0.016	0.022
D	0.55	0.65	0.022	0.026
E	0.95	1.05	0.037	0.041
e	0.325 (TYP.)		0.013 (TYP.)	
L	0.20	0.30	0.008	0.012
L1	0.20	0.35	0.008	0.014
R	0.06 (TYP.)		0.002 (TYP.)	

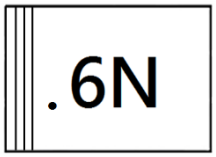
SUGGESTED PAD LAYOUT



Symbol	Unit (mm)	Unit (inch)
A	0.25	0.010
B	0.40	0.016
C	0.20	0.008
D	0.30	0.012
E	0.40	0.016
F	0.60	0.024

Notes:
This recommended land pattern is for reference purposes only. Please consult your manufacturing group to ensure your PCB design guidelines are met.

MARKING DIAGRAM



6N = Marking Code

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