

RTKA2108332H00000BU

User's Manual: Evaluation Board

Industrial Analog and Power

1. Overview

The [RAA210833](#) is a pin-strap configurable 33A step-down PMBus-compliant DC/DC power supply module that integrates a digital PWM controller, synchronous MOSFETs, a power inductor, and passive components. Only input and output capacitors are needed to finish the design. Because of its thermally-enhanced HDA packaging technology, the module can deliver up to 33A of continuous output current without the need for airflow or additional heat sinking. The RAA210833 simplifies configuration and control of Renesas [digital power technology](#) while offering an upgrade path to full PMBus configuration through the pin-compatible ISL8278M.

The RTKA2108332H00000BU evaluation board is a 4in x 4.5in 4-layer FR4 board with 2oz. copper in all layers. The RAA210833 comes with a preprogrammed configuration for operating in a pin-strap mode. Output voltage, switching frequency, input UVLO, soft-start/stop delay and ramp times, and the device SMBus address can be programmed with external pin-strap resistors.

The ZLUSBEVAL3Z (USB to PMBus adapter) is provided with this evaluation board, which connects the evaluation board to a PC to activate the PMBus communication interface. The PMBus command set is accessed by using PowerNavigator™ evaluation software from a PC running Microsoft Windows.

The RTKA2108332H00000BBU can operate in Pin-Strap mode without needing the ZLUSBEVAL3Z adapter or PMBus communication.

1.1 Key Features

- V_{IN} range of 4.5V to 14V, V_{OUT} adjustable from 0.6V to 5V
- Pin-Strap mode for standard settings: V_{OUT} , switching frequency, input UVLO, soft-start/stop, and external synchronization
- Real-time telemetry for V_{IN} , V_{OUT} , I_{OUT} , temperature, duty cycle and switching frequency, and fault logging
- ChargeMode™ control that is tunable with pin-strap resistors or the PMBus interface
- Mechanical switch for enable and the power-good LED indicator

1.2 Specifications

This board is configured for the following operating conditions by default:

- $V_{IN} = 5V$ to 12V
- $V_{OUT} = 1.2V$
- $I_{MAX} = 33A$
- $f_{SW} = 364kHz$
- ASCR gain = 250, ASCR residual = 90
- On/off delay = 5ms, on/off ramp time = 5ms
- Input UVLO = 4.2V
- PMBus address = 0x28h

1.3 Ordering Information

| Part Number | Description |
|---------------------|---|
| RTKA2108332H00000BU | RAA210833 board (EVB, ZLUSBEVAL3Z adapter, USB cable) |

1.4 Related Literature

For a full list of related documents, visit our website

- [RAA210833](#) product page

1.5 Recommended Equipment

- DC power supply with minimum 15V/25A sourcing capacity
- Electronic load capable of sinking current up to 33A
- Digital Multimeters (DMMs)
- Oscilloscope with higher than 100MHz bandwidth

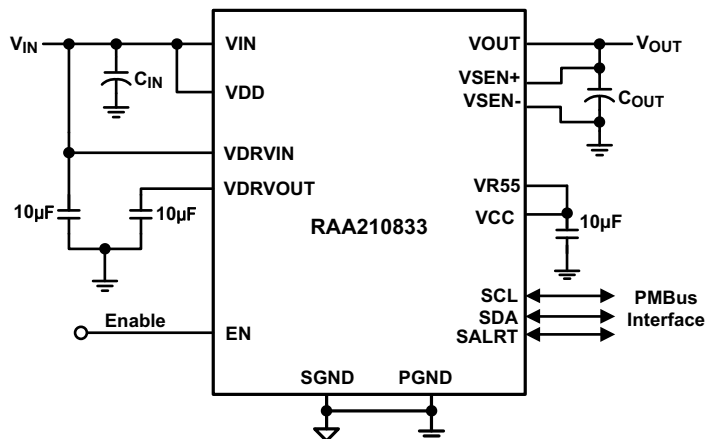


Figure 1. RTKA2108332H00000BU Block Diagram

2. Functional Description

The RTKA2108332H00000BU provides all circuitry required to evaluate the features of the RAA210833. A majority of the features of the RAA210833, such as compensation-free ChargeMode control, soft-start delay, ramp times, external clock synchronization, and Bode plot measurement are available on this evaluation board.

[Figure 4 on page 10](#) shows an image of the RTKA2108332H00000BU evaluation board.

2.1 Operating Range

By default, the RTKA2108332H00000BU is configured to operate at $V_{OUT} = 1.2V$, $f_{SW} = 364kHz$. V_{IN} ranges from 4.5V to 12V. The board can also support a wider operating range to meet the requirements of specific applications. The V_{OUT} can be adjusted from 0.6V to 5V. Load current range is from 0A to 33A. Note that airflow across the board may be needed for continuous operation at 33A at elevated ambient temperature. The f_{SW} and output voltage can also be tuned. However, to ensure sufficient stability margins, the switching frequency and output capacitors should be selected using the “RAA210833 Design Guide Matrix and Output Voltage Response” table in the [RAA210833](#) datasheet.

If the input voltage is less than 5.3V, tie the VCC test point directly to VIN or to a separate 5V power supply for normal operation and best efficiency.

The RTKA2108332H00000BU can handle a 0A to 33A output current transient in which the slew rate is less than 2A/ μ s, such as an electronic load. If the slew rate exceeds the 2A/ μ s, it may be necessary to increase the output capacitance or change the VOUT_OV_FAULT_LIMIT and VOUT_UV_FAULT_LIMIT values for proper operation (refer to [“PMBus Option” on page 5](#)).

If external synchronization is used, connect the SYNC test point to the external clock. Note that the external clock signal should be active before the module is enabled.

2.2 PMBus Operation

The RTKA2108332H00000BU can be evaluated for all features using the provided ZLUSBEVAL3Z dongle and PowerNavigator. Complete the following steps to evaluate the RAA210833 with the PMBus option.

Install the [PowerNavigator](#) evaluation software from the Renesas website.

For board operation, connect the included ZLUSBEVAL3Z dongle to the 6-pin male connector labeled “PMBus DONGLE IN”. Connect the desired load and an appropriate power supply to the input and connect the included USB cable to the PC running PowerNavigator. Set the ENABLE switch to “DISABLE” before turning on the power.

PowerNavigator allows modification of all RAA210833 PMBus parameters for debugging purposes. The RAA210833 device on the board has been preconfigured as described in this document, but the user can modify the operating parameters through PowerNavigator.

The ENABLE switch can then be moved to “ENABLE” and the RTKA2108332H00000BU board can be tested. Alternately, the PMBus ON_OFF_CONFIG and OPERATION commands can be used from PowerNavigator.

2.3 Quick Start Guide

2.3.1 Pin-Strap Option

The RTKA2108332H00000BU can be configured in Pin-Strap mode with standard 1% 0603 resistors. The PMBus interface is not required to evaluate the RAA210833 in Pin-Strap mode. Output voltage (V_{OUT}), switching frequency (f_{SW}), input undervoltage protection (UVLO) threshold, start/stop time delay, ramp time, ASCR settings, and the device PMBus address can be changed by populating the recommended resistors at placeholders provided in the evaluation board. By default, the evaluation board is programmed to regulate at $V_{OUT} = 1.2V$, $f_{SW} = 364kHz$, $UVLO = 4.2V$, $ASCR\ Gain = 250$, $ACSR\ Residual = 90$, $Ton_delay = Ton_rise = Toff_delay = Toff_fall = 5ms$, and PMBus address = 28h.

Complete the following steps to evaluate the RAA210833 in Pin-Strap mode:

- (1) Set the ENABLE switch to “DISABLE”.
- (2) Connect a load to the VOUT lug connectors (J₈ and J₉).
- (3) Connect a power supply to the VIN connectors (J₁ and J₂). Make sure the power supply is not enabled when making the connection.
- (4) Adjust V_{IN} to 12V and turn the power supply on.
- (5) Set the ENABLE switch to “ENABLE”.
- (6) Measure 1.2V V_{OUT} at probe points TP₉ and TP₁₃.
- (7) Observe the switching frequency of 364kHz at the probe point labeled VSWH (TP₈).
- (8) To change V_{OUT}, disconnect the board from the setup and populate with a 1% standard 0603 resistor at the R₆ placeholder location on the bottom layer. Refer to the “Output Voltage Resistor Settings” table in the [RAA210833](#) datasheet for recommended values. By default, VOUT_MAX is set to 110% of V_{OUT} set by the pin-strap resistor.
- (9) To change the switching frequency, disconnect the board from the setup and populate with a 1% standard 0603 resistor at the R₂ placeholder location on the bottom layer. Refer to the “Switching Frequency Resistor Settings” table in the [RAA210833](#) datasheet for recommended values.
- (10) To change the Soft-Start/Stop Ramp time or UVLO, disconnect the board from the setup and populate with a 1% standard 0603 resistor at the R₇ placeholder location on the bottom layer. Refer to the “Soft-Start/Stop and Input UVLO Resistor Settings” table or the “UVLO Resistor Settings” table in the [RAA210833](#) datasheet for the recommended values.
- (11) To change the ASCR, disconnect the board from the setup and populate with a 1% standard 0603 resistor at the R₈ placeholder location on the bottom layer. Refer to the “ASCR Resistor Settings” table in the [RAA210833](#) datasheet for the recommended values.

2.3.2 PMBus Option

The RTKA2108332H00000BU can be evaluated for all features using the provided ZLUSBEVAL3Z dongle and PowerNavigator. Complete the following steps to evaluate the RAA210833 with the PMBus option.

- (1) Install PowerNavigator.
- (2) Set the ENABLE switch to “DISABLE”.
- (3) Connect a load to the VOUT lug connectors (J₈ and J₉).
- (4) Connect a power supply to the VIN connectors (J₁ and J₂). Make sure the power supply is not enabled when making the connection.
- (5) Adjust the V_{IN} to 12V and turn the power supply on.
- (6) Connect the ZLUSBEVAL3Z dongle (USB to PMBus adapter) to the RTKA2108332H00000BU board to the 6-pin male connector labeled “PMBus DONGLE IN”.
- (7) Connect the supplied USB cable from the computer through USB to the ZLUSBEVAL3Z dongle.
- (8) Launch PowerNavigator.
- (9) The RAA210833 device on the board operates in Pin-Strap mode from factory default, but the user can modify the operating parameters through PowerNavigator to monitor faults and debug a test case and read real-time values of input/output parameters, switching frequency, duty cycle, and temperature.
- (10) Set the ENABLE switch to “ENABLE”. Alternatively, the PMBus ON_OFF_CONFIG and OPERATION commands can be used from PowerNavigator to allow PMBus Enable.
- (11) Monitor and configure the RTKA2108332H00000BU board using the PMBus commands in PowerNavigator. PowerNavigator tutorial videos are available at the Renesas [PowerNavigator](#) website.

3. Evaluation Board Information

3.1 External Clock Synchronization

The RAA210833 can synchronize to an external clock. External clock synchronization allows the user to operate multiple converters at the same switching frequency and can lead to improved EMI characteristics. The RTKA2108332H00000BU evaluation board can assess this functionality. A function generator is required. Complete the following steps to operate the RAA210833 with an external clock frequency of 593kHz:

- (1) Set the Enable switch to the “DISABLE” position.
- (2) Solder a 17.8k Ω resistor at RSET on the CFG pin (R₁₆).
- (3) Program the function generator to output a continuous square pulse waveform of 593kHz. Program the pulse width to be at least 150ns.
- (4) Ensure that the clock signal is stable by monitoring the waveform on an oscilloscope.
- (5) After verifying clock stability, connect the output cables from the function generator to test point J₄ (labeled “SYNC”).
- (6) Turn the function generator output to “ON”.
- (7) Enable the module by setting the Enable switch to “ENABLE”.
- (8) Observe the switching frequency at test point TP₈ (labeled “VSWH”).
- (9) The module synchronizes to the 593kHz external clock from the function generator.
- (10) Always ensure that the module is disabled before changing the frequency of the external clock.
- (11) A Loss of Sync fault is generated when the external clock is lost.

3.2 Bode Plot Measurement

Assessing the stability of the converter is an important step in the design process. Bode plots are a useful and reliable tool to identify the converter’s loop response. Phase margin and gain margin give an insight into the stability of the system, and the bandwidth can indicate how quickly the converter responds to disturbances in input voltage or load transients. Correctly measuring the loop response is critical for designing stable converter systems.

A network analyzer is required to perform the frequency response measurements on the RTKA2108332H00000BU evaluation board. Complete the following steps to evaluate the RAA210833 converter loop response on the RTKA2108332H00000BU evaluation board.

- (1) Break the feedback loop by removing the R₉ resistor in the remote sense path, connected between VSEN+ and VOUT.
- (2) Solder a 20 Ω resistor in its place. The value of the resistor should be in the range of 10 Ω to 50 Ω .
- (3) Solder a twisted wire pair to the 20 Ω resistor. Ensure that the wires are short in length. A small twisted pair works well by minimizing noise pickup, which is important for a good measurement.
- (4) Enable the module.
- (5) Use a network analyzer to inject a small AC signal (~20mV) across the 20 Ω resistor as shown in [Figure 2 on page 7](#).
- (6) Measure the amplitudes of the signals at points A and B as shown in [Figure 2](#).
- (7) Sweep the frequency using the network analyzer to observe the bandwidth, phase, and gain margin.

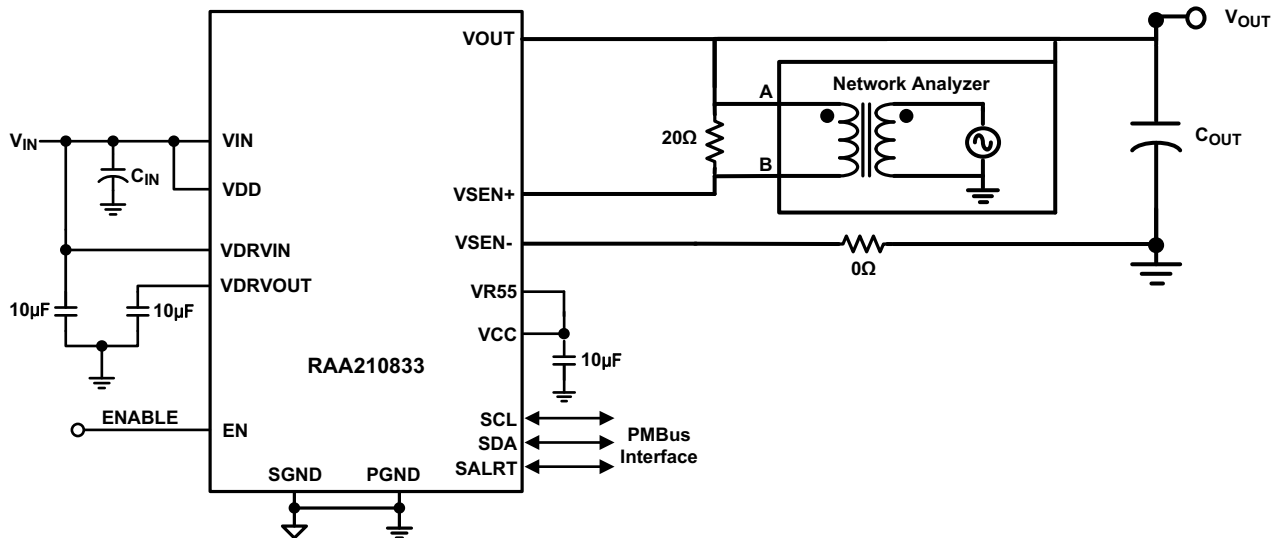


Figure 2. Network Analyzer Connection

Figure 3 shows an example plot generated by the network analyzer for the RAA210833 at 12V input and 1.2V/33A output at 364 kHz. 10x100uF ceramic capacitors + 4x470uF POSCAPs are used at the output, with ASCR gain = 250 and Residual = 90. The plot shows a crossover frequency of 41.69 kHz with a phase margin of 70.2°. A 12.7dB gain margin is observed at 182 kHz.

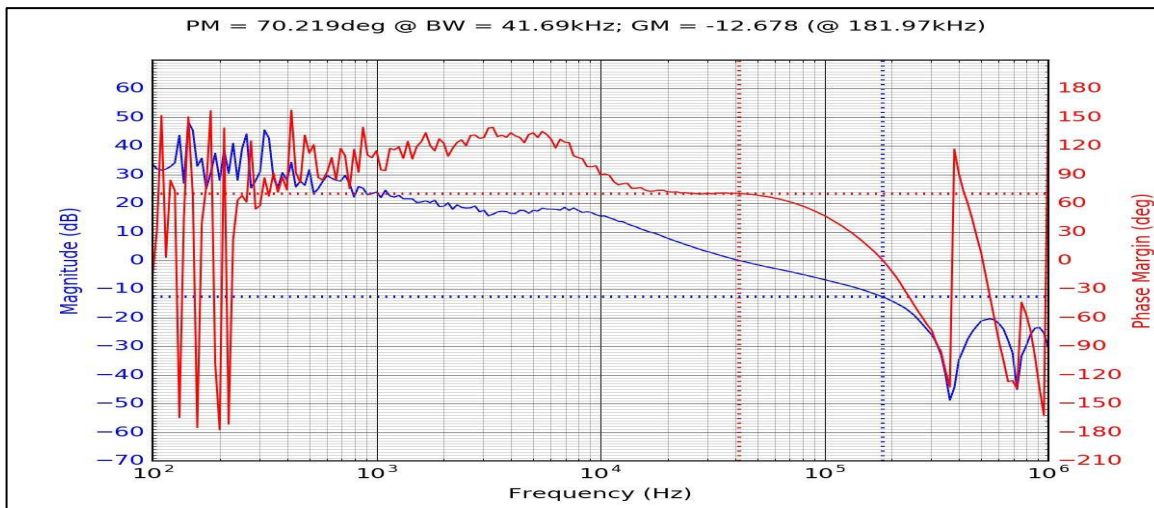


Figure 3. Example of Bode Plot Generated Using Network Analyzer

Refer to the “RAA210833 Design Guide Matrix and Output Voltage Response” table in the [RAA210833](#) datasheet for detailed design guidelines, including selection of input/output capacitors and different ASCR gain and residual values.

3.3 Interleave Operation

When multiple point-of-load converters share a common DC input supply, Renesas recommends adjusting the clock phase offset of each device so that not all devices start to switch simultaneously. Setting each converter to start its switching cycle at a different point in time can dramatically reduce input capacitance requirements and efficiency losses. Because the peak current drawn from the input supply is effectively spread out over a period of

time, the peak current drawn at any given moment is reduced, and the power losses proportional to the I_{RMS}^2 are reduced dramatically.

To enable phase spreading in a multi-module operation, all converters must be synchronized to the same switching clock. The phase offset of each device can be set to any value between 0° and 360° in 22.5° increments by choosing the device PMBus address from the “Interleave Settings from SA” table in the [RAA210833](#) datasheet. The lower four bits of the PMBUS address set the value of the INTERLEAVE command. To implement Interleave functionality for a two module operation, complete the following steps:

- (1) Choose SA (SMBus Address) for Module 1 and Module 2 from the “Interleave Settings from SA” table in the [RAA210833](#) datasheet based on the desired phase difference. Populate the corresponding RSET for SA (R_5) according to the [RAA210833](#) datasheet.
For example, when Module 1 has SA = 28h (INTERLEAVE = 8, 180° phase shift from the rising edge of the external clock) and Module 2 has SA=24h (INTERLEAVE = 4, 90° phase shift from the rising edge of the external clock), the net phase difference between Module 1 and Module 2 is 90° ($180^\circ - 90^\circ$).
- (2) Populate RSET on CFG for both boards to synchronize to an external clock source of a particular switching frequency based on the “External Frequency SYNC Settings” table in the [RAA210833](#) datasheet.
- (3) Connect the power supply to the VIN connectors (VIN/GND) on both boards.
- (4) Connect the ZLUSBEVAL3Z dongle to the 6-pin male connector labeled “PMBus DONGLE In” to one of the boards.
- (5) Daisy chain the second board to the first board by connecting “PMBus DONGLE Out” of the first board to the “PMBus DONGLE In” of the second board.
- (6) Provide an external clock on the SYNC pins of the two boards from a function generator. The external clock frequency from the function generator should be within $\pm 10\%$ of the listed options shown in the “External Frequency SYNC Settings” table in the [RAA210833](#) datasheet. The incoming clock signal must be stable before the enable pin is asserted. The external clock signal must not vary more than 10% from its initial value and should have a minimum pulse width of 150ns.
- (7) Turn the input power supply on. Next, set the ENABLE switch to the “ENABLE” position.
- (8) Monitor the VSWH node at the probe point labeled VSWH (TP8) on the two boards using an oscilloscope to verify the phase spread set. This functionality can also be verified using the INTERLEAVE command in PowerNavigator.

Note that every module gets assigned a unique Rail ID based on the SA setting. This can be observed in the Power Map window of PowerNavigator.

4. PCB Layout Guidelines

To achieve stable operation, low losses, and good thermal performance, some layout considerations are necessary.

The key features of the RTKA2108332H00000BU layout are:

- Establish separate SGND and PGND planes, then connect the SGND plane to the PGND plane in the middle layer. To make connections between SGND/PGND on the top layer and other layers, use multiple vias for each pin to connect to the inner SGND/PGND layers. Do not connect SGND directly to PGND on a top layer. Connecting SGND directly to PGND without establishing the SGND plane bypasses the decoupling capacitor at the internal reference supplies, making the controller susceptible to noise.
- Place enough ceramic capacitors between VIN and PGND and VOUT and PGND. Bypass capacitors between VDD and the ground plane, as close to the module as possible to minimize high-frequency noise.
- Use large copper areas for a power path (VIN, PGND, and VOUT) to minimize conduction loss and thermal stress. Use multiple vias to connect the power planes in different layers. Extra ceramic capacitors at VIN and VOUT can be placed on the bottom layer under the VIN and VOUT pads when using multiple vias to connect copper pads on the top and bottom layers.
- Connect differential remote sensing traces to the regulation point to achieve a tight output voltage regulation. Route a trace from VSEN+ and VSEN- to the point-of-load where tight output voltage is desired. Avoid routing any sensitive signal traces, such as the VSENSE signal, near the VSWH pads.
- For noise sensitive applications, Renesas recommends connecting the VSWH pads only on the top layer; however, thermal performance is sacrificed. External airflow might be required to keep module heat at desired levels. For applications in which switching noise is less critical, excellent thermal performance can be achieved in this power module by increasing the copper mass attached to the VSWH pad. To increase copper mass on the VSWH node, create copper islands in the middle and bottom layers under the VSWH pad and connect them to the top layer with multiple vias. Shield those copper islands with a PGND layer to avoid any interference to noise sensitive signals.

4.1 Thermal Considerations and Current Derating

Board layout is critical for safe module operation and maximum allowable power delivery. To work in high temperature environments and carry large currents, the board layout needs to be carefully designed to maximize thermal performance. To achieve this, select enough trace width, copper weight, and the proper connectors.

The RTKA2108332H00000BU evaluation board is designed for running 33A at room temperature without additional cooling systems. However, if the output voltage is increased or the board is operated at elevated temperatures, then the available current is derated. Refer to the derated current curves in the [RAA210833](#) datasheet to determine the maximum output current the evaluation board can supply. θ_{JA} is measured by inserting a thermocouple inside the module to measure peak junction temperature.

4.2 Board Pictures

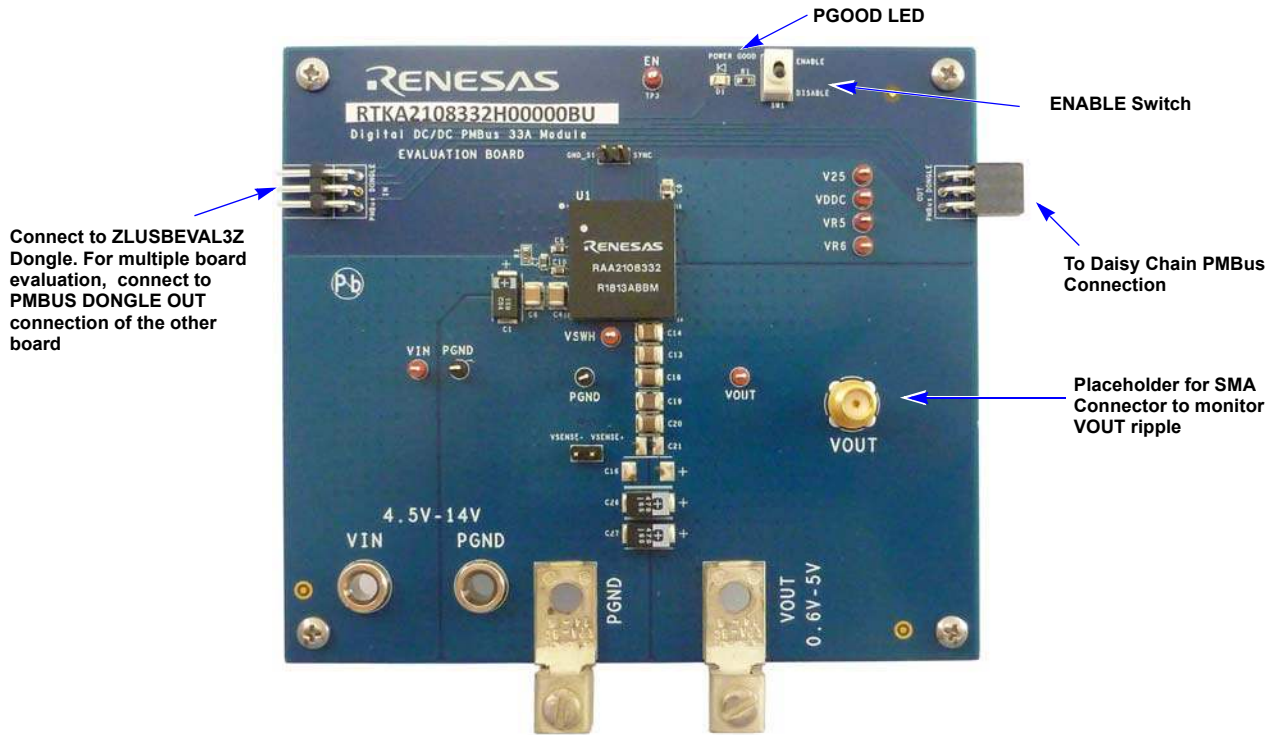


Figure 4. RTKA2108332H00000BU Evaluation Board (Top Side)

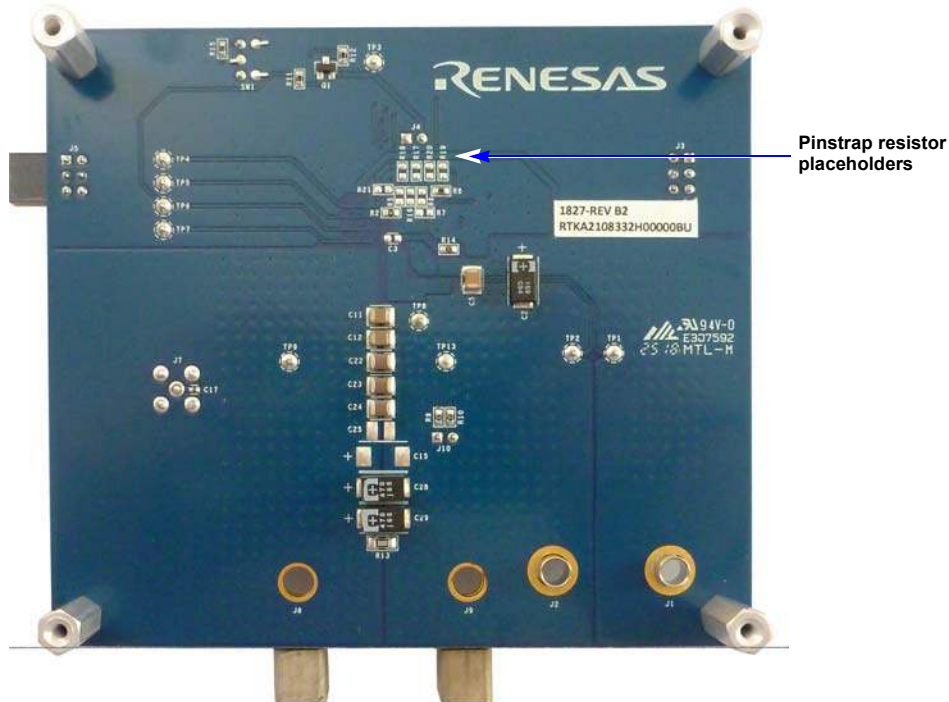


Figure 5. RTKA2108332H00000BU Evaluation Board (Bottom Side)

4.4 Bill of Materials

| Qty | Reference Designator | Description | Manufacturer | Manufacturer Part |
|-----|--|--|------------------------|--------------------------|
| 1 | | PCB, RTKA2108332H00000BU, ROHS | Renesas | PCB, RTKA2108332H00000BU |
| 2 | C1, C2 | CAP-POSCAP, SMD, 7.3x4.3, 150µF, 16V, 20%, 50mΩ, ROHS | Sanyo/ Panasonic | 16TQC150MYF |
| 4 | C26, C27, C28, C29 | CAP TANT POLY 470µF, 6.3V, 20%, 18mΩ 2917, ROHS | Sanyo | 6TPE470MI |
| 2 | C15, C16 | DO NOT POPULATE_PLACE HOLDER | | |
| 10 | C11, C12, C13, C14, C18, C19, C20, C22, C23, C24 | CAP CER 100µF, 6.3V, 20%, X5R, 1210, ROHS | TDK | C3225X5R0J107M |
| 2 | C7, C8 | CAP CER 10µF, 16V, 20%, X5R, 0603, ROHS | Murata | GRM188R61C106MA73D |
| 1 | C10 | CAP CER 4.7µF, 16V, 10%, X5R, 0603, ROHS | Murata | GRM188R61C475KAAJD |
| 3 | C4, C5, C6 | CAP CER 22µF, 25V, 10%, X7R, 1210, ROHS | Murata | GRM32ER71E226KE15L |
| 1 | C17 | CAP CER 1µF, 6.3V, 10%, X5R, 0402, ROHS | Panasonic | ECJ-0EB0J105K |
| 1 | C3 | DO NOT POPULATE_PLACE HOLDER | | |
| 1 | C9 | CAP CER 10µF, 25V, 10%, X5R, 0805, ROHS | TDK | C2012X5R1E106K |
| 2 | C21, C25 | DO NOT POPULATE_PLACE HOLDER | | |
| 9 | R5, R6, R7, R16, R17, R18, R19, R20, R21 | DO NOT POPULATE_PLACE HOLDER | | |
| 4 | R3, R9, R10, R14 | RES SMD 0Ω JUMPER, 1/10W, 0603, ROHS | Panasonic | ERJ-3GEY0R00V |
| 1 | R12 | RES SMD 1kΩ, 1%, 1/10W, 0603, ROHS | Panasonic | ERJ-3EKF1001V |
| 2 | R1, R11 | RES SMD 10kΩ, 1%, 1/10W, 0603, ROHS | Panasonic | ERJ-3EKF1002V |
| 1 | R2 | RES SMD 19.6kΩ, 1%, 1/10W, 0603, ROHS | Panasonic | ERJ-3EKF1962V |
| 1 | R15 | RES SMD 4.99kΩ, 1%, 1/10W, 0603, ROHS | Panasonic | ERJ-3EKF4991V |
| 1 | R8 | RES SMD 51.1kΩ, 1%, 1/10W, 0603, ROHS | Panasonic | ERJ-3EKF5112V |
| 1 | R13 | RES SMD 200Ω, 1%, 1/4W, 1206, ROHS | Panasonic | ERJ-8ENF2000V |
| 1 | U1 | 33A Digital DC/DC PMBus Power Supply Module, ROHS | Renesas | RAA2108332GLG |
| 1 | D1 | LED, SMD, 0805, GREEN, CLEAR, 10mcd, 2.1V, 20mA, 570nm, ROHS | Chicago Miniature Lamp | CMD17-21VGC-TR8 |
| 1 | Q1 | MOSFET N-CH 60V 115MA SOT-23, ROHS | Fairchild | 2N7002 |

| Qty | Reference Designator | Description | Manufacturer | Manufacturer Part |
|-----|--|--|--------------------|-------------------|
| 1 | SW1 | SWITCH-TOGGLE, THRU-HOLE, SPDT, 5P, ROHS | C&K | GT11MCBE |
| 8 | TP1, TP3, TP4, TP5, TP6, TP7, TP8, TP9 | CONN-MINI TEST PT, VERTICAL, RED, ROHS | Keystone | 5000 |
| 2 | TP2, TP13 | CONN-MINI TEST PT, VERTICAL, BLK, ROHS | Keystone | 5001 |
| 2 | J1, J2 | CONN-JACK, MINI BANANA, 0.175 PLUG, NICKEL/BRASS, ROHS | Keystone | 575-4 |
| 2 | J8, J9 | HDWARE, MTG, CABLE TERMINAL, 6-14AWG, LUG&SCREW, ROHS | Burndy | KPA8CTP |
| 1 | J5 | CONN-SOCKET STRIP, TH, 2x3, 2.54mm, TIN, R/A, ROHS | Samtec | SSQ-103-02-T-D-RA |
| 2 | J4, J10 | CONN HEADER 2POS .100" SNGL, ROHS | Samtec | TSW-102-07-F-S |
| 1 | J3 | CONN-HEADER, 2x3, BRKAWY, 2.54mm, TIN, R/A, ROHS | Samtec | TSW-103-08-T-D-RA |
| 1 | J7 | SMA Straight Jack Receptacle, ROHS | Johnson Components | 142-0711-231 |

4.5 RTKA2108332H00000BU Board Layout

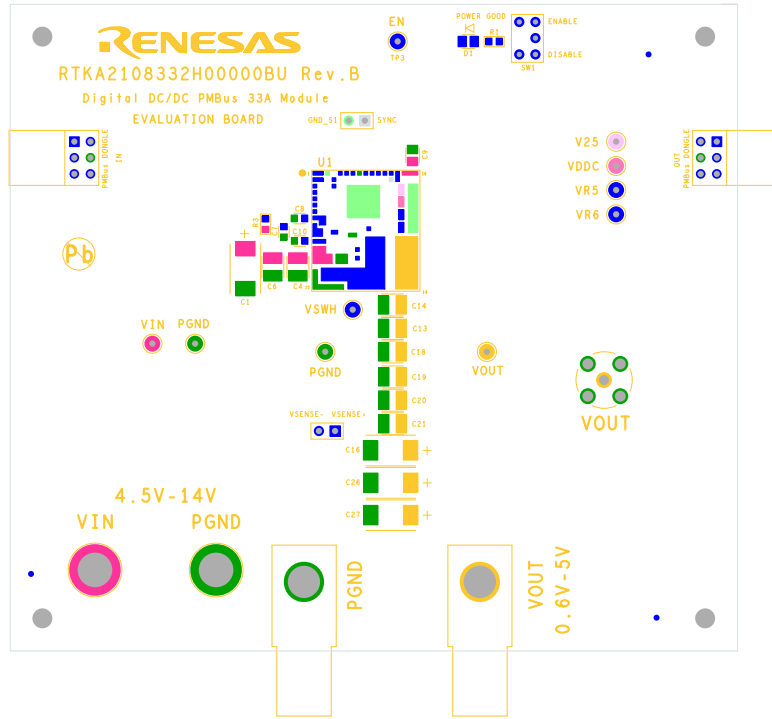


Figure 7. Silkscreen Top

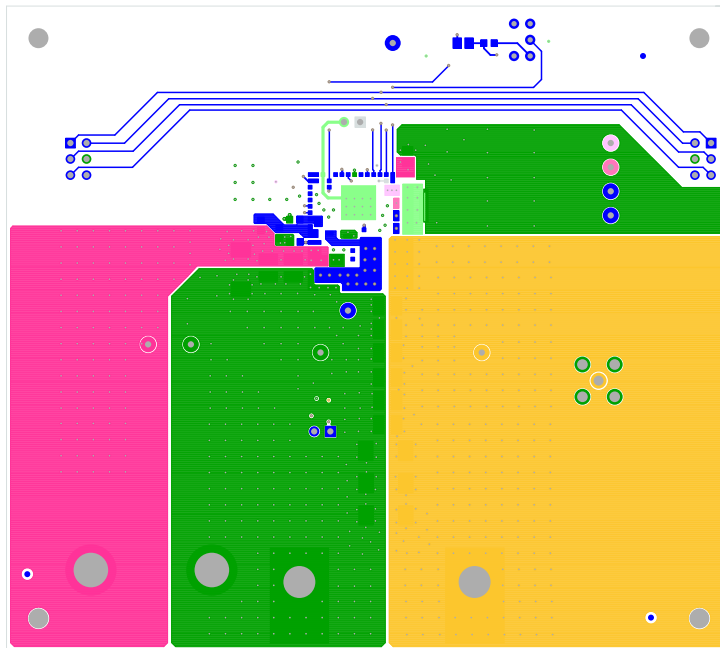


Figure 8. PCB - Top Layer Component Side

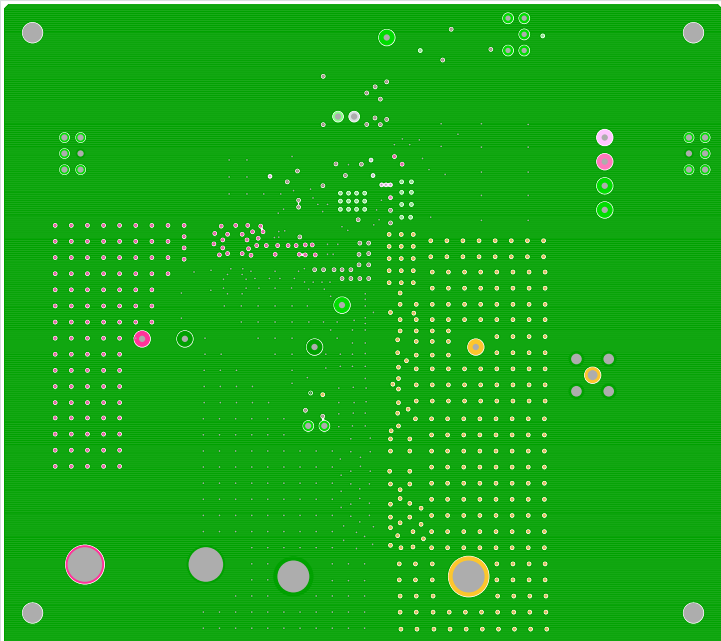


Figure 9. PCB - Layer 2

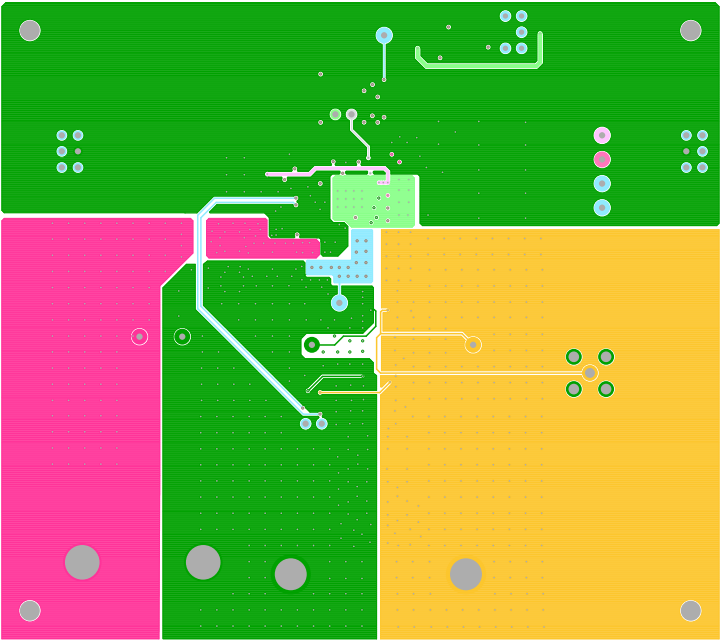


Figure 10. PCB - Layer 3

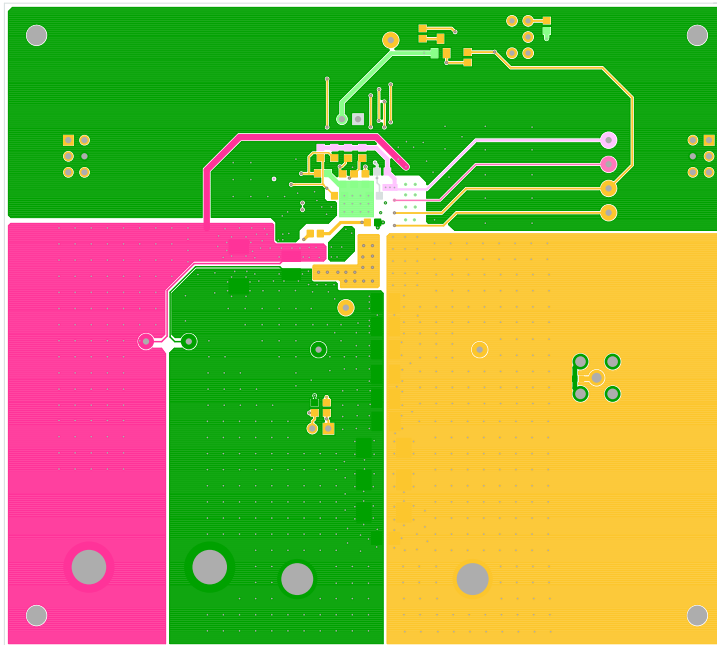


Figure 11. PCB - Layer 4 (Bottom Layer Solder Side)

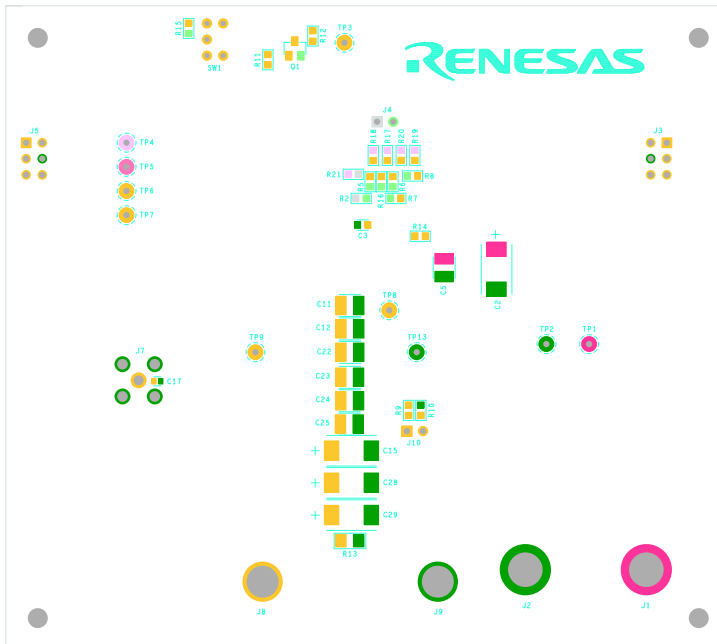


Figure 12. Silkscreen Bottom

5. Typical Performance Curves

The following data was acquired using an RTKA2108332H00000BU evaluation board.

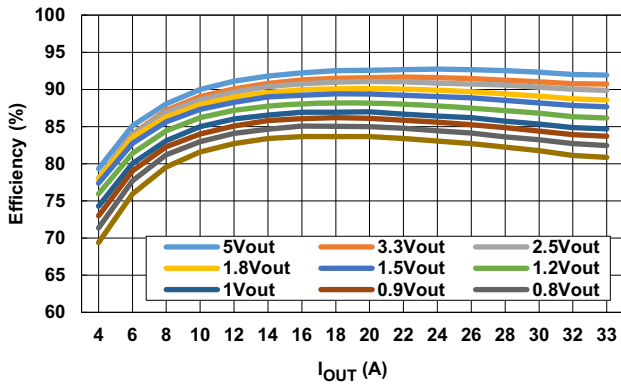


Figure 13. Efficiency vs Output Current at $V_{IN} = 12V$ and $f_{SW} = 364kHz$ for Various Output Voltages

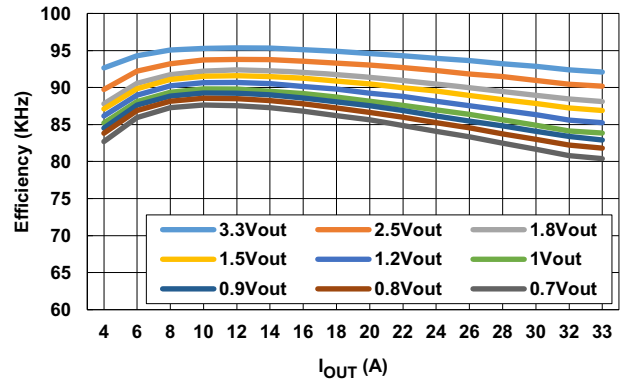


Figure 14. Efficiency vs Output Current at $V_{IN} = 5V$ and $f_{SW} = 364kHz$ for Various Output Voltages

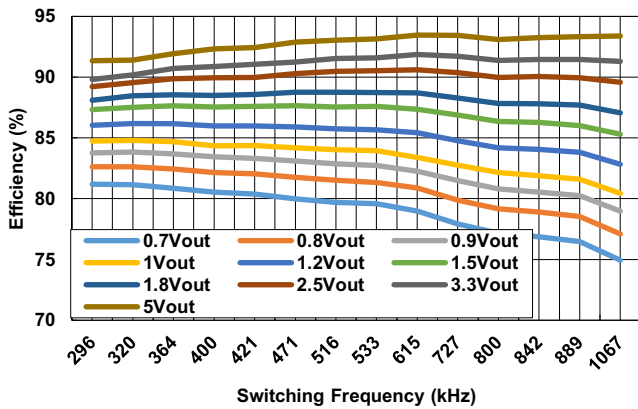


Figure 15. Efficiency vs Switching Frequency at $V_{IN} = 12V$ and $I_{OUT} = 33A$ for Various Output Voltages

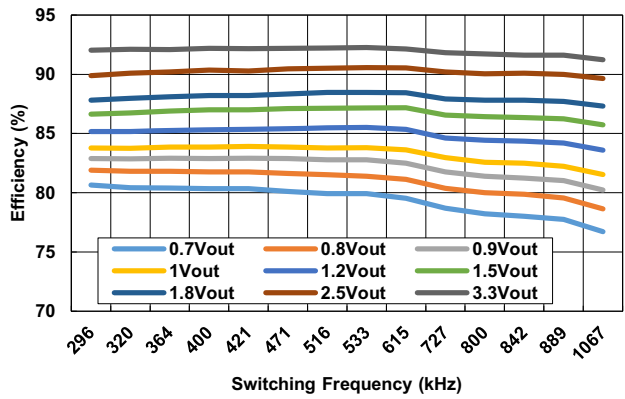


Figure 16. Efficiency vs Switching Frequency at $V_{IN} = 5V$ and $I_{OUT} = 33A$ for Various Output Voltages

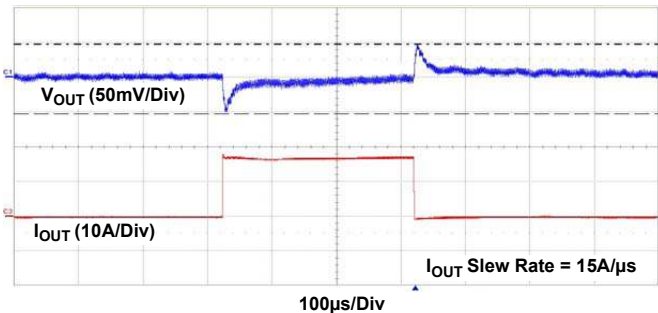


Figure 17. $5V_{IN}$ to $1.2V_{OUT}$, $f_{SW} = 364kHz$, $C_{OUT} = 10x100\mu F$ Ceramic + $4x470\mu F$ POSCAP, ASCR Residual = 90, ASCR Gain = 250

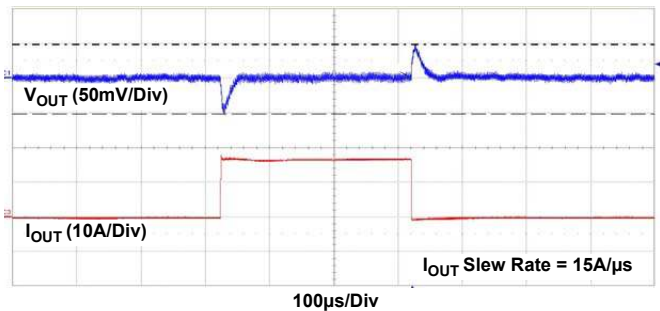


Figure 18. $12V_{IN}$ to $1.2V_{OUT}$, $f_{SW} = 364kHz$, $C_{OUT} = 10x100\mu F$ Ceramic + $4x470\mu F$ POSCAP, ASCR Residual = 90, ASCR Gain = 250

The following data was acquired using an RTKA2108332H00000BU evaluation board. (Continued)

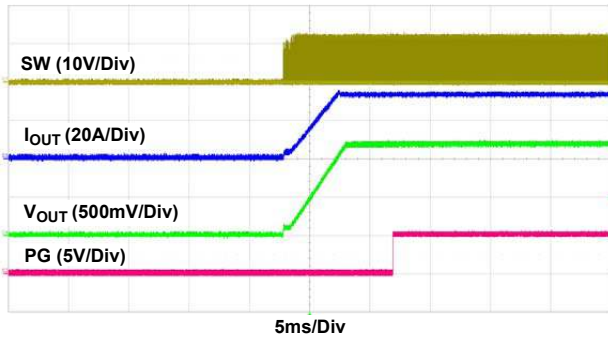


Figure 19. Startup at 12V_{IN}, 1.2V_{OUT}, 33A

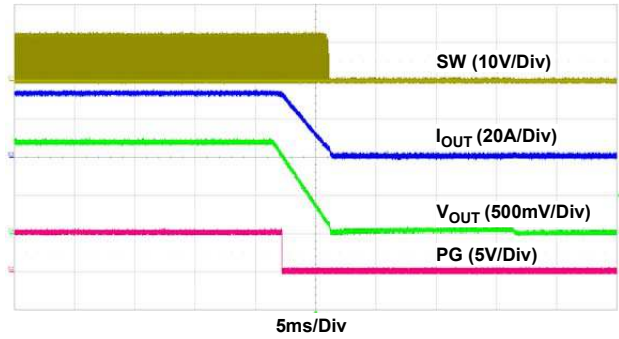


Figure 20. Soft-Off at 12V_{IN}, 1.2V_{OUT}, 33A

6. Revision History

| Rev. | Date | Description |
|------|--------------|-----------------|
| 0.00 | Sep 12, 2018 | Initial release |

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(Rev.4.0-1 November 2017)



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