March 2008

74LCXR2245

Low Voltage Bidirectional Transceiver with 5V Tolerant Inputs and Outputs and 26Ω Series Resistors on Both A and B Ports

Features

- 5V tolerant inputs and outputs
- 2.3V–3.6V V_{CC} specifications provided
- 8.0ns t_{PD} max. (V_{CC} = 3.3V), 10µA I_{CC} max.
- Power down high impedance inputs and outputs
- Supports live insertion/withdrawal(1)
- ±12mA output drive (V_{CC} = 3.0V)
- Implements proprietary noise/EMI reduction circuitry
- Latch-up performance exceeds 500mA
- Equivalent 26Ω series resistor on all outputs
- ESD performance:
  - Human body model > 2000V
  - Machine model > 200V

Note:

1. To ensure the high-impedance state during power up or down, $\overline{OE}$ should be tied to V_{CC} through a pull-up resistor: the minimum value or the resistor is determined by the current-sourcing capability of the driver.

General Description

The LCXR2245 contains eight non-inverting bidirectional buffers with 3-STATE outputs and is intended for bus oriented applications. The device is designed for low voltage (2.5V and 3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment. The T/$\overline{R}$ input determines the direction of data flow through the device. The $\overline{OE}$ input disables both the A and B ports by placing them in a high impedance state. The 26Ω series resistor helps reduce output overshoot and undershoot.

The LCXR2245 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

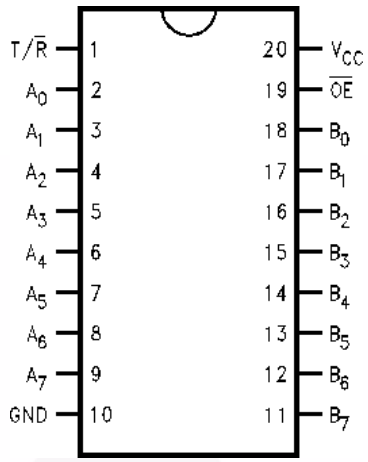
Ordering Information

Order Number	Package Number	Package Description
74LCXR2245WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74LCXR2245SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74LCXR2245MSA	MSA20	20-Lead Shrink Small Outline Package (SSOP), JEDEC MO-150, 5.3mm Wide
74LCXR2245MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

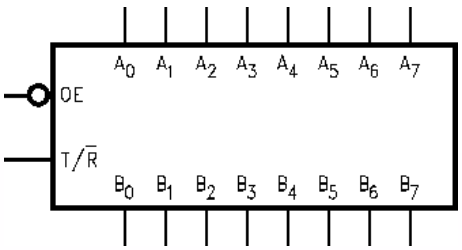
Device also available in Tape and Reel. Specify by appending suffix letter “X” to the ordering number.

All packages are lead free per JEDEC: J-STD-020B standard.

Connection Diagram



Logic Symbol



Pin Description

Pin Names	Description
$\overline{OE}$	Output Enable Input
T/$\overline{R}$	Transmit/Receive Input
A_0–A_7	Side A Inputs or 3-STATE Outputs
B_0–B_7	Side B Inputs or 3-STATE Outputs

Truth Table

Inputs		Outputs
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B_0 – B_7 Data to Bus A_0 – A_7
L	H	Bus A_0 – A_7 Data to Bus B_0 – B_7
H	X	HIGH Z State on A_0 – A_7, B_0 – B_7(2)

H = HIGH Voltage Level

L = LOW Voltage Level

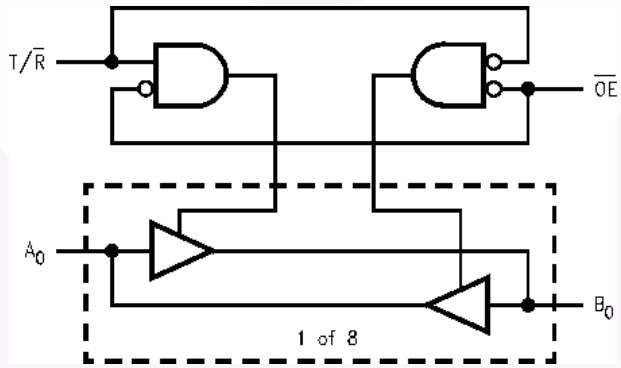
X = Immaterial

Z = High Impedance

Note:

2. Unused bus terminals during HIGH Z State must be held HIGH or LOW.

Logic Diagram



Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	–0.5V to +7.0V
V_I	DC Input Voltage	–0.5V to +7.0V
V_O	DC Output Voltage	
	Output in 3-STATE	–0.5V to +7.0V
	Output in HIGH or LOW State(3)	–0.5V to V_{CC} + 0.5V
I_{IK}	DC Input Diode Current, V_I < GND	–50mA
I_{OK}	DC Output Diode Current	
	V_O < GND	–50mA
	V_O > V_{CC}	+50mA
I_O	DC Output Source/Sink Current	±50mA
I_{CC}	DC Supply Current per Supply Pin	±100mA
I_{GND}	DC Ground Current per Ground Pin	±100mA
T_{STG}	Storage Temperature	–65°C to +150°C

Note:

3. I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions(4)

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Max.	Units
V_{CC}	Supply Voltage			
	Operating	2.0	3.6	V
	Data Retention	1.5	3.6	
V_I	Input Voltage	0	5.5	V
V_O	Output Voltage			
	HIGH or LOW State	0	V_{CC}	V
	3-STATE	0	5.5	
I_{OH} / I_{OL}	Output Current			
	V_{CC} = 3.0V–3.6V		±12	mA
	V_{CC} = 2.7V–3.0V		±8	
	V_{CC} = 2.3V–2.7V		±4	
T_A	Free-Air Operating Temperature	–40	85	°C
$\Delta t / \Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V	0	10	ns/V

Note:

4. Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	Conditions	T_A = –40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage	2.3–2.7		1.7		V
		2.7–3.6		2.0		
V_{IL}	LOW Level Input Voltage	2.3–2.7			0.7	V
		2.7–3.6			0.8	
V_{OH}	HIGH Level Output Voltage	2.3–3.6	I_{OH} = –100µA	V_{CC} – 0.2		V
		2.3	I_{OH} = –4mA	1.8		
		2.7	I_{OH} = –4mA	2.2		
		3.0	I_{OH} = –6mA	2.4		
		2.7	I_{OH} = –8mA	2.0		
		3.0	I_{OH} = –12mA	2.0		
V_{OL}	LOW Level Output Voltage	2.3–3.6	I_{OL} = 100µA		0.2	V
		2.3	I_{OL} = 4mA		0.6	
		2.7	I_{OL} = 4mA		0.4	
		3.0	I_{OL} = 6mA		0.55	
		2.7	I_{OL} = 8mA		0.6	
		3.0	I_{OL} = 12mA		0.8	
I_I	Input Leakage Current	2.3–3.6	$0 \le V_I \le 5.5V$		±5.0	µA
I_{OZ}	3-STATE I/O Leakage	2.3–3.6	$0 \le V_O \le 5.5V$, $V_I = V_{IH}$ or V_{IL}		±5.0	µA
I_{OFF}	Power-Off Leakage Current	0	V_I or V_O = 5.5V		10	µA
I_{CC}	Quiescent Supply Current	2.3–3.6	$V_I = V_{CC}$ or GND		10	µA
		2.3–3.6	$3.6V \le V_I$, $V_O \le 5.5V$(5)		±10	
ΔI_{CC}	Increase in I_{CC} per Input	2.3–3.6	$V_{IH} = V_{CC}$ –0.6V		500	µA

Note:

5. Outputs disabled or 3-STATE only.

AC Electrical Characteristics

Symbol	Parameter	T_A = –40°C to +85°C, R_L = 500Ω						Units
		V_{CC} = 3.3V ± 0.3V, C_L = 50pF		V_{CC} = 2.7V, C_L = 50pF		V_{CC} = 2.5V ± 0.2V, C_L = 30pF		
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{PHL}, t_{PLH}	Propagation Delay, A_n to B_n or B_n to A_n	1.5	8.0	1.5	9.0	1.5	9.6	ns
t_{PZL}, t_{PZH}	Output Enable Time	1.5	9.5	1.5	10.5	1.5	11.0	ns
t_{PLZ}, t_{PHZ}	Output Disable Time	1.5	7.5	1.5	8.5	1.5	9.0	ns
t_{OSHL}, t_{OSLH}	Output to Output Skew(6)		1.0					ns

Note:

6. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}).

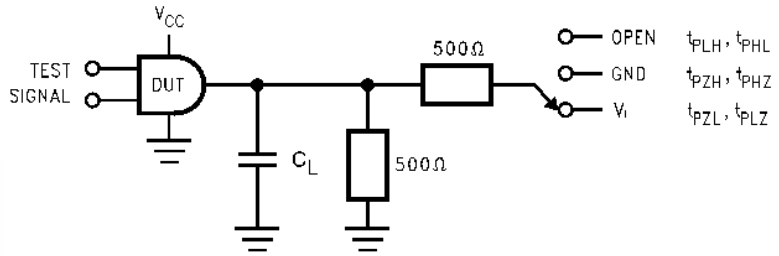
Dynamic Switching Characteristics

Symbol	Parameter	V_{CC} (V)	Conditions	T_A = 25°C Typical	Unit
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	3.3	C_L = 50pF, V_{IH} = 3.3V, V_{IL} = 0V	0.5	V
		2.5	C_L = 30pF, V_{IH} = 2.5V, V_{IL} = 0V	0.4	
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	3.3	C_L = 50pF, V_{IH} = 3.3V, V_{IL} = 0V	0.5	V
		2.5	C_L = 30pF, V_{IH} = 2.5V, V_{IL} = 0V	0.4	

Capacitance

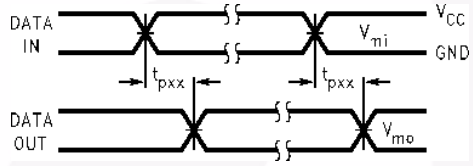
Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, V_I = 0V or V_{CC}	7	pF
C_{OUT}	Output Capacitance	V_{CC} = 3.3V, V_I = 0V or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	V_{CC} = 3.3V, V_I = 0V or V_{CC}, f = 10MHz	25	pF

AC Loading and Waveforms (Generic for LCX Family)

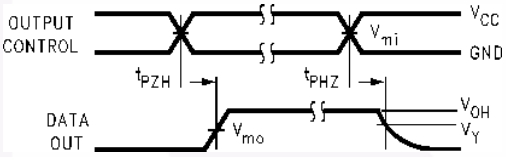


Test	Switch
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6V at V_{CC} = 3.3 ± 0.3V V_{CC} x 2 at V_{CC} = 2.5 ± 0.2V
t_{PZH}, t_{PHZ}	GND

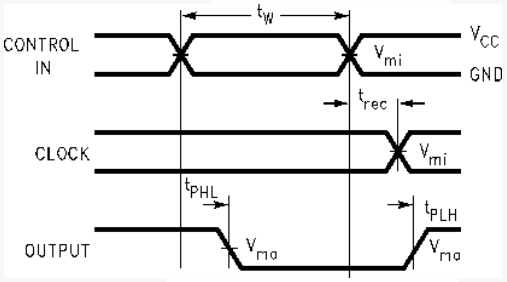
Figure 1. AC Test Circuit (C_L includes probe and jig capacitance)



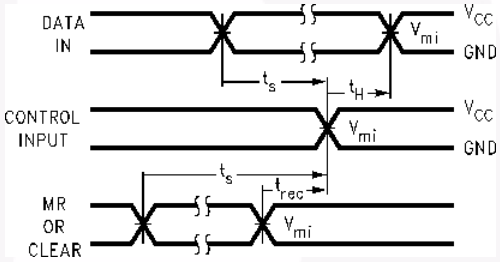
Waveform for Inverting and Non-Inverting Functions



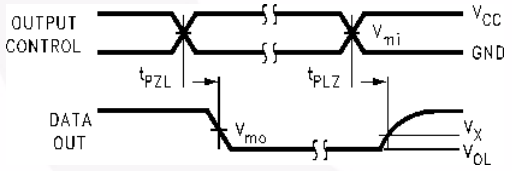
3-STATE Output High Enable and Disable Times for Logic



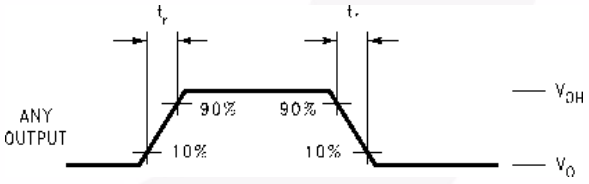
Propagation Delay. Pulse Width and t_{rec} Waveforms



Setup Time, Hold Time and Recovery Time for Logic



3-STATE Output Low Enable and Disable Times for Logic

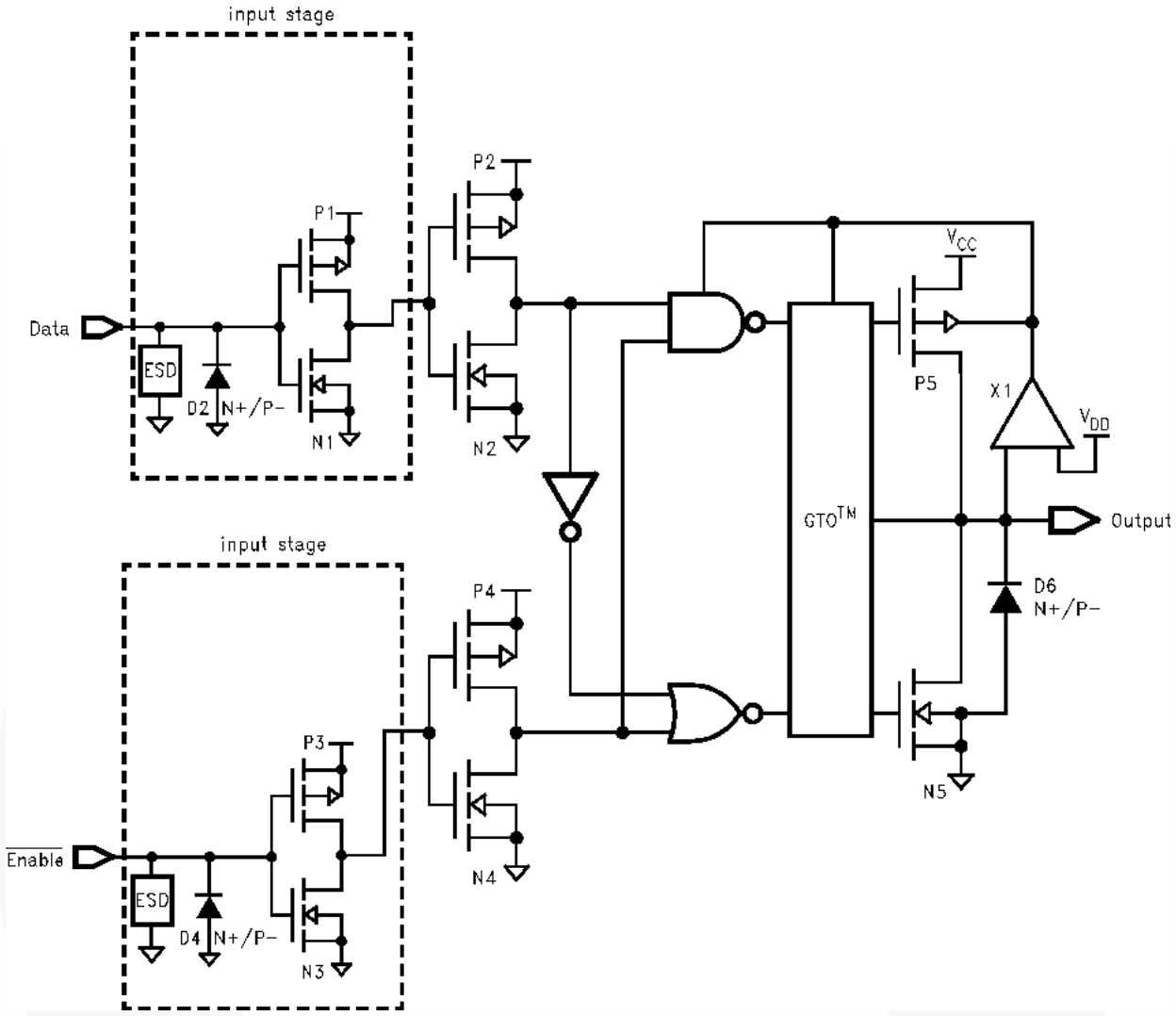


t_{rise} and t_{fall}

Symbol	V_{CC}		
	3.3V ± 0.3V	2.7V	2.5V ± 0.2V
V_{mi}	1.5V	1.5V	V_{CC} / 2
V_{mo}	1.5V	1.5V	V_{CC} / 2
V_x	V_{OL} + 0.3V	V_{OL} + 0.3V	V_{OL} + 0.15V
V_y	V_{OH} – 0.3V	V_{OH} – 0.3V	V_{OH} – 0.15V

Figure 2. Waveforms (Input Characteristics; f = 1MHz, t_r = t_f = 3ns)

Schematic Diagram (Generic for LCX Family)



Physical Dimensions

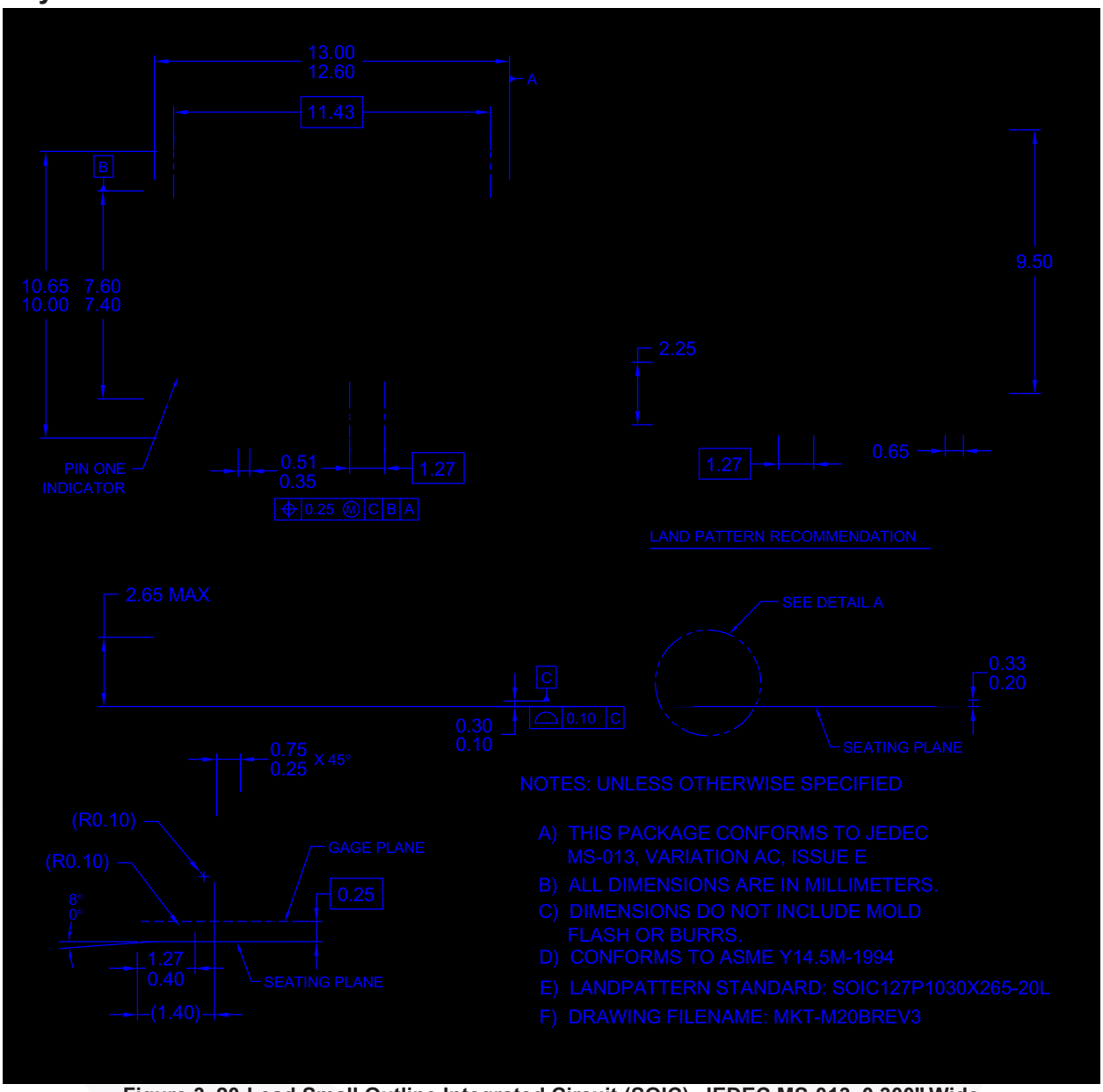


Figure 3. 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide

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Physical Dimensions (Continued)

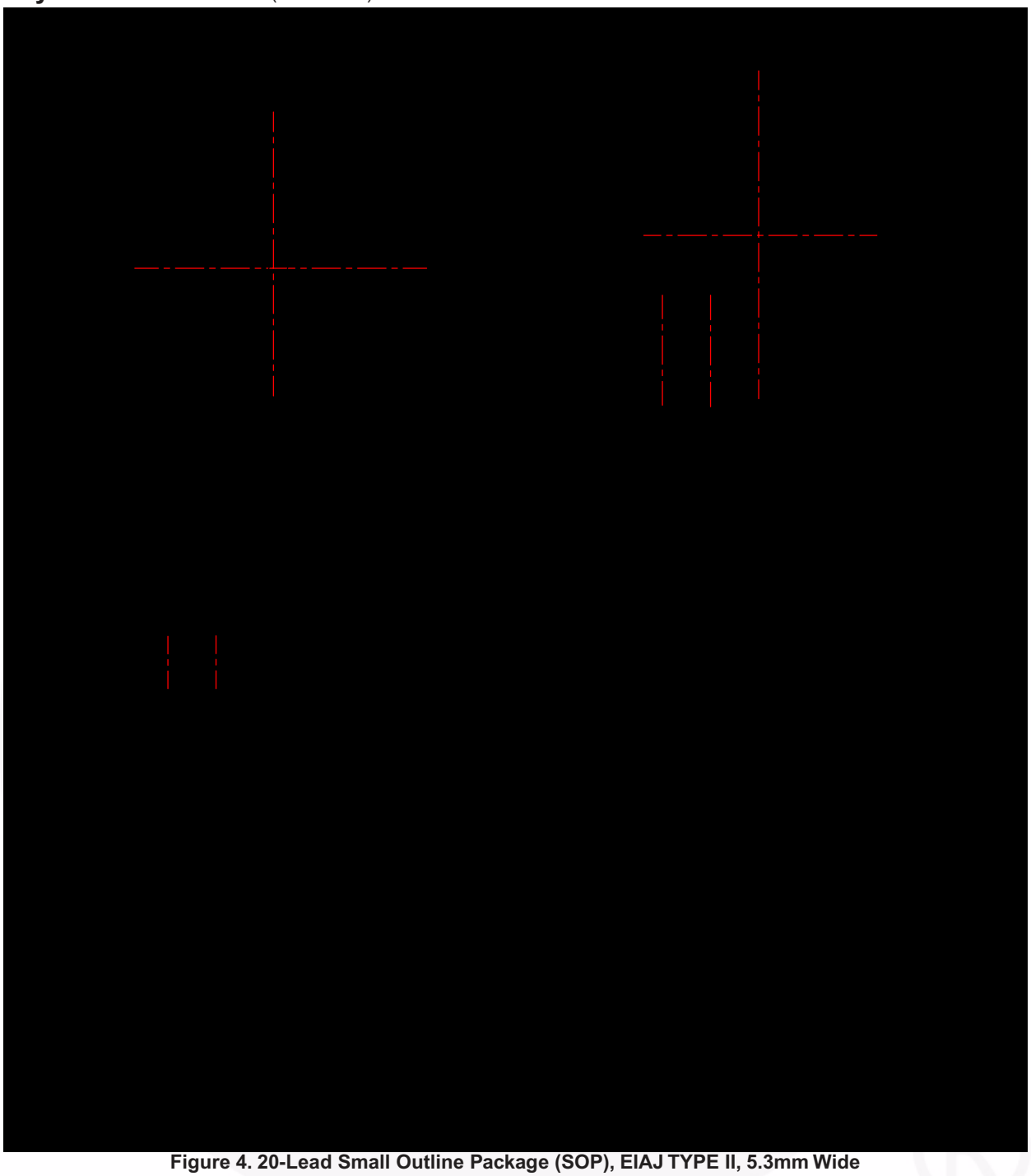

Figure 4. 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide

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Physical Dimensions (Continued)

Figure 5. 20-Lead Shrink Small Outline Package (SSOP), JEDEC MO-150, 5.3mm Wide

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Physical Dimensions (Continued)

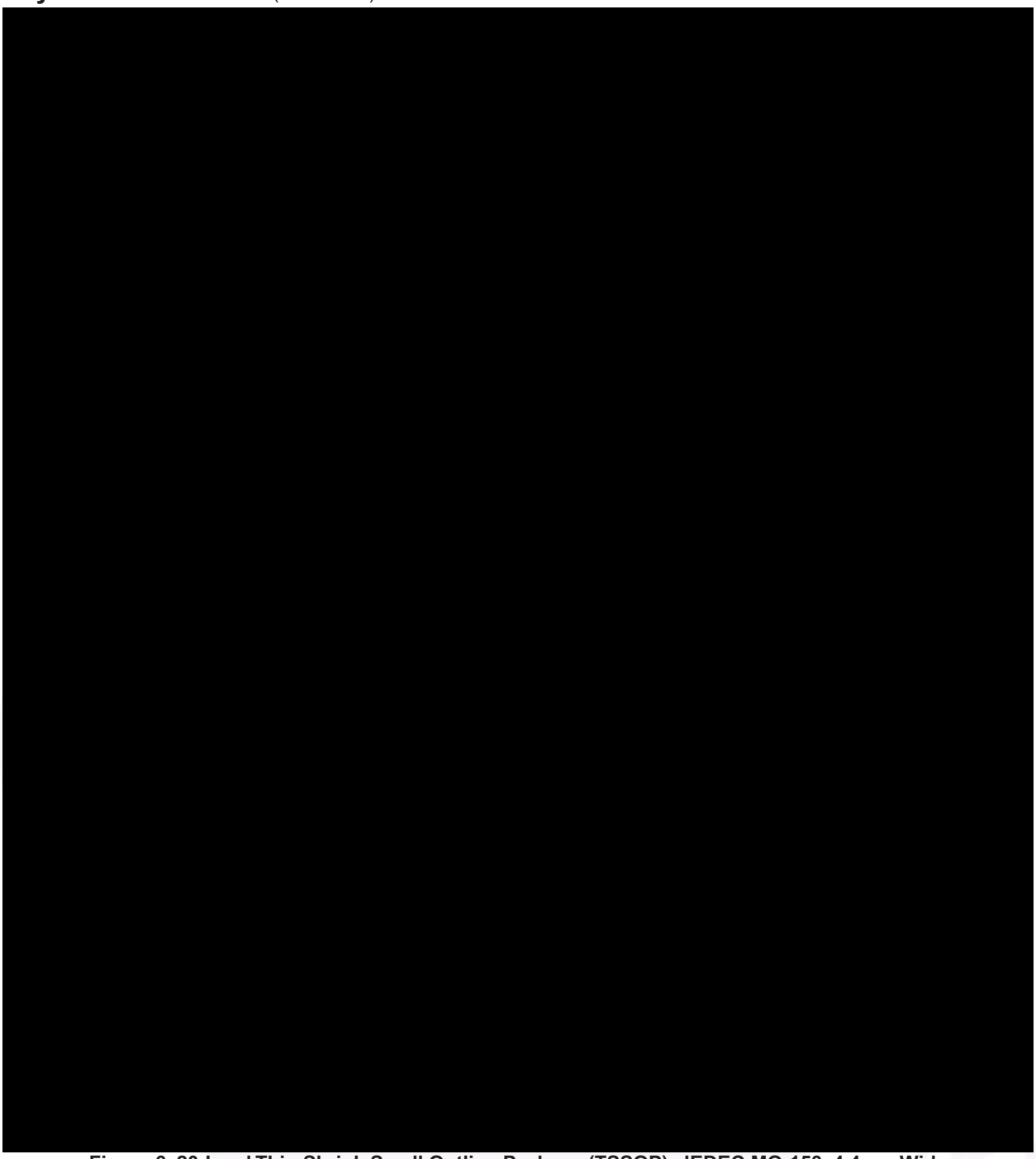

Figure 6. 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

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