

## **Enhanced Quad Clock Translator**

Short Form Data Sheet

January 2014

#### **Features**

- · Four independent clock channels
- Programmable synthesizers generate any clockrate from 1 Hz to 750 MHz
- Four precision synthesizers generate clocks with maximum jitter below 0.63 ps RMS
- Four programmable digital PLLs/Numerically Controlled Oscillators (NCOs)/OTN clock generators based on buffer-fill levels
  - Programmable digital PLLs synchronize to any clock rate from 1 kHz to 750 MHz
  - Flexible two-stage architecture translates between arbitrary data rates, line coding rates and FEC rates
  - Digital PLLs filter jitter with bandwidths from 5 to 896 Hz
  - Automatic hitless reference switching and digital holdover on reference fail
- Eight reference inputs configurable as single ended or differential

#### **Ordering Information**

ZL30168GDG2 144 Pin LBGA Trays Pb Free Tin/Silver/Copper -40°C to +85°C

Package size: 13 x 13 mm

- Eight LVPECL outputs and eight LVCMOS outputs
- Operates from a single crystal resonator or clock oscillator
- Configurable via four selectable default configurations or field programmable via SPI/I2C interface

## **Applications**

- OTN muxponders and transponders
- 10 Gigabit line cards
- Synchronous Ethernet, 10 GBASE-R and 10 GBASE-W
- · SONET/SDH, Fibre Channel, XAUI

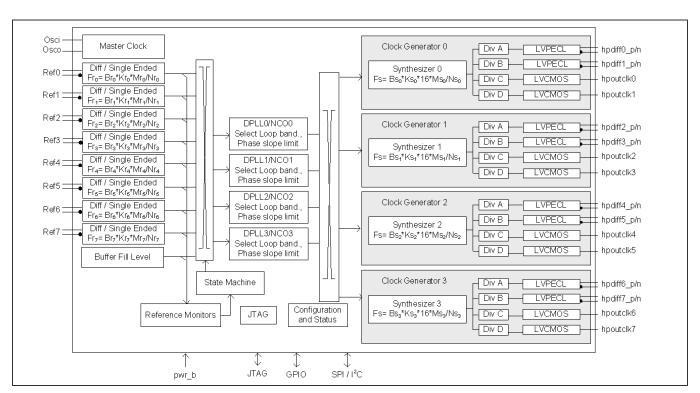


Figure 1 - Functional Block Diagram



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