TPS65217x Single-Chip PMIC for Battery-Powered Systems

1 Features

- ***Charger and Power Path***
  - 2-A Output Current on Power Path
  - Linear Charger; 700-mA Maximum Charge Current
  - 20-V Tolerant USB and AC Inputs
  - Thermal Regulation, Safety Timers
  - Temperature Sense Input
- ***Step-Down Converter (DCDC1, DCDC2, DCDC3)***
  - Three Step-Down Converter With Integrated Switching FETs
  - 2.25-MHz Fixed Frequency Operation
  - Power-Save Mode at Light-Load Current
  - Output Voltage Accuracy in PWM Mode ±2%
  - 100% Duty Cycle for Lowest Dropout
  - Typical 15-µA Quiescent per Converter
  - Passive Discharge to Ground When Disabled
- ***LDO Regulators (LDO1, LDO2)***
  - Two Adjustable LDOs
  - LDO2 can be Configured to Track DCDC3
  - Typical 15-µA Quiescent Current
- ***Load Switches (LDO3, LDO4)***
  - Two Independent Load Switches That Can Be Configured as LDOs
- ***WLED Driver***
  - Internally Generated PWM for Dimming Control
  - 38-V Open-LED Protection
  - Supports Two Strings of up to 10 LEDs at 25 mA Each
  - Internal Low-Side Current Sinks
- ***Protection***
  - Undervoltage Lockout and Battery Fault Comparator
  - Always-On Push-Button Monitor
  - Hardware Reset Pin
  - Password Protected I^{2}C Registers
- ***Interface***
  - I^{2}C Interface (Address 0x24)
  - Password-Protected I^{2}C Registers

2 Applications

- Sitara™ AM335x Processor Power
- Portable Navigation Systems
- Tablet Computing
- 5-V Industrial Equipment

3 Description

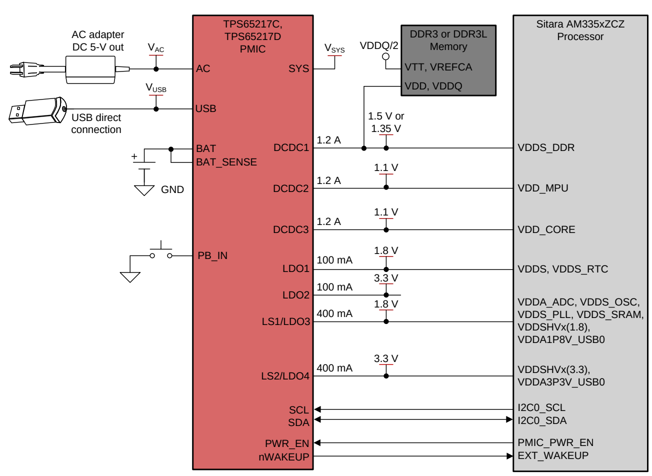
The TPS65217x is a single-chip power management IC (PMIC) specifically designed to power the AM335x ARM® Cortex®-A8 processor in portable and 5-V line-powered applications. The PMIC device provides a linear battery charger for single-cell Li-ion and Li-polymer batteries, dual-input power path, three step-down converters, four low-dropout (LDO) regulators, and a high-efficiency boost converter to power two strings of up to 10 LEDs each. The system can be supplied by any combination of USB port, 5-V AC adaptor, or Li-Ion battery. The device is characterized across a –40°C to +105°C temperature range which makes it suitable for industrial applications. Three high-efficiency 2.25-MHz step-down converters can providing the core voltage, memory, and I/O voltage for a system. The TPS65217x device comes in a 48-pin leadless package (6-mm × 6-mm VQFN) with a 0.4-mm pitch.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS65217A	VQFN (48)	6.00 mm × 6.00 mm
TPS65217B		
TPS65217C		
TPS65217D		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Application Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision H (June 2017) to Revision I — Page

- Changed the diagram in the *Description* section ... 1
- Changed the lists in the *Power-Up Sequencing* section to logical sentences for simplicity ... 20
- Added a description of the *always-on* power supply in the *Push-Button Monitor (PB_IN)* section ... 23
- Changed the *Global State Diagram* ... 39
- Fixed typos in the *Register Address Map* section ... 44
- Changed the list of access types to be more simple and added a note for reserved bits in the *Access Type Codes* table ... 44
- Changed the first paragraph in the *5-V Operation Without a Battery* section ... 77
- Added the *Documentation Support* section ... 83

Changes from Revision G (January 2015) to Revision H — Page

- Added a Reference Design button to the top of the first page ... 1
- Revised Figure 4 ... 20
- Reversed STROBE 14 and STROBE 15 in the second paragraph of Special Strobes (STROBE 14 and 15) ... 22
- Changed PFMENx bit value required to force PWM operation at light loads from 0 to 1 ... 34
- Changed Figure 24 ... 39
- Changed text in RESET paragraph ... 41
- Added a row to Table 37 ... 78
- *Added Receiving Notification...* and *Community Resources* sections ... 83

Changes from Revision F (April 2013) to Revision G	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

5 Device Comparison Table(1)

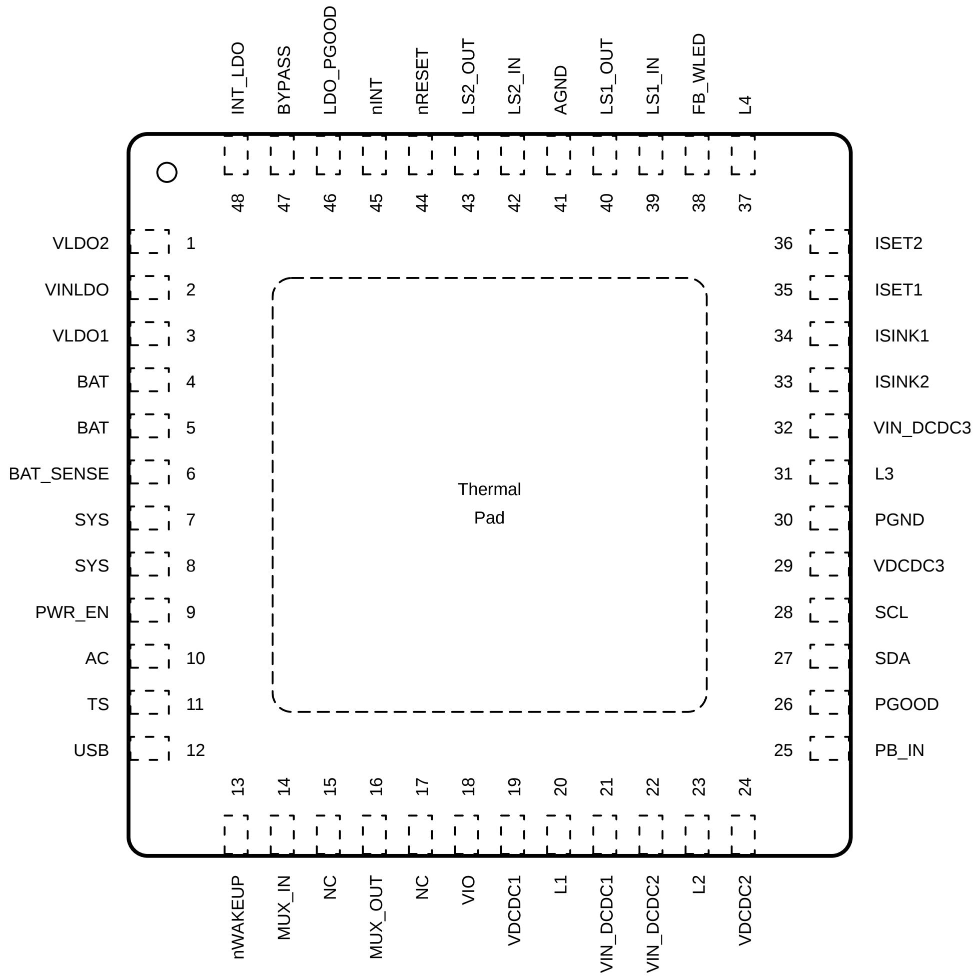
The device comparison table summarizes the default regulator output voltages and sequencing order settings for the four available variants of the TPS65217 device. For details on the preprogrammed register map values that determine these voltage and strobe sequence settings, refer to Register Maps. For details on specific applications, refer to the *Powering the AM335x with the TPS65217x* user's guide.

RAIL	TPS65217A (TARGETED AT AM335x - ZCE)		TPS65217B (TARGETED AT AM335x - ZCZ)		TPS65217C (TARGETED AT AM335x - ZCZ)		TPS65217D (TARGETED AT AM335x - ZCZ)	
	VOLTAGE (V)	SEQUENCE (STROBE)	VOLTAGE (V)	SEQUENCE (STROBE)	VOLTAGE (V)	SEQUENCE (STROBE)	VOLTAGE (V)	SEQUENCE (STROBE)
DCDC1	1.8	1	1.8	1	1.5	1	1.35	1
DCDC2	3.3	2	1.1	5	1.1	5	1.1	5
DCDC3	1.1	3	1.1	5	1.1	5	1.1	5
LDO1 (1)	1.8	15	1.8	15	1.8	15	1.8	15
LDO2	3.3	2	3.3	2	3.3	3	3.3	3
LS1 or LDO3	Load switch	1	3.3 (LDO, 200 mA)	3	1.8 (LDO, 400 mA)	2	1.8 (LDO, 400 mA)	2
LS2 or LDO4	Load switch	4	3.3 (LDO, 200 mA)	4	3.3 (LDO, 400 mA)	4	3.3 (LDO, 400 mA)	4

(1) For more information, see *RESET* in the *PMIC States* section.
(1) Strobe 15 (LDO1) is the first rail to be enabled in a sequence, followed by strobe 1 through strobe 7. For more information, see the *Wake-Up and Power-Up Sequencing* section.

6 Pin Configuration and Functions

RSL Package
48-Pin VQFN With Exposed Thermal Pad
Top View



NC – No internal connection

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
AC	10	I	AC-adapter input to power path. Connect this pin to an external dc supply.
AGND	41	—	Analog ground (GND). Connect the AGND pin to the ground plane.
BAT	4, 5	I/O	Battery charger output. Connect these pins to the battery.
BAT_SENSE	6	I	Battery-voltage sense input. Connect the BAT_SENSE pin to the BAT pin directly at the battery terminal.
BYPASS	47	O	Internal bias voltage (2.25 V). TI does not recommend connecting any external load to this pin.
FB_WLED	38	I	Feedback pin for the WLED boost converter. This pin is also connected to the anode of the WLED strings.
INT_LDO	48	O	Internal bias voltage (2.3 V). TI does not recommend connecting any external load to this pin.
ISET1	35	I	Low-level WLED current set. Connect this pin to a resistor to ground to set the WLED low-level current value.
ISET2	36	I	High-level WLED current set. Connect this pin to a resistor to ground to set the WLED high-level current value.

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
ISINK1	34	I	Input to the WLED current SINK1. Connect this pin to the cathode of the WLED string. Current through the SINK1 pin equals current through the ISINK2 pin. If only one WLED string is used, short the ISINK1 and ISINK2 pins together.
ISINK2	33	I	Input to the WLED current SINK2. Connect this pin to the cathode of the WLED string. Current through the SINK1 pin equals current through the ISINK2 pin. If only one WLED string is used, short the ISINK1 and ISINK2 pins together.
L1	20	O	Switch pin for DCDC1. Connect this pin to the respective inductor.
L2	23	O	Switch pin for DCDC2. Connect this pin to the respective inductor.
L3	31	O	Switch pin for DCDC3. Connect this pin to the respective inductor.
L4	37	O	Switch pin of the WLED boost converter. Connected this pin to the respective inductor.
LDO_PGOOD	46	O	Power-good signal for the LDO regulator (LDO1 and LDO2 only). This pin is a push-pull output. This pin is pulled low when either the LDO1 or LDO2 regulator is out of regulation.
LS1_IN	39	I	Input voltage pin for load switch 1 (LS1) or LDO3
LS1_OUT	40	O	Output voltage pin for load switch 1 (LS1) or LDO3
LS2_IN	42	I	Input voltage pin for load switch 2 (LS2) or LDO4
LS2_OUT	43	O	Output voltage pin for load switch 2 (LS2) or LDO4
MUX_IN	14	O	Input to analog multiplexer
MUX_OUT	16	O	Output pin of analog multiplexer
NC	15, 17		Not used
nINT	45	O	Interrupt output. This pin is an active-low, open-drain output. This pin is pulled low if an interrupt bit is set. The output goes high after the bit causing the interrupt in the INT register is read. The interrupt sources can be masked in the INT register, such that no interrupt is generated when the corresponding interrupt bit is set.
nRESET	44	I	Reset pin. This pin is an active-low input. Pulling this pin low causes the PMIC to shut down. When this pin returns to a high voltage level, the PMIC powers up in its default state after a 1-s delay.
nWAKEUP	13	O	Signal to the host to indicate a power-on event. This pin is an active-low, open-drain output.
PB_IN	25	I	Push-button monitor input. This pin is typically connected to a momentary switch to ground. This pin is an active-low input.
PGND	30		Power ground. Connect this pin to the ground plane.
PGOOD	26	O	Power-good output. This pin is a push-pull output. This pin is pulled low when any of the power rails are out of regulation.
PWR_EN	9	I	Enable input for the DCDC1, DCDC2, and DCDC3 converters, and the LDO1, LDO2, LDO3, and LDO4 regulators. Pull this pin high to start the power-up sequence.
SCL	28	I	Clock input for the I^2C interface
SDA	27	I/O	Data line for the I^2C interface
SYS	7, 8	O	System voltage pin and output of the power path. All voltage regulators are typically powered from this output.
TS	11	I	Temperature sense input. Connect this pin to the NTC thermistor to sense the battery temperature. This pin works with 10-kΩ and 100-kΩ thermistors. For more information, see the *Battery-Pack Temperature Monitoring* section.
USB	12	I	USB voltage input to power path. Connect this pin to an external voltage from a USB port.
VDCDC1	19	I	DCDC1 output and feedback voltage-sense input
VDCDC2	24	I	DCDC2 output and feedback voltage-sense input
VDCDC3	29	I	DCDC3 output and feedback voltage-sense input
VINLDO	2	I	Input voltage for LDO1 and LDO2
VIN_DCDC1	21	I	Input voltage for DCDC1. This pin must be connected to the SYS pin.
VIN_DCDC2	22	I	Input voltage for DCDC2. This pin must be connected to the SYS pin.
VIN_DCDC3	32	I	Input voltage for DCDC3. This pin must be connected to the SYS pin.
VIO	18	I	Output-high supply for output buffers
VLDO1	3	O	Output voltage of LDO1

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
VLDO2	1	O	Output voltage of LDO2
Thermal pad		—	Power-ground connection for the PMIC. Connect the thermal pad to the ground plane.

7 Specifications

7.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)(1) (2)

			MIN	MAX	UNIT
	Supply voltage (with respect to PGND)	BAT	–0.3	7	V
		USB, AC	–0.3	20	
	Input/output voltage (with respect to PGND)	All pins unless specified separately	–0.3	7	V
		ISINK	–0.3	20	
		L4, FB_WLED	–0.3	44	
	Absolute voltage difference between SYS and any VIN_DCDCx pin or SYS and VINLDO		0.3	0.3	V
	Terminal current	SYS, USB, BAT	3000	3000	mA
	Source or Sink current	PGOOD, LDO_PGOOD	6	6	mA
	Sink current	nWAKEUP, nINT	2	2	mA
T_J	Operating junction temperature		125	125	°C
T_A	Operating ambient temperature		–40	105	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage, USB, AC	4.3		5.8	V
Supply voltage, BAT	2.75		5.5	V
Input current from AC			2.5	A
Input current from USB			1.3	A
Battery current			2	A
Input voltage range for DCDC1, DCDC2, and DCDC3	2.7		5.8	V
Input voltage range for LDO1, LDO2	1.8		5.8	V
Input voltage range for LS1 or LDO3, LS2, or LDO4 configured as LDOs	2.7		5.8	V
Input voltage range for LS1 or LDO3, LS2, or LDO4 configured as load switches	1.8		5.8	V
Output voltage range for LDO1	1		3.3	V
Output voltage range for LDO2	0.9		3.3	V
Output voltage range for LS1 or LDO3, LS2, or LDO4	1.8		3.3	V

Recommended Operating Conditions (continued)

over operating ambient temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Output current DCDC1		0		1.2	A
Output current DCDC2		0		1.2	A
Output current DCDC3		0		1.2	A
Output current LDO1, LDO2		0		100	mA
Output current LS1 or LDO3, LS2, or LDO4 configured as LDOs	TPS65217A	0		200	mA
	TPS65217B	0		200	
	TPS65217C	0		400	
	TPS65217D	0		400	
Output current LS1 or LDO, LS2 or LDO4 configured as load switches		0		200	mA

7.4 Thermal Information

THERMAL METRIC(1)		TPS65217 RSL (VQFN) 48 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	30.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	16.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	5.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	5.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

V_{BAT} = 3.6 V ±5%, T_J = 27ºC (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT VOLTAGE AND CURRENTS							
V_{BAT}	Battery input voltage range	USB or AC supply connected		0		5.5	V
		USB and AC not connected		2.75		5.5	
V_{AC}	AC adapter input voltage range	Valid range for charging		4.3		5.8	V
V_{USB}	USB input voltage range	Valid range for charging		4.3		5.8	V
V_{UVLO}	Undervoltage lockout	Measured in respect to V_{BAT}; supply falling; V_{AC} = V_{USB} = 0 V	UVLO[1:0] = 00b		2.73		V
			UVLO[1:0] = 01b		2.89		
			UVLO[1:0] = 10b		3.18		
			UVLO[1:0] = 11b		3.3		
	UVLO accuracy			–2%		2%	
	UVLO deglitch time(1)			4		6	ms
V_{OFFSET}	AC and USB UVLO offset	V_{BAT} < V_{UVLO}; Device shuts down when V_{AC}, V_{USB} drop below V_{UVLO} + V_{OFFSET}			200		mV
I_{OFF}	OFF current, Total current into VSYS, VINDCDCx, VINLDO	All rails disabled, T_A = 27°C			6		µA
I_{SLEEP}	Sleep current, Total current into VSYS, VINDCDCx, VINLDO	LDO1 and LDO2 enabled, no load. All other rails disabled. V_{SYS} = 4 V, T_A = 0.105°C			80	106	µA
POWER PATH AC AND USB DETECTION LIMITS							

(1) Not tested in production

Electrical Characteristics (continued)

V_{BAT} = 3.6 V ±5%, T_J = 27ºC (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IN(DT)}$	AC and USB voltage-detection threshold	$V_{BAT} > V_{UVLO}$, AC and USB valid when $V_{AC-USB} – V_{BAT} > V_{IN(DT)}$	190			mV
		$V_{BAT} < V_{UVLO}$, AC and USB valid when $V_{AC-USB} > V_{IN(DT)}$	4.3			V
$V_{IN(NDT)}$	AC and USB voltage-removal detection threshold	$V_{BAT} > V_{UVLO}$, AC and USB invalid when $V_{AC/USB} – V_{BAT} < V_{IN(DT)}$			125	mV
		$V_{BAT} < V_{UVLO}$, AC and USB invalid when $V_{AC-USB} < V_{IN(DT)}$		V_{UVLO} + V_{OFFSET}		V
t_{RISE}	V_{AC}, V_{USB} rise time	Voltage rising from 100 mV to 4.5 V. If rise time is exceeded, device may not power up.			50	ms
$t_{DG(DT)}$	Power detected deglitch(1)	AC or USB voltage increasing		22.5		ms
$V_{IN(OVP)}$	Input overvoltage detection threshold	USB and AC input	5.8	6	6.4	V
POWER PATH TIMING						
$t_{SW(PSEL)}$	Switching from AC to USB(1)				150	µs
POWER PATH MOSFET CHARACTERISTICS						
$V_{DO, AC}$	AC input switch dropout voltage	IAC[1:0] = 11b (2.5 A), I_{SYS} = 1 A		150		mV
$V_{DO, USB}$	USB input switch dropout voltage	IUSB[1:0] = 01b (500 mA), I_{SYS} = 500 mA		100		mV
		IUSB[1:0] = 10b (1300 mA), I_{SYS} = 800 mA		160		
$V_{DO, BAT}$	Battery switch dropout voltage	V_{BAT} = 3 V, I_{BAT} = 1 A		60		mV
POWER PATH INPUT CURRENT LIMITS						
I_{ACLMT}	Input current limit; AC pin	IAC[1:0] = 00b	90		130	mA
		IAC[1:0] = 01b	480		580	
		IAC[1:0] = 10b	1000	1500		
		IAC[1:0] = 11b	2000	2500		
I_{USBLMT}	Input current limit; USB pin	IUSB[1:0] = 00b	90		100	mA
		IUSB[1:0] = 01b	460		500	
		IUSB[1:0] = 10b	1000	1300		
		IUSB[1:0] = 11b	1500	1800		
I_{BAT}	Battery load current(1)				2	A
POWER PATH BATTERY SUPPLEMENT DETECTION						
V_{BSUP}	Battery supplement threshold	$V_{SYS} \leq V_{BAT}$ – VBSUP1, V_{SYS} falling IUSB[1:0] = 10b		40		mV
	Battery supplement hysteresis	V_{SYS} rising		20		
POWER PATH BATTERY PROTECTION						
$V_{BAT(SC)}$	BAT pin short-circuit detection threshold		1.3	1.5	1.7	V
$I_{BAT(SC)}$	Source current for BAT pin short-circuit detection			7.5		mA
INPUT BASED DYNAMIC POWER PATH MANAGEMENT (DPPM)						
V_{DPPM}	Threshold at which DPPM loop is enabled	I^2C selectable	3.5		4.25	V
BATTERY CHARGER						
V_{OREG}	Battery charger voltage	I^2C selectable	4.1		4.25	V
	Battery charger accuracy		–2%		1%	
V_{LOWV}	Precharge to fast-charge transition threshold	VPRECHG = 0b		2.9		V
		VPRECHG = 1b		2.5		
$t_{DGL1(LOWV)}$	Deglitch time on precharge to fast-charge transition(1)			25		ms
$t_{DGL2(LOWV)}$	Deglitch time on fast-charge to precharge transition(1)			25		ms
I_{CHG}	Battery fast charge current range $V_{OREG} > V_{BAT} > V_{LOWV}$, $V_{IN} = V_{USB}$ = 5 V	ICHRG[1:0] = 00b		300		mA
		ICHRG[1:0] = 01b		400		
		ICHRG[1:0] = 10b	450	500	550	
		ICHRG[1:0] = 11b		700		

Electrical Characteristics (continued)

V_{BAT} = 3.6 V ±5%, T_J = 27ºC (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{PRECHG}	Precharge current	ICHRG[1:0] = 00b			30		mA
		ICHRG[1:0] = 01b			40		
		ICHRG[1:0] = 10b		25	50	75	
		ICHRG[1:0] = 11b			70		
I_{TERM}	Charge current value for termination detection threshold (fraction of I_{CHG})	TERMIF[1:0] = 00b			2.5%		
		TERMIF[1:0] = 01b		3%	7.5%	10%	
		TERMIF[1:0] = 10b			15%		
		TERMIF[1:0] = 11b			18%		
$t_{DGL(TERM)}$	Deglitch time, termination detected(1)				125		ms
V_{RCH}	Recharge detection threshold	Voltage below V_{OREG}		150	100	70	mV
$t_{DGL(RCH)}$	Deglitch time, recharge threshold detected(1)				125		ms
$I_{BAT(DET)}$	Sink current for battery detection	T_J = 27°C		3	7.5	10	mA
t_{DET}	Battery detection timer. $I_{BAT(DET)}$ is pulled from the battery for t_{DET}. If BAT voltage stays above V_{RCH} threshold the battery is connected.(1)	$V_{BAT} < V_{RCH;}$			250		ms
t_{CHG}	Charge safety timer(1)	Safety timer range, thermal and DPPM not active, selectable by I²C		4		8	h
t_{PRECHG}	Precharge timer(1)	Pre charge timer, thermal and DPPM loops not active, selectable by I²C	PCHRGT = 0b		30	60	min
			PCHRGT = 1b		60		
BATTERY NTC MONITOR							
t_{THON}	Thermistor power on time at charger off, sampling mode on				10		ms
t_{THOFF}	Thermistor power sampling period at charger off, sampling mode on				1		s
R_{NTC_PULL}	Pullup resistor from thermistor to Internal LDO, I²C selectable	NTC_TYPE = 1 (10-kΩ NTC)			7.35		kΩ
		NTC_TYPE = 0 (100-kΩ NTC)			60.5		
	Accuracy	T_A = 27°C		–3%		3%	
V_{LTF}	Low-temperature failure threshold	Temperature falling			1660		mV
		Temperature rising			1610		
V_{HTF}	High-temperature failure threshold	Temperature falling	TRANGE = 0b		910		mV
		Temperature rising			860		
		Temperature falling	TRANGE = 1b		667		
		Temperature rising			622		
V_{DET}	Thermistor detection threshold			1750		1850	mV
t_{BATDET}	Thermistor not detected. Battery not present deglitch(1)				26		ms
THERMAL REGULATION							
$T_{J(REG)}$	Temperature regulation limit, temperature at which charge current is decreased			111		123	°C
DCDC1 (BUCK)							
V_{IN}	Input voltage range	VIN_DCDC1 pin		2.7		V_{SYS}	V
$I_{Q,SLEEP}$	Quiescent current in SLEEP mode	No load, V_{SYS} = 4 V, T_A = 25°C			30		µA
V_{OUT}	Output voltage range	External resistor divider (XADJ1 = 1b)		0.6		V_{IN}	V
		I²C selectable in 25-mV steps (XADJ1 = 0b)		0.9		1.8(2)	
	DC output voltage accuracy	V_{IN} = V_{OUT} + 0.3 V to 5.8 V; 0 mA ≤ I_{OUT} ≤ 1.2 A		–2%		3%	
	Power-save mode (PSM) ripple voltage	I_{OUT} = 1 mA, PFM mode L = 2.2 µH, C_{OUT} = 20 µF			40		mV_{pp}
I_{OUT}	Output current range			0		1.2	A

(2) Contact factory for 3.3-V option.

Electrical Characteristics (continued)

V_{BAT} = 3.6 V ±5%, T_J = 27ºC (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$r_{DS(on)}$	High-side MOSFET on-resistance	V_{IN} = 2.7 V		170		mΩ
	Low-side MOSFET on-resistance	V_{IN} = 2.7 V		120		
I_{LEAK}	High-side MOSFET leakage current	V_{IN} = 5.8 V			2	µA
	Low-side MOSFET leakage current	V_{DS} = 5.8 V			1	
I_{LIMIT}	Current limit (high- and low-side MOSFET).	2.7 V < V_{IN} < 5.8 V		1.6		A
f_{SW}	Switching frequency		1.95	2.25	2.55	MHz
V_{FB}	Feedback voltage	XADJ = 1b		600		mV
t_{SS}	Soft-start time	Time to ramp V_{OUT} from 5% to 95%, no load		750		µs
R_{DIS}	Internal discharge resistor at L1 (3)			250		Ω
L	Inductor		1.5	2.2		µH
C_{OUT}	Output capacitor	Ceramic	10	22		µF
	ESR of output capacitor			20		mΩ
DCDC2 (BUCK)						
V_{IN}	Input voltage range	VIN_DCDC2 pin	2.7		V_{SYS}	V
$I_{Q,SLEEP}$	Quiescent current in SLEEP mode	No load, V_{SYS} = 4 V, T_A = 25°C		30		µA
V_{OUT}	Output voltage range	External resistor divider (XADJ2 = 1b)	0.6		V_{IN}	V
		I^2C selectable in 25-mV steps (XADJ2 = 0b)	0.9		3.3	
	DC output voltage accuracy	V_{IN} = V_{OUT} + 0.3 V to 5.8 V; 0 mA ≤ I_{OUT} ≤ 1.2 A	–2%		3%	
	Power-save mode (PSM) ripple voltage	I_{OUT} = 1 mA, PFM mode L = 2.2 µH, C_{OUT} = 20 µF		40		mV_{pp}
I_{OUT}	Output current range		0		1.2	A
$r_{DS(on)}$	High-side MOSFET on-resistance	V_{IN} = 2.7 V		170		mΩ
	Low-side MOSFET on-resistance	V_{IN} = 2.7 V		120		
I_{LEAK}	High-side MOSFET leakage current	V_{IN} = 5.8 V			2	µA
	Low-side MOSFET leakage current	V_{DS} = 5.8 V			1	
I_{LIMIT}	Current limit (high and low side MOSFET).	2.7 V < V_{IN} < 5.8 V		1.6		A
f_{SW}	Switching frequency		1.95	2.25	2.55	MHz
V_{FB}	Feedback voltage	XADJ = 1b		600		mV
t_{SS}	Soft-start time	Time to ramp V_{OUT} from 5% to 95%, no load		750		µs
R_{DIS}	Internal discharge resistor at L2			250		Ω
L	Inductor		1.5	2.2		µH
C_{OUT}	Output capacitor	Ceramic	10	22		µF
	ESR of output capacitor			20		mΩ
DCDC3 (BUCK)						
V_{IN}	Input voltage range	VIN_DCDC3 pin	2.7		V_{SYS}	V
$I_{Q,SLEEP}$	Quiescent current in SLEEP mode	No load, V_{SYS} = 4 V, T_A = 25°C		30		µA
V_{OUT}	Output voltage range	External resistor divider (XADJ3 = 1b)	0.6		V_{IN}	V
		I^2C selectable in 25-mV steps (XADJ3 = 0b)	0.9		1.5 (2)	
	DC output voltage accuracy	V_{IN} = V_{OUT} + 0.3 V to 5.8 V; 0 mA ≤ I_{OUT} ≤ 1.2 A	–2%		3%	
	Power save mode (PSM) ripple voltage	I_{OUT} = 1 mA, PFM mode L = 2.2 µH, C_{OUT} = 20 µF		40		mV_{pp}
I_{OUT}	Output current range		0		1.2	A
$r_{DS(on)}$	High-side MOSFET on-resistance	V_{IN} = 2.7 V		170		mΩ
	Low side MOSFET on-resistance	V_{IN} = 2.7 V		120		

(3) Can be factory disabled.

Electrical Characteristics (continued)

V_{BAT} = 3.6 V ±5%, T_J = 27ºC (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{LEAK}	High-side MOSFET leakage current	V_{IN} = 5.8 V				2	µA
	Low-side MOSFET leakage current	V_{DS} = 5.8 V				1	µA
I_{LIMIT}	Current limit (high- and low-side MOSFET).	2.7 V < V_{IN} < 5.8 V			1.6		A
f_{SW}	Switching frequency			1.95	2.25	2.55	MHz
V_{FB}	Feedback voltage	XADJ = 1b			600		mV
t_{SS}	Soft-start time	Time to ramp V_{OUT} from 5% to 95%, no load			750		µs
R_{DIS}	Internal discharge resistor at L1, L2				250		Ω
L	Inductor			1.5	2.2		µH
C_{OUT}	Output capacitor	Ceramic		10	22		µF
	ESR of output capacitor				20		mΩ
LDO1, LDO2							
V_{IN}	Input voltage range			1.8		5.8	V
$I_{Q,SLEEP}$	Quiescent current in SLEEP mode	No load, V_{SYS} = 4 V, T_A = 25°C			5		µA
V_{OUT}	Output voltage range	LDO1, I²C selectable		1		3.3	V
		LDO2, I²C selectable		0.9		3.3	V
	DC output voltage accuracy	I_{OUT} = 10 mA, V_{IN} > V_{OUT} + 200 mV, V_{OUT} > 0.9 V		–2%		2%	
	Line regulation	V_{IN} = 2.7 V - 5.5 V, V_{OUT} = 1.2 V, I_{OUT} = 100 mA		–1%		1%	
	Load regulation	I_{OUT} = 1 mA - 100 mA, V_{OUT} = 1.2 V, V_{IN} = 3.3 V		–1%		1%	
		I_{OUT} = 0 mA - 1 mA, V_{OUT} = 1.2 V, V_{IN} = 3.3 V		–2.5%		2.5%	
I_{OUT}	Output current range	SLEEP state		0		1	mA
		ACTIVE state		0		100	mA
I_{SC}	Short circuit current limit	Output shorted to GND		100	250		mA
V_{DO}	Dropout voltage	I_{OUT} = 100 mA, V_{IN} = 3.3 V				200	mV
R_{DIS}	Internal discharge resistor at output				430		Ω
C_{OUT}	Output capacitor	Ceramic			2.2		µF
	ESR of output capacitor				20		mΩ
LS1 OR LDO3, AND LS2 OR LDO4, CONFIGURED AS LDOs							
V_{IN}	Input voltage range			2.7		5.8	V
$I_{Q,SLEEP}$	Quiescent current in SLEEP mode	No load, V_{SYS} = 4 V, T_A = 25°C			30		µA
V_{OUT}	Output voltage range	LS1LDO3 = 1b, LS2LDO4 = 1b I²C selectable		1.5		3.3	V
	DC output voltage accuracy	I_{OUT} = 10 mA, V_{IN} > V_{OUT} + 200 mV, V_{OUT} > 1.8 V		–2%		2%	
	Line regulation	V_{IN} = 2.7 V - 5.5 V, V_{OUT} = 1.8 V, I_{OUT} = 200 mA		–1%		1%	
	Load regulation	I_{OUT} = 1 mA - 200 mA, V_{OUT} = 1.8 V, V_{IN} = 3.3 V		–1%		1%	
I_{OUT}	Output current range	TPS65217A		0		200	mA
		TPS65217B		0		200	mA
		TPS65217C		0		400	mA
		TPS65217D		0		400	mA
I_{SC}	Short-circuit current limit	Output shorted to GND	TPS65217A	200	280		mA
			TPS65217B	200	280		mA
			TPS65217C	400	480		mA
			TPS65217D	400	480		mA
V_{DO}	Dropout voltage	I_{OUT} = 200 mA, V_{IN} = 3.3 V				200	mV
R_{DIS}	Internal discharge resistor at output(3)				375		Ω

Electrical Characteristics (continued)

V_{BAT} = 3.6 V ±5%, T_J = 27ºC (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{OUT}	Output capacitor	Ceramic	8	10	12	µF
	ESR of output capacitor			20		mΩ
LS1 OR LDO3, AND LS2 OR LDO4, CONFIGURED AS LOAD SWITCHES						
V_{IN}	Input voltage range	LS1_VIN, LS2_VIN pins	1.8		5.8	V
$R_{DS(ON)}$	P-channel MOSFET on-resistance	V_{IN} = 1.8 V, over full temperature range		300	650	mΩ
I_{SC}	Short circuit current limit	Output shorted to GND	200	280		mA
R_{DIS}	Internal discharge resistor at output			375		Ω
C_{OUT}	Output capacitor	Ceramic	1	10	12	µF
	ESR of output capacitor			20		mΩ
WLED BOOST						
V_{IN}	Input voltage range		2.7		5.8	V
V_{OUT}	Max output voltage	I_{SINK} = 20 mA	32			V
V_{OVP}	Output overvoltage protection		37	38	39	V
$R_{DS(ON)}$	N-channel MOSFET on-resistance	V_{IN} = 3.6 V		0.6		Ω
I_{LEAK}	N-channel leakage current	V_{DS} = 25 V, T_A = 25°C		2		µA
I_{LIMIT}	N-channel MOSFET current limit			1.6	1.9	A
f_{SW}	Switching frequency			1.125		MHz
I_{INRUSH}	Inrush current on start-up	V_{IN} = 3.6 V, 1% duty cycle setting		1.1		A
		V_{IN} = 3.6 V, 100% duty cycle setting		2.1		
L	Inductor			18		µH
C_{OUT}	Output capacitor	Ceramic		4.7		µF
	ESR of output capacitor			20		mΩ
WLED CURRENT SINK1, SINK2						
$V_{SINK1,2}$	Overvoltage protection threshold at ISINK1, ISINK2 pins				19	V
$V_{DO, SINK1,2}$	Current sink drop-out voltage	Measured from ISINK to GND		400		mV
$V_{ISET1,2}$	ISET1, ISET2 pin voltage			1.24		V
$I_{SINK1,2}$	WLED current range (ISINK1, ISINK2)		1		25	mA
	WLED sink current	R_{ISET} = 130.0 kΩ		10		
		R_{ISET} = 86.6 kΩ		15		
		R_{ISET} = 64.9 kΩ		20		
		R_{ISET} = 52.3 kΩ		25		
	DC current set accuracy	I_{SINK} = 5 mA to 25 mA, 100% duty cycle	–5%		5%	
	DC current matching	R_{SET1} = 52.3 kΩ, I_{SINK} = 25 mA, V_{BAT} = 3.6 V, 100% duty cycle	–5%		5%	
		R_{SET1} = 130 kΩ, I_{SINK} = 10 mA, V_{BAT} = 3.6 V, 100% duty cycle	–5%		5%	
f_{PWM}	PWM dimming frequency	FDIM[1:0] = 00b		100		Hz
		FDIM[1:0] = 01b		200		
		FDIM[1:0] = 10b		500		
		FDIM[1:0] = 11b		1000		
ANALOG MULTIPLEXER						
g	Gain, VBAT (V_{BAT} / $V_{OUT,MUX}$); VSYS (V_{SYS} / $V_{OUT,MUX}$)			3		V/V
	Gain, VTS (V_{TS} / $V_{OUT,MUX}$); MUX_IN (V_{MUX_IN} / V_{MUX_OUT})			1		
	Gain, $V_{ICHARGE}$ ($V_{OUT,MUX}$ / $V_{ICHARGE}$)	ICHRG[1:0] = 00b		7.575		V/A
		ICHRG[1:0] = 01b		5.625		
		ICHRG[1:0] = 10b		4.5		
		ICHRG[1:0] = 11b		3.214		
V_{OUT}	Buffer headroom (V_{SYS} – V_{MUX_OUT})	V_{SYS} = 3.6 V, MUX[2:0] = 101b (V_{MUX_IN} – V_{MUX_OUT}) / V_{MUX_IN} > 1%		0.7	1	V

Electrical Characteristics (continued)

V_{BAT} = 3.6 V ±5%, T_J = 27ºC (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{OUT}	Output Impedance			180		Ω
I_{LEAK}	Leakage current	MUX[2:0] = 000b (HiZ), V_{MUX} = 2.25 V			1	µA
LOGIC LEVELS AND TIMING CHARACTERISTICS (SCL, SDA, PB_IN, PGOOD, LDO_PGOOD, PWR_EN, nINT, nWAKEUP, nRESET)						
P_{GTH}	PGOOD comparator treshold, All DC/DC converters and LDOs(1)	Output voltage falling, % of set voltage		90%		
		Output voltage rising, % of set voltage		95%		
P_{GDG}	PGOOD deglitch time	Output voltage falling, DCDC1, DCDC2, DCDC3	2		4	ms
		Output voltage falling, LDO1, LDO2, LDO3, LDO4	1		2	
P_{GDLY}	PGOOD delay time	PGDLY[1:0] = 00b		20		ms
		PGDLY[1:0] = 01b		100		
		PGDLY[1:0] = 10b		200		
		PGDLY[1:0] = 11b		400		
t_{HRST}	PB-IN hard-reset-detect time(1)			8		s
t_{DG}	PB_IN pin deglitch time(1)			50		ms
	PWR_EN pin deglitch time(1)			50		
	nRESET pin deglitch time(1)			30		
R_{PULLUP}	PB_IN internal pullup resistor			100		kΩ
	nRESET internal pullup resistor			100		
V_{IH}	High-level input voltage PB_IN, SCL, SDA, PWR_EN, nRESET		1.2		V_{IN}	V
V_{IL}	Low-level input voltage PB_IN, SCL, SDA, PWR_EN, nRESET		0		0.4	V
I_{BIAS}	Input bias current PB_IN, SCL, SDA			0.01	1	µA
V_{OL}	Output low voltage	nINT, nWAKEUP, I_O = 1 mA			0.3	V
		PGOOD, LDO_PGOOD, I_O = 1 mA			0.3	
V_{OH}	Output high voltage	PGOOD, LDO_PGOOD, I_O = 1 mA	V_{IO} – 0.3			V
I_{LEAK}	Pin leakage current nINT, nWAKEUP	Pin pulled up to 3.3-V supply			0.2	µA
	I^2C slave address			0x24h		
OSCILLATOR						
f_{OSC}	Oscillator frequency			9		MHz
	Oscillator frequency accuracy	T_A = –40°C to 105°C	–10%		10%	
OVERTEMPERATURE SHUTDOWN						
T_{OTS}	Overtemperature shutdown	Increasing junction temperature		150		°C
	Hysteresis	Decreasing junction temperature		20		°C

7.6 I²C Timing Requirements

V_{BAT} = 3.6 V ±5%, T_A = 25ºC, C_L = 100 pF (unless otherwise noted). For the I²C timing diagram, see Figure 1.

			MIN	NOM	MAX	UNIT
f_{SCL}	Serial clock frequency		100		400	kHz
$t_{HD;STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated	SCL = 100 KHz	4			µs
		SCL = 400 KHz	600			ns
t_{LOW}	LOW period of the SCL clock	SCL = 100 KHz	4.7			µs
		SCL = 400 KHz	1.3			
t_{HIGH}	HIGH period of the SCL clock	SCL = 100 KHz	4			µs
		SCL = 400 KHz	600			ns
$t_{SU;STA}$	Set-up time for a repeated START condition	SCL = 100 KHz	4.7			µs
		SCL = 400 KHz	600			ns
$t_{HD;DAT}$	Data hold time	SCL = 100 KHz	0		3.45	µs
		SCL = 400 KHz	0		900	ns
$t_{SU;DAT}$	Data set-up time	SCL = 100 KHz	250			ns
		SCL = 400 KHz	100			
t_r	Rise time of both SDA and SCL signals	SCL = 100 KHz			1000	ns
		SCL = 400 KHz			300	
t_f	Fall time of both SDA and SCL signals	SCL = 100 KHz			300	ns
		SCL = 400 KHz			300	
$t_{SU;STO}$	Set-up time for STOP condition	SCL = 100 KHz	4			µs
		SCL = 400 KHz	600			ns
t_{BUF}	Bus free time between stop and start condition	SCL = 100 KHz	4.7			µs
		SCL = 400 KHz	1.3			
t_{SP}	Pulse duratoin of spikes which mst be suppressed by the input filter	SCL = 100 KHz	NA		NA	
		SCL = 400 KHz	0		50	ns
C_b	Capacitive load for each bus line	SCL = 100 KHz			400	pF
		SCL = 400 KHz			400	

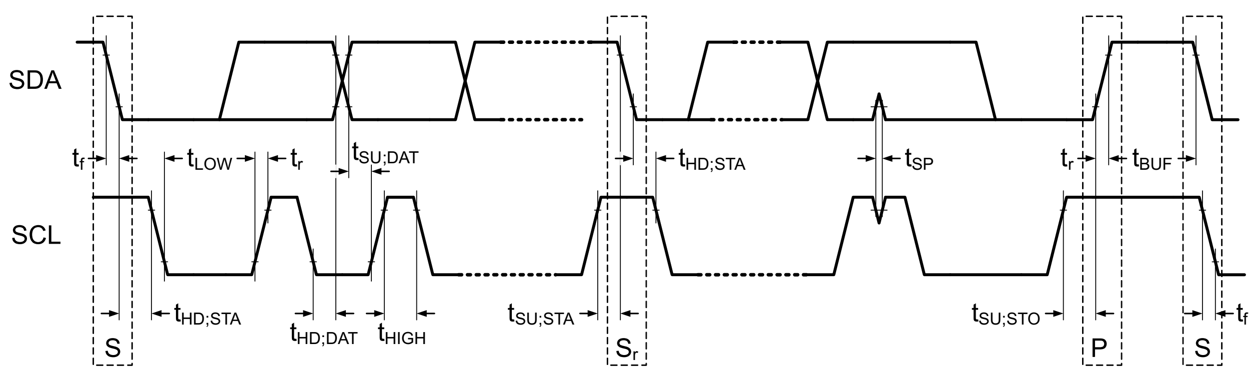


Figure 1. I²C Data Transmission Timing

7.7 Typical Characteristics

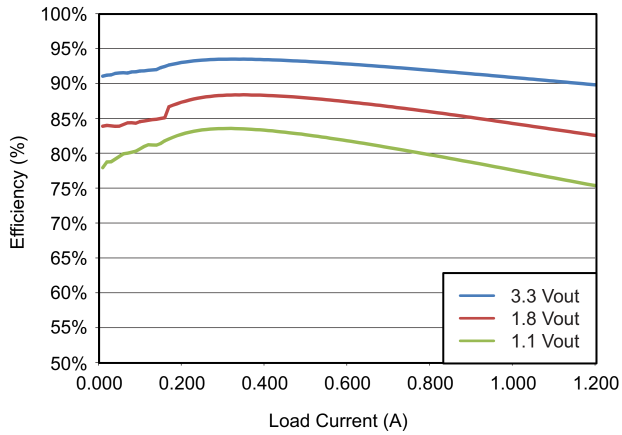


Figure 2. TPS65217x DC/DC Efficiency, 5 V_{IN} and an LQM2HPN2R2MG0L Inductor

8 Detailed Description

8.1 Overview

The TPS65217x device has three step-down converters, two low-dropout (LDO) regulators, two load switches, a linear battery charger, a white LED driver, and a power path. The system can be supplied by any combination of a USB port, 5-V AC adaptor, or Li-ion battery. The device is characterized across a temperature range from –40°C to +105°C, making it suitable for industrial applications where a 5-V power supply rail is available. The device offers configurable power-up and power-down sequencing and several low-speed, system-level functions such as a power-good output, push-button monitor, hardware-reset function, and temperature sensor to protect the battery.

The I^2C interface has comprehensive features for using the TPS65217x device. All rails, load switches, and LDO regulators can be enabled or disabled. Power-up and power-down sequences, overtemperature thresholds, and overcurrent threshold can be programmed through the I^2C interface. The I^2C interface also monitors battery charging and controls LED dimming parameters.

The three DC/DC step-down converters can each supply up to 1.2 A of current. The output voltages for each converter can be adjusted through the I^2C interface in real time to support processor clock frequency changes. All three converters feature dynamic voltage positioning to decrease voltage undershoots and overshoots. Typically, the converters work at a fixed-frequency of 2.25 MHz, pulse-width modulation (PWM) at moderate-to-heavy load currents. At light load currents the converters automatically go to power save mode and operate in pulse-frequency modulation (PFM) for maximum efficiency across the widest possible range of load currents. For low-noise applications, each converter can be forced into fixed-frequency PWM using the I^2C interface. The step-down converters allow the use of small inductors and capacitors to achieve a small solution size.

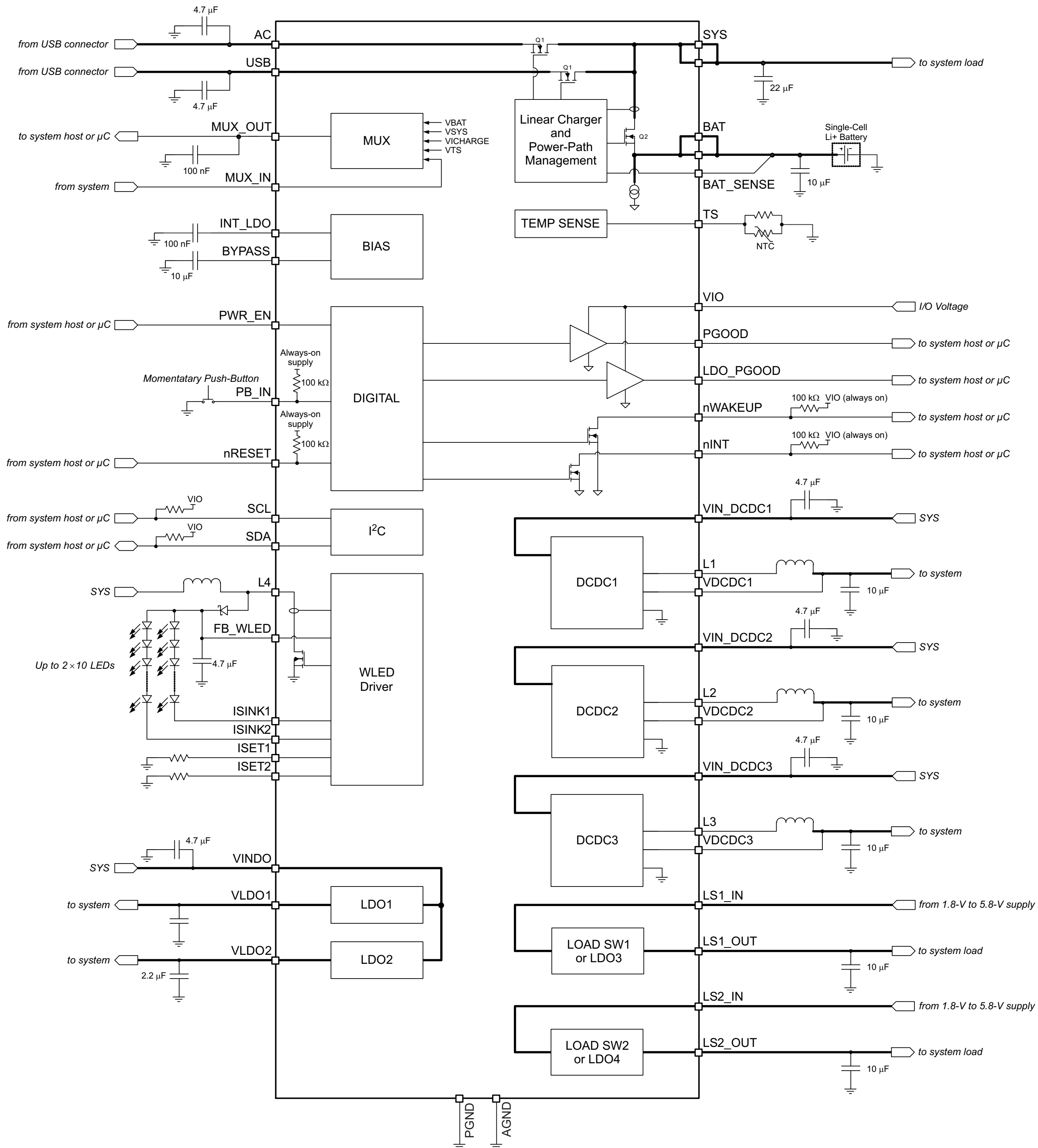
The device has two traditional LDO regulators: LDO1 and LDO2. The LDO1 and LDO2 regulators can support up to 100 mA each during normal operation, but in the SLEEP state they are limited to 1 mA to decrease quiescent current while supporting system-standby mode. The TPS65217A variant of the device also has two load switches: LS1 and LS2. For all other TPS65217x variants, these two outputs are configured as LDO regulators: LDO3 and LDO4. The LDO3 and LDO4 regulators can support up to 200 mA (TPS65217B), or 400 mA (TPS65217C and TPS65217D). All four LDO regulators have a wide input voltage range that allows them to be supplied either from one of the DC/DC converters or directly from the system voltage node.

The device has two power-good logic signals. The primary power-good signal, PGOOD, monitors the DCDC1, DCDC2, and DCDC3 converters, and LS1 (or LDO3) and LS2 (or LDO4) configurable power outputs. This signal is high in the ACTIVE state, but low in the SLEEP, RESET, and OFF states. The secondary power-good signal, LDO_PGOOD, monitors LDO1 and LDO2; the signal is high in the ACTIVE and SLEEP states, but low in the RESET and OFF states. The PGOOD and LDO_PGOOD signals are both pulled low when all the monitored rails are pulled low, or when one or more of the monitored rails are enabled and have encountered a fault, typically an output short or overcurrent condition.

The highly-efficient boost converter has two current sinks that can drive two strings of up to 10 LEDs at 25 mA each, or one string of 20 LEDs at 50 mA. An internal PWM signal and I^2C control support brightness and dimming. Both current sources are controlled together and cannot operate independently.

The triple system power path lets simultaneous and independent powering of the system and battery charging through the linear battery charger for single-cell Li-ion and Li-Polymer batteries. The AC input is prioritized over USB input as the power source for charging the battery and powering the system. Both these sources are prioritized over the battery for powering the system to decrease the number of charge and discharge cycles on the battery.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Wake-Up and Power-Up Sequencing

The TPS65217x device has a predefined power-up–power-down sequence which, in a typical application, does not require changing. However, users can define custom sequences through I^2C control. The power-up sequence is defined by strobes and delay times. Each output rail is assigned to a strobe to determine the order in which the rails are enabled. The delay times from one strobe to the next are programmable in a range from 1 ms to 10 ms.

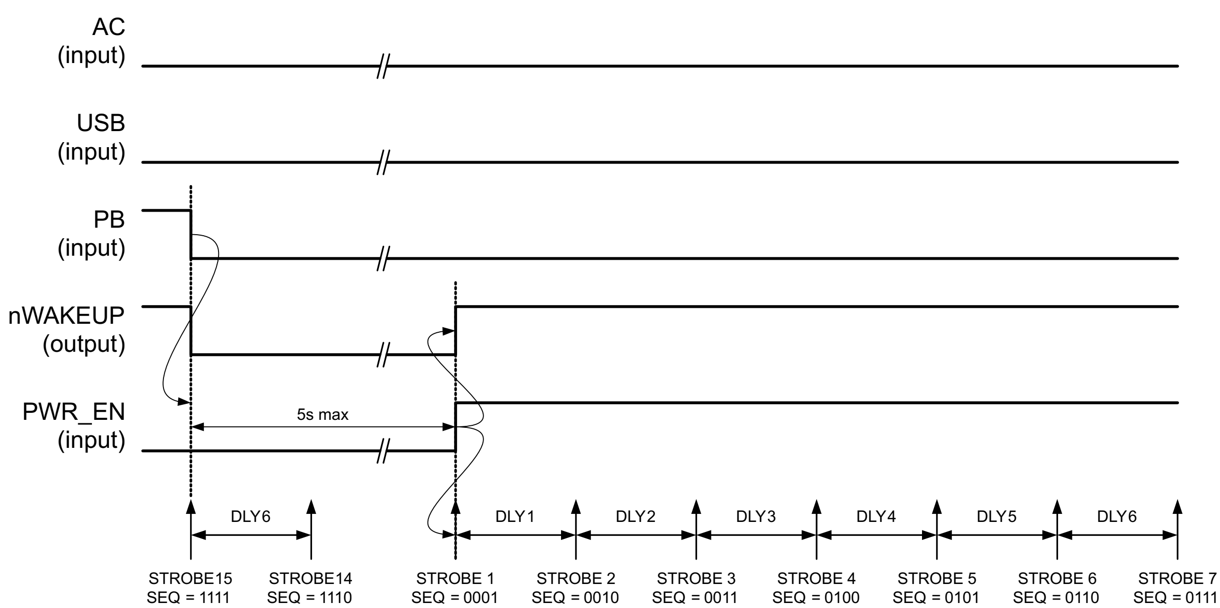
NOTE

Although the user can modify the power-up and power-down sequence through the SEQx registers, those registers are reset to default values when the device goes to the SLEEP, OFF, or RESET state. In practice, this situation means that the power-up sequence is fixed and a custom power-down sequence must be written each time the device is powered up.

Custom power-up and power-down sequences can be tested and verified in the ACTIVE state (PWR_EN pin pulled high) by using I^2C to toggle the SEQUP and SEQDWN bits. Permanent changes to the default power-up sequence timing require custom programming at the TI factory.

8.3.1.1 Power-Up Sequencing

When the power-up sequence is initiated, STROBE1 occurs and any rail assigned to this strobe is enabled. After a delay time of DLY1, STROBE2 occurs and the rail assigned to this strobe is powered up. The sequence continues until all strobes have occurred and all DLYx times have been executed.

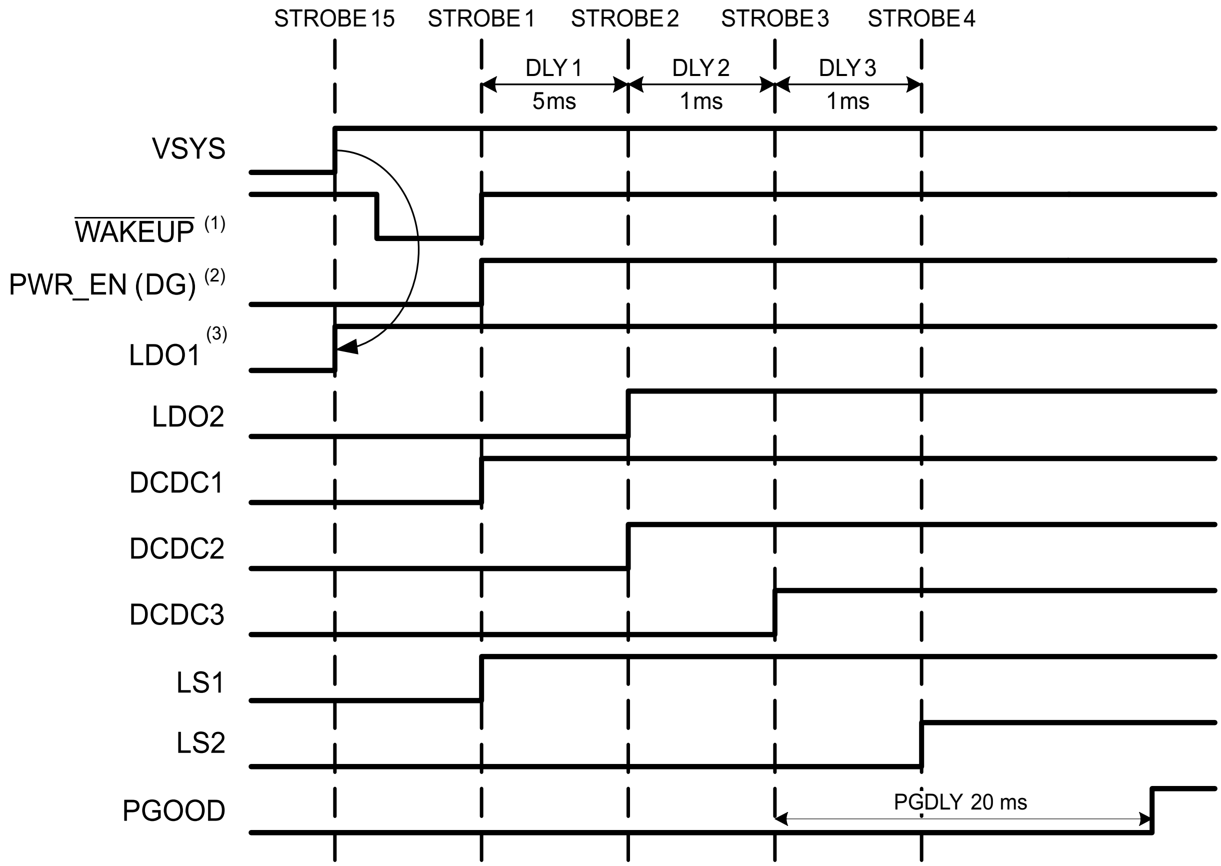


The power-up sequence is defined by strobes and delay times. In this example, push-button low is the power-up event.

Figure 3. Power-Up Sequence

The default power-up sequence can be changed by writing to the SEQ1 through SEQ6 registers. Strobes are assigned to rails by writing to the SEQ1 through SEQ4 registers. A rail can be assigned to only one strobe but multiple rails can be assigned to the same strobe. Delays between strobes are defined in the SEQ5 and SEQ6 registers.

Feature Description (continued)



For default power-up sequences of the other TPS65217x family members, refer to the *Powering the AM335x with the TPS65217x* user's guide.

Figure 4. Default Power-Up Sequence for the TPS65217A Device

The power-up sequence is executed if the following events occurs:

From the OFF state (going to the ACTIVE state):

- Push-button is pressed (falling edge on PB_IN) OR
- USB voltage is asserted (rising edge on USB) OR
- The AC adaptor is inserted (rising edge on the AC pin)

The PWR_EN pin is level-sensitive (opposed to edge-sensitive), and the pin can be asserted before or after the previously listed power-up events. However, the PWR_EN pin must be asserted within 5 s of the power-up event; otherwise, the power-down sequence is triggered and the device goes to the OFF state. If a fault occurs because the device is in undervoltage lockout (UVLO) or requires overtemperature shutdown (OTS), the device goes to the OFF state.

From the SLEEP state (going to the ACTIVE state):

- The push-button is pressed (falling edge on the PB_IN pin) OR
- The USB voltage is asserted (rising edge on the USB pin) OR
- The AC adaptor is inserted (rising edge on the AC pin) OR
- The PWR_EN pin is asserted (pulled high).

In the SLEEP state, the power-up sequence can be triggered by asserting the PWR_EN pin only, and the push-button press or AC and USB assertion are not required. If a fault occurs because the device is in undervoltage lockout (UVLO) or requires overtemperature shutdown (OTS), the device goes to the OFF state.

In the ACTIVE state:

Feature Description (continued)

The sequencer can be triggered any time by setting the SEQUP bit in the SEQ6 register high. The SEQUP bit is automatically cleared after the sequencer is complete.

Rails that are not assigned to a strobe (the SEQ bit set to 0000b) are not affected by power-up and power-down sequencing and stay in their current ON or OFF state regardless of the sequencer. Any rail can be enabled or disabled at any time by setting the corresponding enable bit in the ENABLE register with the only exception that the ENABLE register cannot be accessed while the sequencer is active. Enable bits always reflect the current enable state of the rail, that is, the sequencer sets or resets the enable bits for the rails under its control. Also, whenever faults occur which shut-down the power-rails, the corresponding enable bits are reset.

8.3.1.2 Power-Down Sequencing

By default, power-down sequencing follows the reverse power-up sequence. When the power-down sequence is triggered, STROBE7 occurs first, and any rail assigned to STROBE7 is shut down. After a delay time of DLY6, STROBE6 occurs, and any rail assigned to STROBE6 is shut down. The sequence continues until all strobes have occurred and all DLYx times have been executed.

In some applications, all rails may be required to shut down at the same time with no delay between rails. Set the INSTDWN bit in the SEQ6 register to bypass all delay times and shut-down all rails at the same time when the power-down sequence is triggered.

A power-down sequence is executed if one of the following events occurs:

- The SEQDWN bit is set.
- The PWR_EN pin is pulled low.
- The push-button is pressed for more than 8 s.
- The nRESET pin is pulled low.
- A fault occurs in the device (either an OTS, UVLO, or PGOOD failure).
- The PWR_EN pin is not asserted (pulled high) within 5 s of a power-up event and the OFF bit is set to 1b.

When the device goes from the ACTIVE to the OFF state, any rail not controlled by the sequencer is shut down after the power-down sequencer is complete. When the device goes from the ACTIVE to the SLEEP state, any rail not controlled by the power-down sequencer stays in its present state.

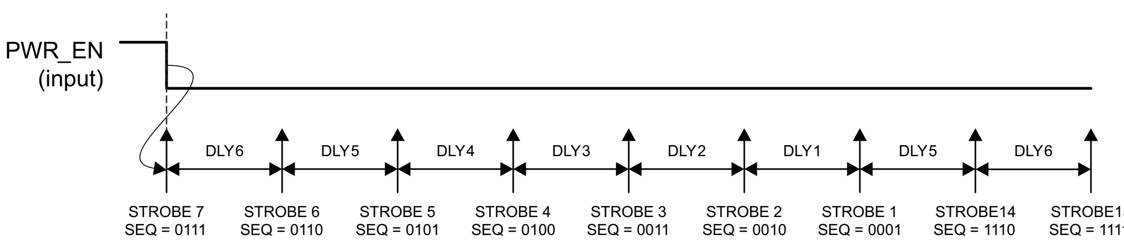
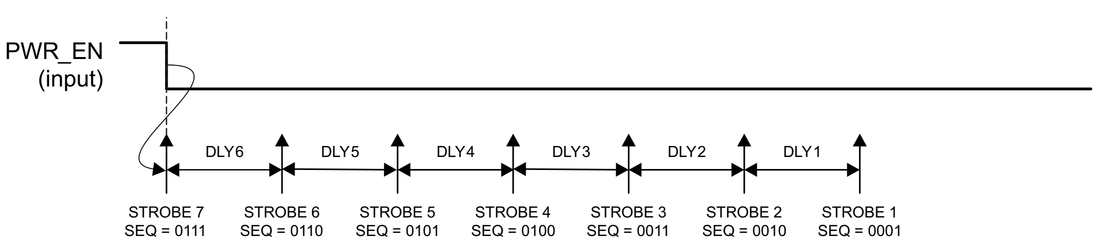


Figure 5. Power-Down Sequence from ON State to OFF State (All Rails Turned OFF)



STROBE14 and STROBE15 are omitted to let the LDO1 or LDO2 regulators stay ON.

Figure 6. Power-Down Sequence from ON State to SLEEP State

Feature Description (continued)

8.3.1.3 Special Strobes (STROBE 14 and 15)

STROBE 14 and STROBE 15 are not assigned to the sequencer but used to control rails that are *always-on*, that is, are powered up as soon as the device goes out of the OFF state and stay ON in the SLEEP state. STROBE 14 and STROBE 15 options are available only for the LDO1 and LDO2 rails and not for any of the other rails.

STROBE 15 occurs as soon as the push-button is pressed or the USB or AC adaptor is connected to the device. STROBE 14 occurs after a delay time of DLY6. The LDO1 and LDO2 rails can be assigned to either strobe but by default only LDO1 is assigned to special STROBE 15 (default settings must be programmed by TI at the factory because all registers are reset during transitions to the OFF or SLEEP states).

When a power-down sequence is initiated, STROBE 15 and STROBE 14 occur only if the OFF bit is set. Otherwise both strobes are omitted, and the LDO1 and LDO2 rails keep their state.

8.3.2 Power Good

The power-good signals are used to indicate if an output rail is in regulation or at fault. Internally, all power-good signals of the enabled rails are monitored at all times and if any of the signals goes low, a fault is declared. All power-good signals are internally deglitched. When a fault occurs, all output rails are powered down and the device goes to the OFF state.

The TPS65217x device has two power-good output pins: one is dedicated to the LDO1 and LDO2 rails (LDO_PGOOD) and one for all other rails (PGOOD). The power-good signals that are indicated by the PGOOD pin are programmable. The following rules apply to both output pins:

- The power-up default state for the PGOOD pin and the LDO_PGOOD pin is low. When all rails are disabled, the PGOOD and LDO_PGOOD pins are both low.
- Only enabled rails are monitored. Disabled rails are ignored.
- Power-good monitoring of a particular rail starts 5 ms after the rail has been enabled. The power-good signal is continuously monitored after the 5-ms deglitch time expires.
- The signals controlling the PGOOD and LDO_PGOOD pins are delayed by the PGDLY (20 ms default) after the sequencer is done.
- If a fault occurs on an enabled rail (such as a shorted output, OTS condition, or UVLO condition), the PGOOD pin, LDO_PGOOD pin, or both pins are pulled low, and all rails are shut down.
- If the user disables a rail (either manually or through the sequencer), this action has no effect on the PGOOD or LDO_PGOOD pin.
- If the user disables all rails (either manually or through the sequencer), the PGOOD pin, LDO_PGOOD pin, or both pins are pulled low.

8.3.2.1 LDO1, LDO2 Power-Good (LDO_PGOOD)

The LDO_PGOOD pin is a push-pull output that is driven to a high level when either the LDO1 regulator or the LDO2 regulator is enabled and in regulation. The LDO_PGOOD pin is pulled low when both LDO regulators are disabled or one is enabled but has encountered a fault. A typical fault is an output short or overcurrent condition. In normal operation, the LDO_PGOOD pin is high in the ACTIVE and SLEEP states and low in the RESET and OFF states.

8.3.2.2 Primary Power-Good (PGOOD)

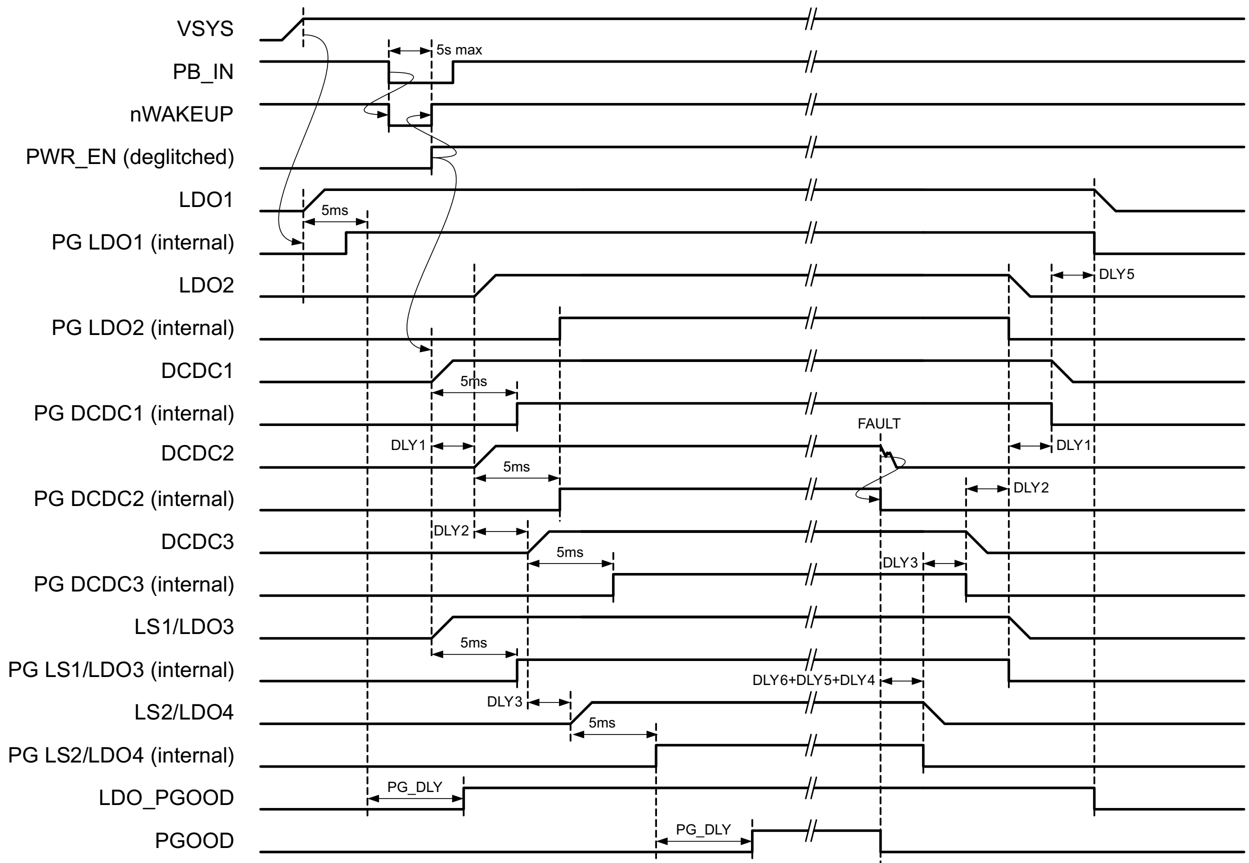
The primary PGOOD pin has similar functionality to the LDO_PGOOD pin except that PGOOD monitors the DCDC1, DCDC2, and DCDC3 converters, and the LDO3 and LDO4 outputs configured as LDO regulators. The user can also choose to monitor the LDO1 and LDO2 regulators by setting the LDO1PGM and LDO2PGM mask bits low in the DEFPG register. By default, the power-good signal of the LDO1 and LDO2 regulators does not affect the PGOOD pin (mask bits are set to 1b by default). In normal operation the PGOOD pin is high in the ACTIVE state but low in the SLEEP, RESET, and OFF states.

In the SLEEP state and the WAIT PWR_EN state, the PGOOD pin is forced low. The PGOOD pin is set high after the device goes to the ACTIVE state, the power sequencer is complete, and the PGDLY time is expired.

Feature Description (continued)

8.3.2.3 Load Switch PGOOD

When either LS1 or LS2 is configured as a load switch, the device ignores the respective power-good signal. An overcurrent or short condition present on the LS1 or LS2 load switch does not affect the PGOOD pin or any of the power rails unless the power dissipation leads to thermal shutdown.



This figure also shows the power-down sequence for the case of a short on the DCDC2 output.

Figure 7. Default Power-Up Sequence

8.3.3 Push-Button Monitor (PB_IN)

The TPS65217x device has an active-low PB_IN input pin that is typically connected to ground through a push-button switch. The PB_IN input has a 50-ms deglitch time and an internal pull-up resistor that is connected to an always-on supply. The always-on supply is an unregulated internal power rail that is functionally equivalent to the power path. The source of the always-on supply is the same as the source of the SYS pin. The push-button monitor has two functions. The first is to power-up the device from the OFF or SLEEP state when a falling edge is detected on the PB_IN pin. The second is to power cycle the device when the PB_IN pin is held low for more than 8 s.

For a description of each function, see the *Device Functional Modes* section. A change in push-button status (the PB_IN pin goes from high to low or low to high) is signaled to the host through the PBI interrupt bit in the INT register. The current status of the interrupt can be checked by reading the PB status bit in the STATUS register. Figure 8 shows a timing diagram for the push-button monitor.

Feature Description (continued)

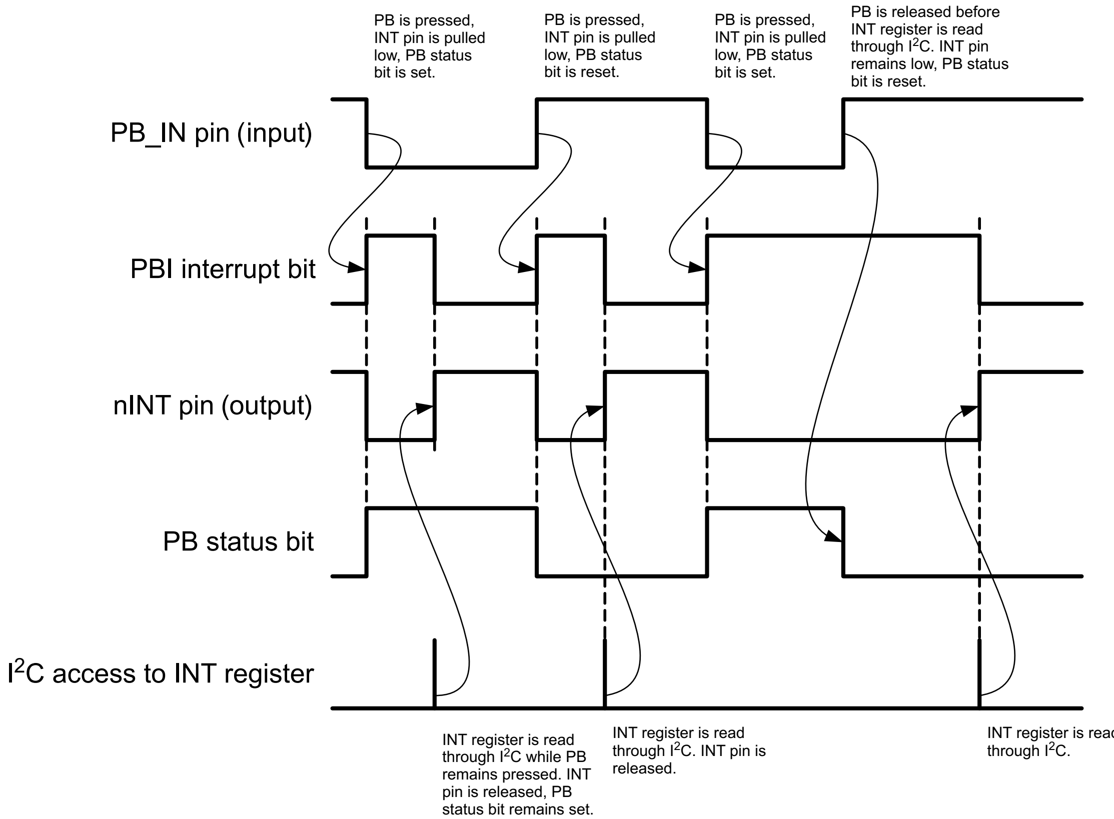


Figure 8. Timing Diagram of the Push-Button Monitor Circuit

8.3.4 nWAKEUP Pin (nWAKEUP)

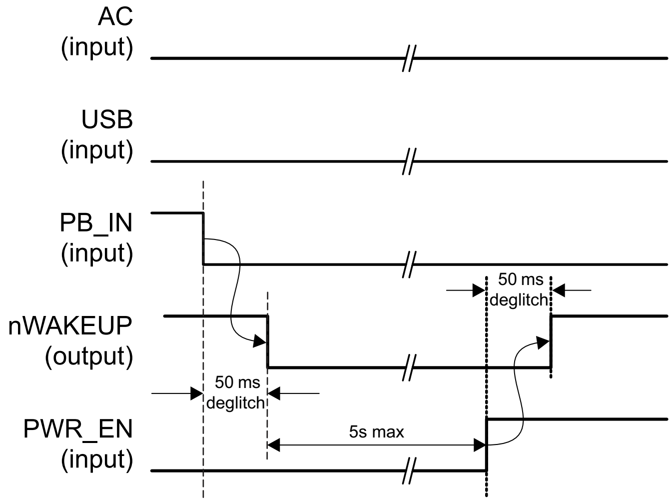
The nWAKEUP pin is an open-drain, active-low output that is used to signal a wakeup event to the system host. This pin is pulled low whenever the device is in the OFF or SLEEP state and detects a wakeup event as described in the *Device Functional Modes* section. The nWAKEUP pin is delayed for 50 ms over the power-up event and stays low for 50 ms after the PWR_EN pin has been asserted. If the PWR_EN pin is not asserted within 5 s of the power-up event, the device shuts down and goes to the OFF state. In the ACTIVE state, the nWAKEUP pin is always high. Figure 9 shows the timing diagram for the nWAKEUP pin.

8.3.5 Power Enable Pin (PWR_EN)

The PWR_EN pin is used to keep the device in the ACTIVE mode after it detects a wakeup event as described in the *Device Functional Modes* section. If the PWR_EN pin is not asserted within 5 s of the nWAKEUP pin being pulled low, the device shuts down the power and goes to either the OFF or SLEEP state, depending on the OFF bit in the STATUS register. The PWR_EN pin is level-sensitive, meaning that PWR_EN may be pulled high before the wake-up event.

The PWR_EN pin can also be used to toggle between the ACTIVE and SLEEP states. For more information, see *SLEEP* in the *PMIC States* section.

Feature Description (continued)



In the example shown, the wakeup event is a falling edge on the PB_IN.

(1) If the PWR_EN pin is not asserted within 5 s of the WAKEUP pin being pulled low, the device goes to the OFF or SLEEP state

Figure 9. nWAKEUP Timing Diagram

8.3.6 Reset Pin (nRESET)

When the nRESET pin is pulled low, all power rails, including LDO1 and LDO2, are powered down, and the default register settings are restored. The device stays powered down as long as the nRESET pin is held low, but for a minimum of 1 s. After the nRESET pin is pulled high, the device goes to the ACTIVE state, and the default power-up sequence executes. For more information, see *RESET* in the *PMIC States* section.

8.3.7 Interrupt Pin (nINT)

The interrupt pin is used to signal any event or fault condition to the host processor. Whenever a fault or event occurs in the device, the corresponding interrupt bit is set in the INT register, and the open-drain output is pulled low. The nINT pin is released (Hi-Z) and the fault bits are cleared when the INT register is read by the host. However, if a failure continues, the corresponding INT bit stays set and the nINT pin is pulled low again after a maximum of 32 µs.

Interrupt events include pushing or releasing the push-button and a change in the USB or AC voltage status.

The mask bits in the INT register are used to mask events from generating interrupts. The mask settings affect the nINT pin only and have no impact on the protection and monitor circuits themselves.

NOTE

Continuous event conditions such as an ISINK-enabled shutdown can cause the nINT pin to be pulled low for an extended period of time, which can keep the host in a loop trying to resolve the interrupt. If this behavior is not desired, set the corresponding mask bit after receiving the interrupt and poll the INT register to determine when the event condition resolves and the corresponding interrupt bit is cleared. Then the interrupt that caused the nINT pin to stay low can be un-masked.

8.3.8 Analog Multiplexer

The TPS65217x device has an analog multiplexer (mux) that provides access to critical system voltages. The voltages that can be measured by an ADC at the MUX_OUT pin are as follows:

- Battery voltage (VBAT)
- System voltage (VSYS)

Feature Description (continued)

- Temperature-sense voltage (VTS), and
- VICHARGE, a voltage proportional to the charging current, and
- MUX_IN, an external input pin to monitor an additional system voltage

In addition, one external input is available. The VBAT and VSYS voltages are divided by three (for example, MUX_OUT = VBAT / 3) to be compatible with the input-voltage range of the ADC that resides on the system-host side. The output of the MUX is buffered and can drive a maximum of 1-mA load current.

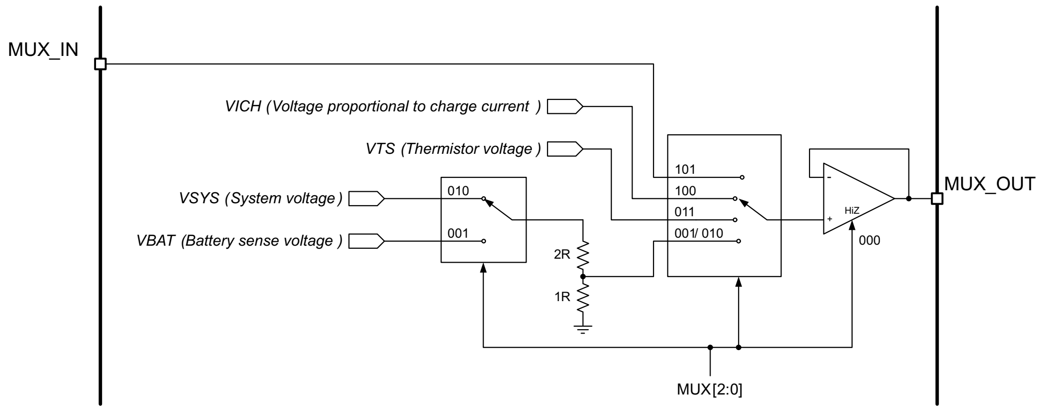


Figure 10. Analog Multiplexer

8.3.9 Battery Charger and Power Path

The TPS65217x device has a linear charger for Li+ batteries and a triple system-power path targeted at space-limited portable applications. The power path lets simultaneous and independent charging of the battery and powering of the system. This feature enables the system to run with a defective or absent battery pack and lets instant system turnon even with a totally discharged battery. The input power source for charging the battery and running the system can be either an AC adapter or a USB port. The power path prioritizes the AC input over the USB input, and both over the battery input, to decrease the number of charge and discharge cycles on the battery. Charging current is automatically decreased when the system load increases to the point where the AC or USB power supply reach the maximum allowable current. If the AC or USB power supply cannot provide enough current to the system, the battery supplies the additional current required and the battery will discharge until the system load is reduced. Figure 11 shows a block diagram of the power path. Figure 12 shows an example of the power path management function.

Feature Description (continued)

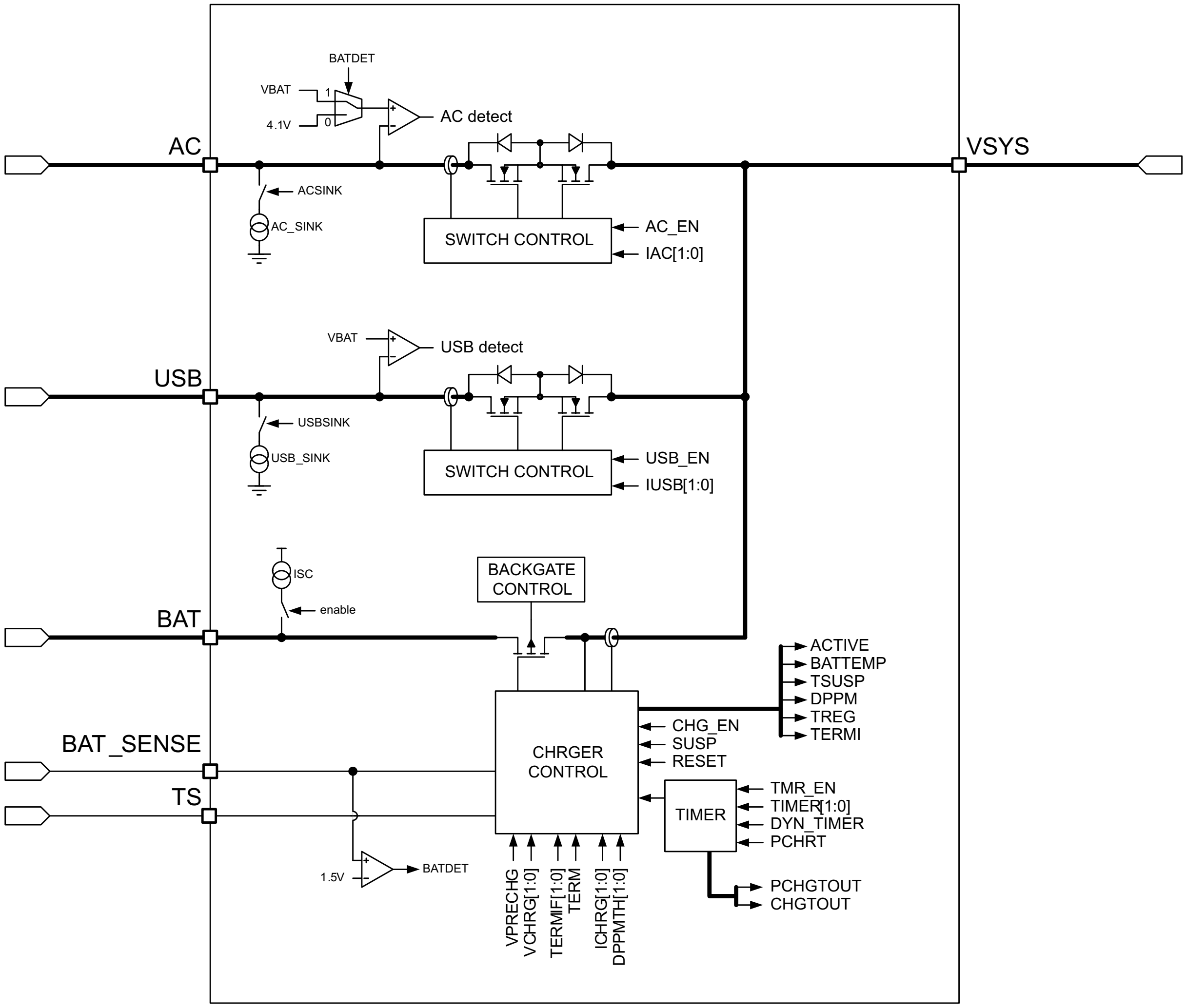
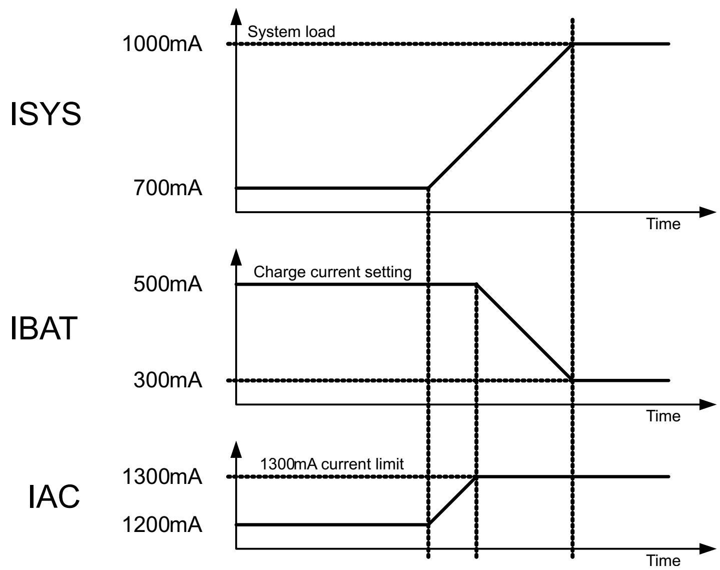


Figure 11. Block Diagram of the Power Path and Battery Charger

Feature Description (continued)



In this example, the AC input current limit is set to 1300 mA, battery charge current is 500 mA, and system load is 700 mA. As the system load increases to 1000 mA, the battery charging current is decreased to 300 mA to keep the AC input current of 1300 mA.

Figure 12. Power Path Management

The detection thresholds for AC and USB inputs are a function of the battery voltage, and three basic use cases must be considered: shorted or absent battery, dead battery, and good battery.

8.3.9.1 Shorted or Absent Battery (V_{BAT} < 1.5 V)

The AC or USB inputs are valid and the device powers up if the AC or USB input voltage increases above 4.3 V. After powering up, the input voltage can decrease to a value of V_{UVLO} + V_{OFFSET} (for example, 3.3 V + 200 mV) before the device powers down.

The AC input is prioritized over the USB input; that is, if both inputs are valid, current is pulled from the AC input and not the USB input. If both AC and USB supplies are available, the power-path switches to the USB input if AC voltage decreases to less than 4.1 V (fixed threshold).

NOTE

The rise time of the AC and USB input voltage must be less than 50 ms for the detection circuits to operate correctly. If the rise time is longer than 50 ms, the device may fail to power up.

The linear charger periodically applies a 10-mA current source to the BAT pin to check for the presence of a battery. This applied current causes the BAT pin to float up to more than 3 V, which may interfere with AC removal detection and prevent switching from the AC to the USB input. For this reason, TI does not recommend using both the AC and USB inputs when the battery is absent.

8.3.9.2 Dead Battery (1.5 V < V_{BAT} < V_{UVLO})

Functionality for this case is the same as for the shorted battery case. The only difference is that after the AC input is selected as the input, the power-path does not switch back to the USB input as AC input voltage decreases to less than 4.1 V.

Feature Description (continued)

8.3.9.3 Good Battery ($V_{BAT} > V_{UVLO}$)

The AC and USB supplies are detected when the input is 190 mV above the battery voltage, and are considered absent when the voltage difference to the battery is less than 125 mV. This feature makes sure that the AC and USB supplies are used whenever possible to save battery life. The USB and AC inputs are both current-limited and controlled through the PPATH register.

In case AC or USB is not present or is blocked by the power path control logic (for example, in the OFF state), the battery voltage always supplies the system (SYS pin).

8.3.9.4 AC and USB Input Discharge

The AC and USB inputs have 90-µA internal current sinks which are used to discharge the input pins to avoid false detection of an input source. The AC sink is enabled when the USB input is a valid supply and the AC voltage (V_{AC}) is less than the detection threshold. Likewise, the USB sink is enabled when the AC input is a valid supply and the USB voltage (V_{USB}) is less than the detection limit. Both current sinks can be forced OFF by setting the ACSINK and USBSINK bits to 11b. Both bits are located in the PPATH register (address 0x01).

NOTE

Setting the ACSINK or USBSINK bit to 01b and 10b is not recommended as these settings may cause unexpected enabling and disabling of the current sinks.

8.3.10 Battery Charging

When the charger is enabled (the CH_EN bit is set to 1b), it first checks for a short circuit on the BAT pin by sourcing a small current and monitoring the BAT voltage. If the voltage on the BAT pin increases to more than the BAT pin short-circuit detection threshold ($V_{BAT(SC)}$), a battery is present and charging can start. The battery is charged in three phases: precharge, constant-current fast charge (current regulation), and constant-voltage (CV) charge (voltage regulation). In all charge phases, an internal control loop monitors the device junction temperature and decreases the charge current if an internal temperature threshold is exceeded. Figure 13 shows a typical charging profile. Figure 14 shows a modified charging profile.

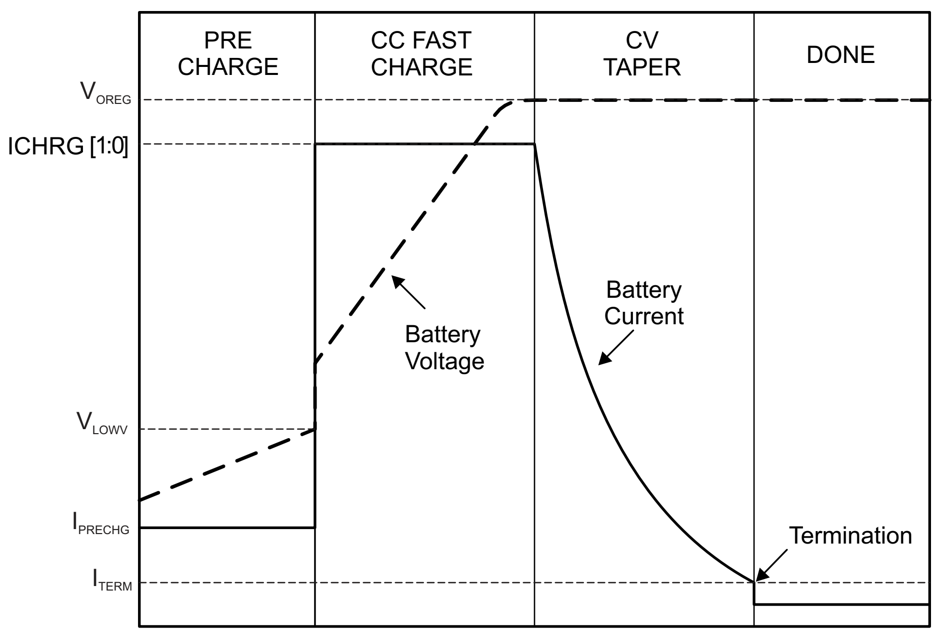


Figure 13. Charging Profiles—Typical Charge Current Profile With Termination Enabled

Feature Description (continued)

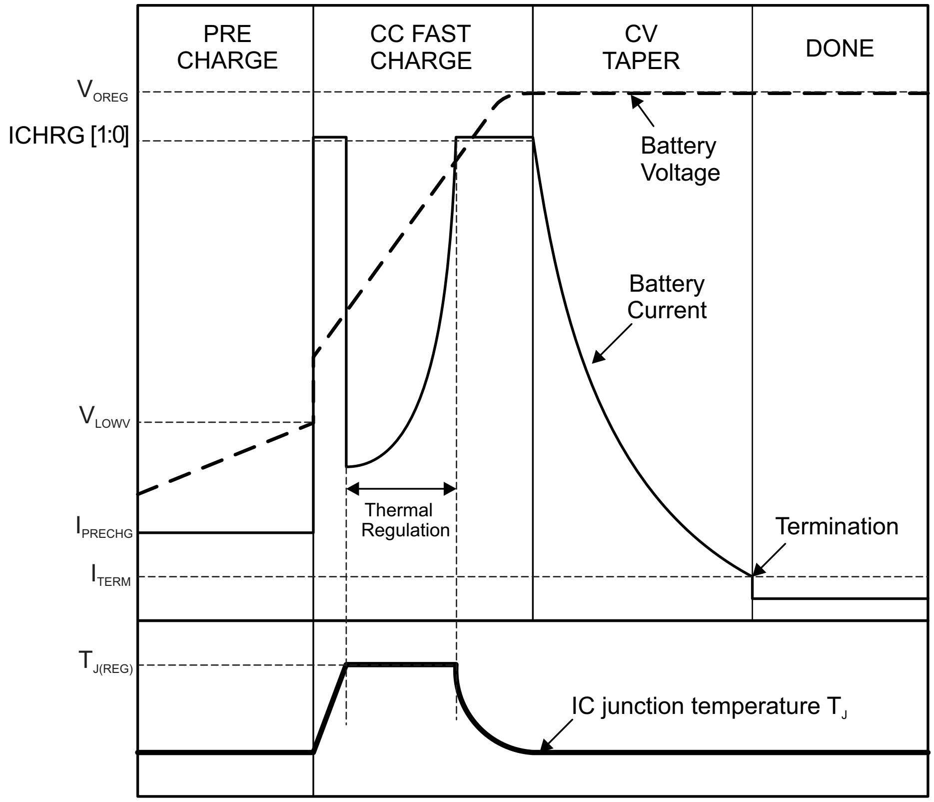


Figure 14. Charging Profiles—Modified Charging Profile With Thermal Regulation Loop Active and Termination Enabled

In the precharge phase, the battery is charged at the precharge current (I_{PRECHG}), which is typically 10% of the fast-charge current rate. The battery voltage starts rising. After the battery voltage crosses the precharge-to-fast-charge transition threshold (V_{LOWV}), the battery is charged at the fast charge current (I_{CHG}). The battery voltage continues to rise. When the battery voltage reaches the battery charger voltage (V_{OREG}), the battery is held at a constant value of V_{OREG}. The battery current now decreases as the battery approaches full charge. When the battery current reaches the charge current for termination detection threshold (I_{TERM}), the TERMI bit in the CHGCONFIG0 register is set to 1b. To avoid false termination when the charger goes to either the dynamic power path management (DPPM) loop or thermal loop, termination is disabled when either loop is active.

The charge current cannot exceed the input current limit of the power path minus the load current on the SYS pin because the power-path manager decreases the charge current to support the system load if the input current limit is exceeded. Whenever the nominal charge current is decreased by action of the power-path manger, the DPPM loop, or the thermal loop, the safety timer is clocked with half the nominal frequency to extend the charging time by a factor of 2.

8.3.11 Precharge

The precharge current is preset to a factor of 10% of the fast-charge current (ICHRG[1:0]) and cannot be changed by the user.

8.3.12 Charge Termination

When the charging current decreases to less than the termination current threshold, the charger is turned off. The value of the termination current threshold can be set in the CHGCONFIG3 register using the TERMIF[1:0] bits. The termination current has a default setting of 7.5% of the ICHRG[1:0] setting.

Feature Description (continued)

Charge termination is enabled by default and can be disabled by setting the TERM bit of the CHGCONFIG1 register to 1b. When termination is disabled, the device goes through the precharge, fast-charge, and CV phases, then stays in the CV phase. The charger behaves like an LDO regulator with an output voltage equal to the battery charger voltage (V_{OREG}) and can source current up to the fast charge current (I_{CHG}) or maximum input current ($I_{IN\text{-}MAX}$), whichever is less. Battery detection is not performed.

NOTE

The termination current threshold is not a tightly controlled parameter. Using the lowest setting (2.5% of the nominal charge current) is not recommended because the minimum termination current can be very close to 0. Any leakage on the battery side may cause the termination not to trigger and charging to time out eventually.

8.3.13 Battery Detection and Recharge

Whenever the battery voltage decreases to less than the recharge detection threshold (V_{RCH}), the sink current for battery detection ($I_{BAT(DET)}$) is pulled from the battery for the battery detection time (t_{DET}) to determine if the battery was removed. The voltage on the BAT pin staying above V_{LOWV} voltage indicates that the battery is still connected. If the charger is enabled (the CH_EN bit set to 1b), a new battery charging cycle starts.

When the BAT pin voltage is decreasing and less than the V_{LOWV} voltage in the battery detection test, this indicates that the battery was removed. The device then checks for battery insertion by turning on the charging path and sources the I_{PRECHG} current out of the BAT pin for the t_{DET} time. Failure of the voltage to increase to greater than the V_{RCH} voltage indicates that a battery has been inserted, and a new charge cycle can start. If, however, the voltage is already greater than the V_{RCH} voltage, a fully charged battery was possibly inserted. To check for this case, the $I_{BAT(DET)}$ current is pulled from the battery for the t_{DET} time and if the voltage falls below the V_{LOWV} voltage, no battery is present. The battery detection cycle continues until the device detects a battery or the charger is disabled.

When the battery is removed from the system, the charger also flags a BATTEMP error which indicates that the TS input is not connected to a thermistor.

8.3.14 Safety Timer

The TPS65217x device hosts an internal safety timer for the precharge and fast-charge phases to help prevent potential damage to either the battery or the system. The default fast-charge time can be changed in the CHGCONFIG1 register and the precharge time can be changed in the CHGCONFIG3 register. The timer functions can be disabled by resetting the TMR_EN bit of the CHGCONFIG1 register to 0b. Both timers are disabled when the charge termination is disabled (the TERM bit is cleared to 0b).

8.3.14.1 Dynamic Timer Function

Under some circumstances, the charger current is decreased to ensure support when changes in the system load or junction temperature occur. Two events can decrease the charging current. The first event is an increase in the system load current, which causes the DPPM loop to decrease the available charging current. The second event is when the junction temperature exceeds the temperature regulation limit ($T_{J(REG)}$), which causes the device to go to thermal regulation.

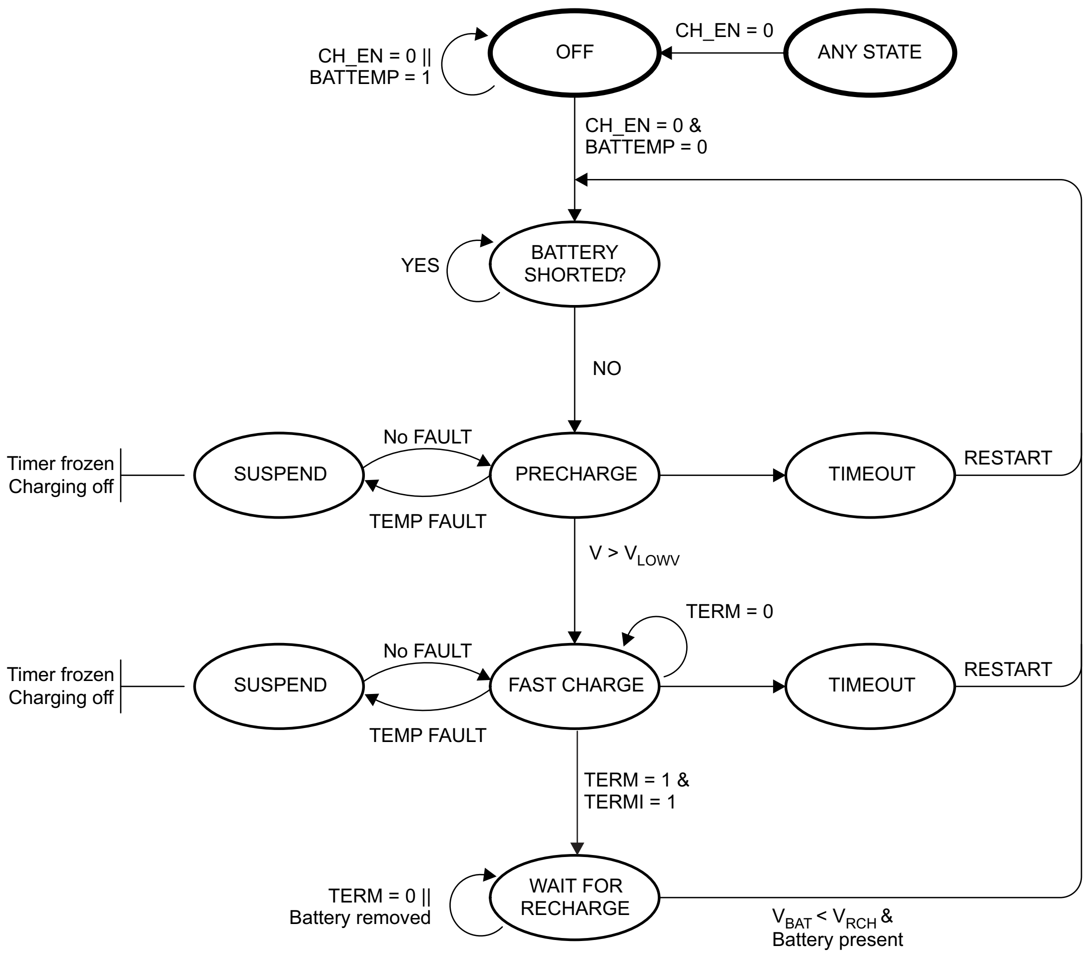
In each of these events, the timer is clocked with half-frequency to extend the charger time by a factor of 2, and charger termination is disabled. Normal operation starts again after the device junction temperature decreases to less than ($T_{J(REG)}$) and the system load decreases to a level where enough current is available to charge the battery at the desired charge rate. This feature is enabled by default and can be disabled by resetting the DYNTMR bit in the CHGCONFIG2 register to 0b. Figure 14 shows a modified charge cycle with the thermal loop active.

8.3.14.2 Timer Fault

A timer fault occurs if the battery voltage does not exceed the V_{LOWV} voltage in the t_{PRECHG} time during precharging. A timer fault also occurs if the battery current does not reach the I_{TERM} current in fast charge before the safety timer expires. Fast-charge time is measured from the start of the fast-charge cycle.

Feature Description (continued)

The fault status is indicated by the CHTOUT and PCHTOUT bits in the CHGCONFIG0 register. Time-out faults are cleared and a new charge cycle is started when either the USB or AC supply is connected (rising edge of V_{USB} or V_{AC}), the charger RESET bit is set to 1b in the CHGCONFIG1 register, or the battery voltage decreases to less than the recharge threshold (V_{RCH}).



(1) TEMP FAULT = Battery HOT || Battery cold || Thermal shutdown

(2) RESTART = V_{USB} (↑) || V_{AC} (↑) || Charger RESET bit (↑) || $V_{BAT} < V_{RCH}$

Figure 15. State Diagram of Battery Charger

8.3.15 Battery-Pack Temperature Monitoring

The TS pin of the TPS65217x device connects to the NTC resistor in the battery pack. During charging, if the NTC resistance indicates that battery operation is less than or greater than the limits of normal operation, charging is suspended and the safety timer value is paused and held at the present value. When the battery pack temperature returns to within the limits of normal operation, charging resumes and the safety time is started again without resetting.

By default, the device supports a 10-kΩ NTC resistor with a B-value of 3480. The NTC resistor is biased through a 7.35-kΩ internal resistor connected to the BYPASS rail (2.25 V) and requires an external 75-kΩ resistor parallel to the NTC resistor to linearize the temperature response curve.

The TPS65217x device supports two different temperature ranges for charging: 0°C to 45°C and 0°C to 60°C. The temperature range is selected through the TRANGE bit in the CHCONFIG3 register.

Feature Description (continued)

NOTE

The device can be configured to support a 100-kΩ NTC resistor (with a B-value of 3960) by setting the NTC_TYPE bit to 1b in the CHGCONFIG1 register. However, TI does not recommended this real-time manual configuration. In the SLEEP state, the charger continues charging the battery, but all register values are reset to default values, in which case the charger gets the wrong temperature information. If 100-kΩ NTC resistor support is required, custom programming during production at the TI factory is required.

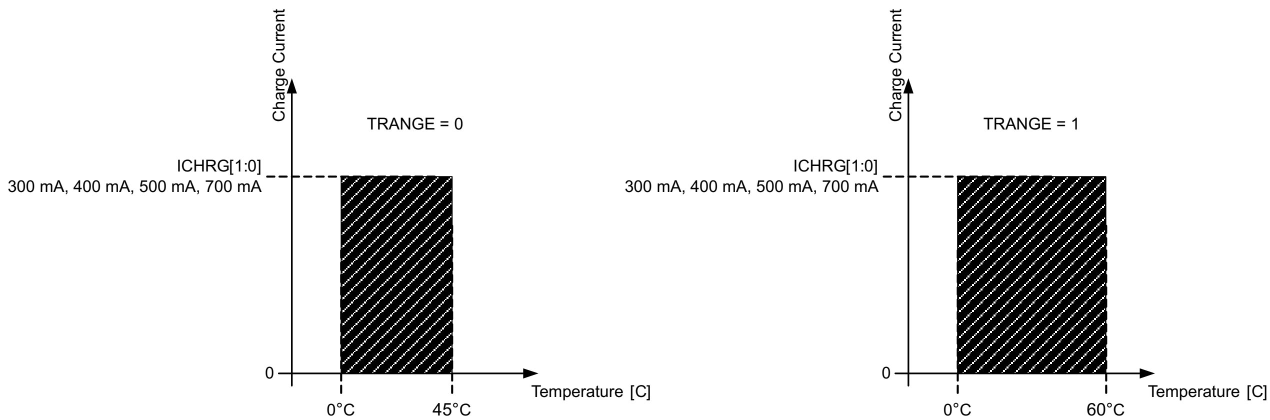


Figure 16. Charge Current as a Function of Battery Temperature

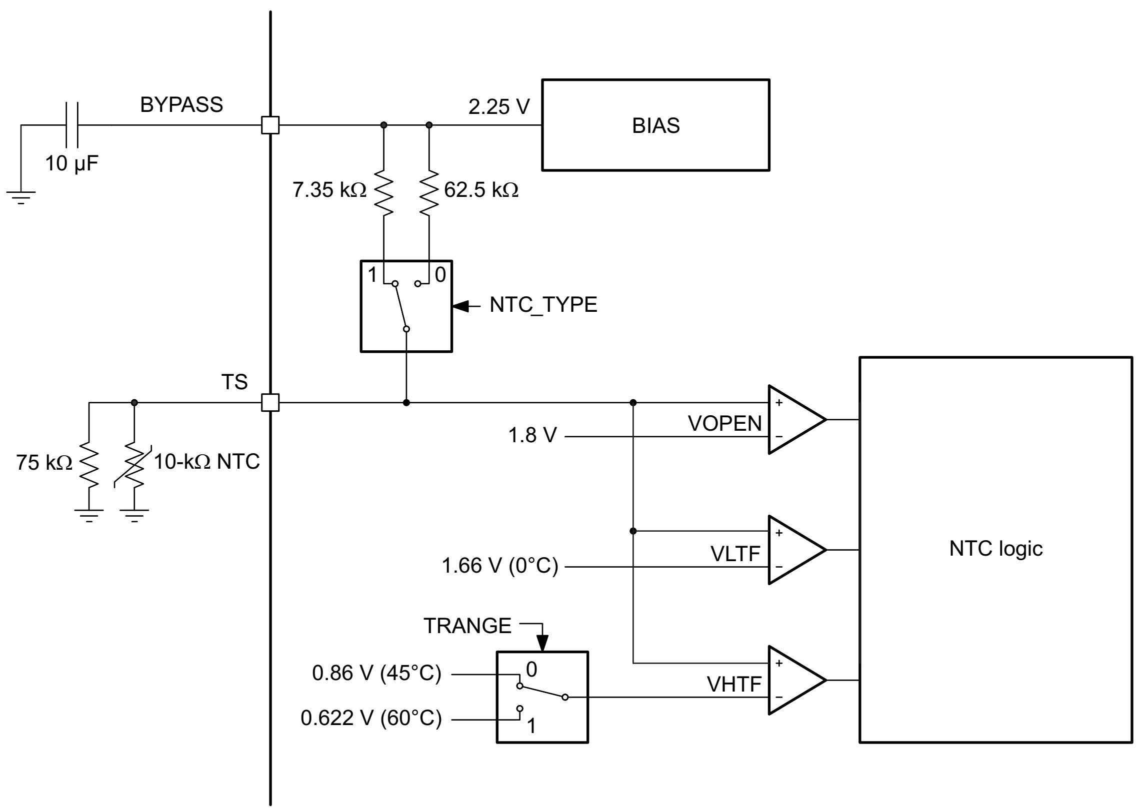


Figure 17. NTC Bias Circuit

Feature Description (continued)

8.3.16 DC/DC Converters

8.3.16.1 Operation

The TPS65217x step-down converters typically operate with 2.25-MHz fixed-frequency pulse-width modulation (PWM) at moderate-to-heavy load currents. At light load currents, the converter automatically goes to power-save mode and operates in pulse-frequency modulation (PFM).

During PWM operation, the converter uses a unique fast-response voltage-mode controller scheme with input-voltage feed-forward to achieve good line and load regulation. This controller scheme allows the use of small ceramic input and output capacitors. At the start of each clock cycle, the high-side MOSFET is turned on. The current flows from the input capacitor through the high-side MOSFET through the inductor to the output capacitor and load. During this phase, the current ramps up until the PWM comparator trips and the control logic turns off the switch. The current-limit comparator also turns off the switch in case the current limit of the high-side MOSFET switch is exceeded. After a dead time to prevent shoot-through current, the low-side MOSFET rectifier is turned on and the inductor current ramps down. The direction of current flow is now from the inductor to the output capacitor and to the load. The current returns back to the inductor through the low-side MOSFET rectifier.

The next cycle turns off the low-side MOSFET rectifier and turns on the on the high-side MOSFET.

The DC/DC converters operate in synchronization with each other, with converter 1 as the master. A 120° phase shift between DCDC1 and DCDC2 and between DCDC2 and DCDC3 decreases the combined input root mean square (RMS) current at the VIN_DCDCx pins. Therefore, smaller input capacitors can be used.

8.3.16.2 Output Voltage Setting

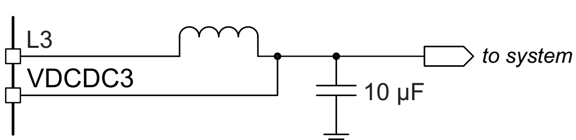
The setpoint of the output voltage for the DC/DC converters is determined in one of two different ways. The first way is as a fixed-voltage converter where the voltage is defined in the DEFDCDCx register. The second way is an external resistor network. Set the XADJx bit in the DEFDCDCx register and use Equation 1 to calculate the output voltage.

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_1}{R_2}\right)$$

where

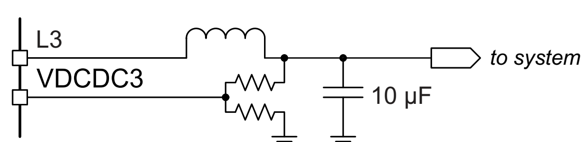
- V_{REF} is the feedback voltage of 0.6 V (1)

TI recommends selecting values to keep the combined resistance of the R1 and R2 resistors less than 1 MΩ. Shield the VDCDC1, VDCDC2, and VDCDC3 lines from switching nodes and from the L1, L2, and L3 inductors to prevent coupling of noise into the feedback pins.



DCDC1, DCDC2, and DCDC3 offer two methods to adjust the output voltage.

Figure 18. Example for DCDC3—Fixed-Voltage Options Programmable Through I²C (XADJ3 = 0b, default)



DCDC1, DCDC2, and DCDC3 offer two methods to adjust the output voltage.

Figure 19. Example for DCDC3—Voltage is Set by External Feedback Resistor Network (XADJ3 = 1b)

8.3.16.3 Power-Save Mode and Pulse-Frequency Modulation (PFM)

By default, all three DC/DC converters go to pulse-frequency modulation (PFM) mode at light loads, and fixed-frequency pulse-width modulation (PWM) mode at heavy loads. In some applications, forcing PWM operation even at light loads is required, which is done by setting the PFM_ENx bits in the DEFSLEW registers to 1b (default setting is 0b). In PFM mode, the converter skips switching cycles and operates with decreased frequency with a minimum quiescent current to keep high efficiency. The converter positions the output voltage typically 1% above the nominal output voltage. This voltage-positioning feature minimizes the voltage drop caused by a sudden load step.

The converters go from PWM to PFM mode after the inductor current in the low-side MOSFET switch becomes 0 A.

When the converters are in power-save mode, the output voltage is monitored with a PFM comparator. As the output voltage decreases to less than the PFM comparator threshold of V_{OUT} + 1%, the device starts a PFM current pulse. Starting the pulse is done by turning on the high-side MOSFET and ramping up the inductor current. Then the high-side MOSFET turns off and the low-side MOSFET switch turns on until the inductor current becomes 0 A again.

The converter effectively delivers a current to the output capacitor and the load. If the load is less than the delivered current, the output voltage rises. If the output voltage is equal to or greater than the PFM comparator threshold, the device stops switching and goes to a sleep mode with a typical 15-µA current consumption. In case the output voltage is still less than the PFM comparator threshold, additional PFM current pulses are generated until the PFM comparator threshold is reached. The converter starts switching again after the output voltage decreases to less than the PFM comparator threshold.

With one threshold comparator, the output-voltage ripple during PFM mode operation can be kept very small. The ripple voltage depends on the PFM comparator delay, the size of the output capacitor, and the inductor value. Increasing the value of the output capacitors, inductors, or both keeps the output ripple at a minimum.

The converter goes from PFM mode and goes to PWM mode the output current can no longer be supported in PFM mode or if the output voltage decreases to less than a second threshold, called the PFM comparator-low threshold. This PFM comparator-low threshold is set to a value of V_{OUT} – 1% and enables a fast transition from power-save mode to PWM mode during a load step.

The power-save mode can be disabled through the I^2C interface for each of the step-down converters, independently of each other. If the power-save mode is disabled, the converter then operates in fixed-PWM mode.

8.3.16.4 Dynamic Voltage Positioning

This feature decreases the voltage undershoots and overshoots at load steps from light to heavy load and from heavy to light load. This feature is active in power-save mode and provides more headroom for both the voltage drop at a load step and the voltage increase at a load removal. This improves load-transient behavior. At light loads in which the converter operates in PFM mode, the output voltage is regulated typically 1% greater than the nominal value (V_{OUT}). In case of a load transient from light load to heavy load, the output voltage drops until it reaches the low threshold of the PFM comparator set to –1% less than the nominal value, and goes to PWM mode. During a load removal from heavy load to light load, the voltage overshoot is low because of active regulation turning on the low-side MOSFET.

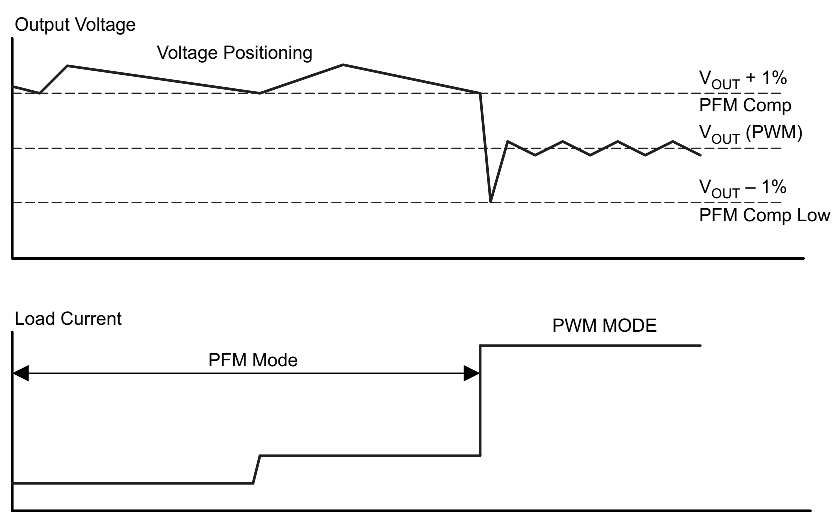


Figure 20. Dynamic Voltage Positioning in Power Save Mode

8.3.16.5 100% Duty-Cycle Low-Dropout Operation

The converter starts to go to the 100% duty-cycle mode after the input voltage (V_{IN}) comes close to the nominal output voltage. To keep the output voltage steady, the high-side MOSFET is turned on 100% for one or more cycles. As the V_{IN} voltage decreases further, the high-side MOSFET is turned on completely. In this case, the converter offers a low input-to-output voltage difference which is particularly useful in battery-powered applications to achieve longest operation time by taking full advantage of the whole battery voltage range.

Use Equation 2 to calculate the minimum input voltage to keep regulation ($V_{IN,MIN}$) which depends on the load current and output voltage.

$$V_{IN,MIN} = V_{OUT,MAX} + I_{OUT,MAX} \times \left(R_{DSON,MAX} + R_L\right)$$

where

- $V_{OUT,MAX}$ is the nominal output voltage plus the maximum output voltage tolerance.
- $I_{OUT,MAX}$ the maximum output current plus the inductor ripple current.
- $R_{DSON,MAX}$ is the maximum upper MOSFET switch R_{DSON} resistance.
- R_L is the DC resistance of the inductor. (2)

8.3.16.6 Short-Circuit Protection

High-side and low-side MOSFET switches are short-circuit protected. After the high-side MOSFET switch reaches its current limit, it is turned off and the low-side MOSFET switch is turned on. The high-side MOSFET switch can only turn on again after the current in the low-side MOSFET switch decreases to less than its current limit.

8.3.16.7 Soft Start

The three step-down converters in the TPS65217x device have an internal soft-start circuit that controls the ramp-up of the output voltage. The output voltage ramps up from 5% to 95% of its nominal value within 750 µs. This ramp up limits the inrush current in the converter during start-up and prevents possible input voltage drops when a battery or high-impedance power source is used. The soft-start circuit is enabled after the start-up time, t_{Start}, expires.

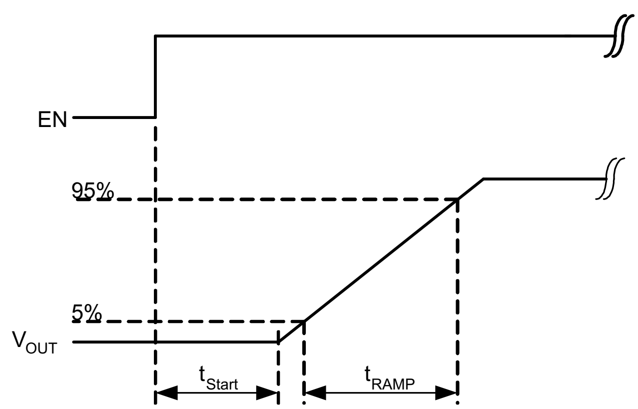


Figure 21. Output of the DC/DC Converters is Ramped Up Within 750 µs

8.3.17 Standby LDO Regulators (LDO1, LDO2)

The LDO1 and LDO2 regulators support up to 100 mA each, are internally current limited, and have a maximum dropout voltage of 200 mV at the rated output current. In SLEEP mode, however, the output current is limited to 1 mA each. When disabled, both outputs are discharged to ground through a 430-Ω resistor.

The LDO1 regulator supports an output voltage range from 1 V to 1.8 V, which is controlled through the DEFLDO1 register. The LDO2 regulator supports an output voltage range from 0.9 V to 1.5 V, and is controlled through the DEFLDO2 register. By default, the LDO1 regulator is enabled immediately after a power-up event as described in the *PMIC States* section and stays on in the SLEEP state to support system standby. Each LDO regulator has low standby current of less than 15 µA (typical).

The LDO2 regulator can be configured to track the output voltage of the DCDC3 converter (core voltage). When the TRACK bit is set to 1b in the DEFLDO2 register, the output is determined by the DCDC3[5:0] bits of the DEFDCDC3 register and the LDO2[5:0] bits of the DEFLDO2 register are ignored.

The LDO1 and LDO2 regulators can be controlled through STROBE 1 through 6, special STROBES 14 and 15, or through the corresponding enable bits in the ENABLE register. By default, the LDO1 regulator is controlled by STROBE 15, which keeps LDO1 on in the SLEEP state. The STROBE assignments can be changed by the user while the device is in the ACTIVE state, but all register settings are reset to the default values when the device goes to the SLEEP or OFF state. TI does not recommend real-time modification of the STROBE assignments of the LDO1 or LDO2 regulator. For permanent changes to the default STROBE assignments, custom programming during production at the TI factory is required.

8.3.18 Load Switches or LDO Regulators (LS1 or LDO3, LS2 or LDO4)

The TPS65217x device has two general-purpose load switches that can also be configured as LDOs. As LDOs, they support up to 200 mA (TPS65217B) or 400 mA (TPS65217C and TPS65217D) each, are internally current-limited, and have a maximum dropout voltage of 200 mV at rated output current. These two outputs are configured as LS1 and LS2 load switched in the TPS65217A variant of the device. The on-off state of the load switches (LS1 and LS2) or the LDO regulators (LDO3 and LDO4) is controlled either through the sequencer or the LS1_EN and LS2_EN bits of the ENABLE register. When disabled, both outputs are discharged to ground through a 375-Ω resistor.

Configured as load switches, LS1 and LS2 have a maximum impedance of 650 mΩ. Different from LDO operation, load switches can stay in current limit indefinitely without affecting the internal power-good signal or affecting the other rails.

NOTE

Excessive power dissipation in the switches may cause thermal shutdown of the device.

Load switch and LDO modes are controlled by the LS1LDO3 and LS2LDO4 bits of the DEFLS1 and DEFLS2 registers.

8.3.19 White LED Driver

The TPS65217x device has a boost converter and two current sinks capable of driving two strings containing up to 10 LEDs in each string (also known as a 2 × 10 matrix) LEDs at 25 mA or one string of up to 10 LEDs at 50 mA of current. Use Equation 3 to calculate the current of each current sink.

$$I_{LED} = 1048 \times \frac{1.24\ V}{R_{SET}} \tag{3}$$

Two different current levels can be programmed using two external R_{SET} resistors. Only one current setting is active at any given time, and both current sinks are always regulated to the same current. The active current setting is selected through the ISEL bit of the WLEDCTRL1 register.

An internal PWM signal and I^2C control support brightness and dimming. Both current sources are controlled together and cannot operate independently. By default, the PWM frequency is set to 200 Hz, but can be changed to 100 Hz, 500 Hz, or 1000 Hz. The PWM duty cycle can be adjusted from 1% (default) to 100% in 1% steps through the WLEDCTRL2 register.

When the ISINK_EN bit of WLEDCTRL1 register is set to 1b, both current sinks are enabled, and the boost output voltage at the FB_WLED pin is regulated to support the same sink current through each current sink. The boost output voltage, however, is internally limited to 39 V.

If only one WLED string is required, short the ISINK1 and ISINK2 pins together and connect them to the cathode of the diode string. In this case, the LED current two times the sink current. Figure 22 shows the basic schematic and internal circuitry of the WLED driver used to drive two strings. Figure 23 shows the basic schematic and internal circuitry of the WLED driver used to one string. Table 33 and Table 34 list the recommended inductors and output capacitors for the WLED boost converters.

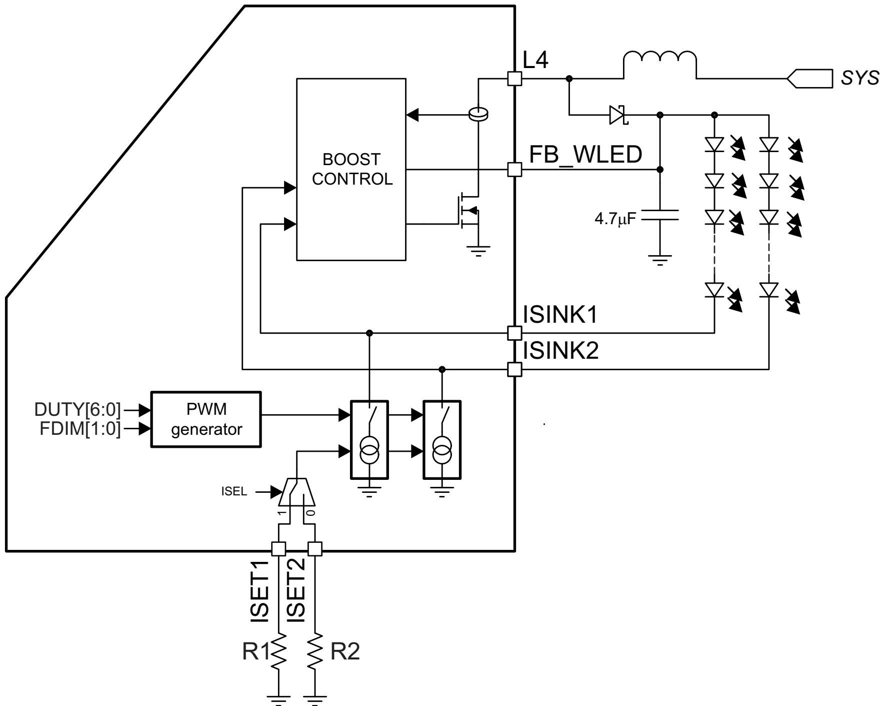
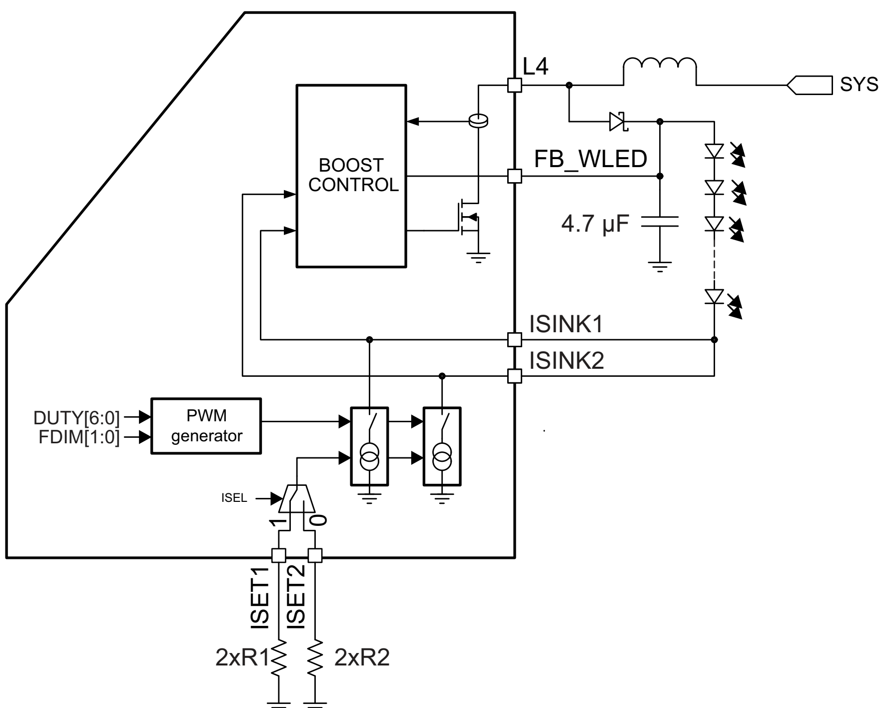


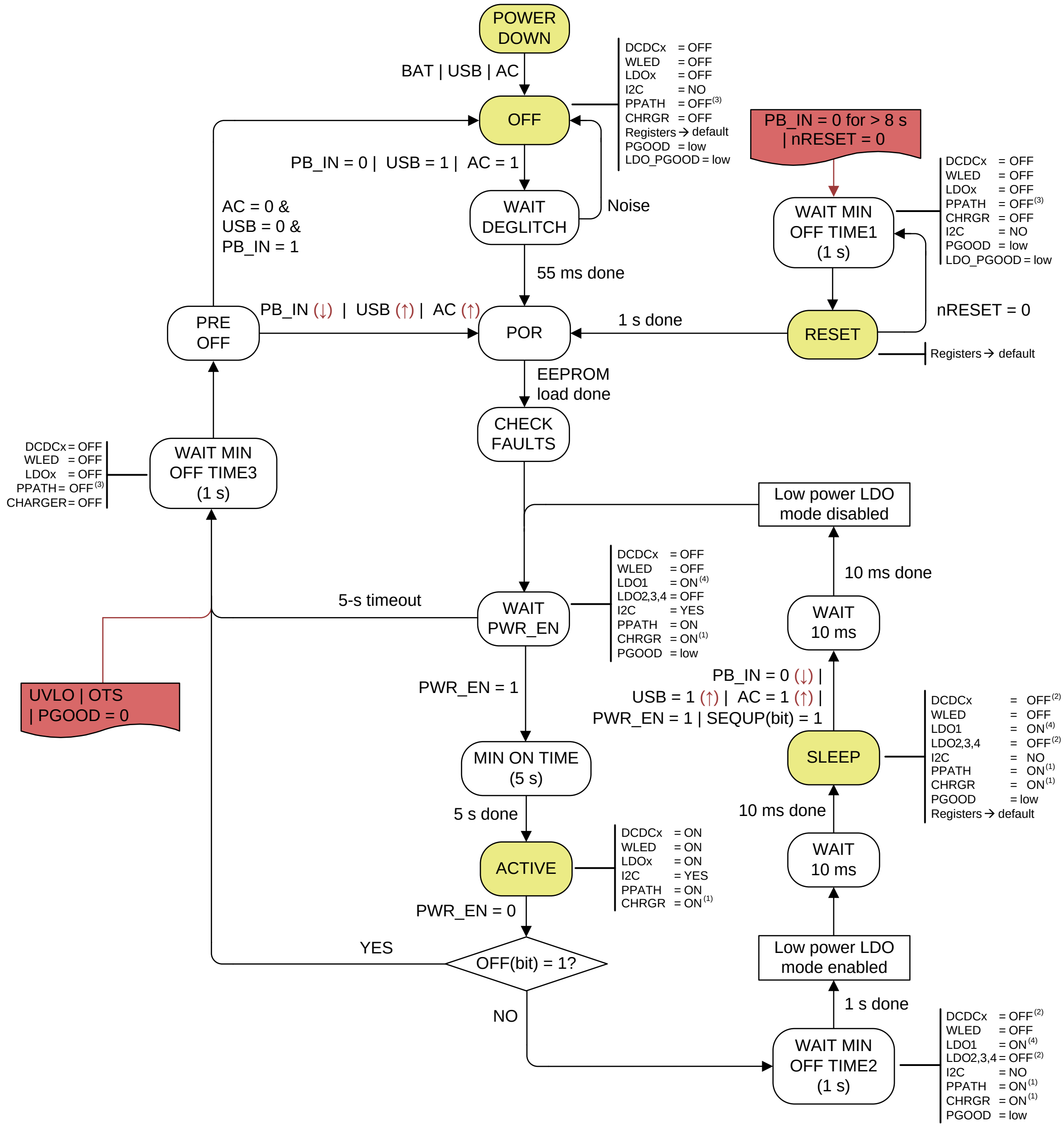
Figure 22. Block Diagram of WLED Driver—Dual-String Operation



This operation has the same LED current as dual-string operation. For single-string operation, both ISINK pins are shorted together and the RSET resistor values (R1 and R2) are doubled to halve the current that each ISINKx pin pulls, resulting in the same current through the LEDs as in dual-string operation.

Figure 23. Block Diagram of WLED Driver—Single-String Operation

8.4 Device Functional Modes



(1) Only if USB or AC supply is present

(2) Rails are powered-down as controlled by the sequencer in default EEPROM settings

(3) Battery voltage always supplies the system (from BAT pin to SYS pin)

(4) LDO1 is assigned to STROBE15 in default EEPROM settings and this special strobe is not controlled by the sequencer. LDO1 can only source 1 mA in the SLEEP state

(5) The 9-MHz oscillator is enabled only when WLED or DCDC or PPATH or CHARGER is enabled.

(6) The charger, auto-discharge, PPATH, and 9-MHz oscillator are ON in the SLEEP state if AC or USB is present and the charger is enabled and not fully charged.

(7) Any USB = 1(↑) or AC = 1 (↑) event in the WAIT MIN OFF TIME2 state makes the device go from the SLEEP state when the timer expires. Any USB = 1(↑) or AC = 1 (↑) event in the WAIT MIN OFF TIME3 state makes the device go from the PRE-OFF state when the timer expires.

(8) All user registers are reset to default values each time the device goes to the SLEEP state.

(9) UVLO and OTS are monitored in all the states except the OFF, POR, and WAIT DEGLITCH states.

Figure 24. Global State Diagram

Device Functional Modes (continued)

8.4.1 PMIC States

8.4.1.1 OFF State

In the OFF state, the PMIC is completely shut down with the exception of a few circuits to monitor the voltage on the AC, USB, and PB_IN pins. All output power rails are turned off and the registers are reset to their default values. The I^2C communication interface is turned off. The lowest amount of power is used in this state. To exit the OFF state, one of the following wake-up events must occur:

- The PB_IN pin is pulled low.
- The USB supply is connected (positive edge).
- The AC adapter is connected (positive edge).

To go to the OFF state, set the OFF bit in the STATUS register to 1b, and then pull the PWR_EN pin low. In normal operation, the device can only go to the OFF state from the ACTIVE state. Whenever a fault occurs during operation, such as thermal shutdown, power-good fail, undervoltage lockout, or a PWR_EN pin timeout, all power rails are shut down and the device goes to the OFF state. The device stays in the OFF state until the fault is removed then a new power-up event occurs.

8.4.1.2 ACTIVE State

This state is the typical mode of operation when the system is up and running. All DC/DC converters, LDO regulators, load switches, the WLED driver, and the battery charger are operational and can be controlled through the I^2C interface.

After a wake-up event, the PMIC enables all rails not controlled by the sequencer and pulls the nWAKEUP pin low to signal the event to the host processor. The device goes to the ACTIVE state only if the host asserts the PWR_EN pin within 5 s after the wake-up event. Otherwise, the device goes to the OFF state. In the ACTIVE state, the sequencer is triggered to automatically enable the remaining power rails. The nWAKEUP pin returns to the Hi-Z state after the PWR_EN pin has been asserted. Figure 3 shows a timing diagram. The device can also go directly to the ACTIVE state from the SLEEP state by pulling the PWR_EN pin high. For more information, see the description of the *SLEEP State*.

The PWR_EN pin must be pulled low for the device to go from ACTIVE state.

8.4.1.3 SLEEP State

The SLEEP state is a low-power mode of operation intended to support system standby. Typically, all power rails are turned off with the exception of the LDO1 rail, and the registers are reset to their default values. The LDO1 rail stays operational but can support only a limited amount of current (1 mA typical).

To go to the SLEEP state, set the OFF bit in the STATUS register to 0b (default), and then pull the PWR_EN pin low. All power rails controlled by the power-down sequencer are shut down, and after 1 s the device goes to the SLEEP state. If the LDO1 rail was enabled in the ACTIVE state, the LDO1 rail stays enabled in the SLEEP sate. All rails not controlled by the power-down sequencer also keep state. The battery charger stays active for as long as either the USB or AC supply is connected to the device. All register values are reset when the device goes to the SLEEP state, including charger parameters.

The device goes to the ACTIVE state after detecting a wake-up event as described in the previous sections. In addition, the device goes from the SLEEP to the ACTIVE state when the PWR_EN pin is pulled high. The system host can go between the ACTIVE and SLEEP states by control of the PWR_EN pin only. This feature bypasses the requirement for a wake-up event from an external source to occur.

Device Functional Modes (continued)

8.4.1.4 RESET State

The TPS65217x device can be reset by either pulling the nRESET pin low or by holding the PB_IN pin low for more than 8 s. All rails are shut down by the sequencer and all register values are reset to their default values. Rails not controlled by the sequencer are shut down after the power-down sequencer is complete. The device stays in the this state for as long as the reset pin is held low, and the nRESET pin must be high for the device to go from the RESET state. However, the device stays in the RESET state for a minimum of 1 s before going back to the ACTIVE state. As detailed in the description of the *ACTIVE State*, the PWR_EN pin must be asserted within 5 s of the nWAKEUP pin going low for the device to go to the ACTIVE state. The RESET function power-cycles the device and only shuts down the output rails temporarily. Resetting the device does put the device in the OFF state.

If the PB_IN pin is kept low for an extended amount of time, the device continues to cycle between the ACTIVE and RESET states, and goes to the RESET state after each 8-s time period.

8.5 Programming

8.5.1 I²C Bus Operation

The TPS65217x device hosts a slave I²C interface that is compliant with I²C standard 3.0 and supports data rates up to 400 kbit/s and auto-increments addressing.

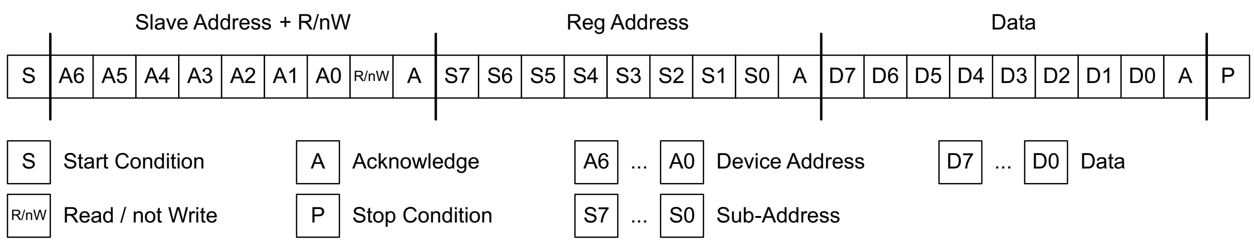


Figure 25. Subaddress in I²C Transmission

The I²C bus is a communications link between a controller and a series of slave terminals. The link is established using a two-wire bus consisting of a serial clock signal (SCL) and a serial data signal (SDA). The serial clock is sourced from the controller in all cases, where the serial data line is bidirectional for data communication between the controller and the slave terminals. Each device has an open-drain output to transmit data on the serial data line. An external pullup resistor must be placed on the serial data line to pull the drain output high during data transmission.

Data transmission is initiated with a start bit from the controller as shown in Figure 28. The start condition is recognized when the SDA line goes from high to low during the high portion of the SCL signal. On reception of a start bit, the device receives serial data on the SDA input and checks for valid address and control information. If the appropriate group and address bits are set for the device, then the device issues an acknowledge (ACK) pulse and prepares for the reception of subaddress data. Subaddress data is decoded and responded to according to the *Register Maps*. Data transmission is completed by either the reception of a stop condition or the reception of the data word sent to the device. A stop condition is recognized as a low-to-high transition of the SDA input during the high portion of the SCL signal. All other transitions of the SDA line must occur during the low portion of the SCL signal. An acknowledge is issued after the reception of a valid address, subaddress, and data words. The I²C interface auto-sequences through the register addresses, so that multiple data words can be sent for a given I²C transmission. For details, see Figure 26, Figure 27, and Figure 28.

Programming (continued)

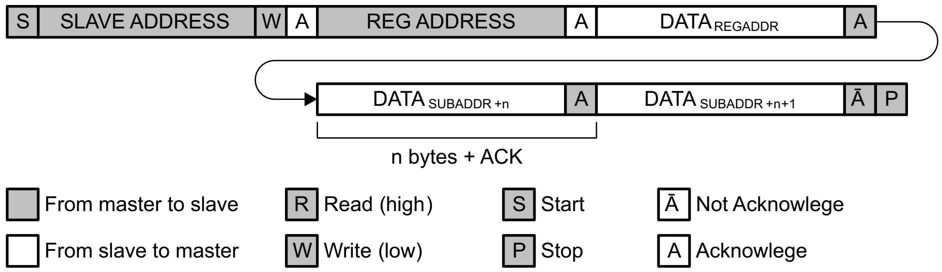


Figure 26. I²C Data Protocol—Master Writes Data To Slave

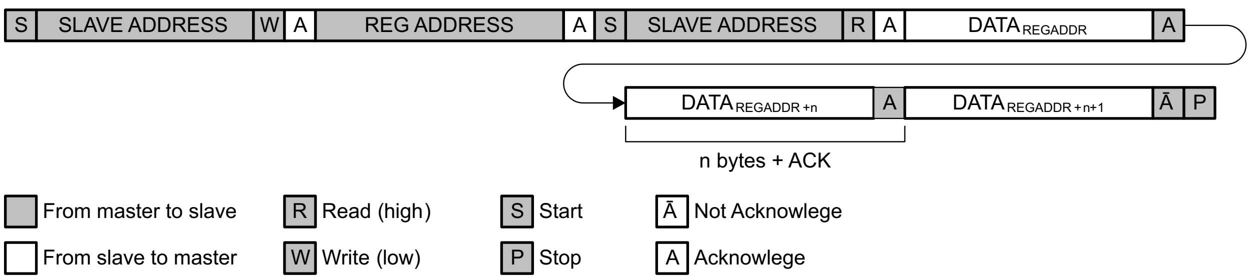


Figure 27. I²C Data Protocol—Master Reads Data from Slave

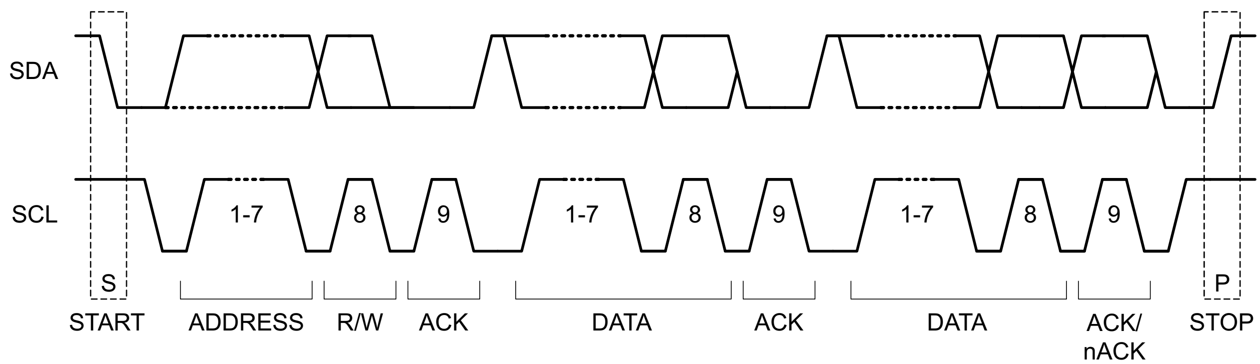


Figure 28. I²C Start-Stop-Acknowledge Protocol

Programming (continued)

8.5.2 Password Protection

Registers 0x0B through 0x1F, with the exception of the password register, are protected against accidental writing by an 8-bit password. The password must be written before writing to a protected register and is automatically reset to 0x00 after the following I^2C transaction, regardless of the register that was accessed and regardless of the transaction type (read or write). The password is required for write access only and is not required for read access.

8.5.2.1 Level1 Protection

To write to a Level1 protected register, follow these steps:

1. Write the address of the destination register, XORed with the protection password (0x7D) to the PASSWORD register.
2. Write data to the password-protected register.
3. Data is only transferred to the protected register if the content of the PASSWORD register XORed with the address sent in Step 2 matches 0x7D. Otherwise, the transaction is ignored. The PASSWORD register is reset to 0x00 after the transaction regardless of whether the XOR logical function matched 0x7D or not.

The cycle must be repeated for any other register that is Level1 write protected.

8.5.2.2 Level2 Protection

To write to a Level2 protected register, follow these steps:

1. Write the address of the destination register, XORed with the protection password (0x7D) to the PASSWORD register.
2. Write data to the password-protected register.
3. The data is temporarily stored if the content of the PASSWORD register XORed with the address sent in Step 2 matches 0x7D. The register value does not change at this point, but the PASSWORD register is reset to 0x00 after the transaction regardless of whether the XOR logical function matched 0x7D or not.
4. Write the address of the destination register, XORed with the protection password (0x7D) to the PASSWORD register.
5. Write the same data as in Step 2 to the password protected register.
6. The content of the PASSWORD register is XORed again with the address sent in Step 5 must match 0x7D for the data to be valid.
7. The register is updated only if both data transfers in Step 2 and Step 5 were valid, and the transferred data matched.

NOTE

No other I^2C transaction can occur between Step 2 and Step 5, and the register is not updated if any other transaction occurs between Step 2 and Step 5. The cycle must be repeated for any other register that is Level2 write protected.

8.5.3 Resetting of Registers to Default Values

All registers are reset to default values when one or more of the following conditions occur:

- The device goes from the ACTIVE state to the SLEEP state or OFF state.
- The BAT or USB supply is applied from a power-less state (power-on reset).
- The push-button input is pulled low for more than 8 s.
- The nRESET pin is pulled low.
- A fault occurs.

8.6 Register Maps

8.6.1 Register Address Map

Figure 29 lists the memory-mapped registers for the device registers. All register offset addresses not listed in should be considered as reserved locations and the register contents should not be modified.

Figure 29. Register Address Map

Address (Decimal)	Address (Hexadecimal)	Name	Password Protection Level	Default Value	Description	Section
0	0x00	CHIPID	None	X	Chip ID	Go
1	0x01	PPATH	None	0x3D	Power path control	Go
2	0x02	INT	None	0x80	Interrupt flags and masks	Go
3	0x03	CHGCONFIG0	None	0x00	Charger control register 0	Go
4	0x04	CHGCONFIG1	None	0xB1	Charger control register 1	Go
5	0x05	CHGCONFIG2	None	0x80	Charger control register 2	Go
6	0x06	CHGCONFIG3	None	0xB2	Charger control register 3	Go
7	0x07	WLEDCTRL1	None	0xB1	WLED control register	Go
8	0x08	WLEDCTRL2	None	0x00	WLED PWM duty cycle	Go
9	0x09	MUXCTRL	None	0x00	Analog multiplexer control register	Go
10	0x0A	STATUS	None	0x00	Status register	Go
11	0x0B	PASSWORD	None	0x00	Write password	Go
12	0x0C	PGOOD	None	0x00	Power good (PG) flags	Go
13	0x0D	DEFPG	Level1	0x0C	Power good (PG) delay	Go
14	0x0E	DEFDCDC1	Level2	X	DCDC1 voltage adjustment	Go
15	0x0F	DEFDCDC2	Level2	X	DCDC2 voltage adjustment	Go
16	0x10	DEFDCDC3	Level2	0x08	DCDC3 voltage adjustment	Go
17	0x11	DEFSLEW	Level2	0x06	Slew control for DCDC1, DCDC2, DCDC3, and PFM mode enable	Go
18	0x12	DEFLDO1	Level2	0x09	LDO1 voltage adjustment	Go
19	0x13	DEFLDO2	Level2	0x38	LDO2 voltage adjustment	Go
20	0x14	DEFLS1	Level2	X	LS1 or LDO3 voltage adjustment	Go
21	0x15	DEFLS2	Level2	X	LS2 or LDO4 voltage adjustment	Go
22	0x16	ENABLE	Level1	0x00	Enable register	Go
23	0x18	DEFUVLO	Level1	0x03	UVLO control register	Go
24	0x19	SEQ1	Level1	X	Power-up STROBE definition	Go
25	0x1A	SEQ2	Level1	X	Power-up STROBE definition	Go
26	0x1B	SEQ3	Level1	X	Power-up STROBE definition	Go
27	0x1C	SEQ4	Level1	0x40	Power-up STROBE definition	Go
28	0x1D	SEQ5	Level1	X	Power-up delay times	Go
29	0x1E	SEQ6	Level1	0x00	Power-up delay times	Go

Bit access types are abbreviated to fit into small table cells. Table 1 shows the abbreviation codes that are used for access types in this section. Registers that are different for each TPS65217x variant will have different hexadecimal reset values and are shown as *X*. The hexadecimal reset value can de determined by converting the binary reset value.

Table 1. Access Type Codes

Access Type (1)	Code	Description
Read	R	Read-only
Read/Write	R/W	Read and Write

(1) Reserved bits can be R or R/W. Read-only (R) Reserved bits are not used and writing data to these bits will have no effect on device operation. Read and Write (R/W) Reserved bits are settings that cannot be modified. The reset value must always be written to these bits. Modifying a R/W Reserved bit will have an impact on device operation and can produce unwanted device behavior.

8.6.2 Chip ID Register (CHIPID) (Address = 0x00) [reset = X]

CHIPID is shown in Figure 30 and described in Table 2.

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Figure 30. CHIPID Register

DATA BIT		7	6	5	4	3	2	1	0
FIELD NAME		CHIP[3:0]				REV[3:0]			
READ/WRITE		R	R	R	R	R	R	R	R
RESET VALUE	TPS65217A	0b	1b	1b	1b	0b	0b	1b	0b
	TPS65217B	1b	1b	1b	1b	0b	0b	1b	0b
	TPS65217C	1b	1b	1b	0b	0b	0b	1b	0b
	TPS65217D	0b	1b	1b	0b	0b	0b	1b	0b

Table 2. CHIPID Register Field Descriptions

Bit	Field	Type	Reset	Description
7–4	CHIP[3:0]	R	TPS65217A: 0111b TPS65217B: 1111b TPS65217C: 1110b TPS65217D: 0110b	Chip ID 0000b = Future use 0001b = Future use 0110b = TPS65217D 0111b = TPS65217A 1000b = Future use 1001b to 1101b = Reserved 1110b = TPS65217C 1111b = TPS65217B
3–0	REV[3:0]	R	0010b	Revision code 0000b = revision 1.0 0001b = revision 1.1 0010b = revision 1.2 0011b to 1110b = Reserved 1111b = Future use

8.6.3 Power Path Control Register (PPATH) (Address = 0x01) [reset = 0x3D]

PPATH is shown in Figure 31 and described in Table 3.

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Figure 31. PPATH Register

DATA BIT	7	6	5	4	3	2	1	0
FIELD NAME	ACSINK	USBSINK	AC_EN	USB_EN	IAC[1:0]		IUSB[1:0]	
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET VALUE	0b	0b	1b	1b	1b	1b	0b	1b

Table 3. PPATH Register Field Descriptions

Bit	Field	Type	Reset	Description
7	ACSINK	R/W	0b	AC current-sink control NOTE: [ACSINK, USBSINK] = 01b and 10b combinations are not recommended, as these may lead to unexpected enabling and disabling of the current sinks. 0b = AC sink is enabled when USB is a valid supply and V_{AC} is less than the detection threshold 1b = Set ACSINK and USBSINK to 1b at the same time to force both (AC and USB) current sinks OFF
6	USBSINK	R/W	1b	USB current-sink control NOTE: [ACSINK, USBSINK] = 01b and 10b combinations are not recommended, as these may lead to unexpected enabling and disabling of the current sinks. 0b = USB sink is enabled when AC is a valid supply and V_{USB} is less than the detection threshold 1b = Set ACSINK and USBSINK to 1b at the same time to force both (AC and USB) current sinks OFF
5	AC_EN	R/W	1b	AC power path enable 0b = AC power input is turned off. 1b = AC power input is turned on.
4	USB_EN	R/W	1b	USB power path enable 0b = USB power input is turned off (USB suspend mode). 1b = USB power input is turned on.
3–2	IAC[1:0]	R/W	11b	AC input-current limit 00b = 100 mA 01b = 500 mA 10b = 1300 mA 11b = 2500 mA
1–0	IUSB[1:0]	R/W	01b	USB input-current limit 00b = 100 mA 01b = 500 mA 10b = 1300 mA 11b = 1800 mA

8.6.4 Interrupt Register (INT) (Address = 0x02) [reset = 0x80]

INT is shown in Figure 32 and described in Table 4.

Return to Summary Table.

Figure 32. INT Register

DATA BIT	7	6	5	4	3	2	1	0
FIELD NAME	Reserved	PBM	ACM	USBM	Reserved	PBI	ACI	USBI
READ/WRITE	R/W	R/W	R/W	R/W	R	R	R	R
RESET VALUE	1b	0b	0b	0b	0b	0b	0b	0b

Table 4. INT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R/W	1b	This bit is reserved
6	PBM	R/W	0b	Push-button status change interrupt mask 0b = Interrupt is issued when PB status changes. 1b = No interrupt is issued when PB status changes.
5	ACM	R/W	0b	AC interrupt mask 0b = Interrupt is issued when power to the AC input is applied or removed. 1b = No interrupt is issued when power to the AC input is applied or removed.
4	USBM	R/W	0b	USB power status change interrupt mask 0b = Interrupt is issued when power to USB input is applied or removed. 1b = No interrupt is issued when power to USB input is applied or removed.
3	Reserved	R	0b	This bit is reserved
2	PBI	R	0b	Push-button status change interrupt NOTE: Status information is available in the STATUS register. 0b = No change in status 1b = Push-button status change (PB_IN changed high to low or low to high)
1	ACI	R	0b	AC power status change interrupt NOTE: Status information is available in the STATUS register. 0b = No change in status 1b = AC power status change (power to the AC pin has either been applied or removed)
0	USBI	R	0b	USB power status change interrupt NOTE: Status information is available in the STATUS register. 0b = No change in status 1b = USB power status change (power to the USB pin has either been applied or removed)

8.6.5 Charger Configuration Register 0 (CHGCONFIG0) (Address = 0x03) [reset = 0x00]

CHGCONFIG0 is shown in Figure 33 and described in Table 5.

Return to Summary Table.

Figure 33. CHGCONFIG0 Register

DATA BIT	7	6	5	4	3	2	1	0
FIELD NAME	TREG	DPPM	TSUSP	TERMI	ACTIVE	CHGTOUT	PCHGTOUT	BATTEMP
READ/WRITE	R	R	R	R	R	R	R	R
RESET VALUE	0b	0b	0b	0b	0b	0b	0b	0b

Table 5. CHGCONFIG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	TREG	R	0b	Thermal regulation 0b = Charger is in normal operation. 1b = Charge current is reduced because of high chip temperature.
6	DPPM	R	0b	DPPM active 0b = DPPM loop is not active. 1b = DPPM loop is active; charge current is reduced to support the load with the current required.
5	TSUSP	R	0b	Thermal suspend 0b = Charging is allowed. 1b = Charging is temporarily suspended because battery temperature is out of range.
4	TERMI	R	0b	Termination current detect 0b = Charging, charge termination current threshold has not been crossed. 1b = Charge termination current threshold has been crossed and charging has been stopped. This can be from a battery reaching full capacity or to a battery removal condition.
3	ACTIVE	R	0b	Charger active bit 0b = Charger is not charging. 1b = Charger is charging (DPPM or thermal regulation may be active).
2	CHGTOUT	R	0b	Charge timer time-out 0b = Charging, timers did not time out. 1b = One of the timers has timed out and charging has been terminated.
1	PCHGTOUT	R	0b	Precharge timer time-out 0b = Charging, precharge timer did not time out. 1b = Precharge timer has timed out and charging has been terminated.
0	BATTEMP	R	0b	Battery temperature and NTC error NOTE: This bit does not indicate that the battery temperature is within the valid range for charging. 0b = Battery temperature is in the allowed range for charging. 1b = No temperature sensor detected or battery temperature outside valid charging range

8.6.6 Charger Configuration Register 1 (CHGCONFIG1) (Address = 0x04) [reset = 0xB1]

CHGCONFIG1 is shown in Figure 34 and described in Table 6.

Return to Summary Table.

Figure 34. CHGCONFIG1 Register

DATA BIT	7	6	5	4	3	2	1	0
FIELD NAME	TIMER[1:0]		TMR_EN	NTC_TYPE	RESET	TERM	SUSP	CHG_EN
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET VALUE	1b	0b	1b	1b	0b	0b	0b	1b

Table 6. CHGCONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7–6	TIMER[1:0]	R/W	10b	Charge safety timer setting (fast-charge timer) 00b = 4h 01b = 5h 10b = 6h 11b = 8h
5	TMR_EN	R/W	1b	Safety timer enable 0b = Precharge timer and fast charge timer are disabled. 1b = Precharge timer and fast charge time are enabled.
4	NTC_TYPE	R/W	1b	NTC type (for battery temperature measurement) 0b = 100k (curve 1, B = 3960) 1b = 10k (curve 2, B = 3480)
3	RESET	R/W	0b	Charger reset 0b = Inactive 1b = Reset active. This bit must be set and then reset via the serial interface to restart the charge algorithm.
2	TERM	R/W	0b	Charge termination on-off 0b = Charge termination enabled, based on timers and termination current 1b = Current-based charge termination does not occur and the charger is always on
1	SUSP	R/W	0b	Suspend charge 0b = Safety timer and precharge timers are not suspended. 1b = Safety timer and precharge timers are suspended.
0	CHG_EN	R/W	1b	Charger enable 0b = Charger is disabled. 1b = Charger is enabled.

8.6.7 Charger Configuration Register 2 (CHGCONFIG2) (Address = 0x05) [reset = 0x80]

CHGCONFIG2 is shown in Figure 35 and described in Table 7.

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Figure 35. CHGCONFIG2 Register

DATA BIT	7	6	5	4	3	2	1	0
FIELD NAME	DYNTMR	VPRECHG	VOREG[1:0]		Reserved	Reserved	Reserved	Reserved
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET VALUE	1b	0b	0b	0b	0b	0b	0b	0b

Table 7. CHGCONFIG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	DYNTMR	R/W	1b	Dynamic timer function 0b = Safety timers run with their nominal clock speed. 1b = Clock speed is divided by 2 if thermal loop or DPPM loop is active.
6	VPRECHG	R/W	0b	Precharge voltage 0b = Precharge to fast-charge transition voltage is 2.9 V. 1b = Precharge to fast-charge transition voltage is 2.5 V.
5–4	VOREG[1:0]	R/W	00b	Charge voltage selection 00b = 4.1 V 01b = 4.15 V 10b = 4.2 V 11b = 4.2 V
3–0	Reserved	R/W	0000b	These bits are reserved

8.6.8 Charger Configuration Register 3 (CHGCONFIG3) (Address = 0x06) [reset = 0xB2]

CHGCONFIG3 is shown in Figure 36 and described in Table 8.

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Figure 36. CHGCONFIG3 Register

DATA BIT	7	6	5	4	3	2	1	0
FIELD NAME	ICHRG[1:0]		DPPMTH[1:0]		PCHRGT	TERMIF[1:0]		TRANGE
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET VALUE	1b	0b	1b	1b	0b	0b	1b	0b

Table 8. CHGCONFIG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7–6	ICHRG[1:0]	R/W	10b	Charge current setting 00b = 300 mA 01b = 400 mA 10b = 500 mA 11b = 700 mA
5–4	DPPMTH[1:0]	R/W	11b	Power path DPPM threshold 00b = 3.5 V 01b = 3.75 V 10b = 4 V 11b = 4.25 V
3	PCHRGT	R/W	0b	Precharge time 0b = 30 min 1b = 60 min
2–1	TERMIF[1:0]	R/W	01b	Termination current factor NOTE: Termination current = TERMIF x ICHRG 00b = 2.5% 01b = 7.5% 10b = 15% 11b = 18%
0	TRANGE	R/W	0b	Temperature range for charging 0b = 0°C to 45°C 1b = 0°C to 60°C

8.6.9 WLED Control Register 1 (WLEDCTRL1) (Address = 0x07) [reset = 0xB1]

WLEDCTRL1 is shown in Figure 37 and described in Table 9.

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Figure 37. WLEDCTRL1 Register

DATA BIT	7	6	5	4	3	2	1	0
FIELD NAME	Reserved	Reserved	Reserved	Reserved	ISINK_EN	ISEL	FDIM[1:0]	
READ/WRITE	R	R	R	R	R/W	R/W	R/W	R/W
RESET VALUE	0b	0b	0b	0b	0b	0b	0b	1b

Table 9. WLEDCTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7–4	Reserved	R	0000b	These bits are reserved
3	ISINK_EN	R/W	0b	Current sink enable NOTE: This bit enables both current sinks. 0b = Current sink is disabled (OFF). 1b = Current sink is enabled (ON).
2	ISEL	R/W	0b	ISET selection bit 0b = Low-level (define by ISET1 pin) 1b = High-level (defined by ISET2 pin)
1–0	FDIM[1:0]	R/W	01b	PWM dimming frequency 00b = 100 Hz 01b = 200 Hz 10b = 500 Hz 11b = 1000 Hz

8.6.10 WLED Control Register 2 (WLEDCTRL2) (Address = 0x08) [reset = 0x00]

WLEDCTRL2 is shown in Figure 38 and described in Table 10.

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Figure 38. WLEDCTRL2 Register

DATA BIT	7	6	5	4	3	2	1	0
FIELD NAME	Reserved	DUTY[6:0]						
READ/WRITE	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET VALUE	0b	0b	0b	0b	0b	0b	0b	0b

Table 10. WLEDCTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R	0b	This bit is reserved
6–0	DUTY[6:0]	R/W	0000000b	PWM dimming duty cycle 000 0000b = 1% 000 0001b = 2% ... 110 0010b = 99% 110 0011b = 100% 110 0100b = 0% ... 111 1110b = 0% 111 1111b = 0%

8.6.11 MUX Control Register (MUXCTRL) (Address = 0x09) [reset = 0x00]

MUXCTRL is shown in Figure 39 and described in Table 11.

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Figure 39. MUXCTRL Register

DATA BIT	7	6	5	4	3	2	1	0
FIELD NAME	Reserved	Reserved	Reserved	Reserved	Reserved	MUX[2:0]		
READ/WRITE	R	R	R	R	R	R/W	R/W	R/W
RESET VALUE	0b	0b	0b	0b	0b	0b	0b	0b

Table 11. MUXCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7–3	Reserved	R	00000b	These bits are reserved
2–0	MUX[2:0]	R/W	000b	Analog multiplexer selection 000b = MUX is disabled, output is Hi-Z. 001b = VBAT 010b = VSYS 011b = VTS 100b = VICHARGE 101b = MUX_IN (external input) 110b = MUX is disabled, output is Hi-Z. 111b = MUX is disabled, output is Hi-Z.

8.6.12 Status Register (STATUS) (Address = 0x0A) [reset = 0x00]

STATUS is shown in Figure 40 and described in Table 12.

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Figure 40. STATUS Register

DATA BIT	7	6	5	4	3	2	1	0
FIELD NAME	OFF	Reserved	Reserved	Reserved	ACPWR	USBPWR	Reserved	PB
READ/WRITE	R/W	R	R	R	R	R	R	R
RESET VALUE	0b	0b	0b	0b	0b	0b	0b	0b

Table 12. STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OFF	R/W	0b	OFF bit. Set this bit to 1b to enter the OFF state when PWR_EN pin is pulled low. The bit is automatically reset to 0b.
6–4	Reserved	R	000b	These bits are reserved
3	ACPWR	R	0b	AC power status bit 0b = AC power is not present and/or not in the range valid for charging. 1b = AC source is present and in the range valid for charging.
2	USBPWR	R	0b	USB power 0b = USB power is not present and/or not in the range valid for charging. 1b = USB source is present and in the range valid for charging.
1	Reserved	R	0b	This bit is reserved
0	PB	R	0b	Push Button status bit 0b = Push-button is inactive (PB_IN is pulled high). 1b = Push-button is active (PB_IN is pulled low).

8.6.13 Password Register (PASSWORD) (Address = 0x0B) [reset = 0x00]

PASSWORD is shown in Figure 41 and described in Table 13.

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Figure 41. PASSWORD Register

DATA BIT	7	6	5	4	3	2	1	0
FIELD NAME	PWRD[7:0]							
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET VALUE	0b	0b	0b	0b	0b	0b	0b	0b

Table 13. Password Register (PASSWORD) Field Descriptions

Bit	Field	Type	Reset	Description
7–0	PWRD[7:0]	R/W	00000000b	Password protection locking and unlocking NOTE: Register is automatically reset to 0x00 after the following I^2C transaction. See the *Password Protection* section for details. 0000 0000b = Password-protected registers are locked for write access. ... 0111 1100b = Password-protected registers are locked for write access. 0111 1101b = Allows writing to a password-protected register in the next write cycle 0111 1110b = Password-protected registers are locked for write access. ... 1111 1111b = Password-protected registers are locked for write access.

8.6.14 Power Good Register (PGOOD) (Address = 0x0C) [reset = 0x00]

PGOOD is shown in Figure 42 and described in Table 14.

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Figure 42. PGOOD Register

DATA BIT	7	6	5	4	3	2	1	0
FIELD NAME	Reserved	LDO3_PG	LDO4_PG	DC1_PG	DC2_PG	DC3_PG	LDO1_PG	LDO2_PG
READ/WRITE	R	R	R	R	R	R	R	R
RESET VALUE	0b	0b	0b	0b	0b	0b	0b	0b

Table 14. PGOOD Register Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R	0b	This bit is reserved
6	LDO3_PG	R	0b	LDO3 power-good 0b = LDO is either disabled or not in regulation. 1b = LDO is in regulation or LS1 or LDO3 is configured as a switch.
5	LDO4_PG	R	0b	LDO4 power-good 0b = LDO is either disabled or not in regulation 1b = LDO is in regulation or LS2 or LDO4 is configured as a switch.
4	DC1_PG	R	0b	DCDC1 power-good 0b = DCDC1 is either disabled or not in regulation. 1b = DCDC1 is in regulation.
3	DC2_PG	R	0b	DCDC2 power-good 0b = DCDC2 is either disabled or not in regulation. 1b = DCDC2 is in regulation.
2	DC3_PG	R	0b	DCDC3 power-good 0b = DCDC3 is either disabled or not in regulation. 1b = DCDC3 is in regulation.
1	LDO1_PG	R	0b	LDO1 power-good. 0b = LDO is either disabled or not in regulation 1b = LDO is in regulation
0	LDO2_PG	R	0b	LDO2 power-good 0b = LDO is either disabled or not in regulation 1b = LDO is in regulation

8.6.15 Power-Good Control Register (DEFPG) (Address = 0x0D) [reset = 0x0C]

DEFPG is shown in Figure 43 and described in Table 15.

Return to Summary Table.

This register is password protected.

Figure 43. DEFPG Register

DATA BIT	7	6	5	4	3	2	1	0
FIELD NAME	Reserved	Reserved	Reserved	Reserved	LDO1PGM	LDO2PGM	PGDLY[1:0]	
READ/WRITE	R	R	R	R	R/W	R/W	R/W	R/W
RESET VALUE	0b	0b	0b	0b	1b	1b	0b	0b

Table 15. DEFPG Register Field Descriptions

Bit	Field	Type	Reset	Description
7–4	Reserved	R	0000b	These bits are reserved
3	LDO1PGM	R/W	1b	LDO1 power-good masking bit 0b = PGOOD pin is pulled low if LDO1_PG is low 1b = LDO1_PG status does not affect the status of the PGOOD output pin.
2	LDO2PGM	R/W	1b	LDO2 power-good masking bit 0b = PGOOD pin is pulled low if LDO2_PG is low 1b = LDO2_PG status does not affect the status of the PGOOD output pin.
1–0	PGDLY[1:0]	R/W	00b	Power-good delay NOTE: PGDLY applies to the PGOOD pin. 00b = 20 ms 01b = 100 ms 10b = 200 ms 11b = 400 ms

8.6.16 DCDC1 Control Register (DEFDCDC1) (Address = 0x0E) [reset = X]

DEFDCDC1 is shown in Figure 44 and described in Table 16.

Return to Summary Table.

This register is password protected.

Figure 44. DEFDCDC1 Register

DATA BIT		7	6	5	4	3	2	1	0
FIELD NAME		XADJ1	Reserved	DCDC1[5:0]					
READ/WRITE		R/W	R	R/W	R/W	R/W	R/W	R/W	R/W
RESET VALUE	TPS65217A	0b	0b	0b	1b	1b	1b	1b	0b
	TPS65217B	0b	0b	0b	1b	1b	1b	1b	0b
	TPS65217C	0b	0b	0b	1b	1b	0b	0b	0b
	TPS65217D	0b	0b	0b	1b	0b	0b	1b	0b

Table 16. DEFDCDC1 Register Field Descriptions

Bit	Field	Type	Reset	Description			
7	XADJ1	R/W	0b	DCDC1 voltage adjustment option 0b = Output voltage is adjusted through the register setting. 1b = Output voltage is externally adjusted.			
6	Reserved	R	0b	This bit is reserved			
5–0	DCDC1[5:0]	R/W	TPS65217A: 01 1110b TPS65217B: 01 1110b TPS65217C: 01 1000b TPS65217D: 01 0010b	DCDC1 output-voltage setting			
				00 0000b = 0.9 V 00 0001b = 0.925 V 00 0010b = 0.95 V 00 0011b = 0.975 V 00 0100b = 1 V 00 0101b = 1.025 V 00 0110b = 1.05 V 00 0111b = 1.075 V 00 1000b = 1.1 V 00 1001b = 1.125 V 00 1010b = 1.15 V 00 1011b = 1.175 V 00 1100b = 1.2V 00 1101b = 1.225 V 00 1110b = 1.25 V 00 1111b = 1.275 V	01 0000b = 1.3 V 01 0001b = 1.325 V 01 0010b = 1.35 V 01 0011b = 1.375 V 01 0100b = 1.4 V 01 0101b = 1.425 V 01 0110b = 1.45 V 01 0111b = 1.475 V 01 1000b = 1.5 V 01 1001b = 1.55 V 01 1010b = 1.6 V 01 1011b = 1.65 V 01 1100b = 1.7 V 01 1101b = 1.75 V 01 1110b = 1.80V 01 1111b = 1.85 V	10 0000b = 1.9 V 10 0001b = 1.95 V 10 0010b = 2 V 10 0011b = 2.05 V 10 0100b = 2.1 V 10 0101b = 2.15 V 10 0110b = 2.2 V 10 0111b = 2.25 V 10 1000b = 2.3 V 10 1001b = 2.35 V 10 1010b = 2.4 V 10 1011b = 2.45 V 10 1100b = 2.5 V 10 1101b = 2.55 V 10 1110b = 2.6 V 10 1111b = 2.65 V	11 0000b = 2.7 V 11 0001b = 2.75 V 11 0010b = 2.8 V 11 0011b = 2.85 V 11 0100b = 2.9 V 11 0101b = 3 V 11 0110b = 3.1 V 11 0111b = 3.2 V 11 1000b = 3.3 V 11 1001b = 3.3 V 11 1010b = 3.3 V 11 1011b = 3.3 V 11 1100b = 3.3 V 11 1101b = 3.3 V 11 1110b = 3.3 V 11 1111b = 3.3 V

8.6.17 DCDC2 Control Register (DEFDCDC2) (Address = 0x0F) [reset = X]

DEFDCDC2 is shown in Figure 45 and described in Table 17.

Return to Summary Table.

This register is password protected.

Figure 45. DEFDCDC2 Register

DATA BIT		7	6	5	4	3	2	1	0
FIELD NAME		XADJ2	Reserved	DCDC2[5:0]					
READ/WRITE		R/W	R	R/W	R/W	R/W	R/W	R/W	R/W
RESET VALUE	TPS65217A	0b	0b	1b	1b	1b	0b	0b	0b
	TPS65217B	0b	0b	0b	0b	1b	0b	0b	0b
	TPS65217C	0b	0b	0b	0b	1b	0b	0b	0b
	TPS65217D	0b	0b	0b	0b	1b	0b	0b	0b

Table 17. DEFDCDC2 Register Field Descriptions

Bit	Field	Type	Reset	Description			
7	XADJ2	R/W	0b	DCDC2 voltage adjustment option 0b = Output voltage is adjusted through the register setting. 1b = Output voltage is externally adjusted.			
6	Reserved	R	0b	This bit is reserved			
5–0	DCDC2[5:0]	R/W	TPS65217A: 11 1000b TPS65217B: 00 1000b TPS65217C: 00 1000b TPS65217D: 00 1000b	DCDC2 output voltage setting			
				00 0000b = 0.9 V	01 0000b = 1.3 V	10 0000b = 1.9 V	11 0000b = 2.7 V
				00 0001b = 0.925 V	01 0001b = 1.325 V	10 0001b = 1.95 V	11 0001b = 2.75 V
				00 0010b = 0.950V	01 0010b = 1.35 V	10 0010b = 2 V	11 0010b = 2.8 V
				00 0011b = 0.975 V	01 0011b = 1.375 V	10 0011b = 2.05 V	11 0011b = 2.85 V
				00 0100b = 1 V	01 0100b = 1.4 V	10 0100b = 2.1 V	11 0100b = 2.9 V
				00 0101b = 1.025 V	01 0101b = 1.425 V	10 0101b = 2.15 V	11 0101b = 3 V
				00 0110b = 1.05 V	01 0110b = 1.45 V	10 0110b = 2.2 V	11 0110b = 3.1 V
				00 0111b = 1.075 V	01 0111b = 1.475 V	10 0111b = 2.25 V	11 0111b = 3.2 V
				00 1000b = 1.1 V	01 1000b = 1.5 V	10 1000b = 2.3 V	11 1000b = 3.3 V
				00 1001b = 1.125 V	01 1001b = 1.55 V	10 1001b = 2.35 V	11 1001b = 3.3 V
				00 1010b = 1.15 V	01 1010b = 1.6 V	10 1010b = 2.4 V	11 1010b = 3.3 V
				00 1011b = 1.175 V	01 1011b = 1.65 V	10 1011b = 2.45 V	11 1011b = 3.3 V
				00 1100b = 1.2 V	01 1100b = 1.7 V	10 1100b = 2.5 V	11 1100b = 3.3 V
				00 1101b = 1.225 V	01 1101b = 1.75 V	10 1101b = 2.55 V	11 1101b = 3.3 V
				00 1110b = 1.25 V	01 1110b = 1.8 V	10 1110b = 2.6 V	11 1110b = 3.3 V
				00 1111b = 1.275 V	01 1111b = 1.85 V	10 1111b = 2.65 V	11 1111b = 3.3 V

8.6.18 DCDC3 Control Register (DEFDCDC3) (Address = 0x10) [reset = 0x08]

DEFDCDC3 is shown in Figure 46 and described in Table 18.

Return to Summary Table.

This register is password protected.

Figure 46. DEFDCDC3 Register

DATA BIT	7	6	5	4	3	2	1	0
FIELD NAME	XADJ3	Reserved	DCDC3[5:0]					
READ/WRITE	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W
RESET VALUE	0b	0b	0b	0b	1b	0b	0b	0b

Table 18. DEFDCDC3 Register Field Descriptions

Bit	Field	Type	Reset	Description			
7	XADJ3	R/W	0b	DCDC3 voltage adjustment option 0b = Output voltage is adjusted through register setting 1b = Output voltage is externally adjusted			
6	Reserved	R	0b	This bit is reserved			
5–0	DCDC3[5:0]	R/W	00 1000b	DCDC3 output voltage setting			
				00 0000b = 0.9 V	01 0000b = 1.3 V	10 0000b = 1.9 V	11 0000b = 2.7 V
				00 0001b = 0.925 V	01 0001b = 1.325 V	10 0001b = 1.95 V	11 0001b = 2.75 V
				00 0010b = 0.95 V	01 0010b = 1.35 V	10 0010b = 2 V	11 0010b = 2.8 V
				00 0011b = 0.975 V	01 0011b = 1.375 V	10 0011b = 2.05 V	11 0011b = 2.85 V
				00 0100b = 1 V	01 0100b = 1.4 V	10 0100b = 2.1 V	11 0100b = 2.9 V
				00 0101b = 1.025 V	01 0101b = 1.425 V	10 0101b = 2.15 V	11 0101b = 3 V
				00 0110b = 1.05 V	01 0110b = 1.45 V	10 0110b = 2.2 V	11 0110b = 3.1 V
				00 0111b = 1.075 V	01 0111b = 1.475 V	10 0111b = 2.25 V	11 0111b = 3.2 V
				00 1000b = 1.1 V	01 1000b = 1.5 V	10 1000b = 2.30 V	11 1000b = 3.3 V
				00 1001b = 1.125 V	01 1001b = 1.55 V	10 1001b = 2.35 V	11 1001b = 3.3 V
				00 1010b = 1.15 V	01 1010b = 1.6 V	10 1010b = 2.4 V	11 1010b = 3.3 V
				00 1011b = 1.175 V	01 1011b = 1.65 V	10 1011b = 2.45 V	11 1011b = 3.3 V
				00 1100b = 1.2 V	01 1100b = 1.7 V	10 1100b = 2.5 V	11 1100b = 3.3 V
				00 1101b = 1.225 V	01 1101b = 1.75 V	10 1101b = 2.55 V	11 1101b = 3.3 V
				00 1110b = 1.25 V	01 1110b = 1.8 V	10 1110b = 2.6 V	11 1110b = 3.3 V
				00 1111b = 1.275 V	01 1111b = 1.85 V	10 1111b = 2.65 V	11 1111b = 3.3 V

8.6.19 Slew-Rate Control Register (DEFSLEW) (Address = 0x11) [reset = 0x06]

DEFSLEW is shown in Figure 47 and described in Table 19.

Return to Summary Table.

Slew-rate control applies to all three DC/DC converters.
This register is password protected.

Figure 47. DEFSLEW Register

DATA BIT	7	6	5	4	3	2	1	0
FIELD NAME	GO	GODSBL	PFM_EN1	PFM_EN2	PFM_EN3	SLEW[2:0]		
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET VALUE	0b	0b	0b	0b	0b	1b	1b	0b

Table 19. DEFSLEW Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GO	R/W	0b	Go bit NOTE: Bit is automatically reset at the end of the voltage transition. 0b = No change 1b = Initiates the transition from the present state to the output voltage setting currently stored in the DEFDCDCx register
6	GODSBL	R/W	0b	Go Disable bit 0b = Enabled 1b = Disabled; DCDCx output voltage changes whenever setpoint is updated in DEFDCDCx register without having to write to the GO bit. SLEW[2:0] setting does apply.
5	PFM_EN1	R/W	0b	PFM enable bit, DCDC1 0b = DC/DC converter operates in the PWM or PFM mode, depending on load. 1b = DC/DC converter is forced into the fixed-frequency PWM mode.
4	PFM_EN2	R/W	0b	PFM enable bit, DCDC2 0b = DC/DC converter operates in the PWM or PFM mode, depending on load. 1b = DC/DC converter is forced into the fixed-frequency PWM mode.
3	PFM_EN3	R/W	0b	PFM enable bit, DCDC3 0b = DC/DC converter operates in the PWM or PFM mode, depending on load. 1b = DC/DC converter is forced into the fixed-frequency PWM mode.
2–0	SLEW[2:0]	R/W	0110b	Output slew-rate setting NOTE: The actual slew rate depends on the voltage step per code. See the DCDC1 and DCDC2 registers for details. 000b = 224 µs/step (0.11 mV/µs at 25 mV per step) 001b = 112 µs/step (0.22 mV/µs at 25 mV per step) 010b = 56 µs/step (0.45 mV/µs at 25 mV per step) 011b = 28 µs/step (0.90 mV/µs at 25 mV per step) 100b = 14 µs/step (1.80 mV/µs at 25 mV per step) 101b = 7 µs/step (3.60 mV/µs at 25 mV per step) 110b = 3.5 µs/step (7.2 mV/µs at 25 mV per step) 111b = Immediate; slew rate is only limited by the control loop response time.

8.6.20 LDO1 Control Register (DEFLDO1) (Address = 0x12) [reset = 0x09]

DEFLDO1 is shown in Figure 48 and described in Table 20.

Return to Summary Table.

This register is password protected.

Figure 48. DEFLDO1 Register

DATA BIT	7	6	5	4	3	2	1	0
FIELD NAME	Reserved	Reserved	Reserved	Reserved	LDO1[3:0]			
READ/WRITE	R	R	R	R	R/W	R/W	R/W	R/W
RESET VALUE	0b	0b	0b	0b	1b	0b	0b	1b

Table 20. DEFLDO1 Register Field Descriptions

Bit	Field	Type	Reset	Description	
7–4	Reserved	R	0000b	These bits are reserved	
3–0	LDO1[3:0]	R/W	1001b	LDO1 output voltage setting	
				0000b = 1 V 0001b = 1.1 V 0010b = 1.2 V 0011b = 1.25 V 0100b = 1.3 V 0101b = 1.35 V 0110b = 1.4 V 0111b = 1.5 V	1000b = 1.6 V 1001b = 1.8 V 1010b = 2.5 V 1011b = 2.75 V 1100b = 2.8 V 1101b = 3 V 1110b = 3.1 V 1111b = 3.3 V

8.6.21 LDO2 Control Register (DEFLDO2) (Address = 0x13) [reset = 0x38]

DEFLDO2 is shown in Figure 49 and described in Table 21.

Return to Summary Table.

This register is password protected.

Figure 49. DEFLDO2 Register

DATA BIT	7	6	5	4	3	2	1	0
FIELD NAME	Reserved	TRACK	LDO2[5:0]					
READ/WRITE	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET VALUE	0b	0b	1b	1b	1b	0b	0b	0b

Table 21. DEFLDO2 Register Field Descriptions

Bit	Field	Type	Reset	Description			
7	Reserved	R	0b	This bit is reserved			
6	TRACK	R/W	0b	LDO2 tracking bit 0b = Output voltage is defined by the LDO2[5:0] bits. 1b = Output voltage follows the DCDC3 voltage setting (DEFDCDC3 register).			
5–0	LDO2[5:0]	R/W	11 1000b	LDO2 output voltage setting			
				00 0000b = 0.9 V	01 0000b = 1.3 V	10 0000b = 1.9 V	11 0000b = 2.7 V
				00 0001b = 0.925 V	01 0001b = 1.325 V	10 0001b = 1.95 V	11 0001b = 2.75 V
				00 0010b = 0.95 V	01 0010b = 1.35 V	10 0010b = 2 V	11 0010b = 2.8 V
				00 0011b = 0.975 V	01 0011b = 1.375 V	10 0011b = 2.05 V	11 0011b = 2.85 V
				00 0100b = 1 V	01 0100b = 1.4 V	10 0100b = 2.1 V	11 0100b = 2.9 V
				00 0101b = 1.025 V	01 0101b = 1.425 V	10 0101b = 2.15 V	11 0101b = 3 V
				00 0110b = 1.05 V	01 0110b = 1.45 V	10 0110b = 2.2 V	11 0110b = 3.1 V
				00 0111b = 1.075 V	01 0111b = 1.475 V	10 0111b = 2.25 V	11 0111b = 3.2 V
				00 1000b = 1.1 V	01 1000b = 1.5 V	10 1000b = 2.3 V	11 1000b = 3.3 V
				00 1001b = 1.125 V	01 1001b = 1.55 V	10 1001b = 2.35 V	11 1001b = 3.3 V
				00 1010b = 1.15 V	01 1010b = 1.60 V	10 1010b = 2.4 V	11 1010b = 3.3 V
				00 1011b = 1.175 V	01 1011b = 1.65 V	10 1011b = 2.45 V	11 1011b = 3.3 V
				00 1100b = 1.2 V	01 1100b = 1.7 V	10 1100b = 2.5 V	11 1100b = 3.3 V
				00 1101b = 1.225 V	01 1101b = 1.75 V	10 1101b = 2.55 V	11 1101b = 3.3 V
				00 1110b = 1.25 V	01 1110b = 1.8 V	10 1110b = 2.6 V	11 1110b = 3.3 V
				00 1111b = 1.275 V	01 1111b = 1.85 V	10 1111b = 2.65 V	11 1111b = 3.3 V

8.6.22 Load Switch1 or LDO3 Control Register (DEFLS1) (Address = 0x14) [reset = X]

DEFLS1 is shown in Figure 50 and described in Table 22.

Return to Summary Table.

This register is password protected.

Figure 50. DEFLS1 Register

DATA BIT		7	6	5	4	3	2	1	0
FIELD NAME		Reserved	Reserved	LS1LDO3	LDO3[4:0]				
READ/WRITE		R	R	R/W	R/W	R/W	R/W	R/W	R/W
RESET VALUE	TPS65217A	0b	0b	0b	0b	0b	1b	1b	0b
	TPS65217B	0b	0b	1b	1b	1b	1b	1b	1b
	TPS65217C	0b	0b	1b	0b	0b	1b	1b	0b
	TPS65217D	0b	0b	1b	0b	0b	1b	1b	0b

Table 22. DEFLS1 Register Field Descriptions

Bit	Field	Type	Reset	Description	
7–6	Reserved	R	00b	This bit is reserved	
5	LS1LDO3	R/W	TPS65217A: 0b TPS65217B: 1b TPS65217C: 1b TPS65217D: 1b	LS or LDO tracking bit 0b = FET functions as load switch (LS1). 1b = FET is configured as LDO3.	
4–0	LDO3[4:0]	R/W	TPS65217A: 0 0110b TPS65217B: 1 1111b TPS65217C: 0 0110b TPS65217D: 0 0110b	LDO3 output voltage setting (LS1LDO3 = 1b)	
				0 0000b = 1.5 V	1 0000b = 2.55 V
				0 0001b = 1.55 V	1 0001b = 2.6 V
				0 0010b = 1.6 V	1 0010b = 2.65 V
				0 0011b = 1.65 V	1 0011b = 2.7 V
				0 0100b = 1.7 V	1 0100b = 2.75 V
				0 0101b = 1.75 V	1 0101b = 2.8 V
				0 0110b = 1.8 V	1 0110b = 2.85 V
				0 0111b = 1.85 V	1 0111b = 2.9 V
				0 1000b = 1.90V	1 1000b = 2.95 V
				0 1001b = 2 V	1 1001b = 3 V
				0 1010b = 2.1 V	1 1010b = 3.05 V
				0 1011b = 2.2 V	1 1011b = 3.1 V
				0 1100b = 2.3 V	1 1100b = 3.15 V
				0 1101b = 2.4 V	1 1101b = 3.2 V
				0 1110b = 2.45 V	1 1110b = 3.25 V
				0 1111b = 2.5 V	1 1111b = 3.3 V

8.6.23 Load Switch2 or LDO4 Control Register (DEFLS2) (Address = 0x15) [reset = X]

DEFLS2 is shown in Figure 51 and described in Table 23.

Return to Summary Table.

This register is password protected.

Figure 51. DEFLS2 Register

DATA BIT		7	6	5	4	3	2	1	0
FIELD NAME		Reserved	Reserved	LS2LDO4	LDO4[4:0]				
READ/WRITE		R	R	R/W	R/W	R/W	R/W	R/W	R/W
RESET VALUE	TPS65217A	0b	0b	0b	1b	0b	1b	0b	1b
	TPS65217B	0b	0b	1b	1b	1b	1b	1b	1b
	TPS65217C	0b	0b	1b	1b	1b	1b	1b	1b
	TPS65217D	0b	0b	1b	1b	1b	1b	1b	1b

Table 23. DEFLS2 Register Field Descriptions

Bit	Field	Type	Reset	Description	
7–6	Reserved	R	00b	These bits are reserved	
5	LS2LDO4	R/W	TPS65217A: 0b TPS65217B: 1b TPS65217C: 1b TPS65217D: 1b	LS or LDO configuration bit 0b = FET functions as load a switch (LS2). 1b = FET is configured as LDO4.	
4–0	LDO4[4:0]	R/W	TPS65217A: 1 0101b TPS65217B: 1 1111b TPS65217C: 1 1111b TPS65217D: 1 1111b	LDO4 output voltage setting (LS2LDO4 = 1b)	
				0 0000b = 1.5 V	1 0000b = 2.55 V
				0 0001b = 1.55 V	1 0001b = 2.6 V
				0 0010b = 1.6 V	1 0010b = 2.65 V
				0 0011b = 1.65 V	1 0011b = 2.7 V
				0 0100b = 1.7 V	1 0100b = 2.75 V
				0 0101b = 1.75 V	1 0101b = 2.8 V
				0 0110b = 1.8 V	1 0110b = 2.85 V
				0 0111b = 1.85 V	1 0111b = 2.9 V
				0 1000b = 1.9 V	1 1000b = 2.95 V
				0 1001b = 2 V	1 1001b = 3 V
				0 1010b = 2.1 V	1 1010b = 3.05 V
				0 1011b = 2.2 V	1 1011b = 3.1 V
				0 1100b = 2.3 V	1 1100b = 3.15 V
				0 1101b = 2.4 V	1 1101b = 3.2 V
				0 1110b = 2.45 V	1 1110b = 3.25 V
				0 1111b = 2.5 V	1 1111b = 3.3 V

8.6.24 Enable Register (ENABLE) (Address = 0x16) [reset = 0x00]

ENABLE is shown in Figure 52 and described in Table 24.

Return to Summary Table.

This register is password protected.

Figure 52. ENABLE Register

DATA BIT	7	6	5	4	3	2	1	0
FIELD NAME	Reserved	LS1_EN	LS2_EN	DC1_EN	DC2_EN	DC3_EN	LDO1_EN	LDO2_EN
READ/WRITE	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET VALUE	0b	0b	0b	0b	0b	0b	0b	0b

Table 24. ENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R	0b	This bit is reserved
6	LS1_EN	R/W	0b	LSW1 or LDO3 enable bit NOTE: PWR_EN pin must be high to enable LS1 or LDO3. 0b = Disabled 1b = Enabled
5	LS2_EN	R/W	0b	LS2 or LDO4 enable bit NOTE: PWR_EN pin must be high to enable LS2 or LDO4. 0b = Disabled 1b = Enabled
4	DC1_EN	R/W	0b	DCDC1 enable bit NOTE: PWR_EN pin must be high to enable the DC/DC converter. 0b = DCDC1 is disabled. 1b = DCDC1 is enabled.
3	DC2_EN	R/W	0b	DCDC2 enable bit NOTE: PWR_EN pin must be high to enable the DC/DC converter. 0b = DCDC2 is disabled. 1b = DCDC2 is enabled.
2	DC3_EN	R/W	0b	DCDC3 enable bit NOTE: PWR_EN pin must be high to enable the DC/DC converter. 0b = DCDC3 is disabled. 1b = DCDC3 is enabled.
1	LDO1_EN	R/W	0b	LDO1 enable bit 0b = Disabled 1b = Enabled
0	LDO2_EN	R/W	0b	LDO2 enable bit 0b = Disabled 1b = Enabled

8.6.25 UVLO Control Register (DEFUVLO) (Address = 0x18) [reset = 0x03]

DEFUVLO is shown in Figure 53 and described in Table 25.

Return to Summary Table.

This register is password protected.

Figure 53. DEFUVLO Register

DATA BIT	7	6	5	4	3	2	1	0
FIELD NAME	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	UVLO[1:0]	
READ/WRITE	R	R	R	R	R	R/W	R/W	R/W
RESET VALUE	0b	0b	0b	0b	0b	0b	1b	1b

Table 25. DEFUVLO Register Field Descriptions

Bit	Field	Type	Reset	Description
7–3	Reserved	R	00000b	These bits are reserved
2	Reserved	R/W	0b	This bit is reserved
1–0	UVLO[1:0]	R/W	11b	Undervoltage lockout setting 00b = 2.73 V 01b = 2.89 V 10b = 3.18 V 11b = 3.3 V

8.6.26 Sequencer Register 1 (SEQ1) (Address = 0x19) [reset = X]

SEQ1 is shown in Figure 54 and described in Table 26.

Return to Summary Table.

This register is password protected.

Figure 54. SEQ1 Register

DATA BIT		7	6	5	4	3	2	1	0
FIELD NAME		Reserved	DC1_SEQ[2:0]			Reserved	DC2_SEQ[2:0]		
READ/WRITE		R	R/W	R/W	R/W	R	R/W	R/W	R/W
RESET VALUE	TPS65217A	0b	0b	0b	1b	0b	0b	1b	0b
	TPS65217B	0b	0b	0b	1b	0b	1b	0b	1b
	TPS65217C	0b	0b	0b	1b	0b	1b	0b	1b
	TPS65217D	0b	0b	0b	1b	0b	1b	0b	1b

Table 26. SEQ1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R	0b	This bit is reserved
6–4	DC1_SEQ[3:0]	R/W	TPS65217A: 0001b TPS65217B: 0001b TPS65217C: 0001b TPS65217D: 0001b	DCDC1 enable STROBE 0000b = Rail is not controlled by sequencer. 0001b = Enable at STROBE1 0010b = Enable at STROBE2 0011b = Enable at STROBE3 0100b = Enable at STROBE4 0101b = Enable at STROBE5 0110b = Enable at STROBE6 0111b = Enable at STROBE7
3	Reserved	R	0b	This bit is reserved
2–0	DC2_SEQ[3:0]	R/W	TPS65217A: 0010b TPS65217B: 0101b TPS65217C: 0101b TPS65217D: 0101b	DCDC2 enable STROBE 0000b = Rail is not controlled by sequencer. 0001b = Enable at STROBE1 0010b = Enable at STROBE2 0011b = Enable at STROBE3 0100b = Enable at STROBE4 0101b = Enable at STROBE5 0110b = Enable at STROBE6 0111b = Enable at STROBE7

8.6.27 Sequencer Register 2 (SEQ2) (Address = 0x1A) [reset = X]

SEQ2 is shown in Figure 55 and described in Table 27.

Return to Summary Table.

This register is password protected.

Figure 55. SEQ2 Register

DATA BIT		7	6	5	4	3	2	1	0
FIELD NAME		Reserved	DC3_SEQ[2:0]			LDO1_SEQ[3:0]			
READ/WRITE		R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET VALUE	TPS65217A	0b	0b	1b	1b	1b	0b	1b	1b
	TPS65217B	0b	1b	0b	1b	1b	1b	1b	1b
	TPS65217C	0b	1b	0b	1b	1b	1b	1b	1b
	TPS65217D	0b	1b	0b	1b	1b	1b	1b	1b

Table 27. SEQ2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R	0b	This bit is reserved
6–4	DC3_SEQ[2:0]	R/W	TPS65217A: 011b TPS65217B: 101b TPS65217C: 101b TPS65217D: 101b	DCDC3 enable STROBE 000b = Rail is not controlled by sequencer. 001b = Enable at STROBE1 010b = Enable at STROBE2 011b = Enable at STROBE3 100b = Enable at STROBE4 101b = Enable at STROBE5 110b = Enable at STROBE6 111b = Enable at STROBE7
3–0	LDO1_SEQ [3:0]	R/W	TPS65217A: 1011b TPS65217B: 1111b TPS65217C: 1111b TPS65217D: 1111b	LDO1 enable state 0000b = Rail is not controlled by sequencer. 0001b = Enable at STROBE1 0010b = Enable at STROBE2 0011b = Enable at STROBE3 0100b = Enable at STROBE4 0101b = Enable at STROBE5 0110b = Enable at STROBE6 0111b = Enable at STROBE7 1000b = Rail is not controlled by sequencer 1001b = Rail is not controlled by sequencer 1010b to 1101b = Reserved 1110b = Enable at STROBE14 1111b = Enabled at STROBE15 (with SYS)

8.6.28 Sequencer Register 3 (SEQ3) (Address = 0x1B) [reset = X]

SEQ3 is shown in Figure 56 and described in Table 28.

Return to Summary Table.

This register is password protected.

Figure 56. SEQ3 Register

DATA BIT		7	6	5	4	3	2	1	0
FIELD NAME		LDO2_SEQ[3:0]				Reserved	LDO3_SEQ[2:0]		
READ/WRITE		R/W	R/W	R/W	R/W	R	R/W	R/W	R/W
RESET VALUE	TPS65217A	0b	0b	1b	0b	0b	0b	0b	1b
	TPS65217B	0b	0b	1b	0b	0b	0b	1b	1b
	TPS65217C	0b	0b	1b	1b	0b	0b	1b	0b
	TPS65217D	0b	0b	1b	1b	0b	0b	1b	0b

Table 28. SEQ3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7–4	LDO2_SEQ[3:0]	R/W	TPS65217A: 0010b TPS65217B: 0010b TPS65217C: 0011b TPS65217D: 0011b	LDO2 enable STROBE 0000b = Rail is not controlled by sequencer. 0001b = Enable at STROBE1 0010b = Enable at STROBE2 0011b = Enable at STROBE3 0100b = Enable at STROBE4 0101b = Enable at STROBE5 0110b = Enable at STROBE6 0111b = Enable at STROBE7 1000b = Rail is not controlled by sequencer. 1001b = Rail is not controlled by sequencer. 1010b to 1101b = Reserved 1110b = Enable at STROBE14 1111b = Enabled at STROBE15 (with SYS)
3	Reserved	R	0b	This bit is reserved
2–0	LDO3_SEQ[2:0]	R/W	TPS65217A: 001b TPS65217B: 011b TPS65217C: 010b TPS65217D: 010b	LS1 or LDO3 enable state 000b = Rail is not controlled by sequencer 001b = Enable at STROBE1 010b = Enable at STROBE2 011b = Enable at STROBE3 100b = Enable at STROBE4 101b = Enable at STROBE5 110b = Enable at STROBE6 111b = Enable at STROBE7

8.6.29 Sequencer Register 4 (SEQ4) (Address = 0x1C) [reset = 0x40]

SEQ4 is shown in Figure 57 and described in Table 29.

Return to Summary Table.

This register is password protected.

Figure 57. SEQ4 Register

DATA BIT	7	6	5	4	3	2	1	0
FIELD NAME	Reserved	LDO4_SEQ[2:0]			Reserved	Reserved	Reserved	Reserved
READ/WRITE	R	R/W	R/W	R/W	R	R	R	R
RESET VALUE	0b	1b	0b	0b	0b	0b	0b	0b

Table 29. SEQ4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R	0b	This bit is reserved
6–4	LDO4_SEQ[2:0]	R/W	100b	LS2 or LDO4 enable state 0000b = Rail is not controlled by sequencer. 0001b = Enable at STROBE1 0010b = Enable at STROBE2 0011b = Enable at STROBE3 0100b = Enable at STROBE4 0101b = Enable at STROBE5 0110b = Enable at STROBE6 0111b = Enable at STROBE7
3–0	Reserved	R	0000b	These bits are reserved

8.6.30 Sequencer Register 5 (SEQ5) (Address = 0x1D) [reset = X]

SEQ5 is shown in Figure 58 and described in Table 30.

Return to Summary Table.

This register is password protected.

Figure 58. SEQ5 Register

DATA BIT		7	6	5	4	3	2	1	0
FIELD NAME		DLY1[1:0]		DLY2[1:0]		DLY3[1:0]		DLY4[1:0]	
READ/WRITE		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET VALUE	TPS65217A	1b	0b	0b	0b	0b	0b	0b	0b
	TPS65217B	1b	0b	0b	0b	0b	0b	0b	0b
	TPS65217C	0b	0b	1b	0b	0b	0b	0b	0b
	TPS65217D	0b	0b	1b	0b	0b	0b	0b	0b

Table 30. SEQ5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7–6	DLY1[1:0]	R/W	TPS65217A: 10b TPS65217B: 10b TPS65217C: 00b TPS65217D: 00b	Delay1 time 00b = 1 ms 01b = 2 ms 10b = 5 ms 11b = 10 ms
5–4	DLY2[1:0]	R/W	TPS65217A: 00b TPS65217B: 00b TPS65217C: 10b TPS65217D: 10b	Delay2 time 00b = 1 ms 01b = 2 ms 10b = 5 ms 11b = 10 ms
3–2	DLY3[1:0]	R/W	00b	Delay3 time 00b = 1 ms 01b = 2 ms 10b = 5 ms 11b = 10 ms
1–0	DLY4[1:0]	R/W	00b	Delay4 time 00b = 1 ms 01b = 2 ms 10b = 5 ms 11b = 10 ms

8.6.31 Sequencer Register 6 (SEQ6) (Address = 0x1E) [reset = 0x00]

SEQ6 is shown in Figure 59 and described in Table 31.

Return to Summary Table.

This register is password protected.

Figure 59. SEQ6 Register

DATA BIT	7	6	5	4	3	2	1	0
FIELD NAME	DLY5[1:0]		DLY6[1:0]		Reserved	SEQUP	SEQDWN	INSTDWN
READ/WRITE	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W
RESET VALUE	0b	0b	0b	0b	0b	0b	0b	0b

Table 31. SEQ6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7–6	DLY5[1:0]	R/W	00b	Delay5 time 00b = 1 ms 01b = 2 ms 10b = 5 ms 11b = 10 ms
5–4	DLY6[1:0]	R/W	00b	Delay6 time 00b = 1 ms 01b = 2 ms 10b = 5 ms 11b = 10 ms
3	Reserved	R	0b	This bit is reserved
2	SEQUP	R/W	0b	Set this bit to 1b to trigger a power-up sequence. This bit is automatically reset to 0b.
1	SEQDWN	R/W	0b	Set this bit to 1b to trigger a power-down sequence. This bit is automatically reset to 0b.
0	INSTDWN	R/W	0b	Instant shutdown bit NOTE: Shutdown occurs when the PWR_EN pin is pulled low or the SEQDWN bit is set. Only those rails controlled by the sequencer are shut down. 0b = Shutdown follows reverse power-up sequence 1b = All delays are bypassed and all rails are shut down at the same time.

9 Application and Implementation

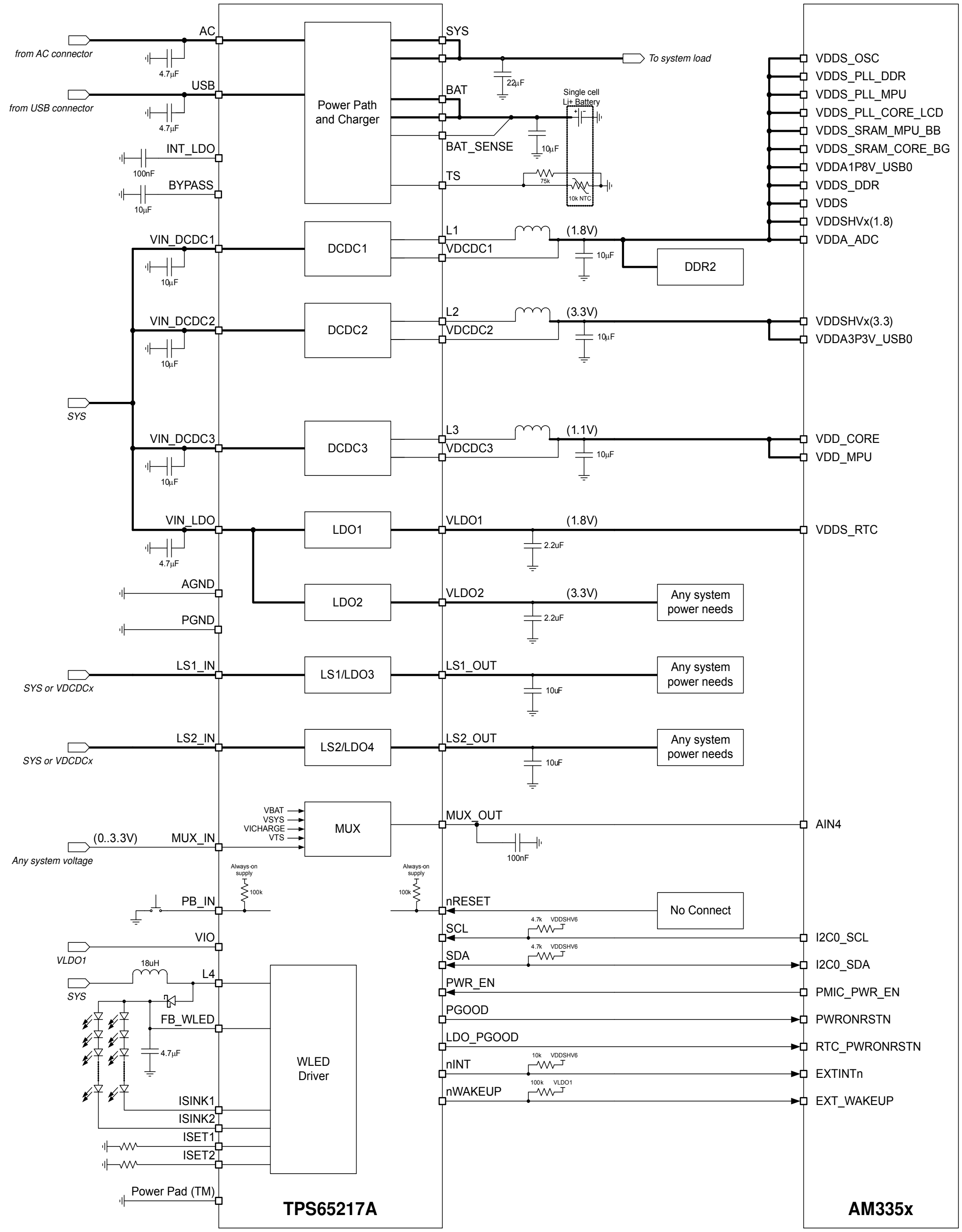
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS65217x device is designed to pair with various application processors. For detailed information on using the TPS65217x device with Sitara AM335x processors, refer to the *Powering the AM335x with the TPS65217x* user's guide.

9.2 Typical Application



For connection diagrams for all members of the TPS65217x family, refer to the *Powering the AM335x with the TPS65217x* user's guide.

Figure 60. Connection Diagram for Typical Application

Typical Application (continued)

9.2.1 Design Requirements

For this design example, use the parameters listed in Table 32.

Table 32. Design Requirements

RAIL	VOLTAGE	SEQUENCE
DCDC1	1.8 V	1
DCDC2	3.3 V	2
DCDC3	1.1 V	3
LDO1	1.8 V	15
LDO2	3.3 V	2
LS1 or LDO3	Load switch	1
LS2 or LDO4	Load switch	4

9.2.2 Detailed Design Procedure

Table 33 lists the recommended inductors for the WLED boost converter. Table 34 lists the recommended capacitor for the WLED boost converter.

Table 33. Recommended Inductors for WLED Boost Converter

PART NUMBER	SUPPLIER	VALUE (µH)	R_{DS} (mΩ) MAX	RATED CURRENT (A)	DIMENSIONS (mm × mm × mm)
CDRH74NP-180M	Sumida	18	73	1.31	7.5 × 7.5 × 4.5
P1167.183	Pulse	18	37	1.5	7.5 × 7.5 × 4.5

Table 34. Recommended Output Capacitor for WLED Boost Converter

PART NUMBER	SUPPLIER	VOLTAGE RATING (V)	VALUE (µF)	DIMENSIONS	DIELECTRIC
UMK316BJ475ML-T	Taiyo Yuden	50	4.7	1206	X5R

9.2.2.1 Output Filter Design (Inductor and Output Capacitor)

9.2.2.1.1 Inductor Selection for Buck Converters

The step-down converters operate typically with 2.2-µH output inductors. Larger or smaller inductor values can be used to optimize the performance of the device for specific operation conditions. The selected inductor must be rated for its dc resistance and saturation current. The dc resistance of the inductance directly influences the efficiency of the converter. Therefore, an inductor with the lowest dc resistance should be selected for highest efficiency.

Use Equation 4 to calculate the maximum inductor current under static load conditions. The saturation current of the inductor should be rated higher than the maximum inductor current, because, during heavy load transients, the inductor current increases to a value greater than the calculated value.

$$I_{L\,max} = I_{OUT\,max} + \frac{\Delta I_L}{2}$$

where

- I_{Lmax} is the maximum inductor current
- I_{OUTmax} is the maximum output current
- ΔI_L is the peak-to-peak inductor ripple current (see Equation 5) (4)

$$\Delta I_L = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f}$$

where

- L is the inductor value.
- f is the switching frequency (2.25 MHz typical). (5)

The highest inductor current occurs at maximum input voltage (V_{IN}). Open-core inductors have a soft saturation characteristic and can usually support greater inductor currents than a comparable shielded inductor.

A more conservative approach is to select the inductor current rating just for the maximum switch current of the corresponding converter. The core material must be considered because it differs from inductor to inductor and has an impact on the efficiency, especially at high switching frequencies. Also, the resistance of the windings greatly affects the converter efficiency at high load. Table 35 lists the recommended inductors.

Table 35. Recommended Inductors for DCDC1, DCDC2, and DCDC3

PART NUMBER	SUPPLIER	VALUE (µH)	R_{DS} (mΩ) MAX	RATED CURRENT (A)	DIMENSIONS (mm)
LQM2HPN2R2MG0L	Murata	2.2	100	1.3	2 x 2.5 x 0.9
VLCF4018T-2R2N1R4-2	TDK	2.2	60	1.44	3.9 x 4.7 x 1.8

9.2.2.1.2 Output Capacitor Selection

The advanced fast-response voltage-mode control scheme of the two converters lets the use of small ceramic capacitors with a typical value of 10 µF, without having large output-voltage undershoots and overshoots during heavy load transients. Ceramic capacitors having low ESR values result in the lowest output voltage ripple and are therefore recommended.

If ceramic output capacitors are used, the capacitor RMS ripple-current rating must always meet the application requirements. Use Equation 6 to calculate the RMS ripple current ($I_{RMSCout}$).

$$I_{RMSCout} = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f} \times \frac{1}{2 \times \sqrt{3}} \quad (6)$$

At the nominal load current, the inductive converters operate in PWM mode and the overall output voltage ripple is the sum of the voltage spike caused by the output capacitor ESR plus the voltage ripple caused by charging and discharging the output capacitor as shown in Equation 7.

$$\Delta V_{OUT} = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f} \times \left(\frac{1}{8 \times C_{OUT} \times f} + ESR \right)$$

where

- the highest output voltage ripple occurs at the highest input voltage (7)

At light-load currents, the converters operate in power-save mode, and the output-voltage ripple depends on the output capacitor value. The output-voltage ripple is set by the internal comparator delay and the external capacitor. The typical output-voltage ripple is less than 1% of the nominal output voltage.

9.2.2.1.3 Input Capacitor Selection

Because the buck converter has a pulsating input current, a low-ESR input capacitor is required for the best input voltage filtering and to minimize the interference with other circuits caused by high input-voltage spikes. The converters require a ceramic input capacitor of 10 µF. The input capacitor can be increased without any limit for better input voltage filtering. Table 36 lists the recommended ceramic capacitors.

Table 36. Recommended Input Capacitors for DCDC1, DCDC2, and DCDC3

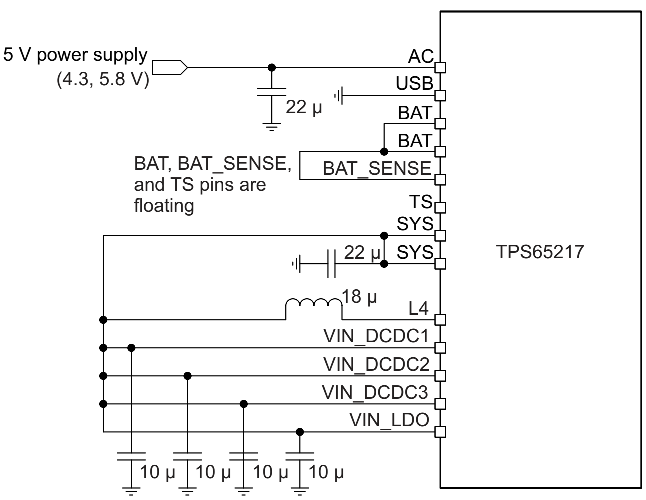
PART NUMBER	SUPPLIER	VALUE (µF)	DIMENSIONS
C2012X5R0J226MT	TDK	22	0805
JMK212BJ226MG	Taiyo Yuden	22	0805
JMK212BJ106M	Taiyo Yuden	10	0805
C2012X5R0J106M	TDK	10	0805

9.2.2.2 5-V Operation Without a Battery

The TPS65217x device has a linear charger for Li+ batteries, and TI recommends that a battery is included in designs for ideal performance. However, the device can operate without a battery attached. Three basic use cases are available for operation without a battery:

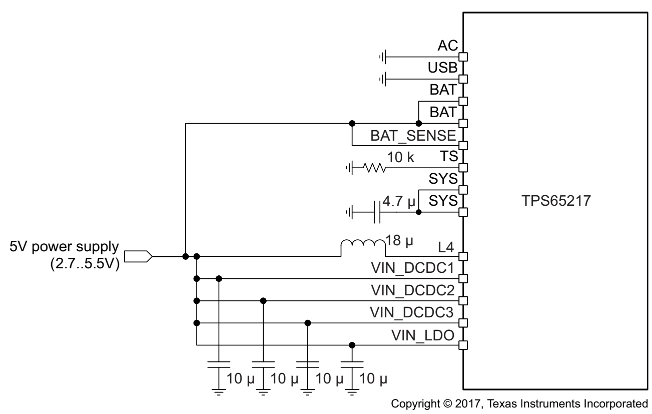
1. The system is designed for battery operation, but the battery is removable and the end user does not have the battery inserted. The system can be powered by connecting an AC adaptor or USB supply.
2. A nonportable system operates on a (regulated) 5-V supply, but the PMIC must provide protection against input overvoltage up to 20 V. Electrically, this case is the same as the previous case where the device is powered by an AC adaptor. The battery pins (BAT and BATSENSE) are shorted together and floating, the temperature sensing pin (TS) is left floating, and power is provided through the AC pin. The DC/DC converters, the WLED driver, and the LDO regulators connect to the overvoltage-protected SYS pins. The load switches (or LDO3 and LDO4, depending on configuration) typically connect to one of the lower system rails, but can also be connected to the SYS pin.
3. A nonportable system operates on a regulated 5-V supply that does not require input overvoltage protection. In this case, the 5-V power supply is connected through the BAT pins. The DC/DC converter inputs, WLED driver, LDO1, and LDO2 are connected directly to the 5-V supply. A standard, constant-value 10-kΩ resistor is connected from the TS pin to ground to simulate the NTC thermistor monitoring the battery. The load switches (or LDO3 and LDO4, depending on configuration) typically connect to one of the lower system rails, but can also be connected directly to the 5-V input supply.

Figure 61 shows the connection of the input power supply to the device for 5-V only operation, with 20-V input overvoltage protection. Figure 62 shows the connection of the input power supply to the device for 5-V only operation without 20-V input overvoltage protection. Table 37 lists the functional differences between both setups.



The SYS node and DC/DC converters are protected against input overvoltage up to 20 V.

Figure 61. Power Connection for 5-V Only Operation With OVP, Without a Battery



(1) The DC/DC converters are not protected against input overvoltage.

Figure 62. Power Connection for 5-V Only Operation Directly Wired to BAT Instead of a Battery

Table 37. Functional Differences Between 5-V Only Operation Without a Battery and With and Without 20-V Input Overvoltage Protection

RESOURCE IMPACTED	POWER SUPPLIED THROUGH AC PIN (CASE (1) AND (2))	POWER SUPPLIED THROUGH BAT PIN (CASE (3))
Input protection	The maximum operating input voltage is 5.8 V, but the device is protected from input overvoltage up to 20 V.	The maximum operating input voltage is 5.5 V.
Power efficiency	The input current for DC/DC converters passes through AC-SYS power-path switch (approximately 150 mΩ).	The internal power path is bypassed to minimize I^2R losses.
BATTEMP bit	The BATTEMP bit (bit 0 in register 0x03) always reads 1, but has no effect on operation of the device.	The BATTEMP bit (bit 0 in register 0x03) always reads 0.
Output rail status on initial power connection	The LDO1 regulator is automatically powered up when the AC pin is connected to the 5-V supply, and the device goes to the **WAIT PWR_EN** state. If the PWR_EN pin is not asserted within 5 s, the LDO1 regulator turns OFF.	The LDO1 regulator is OFF when the BAT pin is connected to the 5-V supply. The PB_IN pin must be pulled low to go to the **WAIT PWR_EN** state. The PB_IN pin cannot stay low for greater than 8 s or a reset will occur.
Response to input overvoltage	Device goes to the **OFF** state.(1)	Not applicable
Power path	In an application with one source of input power, if the input power drops below UVLO and recovers before reaching 100 mV, the rising edge may not be detected by the device. This condition, known as a brownout, can cause a lockup of the device in which the I^2C is responsive but SYS is not connected to the AC or USB through the power path. (2)	Not applicable

(1) If a battery is present in the system, the TPS65217x device automatically switches from using the AC pin as the power supply to using BAT as the supply when the AC input exceeds 6.4 V. The device automatically switches back to supplying power from the AC pin when the AC input recovers and the voltages decreases to less than 5.8 V.

(2) As a workaround, supply power through the BAT input pin or change UVLO to 2.73 V by changing the UVLO[1:0] bits in register 0x18 to 00b. This setting must be changed during initialization after the first power-on event of the device. The bits return to the default value when all I^2C registers reset. As a result, if a brownout condition can occur during the first power-on event, then external circuitry must be added to prevent the TPS65217x device from being affected by the brownout condition.

9.2.3 Application Curves

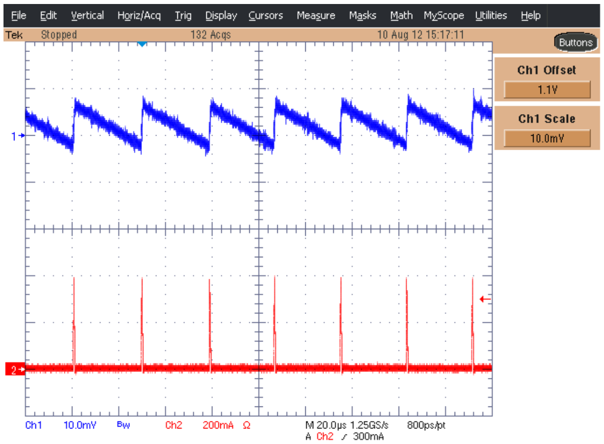


Figure 63. DCDCx Voltage Ripple and Inductor Current at 5 mA Load, 1.1-V V_{OUT}

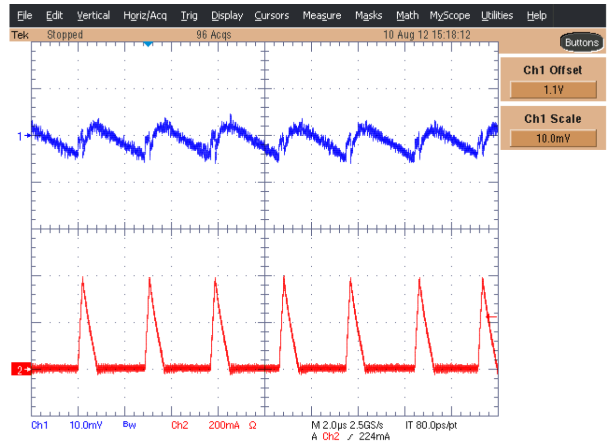


Figure 64. DCDCx Voltage Ripple and Inductor Current at 50 mA Load, 1.1-V V_{OUT}

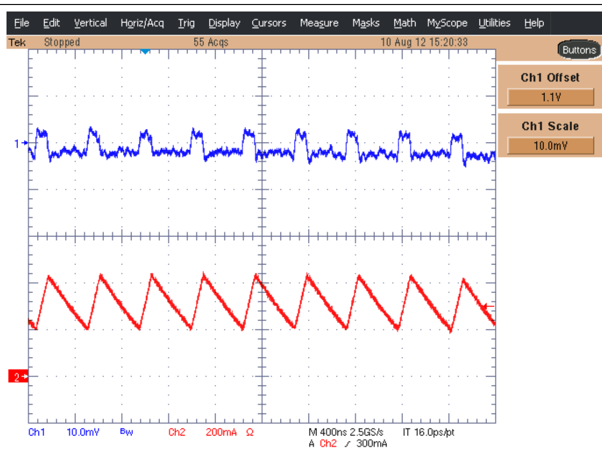


Figure 65. DCDCx Voltage Ripple and Inductor Current at 300 mA Load, 1.1-V V_{OUT}

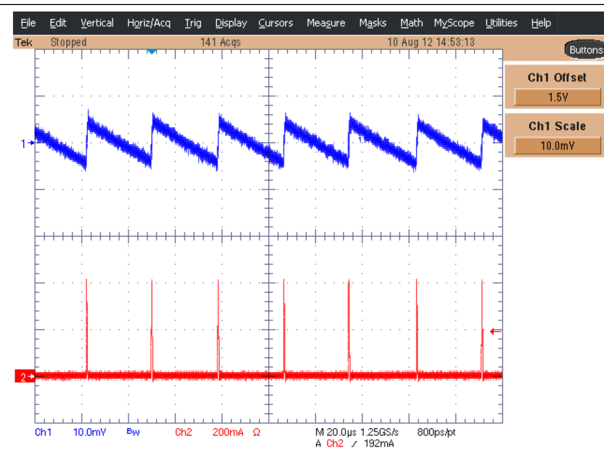


Figure 66. DCDCx Voltage Ripple and Inductor Current at 5 mA Load, 1.5-V V_{OUT}

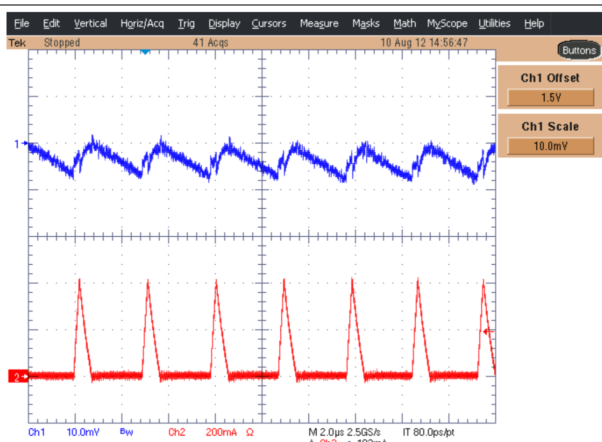


Figure 67. DCDCx Voltage Ripple and Inductor Current at 50 mA Load, 1.5-V V_{OUT}

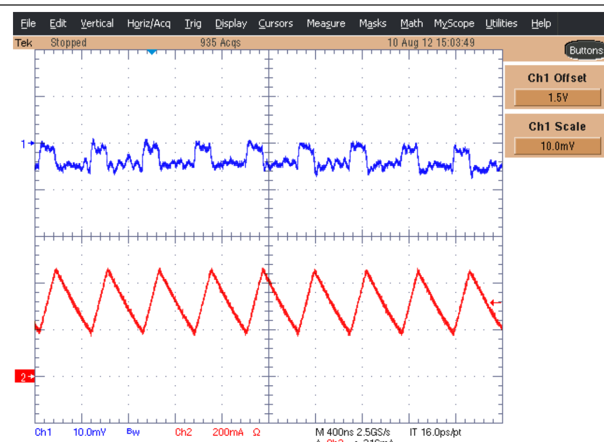


Figure 68. DCDCx Voltage Ripple and Inductor Current at 300 mA Load, 1.5-V V_{OUT}

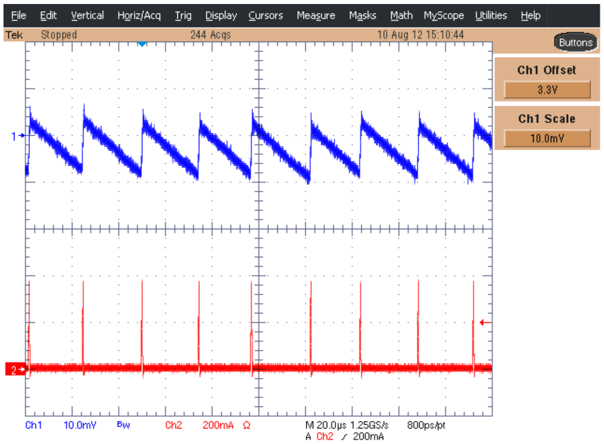


Figure 69. DCDCx Voltage Ripple and Inductor Current at 5 mA Load, 3.3-V V_{OUT}

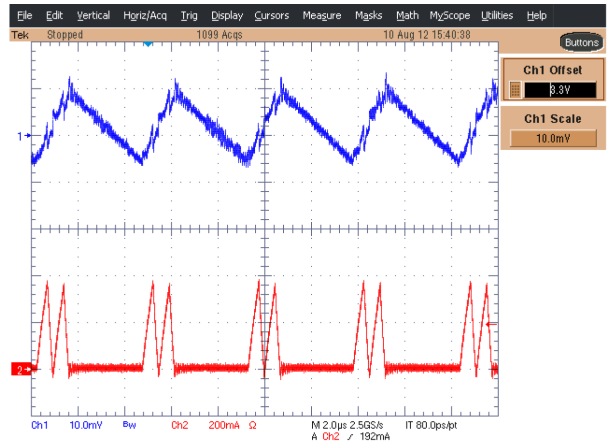


Figure 70. DCDCx Voltage Ripple and Inductor Current at 50 mA Load, 3.3-V V_{OUT}

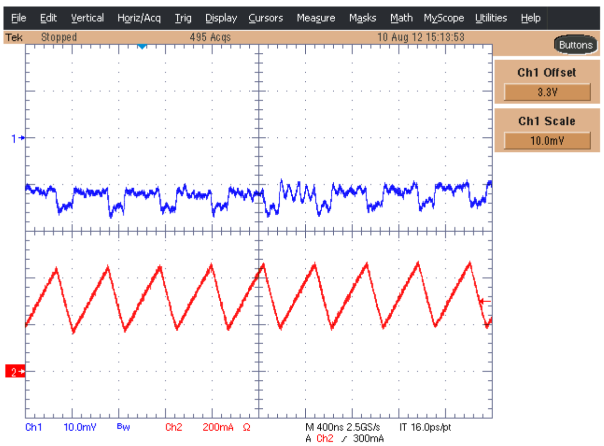


Figure 71. DCDCx Voltage Ripple and Inductor Current at 300 mA Load, 3.3-V V_{OUT}

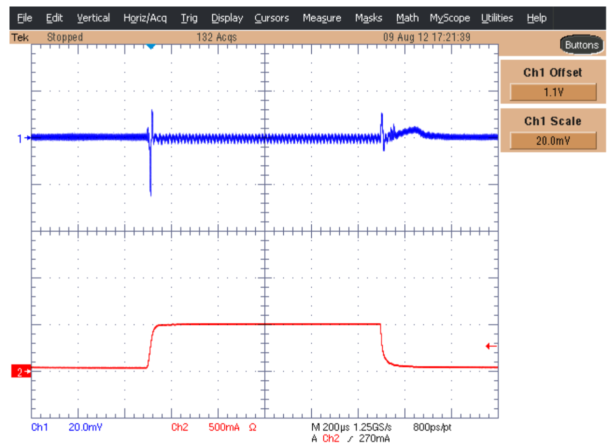


Figure 72. DCDCx Load Transient Response, 1.1 V_{OUT}, 50-500-50 mA Load

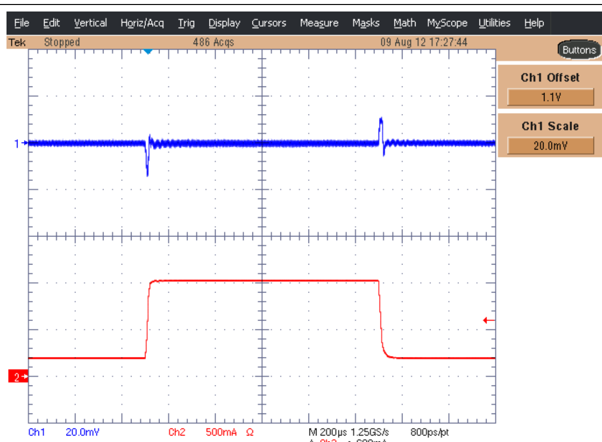


Figure 73. DCDCx Load Transient Response, 1.1 V_{OUT}, 200-1000-200 mA Load

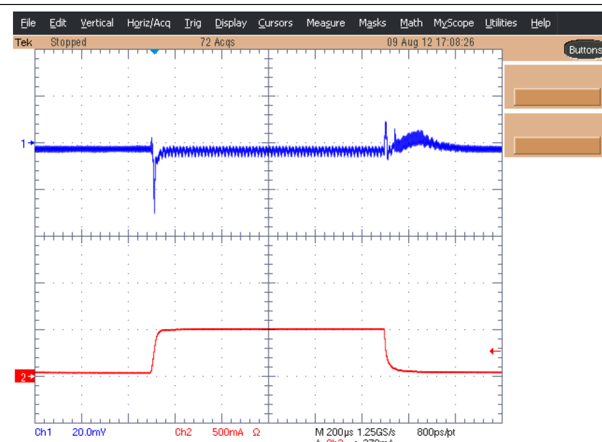


Figure 74. DCDCx Load Transient Response, 1.5 V_{OUT}, 50-500-50 mA Load

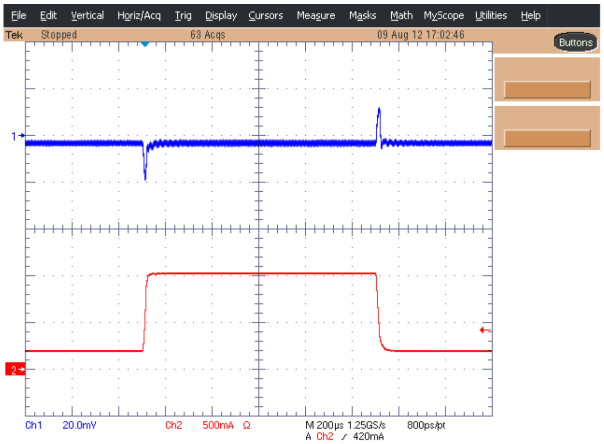


Figure 75. DCDCx Load Transient Response, 1.5 V_{OUT}, 200-1000-200 mA Load

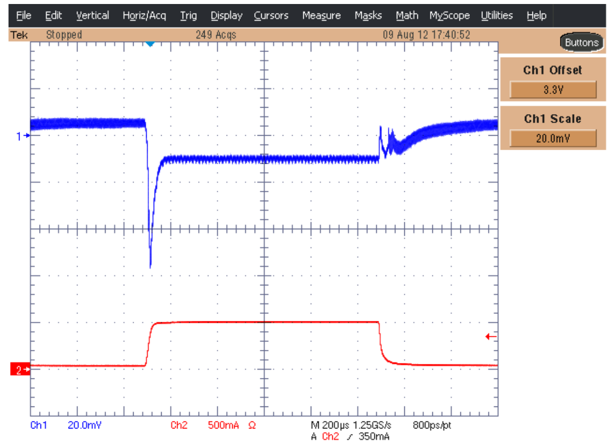


Figure 76. DCDCx Load Transient Response, 3.3 V_{OUT}, 50-500-50 mA Load

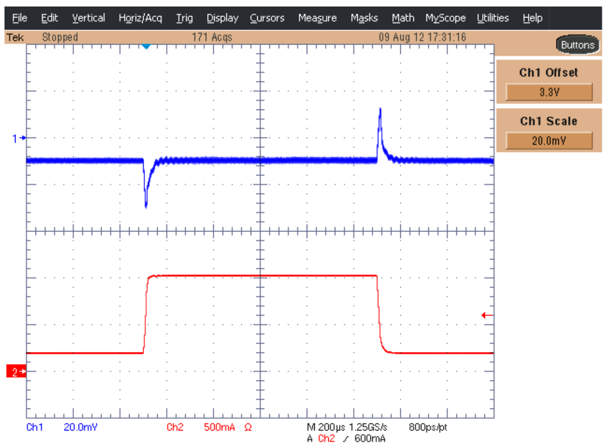


Figure 77. DCDCx Load Transient Response, 3.3 V_{OUT}, 200-1000-200 mA Load

10 Power Supply Recommendations

The device is designed to operate with an input voltage supply range from 2.75 V to 5.8 V. This input supply can be from a single-cell Li-ion, Li-polymer batteries, dc supply, USB supply, or other externally regulated supply. If the input supply is located more than a few inches from the TPS65217x device, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 4.7 µF is a typical choice.

11 Layout

11.1 Layout Guidelines

As for all switching power supplies, the layout is an important step in the design. Proper function of the device requires careful attention to printed circuit-board (PCB) layout. Care must be taken in board layout to get the specified performance.

- The VIN_DCDCx and VINLDO pins should be bypassed to ground with a low-ESR ceramic bypass capacitor. The typical recommended bypass capacitance is 10 μF and 4.7 μF with a X5R or X7R dielectric, respectively.
- The optimum placement of these bypass capacitors is close to the VIN_DCDCx and VINLDO pins of the TPS65217x device. Care should be taken to minimize the loop area formed by the bypass capacitor connection, the VIN_DCDCx and VINLDO pins, and the thermal pad of the device.
- The thermal pad should be tied to the PCB ground plane with multiple vias.
- The inductor traces from the Lx pins to the V_{OUT} node (VDCDCx) of each DCDCx converter should be kept on the PCB top layer and free of any vias.
- The VLDOx and VDCDCx pin (feedback pin labeled FB1 in Figure 78) traces should be routed away from any potential noise source to avoid coupling.
- The DCDCx output capacitance should be placed immediately at the DCDCx pin. Excessive distance between the capacitance and DCDCx pin may cause poor converter performance.

11.2 Layout Example

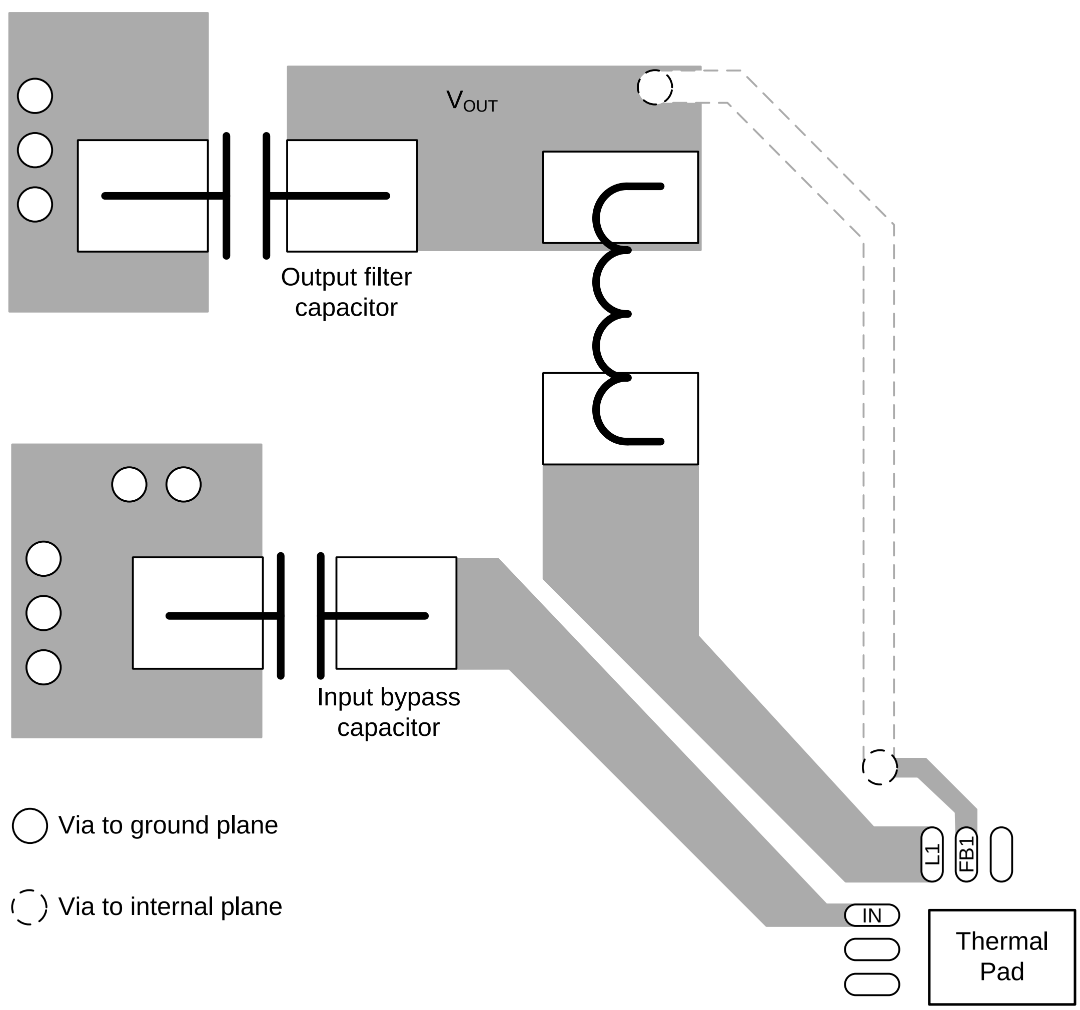


Figure 78. Layout Example Schematic

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Basic Calculation of a Buck Converter's Power Stage* application report
- Texas Instruments, *Designing Robust TPS65217 Systems for V_{IN} Brownout* application report
- Texas Instruments, *Empowering Designs With Power Management IC (PMIC) for Processor Applications* application report
- Texas Instruments, *Evaluation Module for TPS65217 Power Management IC* user's guide
- Texas Instruments, *Powering the AM335x with the TPS65217x* user's guide
- Texas Instruments, *TPS65217x Schematic Checklist*

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 Trademarks

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Sitara is a trademark of Texas Instruments Incorporated.
ARM, Cortex are registered trademarks of ARM Ltd.
All other trademarks are the property of their respective owners.

12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated devices. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS65217ARSLR	ACTIVE	VQFN	RSL	48	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	TPS 65217A	Samples
TPS65217ARSLT	ACTIVE	VQFN	RSL	48	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	TPS 65217A	Samples
TPS65217BRSLR	ACTIVE	VQFN	RSL	48	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	TPS 65217B	Samples
TPS65217BRSLT	ACTIVE	VQFN	RSL	48	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	TPS 65217B	Samples
TPS65217CRSLR	ACTIVE	VQFN	RSL	48	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	TPS 65217C	Samples
TPS65217CRSLT	ACTIVE	VQFN	RSL	48	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	TPS 65217C	Samples
TPS65217DRSLR	ACTIVE	VQFN	RSL	48	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	TPS 65217D	Samples
TPS65217DRSLT	ACTIVE	VQFN	RSL	48	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	TPS 65217D	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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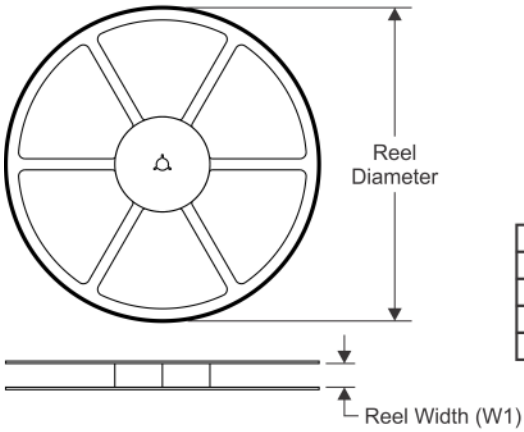
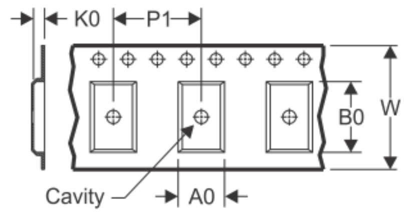
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

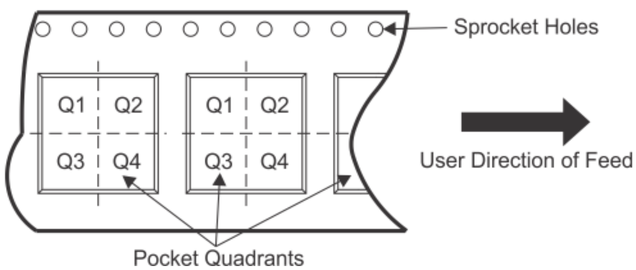


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

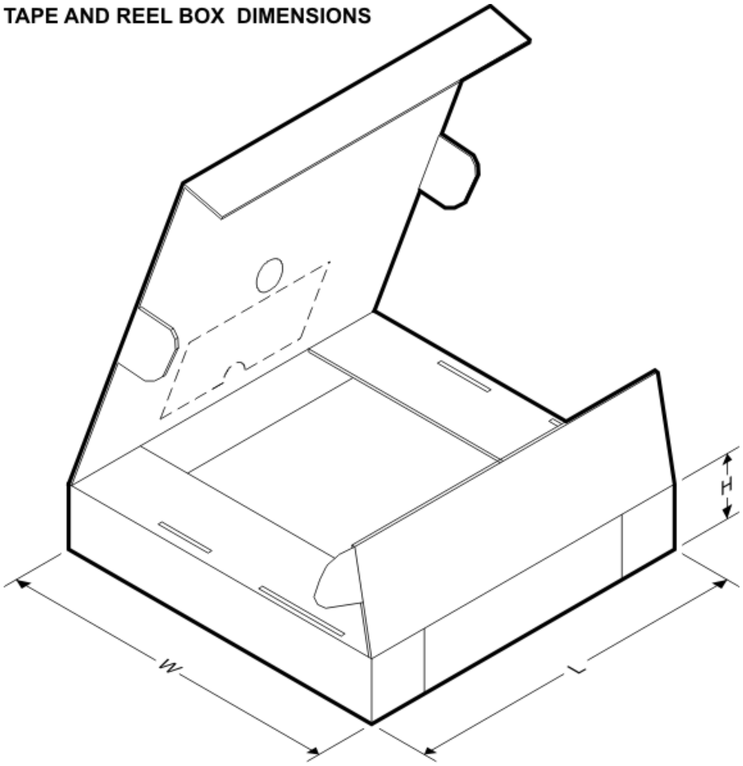
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65217ARSLR	VQFN	RSL	48	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
TPS65217ARSLT	VQFN	RSL	48	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
TPS65217BRSLR	VQFN	RSL	48	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
TPS65217BRSLT	VQFN	RSL	48	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
TPS65217CRSLR	VQFN	RSL	48	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
TPS65217CRSLT	VQFN	RSL	48	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
TPS65217DRSLR	VQFN	RSL	48	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
TPS65217DRSLT	VQFN	RSL	48	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2

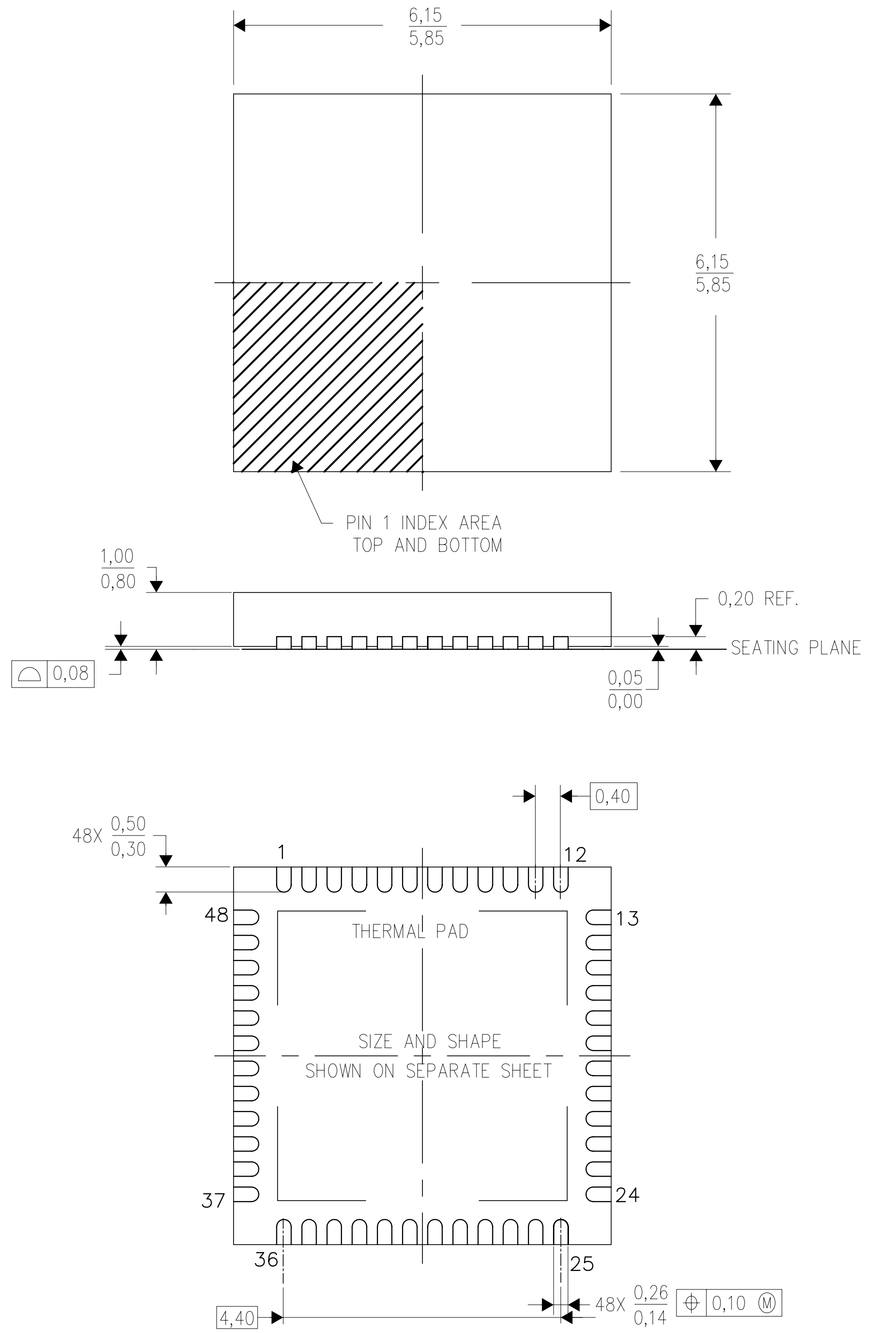
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65217ARSLR	VQFN	RSL	48	2500	367.0	367.0	38.0
TPS65217ARSLT	VQFN	RSL	48	250	210.0	185.0	35.0
TPS65217BRSLR	VQFN	RSL	48	2500	367.0	367.0	38.0
TPS65217BRSLT	VQFN	RSL	48	250	210.0	185.0	35.0
TPS65217CRSLR	VQFN	RSL	48	2500	367.0	367.0	38.0
TPS65217CRSLT	VQFN	RSL	48	250	210.0	185.0	35.0
TPS65217DRSLR	VQFN	RSL	48	2500	367.0	367.0	38.0
TPS65217DRSLT	VQFN	RSL	48	250	210.0	185.0	35.0

RSL (S-PVQFN-N48) PLASTIC QUAD FLATPACK NO-LEAD



4207548/B 06/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No-leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

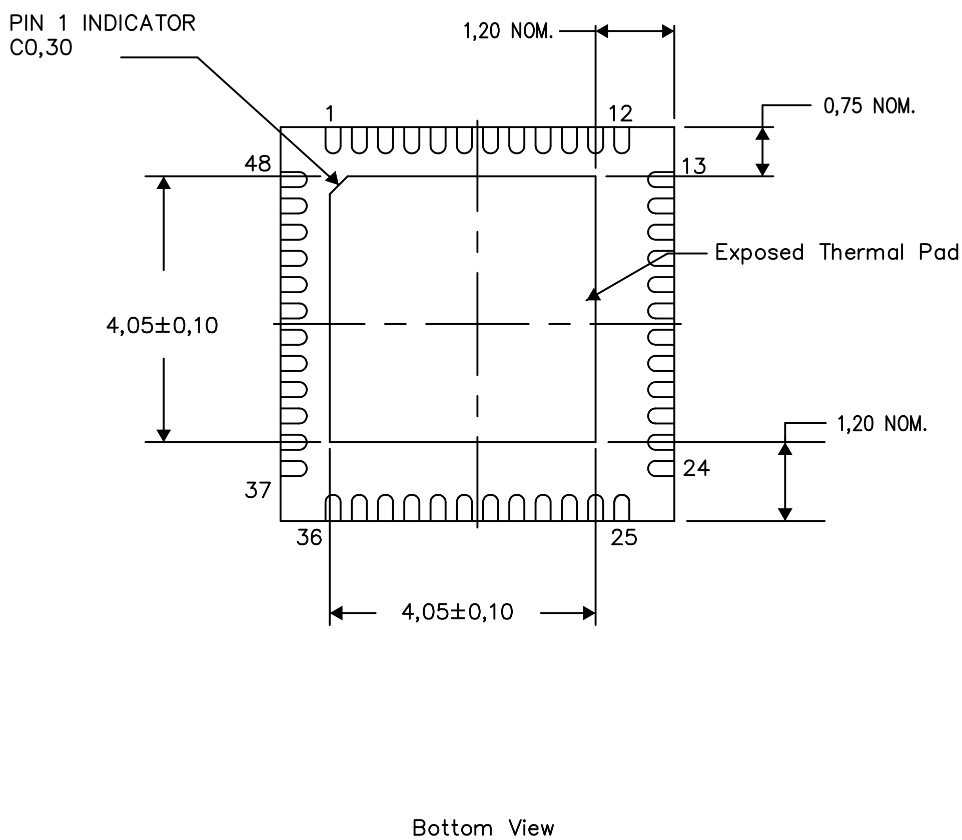
RSL (S-PVQFN-N48) PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

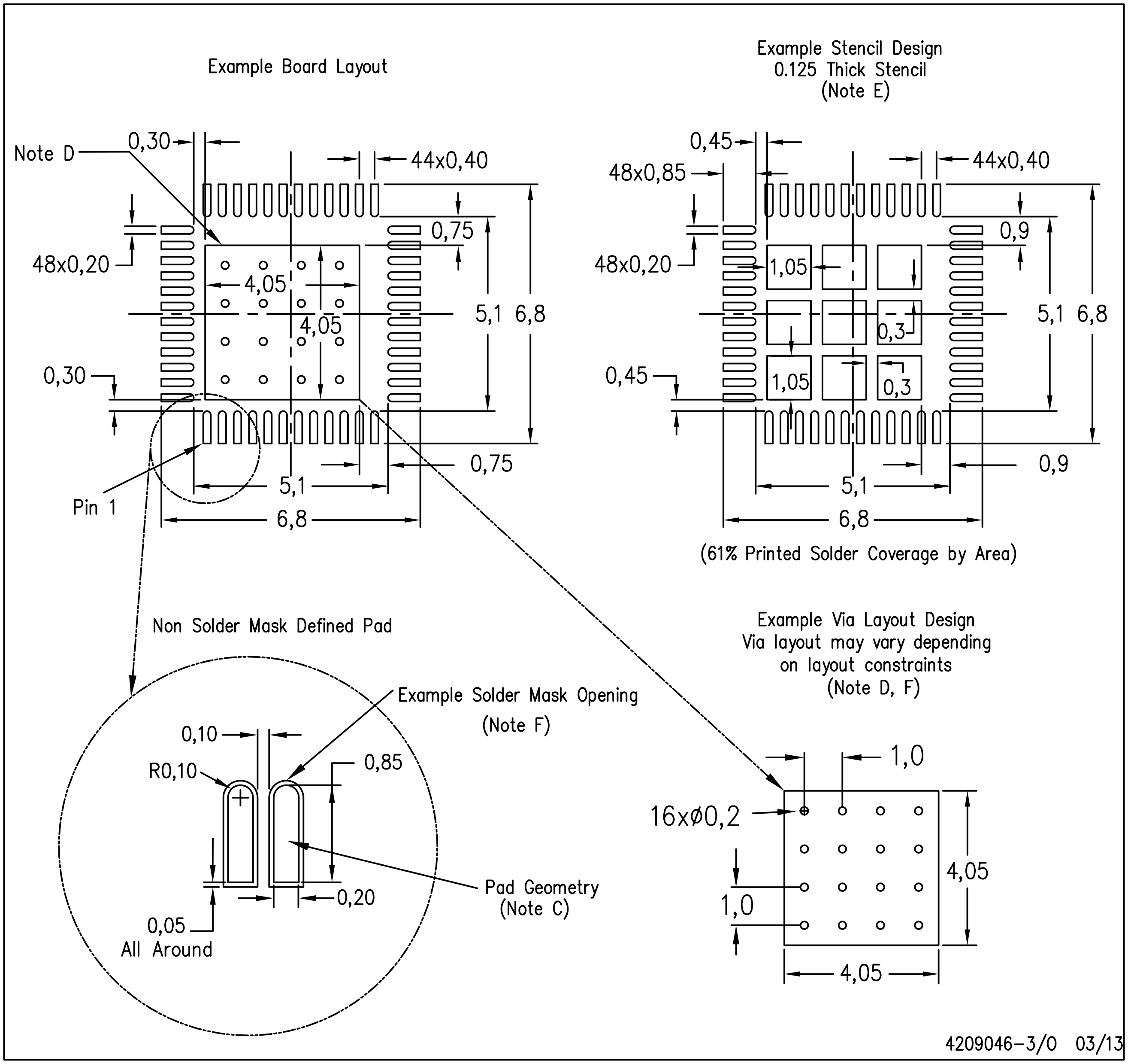


Exposed Thermal Pad Dimensions

4207841-4/P 03/13

NOTE: All linear dimensions are in millimeters

RSL (S-PVQFN-N48) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.