

NL3S2223

High-Speed USB 2.0 (480 Mbps) DPDT Switches

The NL3S2223 is a DPDT switch optimized for high-speed USB 2.0 applications within portable systems. It features ultra-low on capacitance, $C_{ON} = 5.5$ pF (typ), and a bandwidth above 950 MHz. It is optimized for applications that use a single USB interface connector to route multiple signal types. The C_{ON} and R_{ON} of both channels are suitably low to allow the NL3S2223 to pass any speed USB data or audio signals going to a moderately resistive terminal such as an external headset. The device is offered in a UQFN10 1.4 mm x 1.8 mm package.

Features

- Optimized Flow-Through Pinout
- R_{ON} : 5.0 Ω Typ @ $V_{CC} = 4.2$ V
- C_{ON} : 5.5 pF Typ @ $V_{CC} = 3.3$ V
- V_{CC} Range: 1.65 V to 4.5 V
- Typical Bandwidth: 950 MHz
- 1.4 mm x 1.8 mm x 0.50 mm UQFN10
- OVT on Common Signal Pins D+/D- up to 5.25 V
- 8 kV HBM ESD Protection on All Pins
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- High Speed USB 2.0 Data
- Mobile Phones
- Portable Devices

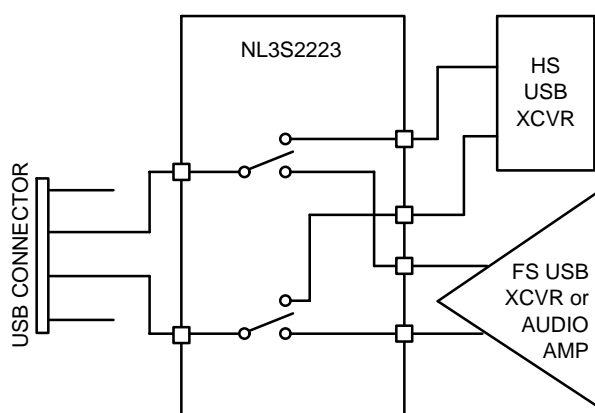


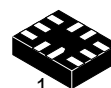
Figure 1. Application Diagram



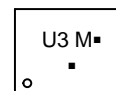
ON Semiconductor®

www.onsemi.com

MARKING DIAGRAM



**UQFN10
CASE 488AT**



U3 = Device Code
M = Date Code
▪ = Pb-Free Device

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NL3S2223MUTBG	UQFN10 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NL3S2223

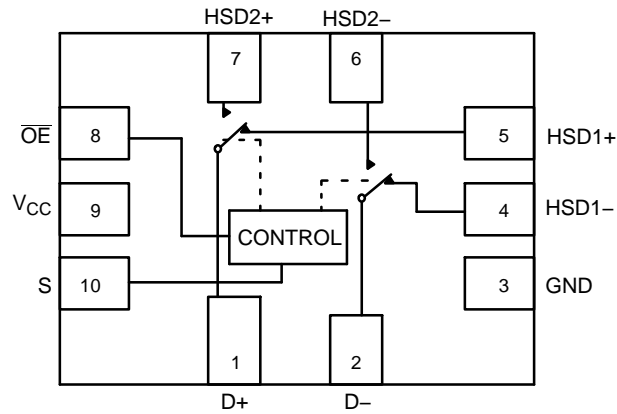


Figure 2. Pin Connections and Logic Diagram (Top View)

Table 1. PIN DESCRIPTION

Pin	Function
S	Control Input
\overline{OE}	Output Enable
HSD1+, HSD1-, HSD2+, HSD2-, D+, D-	Data Ports

Table 2. TRUTH TABLE

\overline{OE}	S	HSD1+, HSD1-	HSD2+, HSD2-
1	X	OFF	OFF
0	0	ON	OFF
0	1	OFF	ON

MAXIMUM RATINGS

Symbol	Pins	Parameter	Value	Unit
V_{CC}	V_{CC}	Positive DC Supply Voltage	-0.5 to +5.5	V
V_{IS}	HSDn+, HSDn-	Analog Signal Voltage	-0.5 to $V_{CC} + 0.3$	V
	D+, D-		-0.5 to +5.25	
V_{IN}	S, \overline{OE}	Control Input Voltage, Output Enable Voltage	-0.5 to +5.5	V
I_{CC}	V_{CC}	Positive DC Supply Current	50	mA
T_S		Storage Temperature	-65 to +150	°C
I_{IS_CON}	HSDn+, HSDn-, D+, D-	Analog Signal Continuous Current-Closed Switch	± 300	mA
I_{IS_PK}	HSDn+, HSDn-, D+, D-	Analog Signal Continuous Current 10% Duty Cycle	± 500	mA
I_{IN}	S, \overline{OE}	Control Input Current, Output Enable Current	± 20	mA
V_{ESD}	HBM MM	Human Body Model Machine Model	8	kV
			400	V
$I_{Latchup}$		Latchup Performance	± 100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

RECOMMENDED OPERATING CONDITIONS

Symbol	Pins	Parameter	Min	Max	Unit
V_{CC}		Positive DC Supply Voltage	1.65	4.5	V
V_{IS}	HSDn+, HSDn-	Analog Signal Voltage	GND	V_{CC}	V
	D+, D-		GND	4.5	
V_{IN}	S, \overline{OE}	Control Input Voltage, Output Enable Voltage	GND	V_{CC}	V
T_A		Operating Temperature	-40	+85	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

CONTROL INPUT, OUTPUT ENABLE VOLTAGE (Typical: T = 25°C)

Symbol	Pins	Parameter	Test Conditions	V _{CC} (V)	-40°C to +85°C			Unit
					Min	Typ	Max	
V _{IH}	S, \overline{OE}	Control Input, Output Enable HIGH Voltage (See Figure 11)		2.7 3.3 4.2	1.25 1.3 1.4	-	-	V
V _{IL}	S, \overline{OE}	Control Input, Output Enable LOW Voltage (See Figure 11)		2.7 3.3 4.2	-	-	0.35 0.4 0.5	V
I _{IN}	S, \overline{OE}	Current Input, Output Enable Leakage Current	0 ≤ V _{IS} ≤ V _{CC}	1.65 – 4.5	-	-	±0.1	μA

SUPPLY CURRENT AND LEAKAGE (Typical: T = 25°C, V_{CC} = 3.3 V)

Symbol	Pins	Parameter	Test Conditions	V _{CC} (V)	-40°C to +85°C			Unit
					Min	Typ	Max	
I _{CC}	V _{CC}	Quiescent Supply Current	0 ≤ V _{IS} ≤ V _{CC} ; I _D = 0 A 0 ≤ V _{IS} ≤ V _{CC} - 0.5 V	1.65 – 3.6 3.6 – 4.5	-	-	0.1 0.1	μA
I _{OZ}		OFF State Leakage	0 ≤ V _{IS} ≤ V _{CC}	1.65 – 4.5	-	±0.1	±0.5	μA
I _{OFF}	D+, D-	Power OFF Leakage Current	0 ≤ V _{IS} ≤ V _{CC}	0	-	-	±0.5	μA

LIMITED V_{IS} SWING ON RESISTANCE (Typical: T = 25°C)

Symbol	Pins	Parameter	Test Conditions	V _{CC} (V)	-40°C to +85°C			Unit
					Min	Typ	Max	
R _{ON}		On-Resistance (Note 1)	I _{ON} = 8 mA V _{IS} = 0 V to 0.4 V	2.7 3.3 4.2	-	6.0 5.5 5.0	8.6 7.6 7.0	Ω
R _{FLAT}		On-Resistance Flatness (Notes 1 and 2)	I _{ON} = 8 mA V _{IS} = 0 V to 0.4 V	2.7 3.3 4.2	-	0.55 0.30 0.20	-	Ω
ΔR _{ON}		On-Resistance Matching (Notes 1 and 3)	I _{ON} = 8 mA V _{IS} = 0 V to 0.4 V	2.7 3.3 4.2	-	0.60 0.60 0.60	-	Ω

1. Guaranteed by design.
2. Flatness is defined as the difference between the maximum and minimum value of On-Resistance as measured over the specified analog signal ranges.
3. ΔR_{ON} = R_{ON(max)} - R_{ON(min)} between HSD1+ and HSD1- or HSD2+ and HSD2-.

FULL V_{IS} SWING ON RESISTANCE (Typical: T = 25°C)

Symbol	Pins	Parameter	Test Conditions	V _{CC} (V)	-40°C to +85°C			Unit
					Min	Typ	Max	
R _{ON}		On-Resistance	I _{ON} = 8 mA V _{IS} = 0 V to V _{CC}	2.7 3.3 4.2	-	10 8.0 7.0	13.5 9.75 8.50	Ω
R _{FLAT}		On-Resistance Flatness (Notes 4 and 5)	I _{ON} = 8 mA V _{IS} = 0 V to V _{CC}	2.7 3.3 4.2	-	4.5 3.0 2.5	-	Ω
ΔR _{ON}		On-Resistance (Note 4 and 6)	I _{ON} = 8 mA V _{IS} = 0 V to V _{CC}	2.7 3.3 4.2	-	0.60 0.60 0.60	-	Ω

4. Guaranteed by design.
5. Flatness is defined as the difference between the maximum and minimum value of On-Resistance as measured over the specified analog signal ranges.
6. ΔR_{ON} = R_{ON(max)} - R_{ON(min)} between HSD1+ and HSD1- or HSD2+ and HSD2-.

NL3S2223

AC ELECTRICAL CHARACTERISTICS

TIMING/FREQUENCY (Typical: T = 25°C, V_{CC} = 3.3 V, R_L = 50 Ω, C_L = 35 pF, f = 1 MHz)

Symbol	Pins	Parameter	Test Conditions	V _{CC} (V)	-40°C to +85°C			Unit
					Min	Typ	Max	
t _{ON}	Closed to Open	Turn-ON Time (See Figures 4 and 5)		1.65 – 4.5	–	13.0	30.0	ns
t _{OFF}	Open to Closed	Turn-OFF Time (See Figures 4 and 5)		1.65 – 4.5	–	12.0	25.0	ns
T _{BBM}		Break-Before-Make Time (See Figure 3)		1.65 – 4.5	2.0	–	–	ns
BW		–3 dB Bandwidth (See Figure 10)	C _L = 5 pF	1.65 – 4.5	–	950	–	MHz

ISOLATION (Typical: T = 25°C, V_{CC} = 3.3 V, R_L = 50 Ω, C_L = 5 pF)

Symbol	Pins	Parameter	Test Conditions	V _{CC} (V)	-40°C to +85°C			Unit
					Min	Typ	Max	
O _{IRR}	Open	OFF-Isolation (See Figure 6)	f = 240 MHz	1.65 – 4.5	–	–22	–	dB
X _{TALK}	HSDn+ to HSDn–	Non-Adjacent Channel Crosstalk	f = 240 MHz	1.65 – 4.5	–	–24	–	dB

CAPACITANCE (Typical: T = 25°C, V_{CC} = 3.3 V, R_L = 50 Ω, C_L = 5 pF)

Symbol	Pins	Parameter	Test Conditions	-40°C to +85°C			Unit
				Min	Typ	Max	
C _{IN}	S, \overline{OE}	Control Pin, Output Enable Input Capacitance	V _{CC} = 0 V, f = 1 MHz	–	1.5	–	pF
			V _{CC} = 0 V, f = 10 MHz	–	1.0	–	
C _{ON}	D+ to HSD1+ or HSD2+	ON Capacitance	V _{CC} = 3.3 V; \overline{OE} = 0 V, f = 1 MHz S = 0 V or 3.3 V	–	5.5	–	pF
			V _{CC} = 3.3 V; \overline{OE} = 0 V, f = 10 MHz S = 0 V or 3.3 V	–	5.5	–	
			V _{CC} = 3.3 V; \overline{OE} = 0 V, f = 240 MHz S = 0 V or 3.3 V	–	5	–	
C _{OFF}	HSD1n or HSD2n	OFF Capacitance	V _{CC} = V _{IS} = 3.3 V; \overline{OE} = 3.3 V or (\overline{OE} = 0 V, S = 3.3 V or 0 V), f = 1 MHz	–	3.8	–	pF
			V _{CC} = V _{IS} = 3.3 V; \overline{OE} = 3.3 V or (\overline{OE} = 0 V, S = 3.3 V or 0 V), f = 10 MHz	–	2.0	–	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

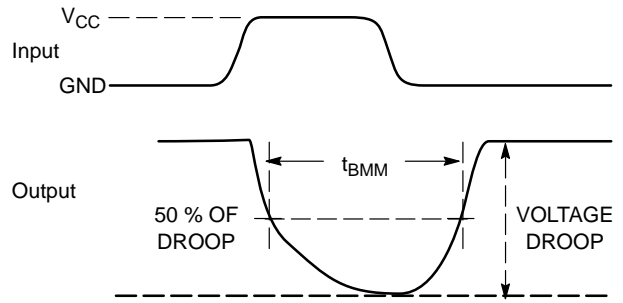
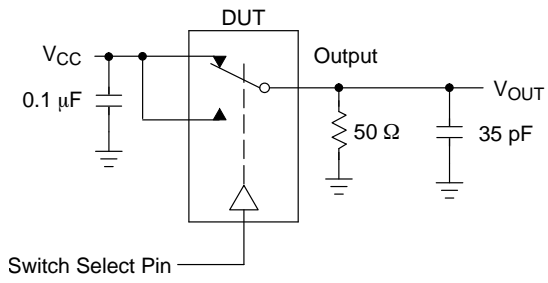


Figure 3. t_{BMM} (Time Break-Before-Make)

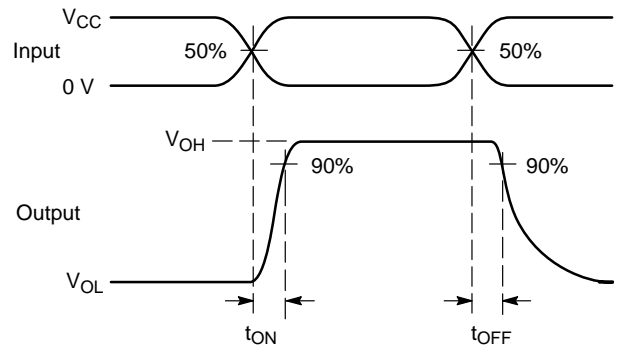
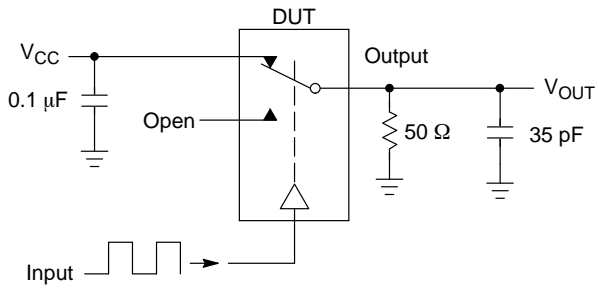


Figure 4. t_{ON}/t_{OFF}

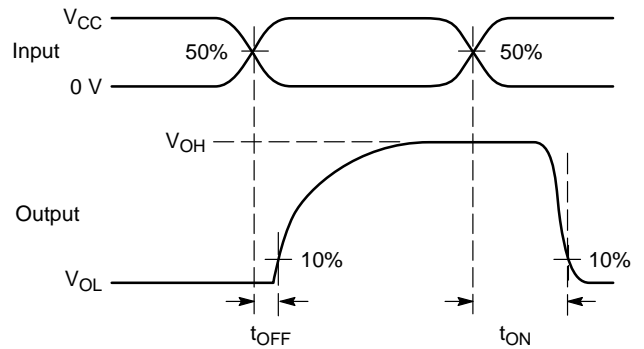
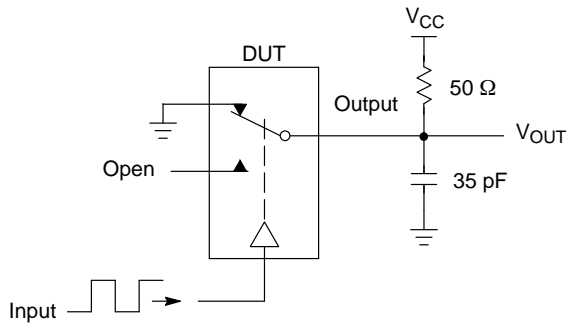
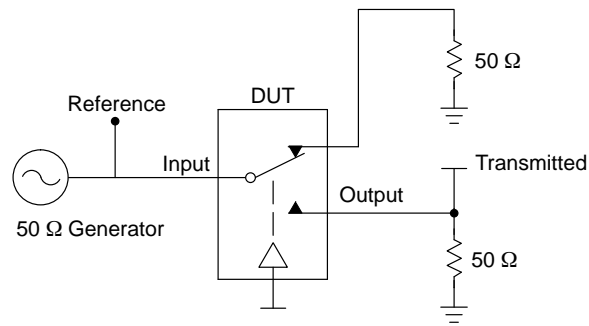


Figure 5. t_{ON}/t_{OFF}

NL3S2223



Channel switch control/s test socket is normalized. Off isolation is measured across an off channel. On loss is the bandwidth of an On switch. V_{ISO} , Bandwidth and V_{ONL} are independent of the input signal direction.

$$V_{ISO} = \text{Off Channel Isolation} = 20 \text{ Log} \left(\frac{V_{OUT}}{V_{IN}} \right) \text{ for } V_{IN} \text{ at } 100 \text{ kHz}$$

$$V_{ONL} = \text{On Channel Loss} = 20 \text{ Log} \left(\frac{V_{OUT}}{V_{IN}} \right) \text{ for } V_{IN} \text{ at } 100 \text{ kHz to } 50 \text{ MHz}$$

Bandwidth (BW) = the frequency 3 dB below V_{ONL}

V_{CT} = Use V_{ISO} setup and test to all other switch analog input/outputs terminated with 50 Ω

Figure 6. Off Channel Isolation/On Channel Loss (BW)/Crosstalk (On Channel to Off Channel)/ V_{ONL}

DETAILED DESCRIPTION

High Speed (480Mbps) USB 2.0 Optimized

The NL3S2223 is a DPDT switch designed for USB applications within portable systems. The R_{ON} and C_{ON} of both switches are maintained at industry-leading low levels in order to ensure maximum signal integrity for USB 2.0 high speed data communication. The NL3S2223 switch can be used to switch between high speed (480Mbps) USB signals and a variety of audio or data signals such as full speed USB, UART or even a moderately resistive audio terminal.

Over Voltage Tolerant

The NL3S2223 features over voltage tolerant I/O protection on the common signal pins D+/D-. This allows the switch to interface directly with a USB connector. The D+/D- pins can withstand a short to V_{BUS} , up to 5.25 V, continuous DC current for up to 24 hours as specified in the USB 2.0 specification. This protection is achieved without the need for any external resistors or protection devices.

NL3S2223

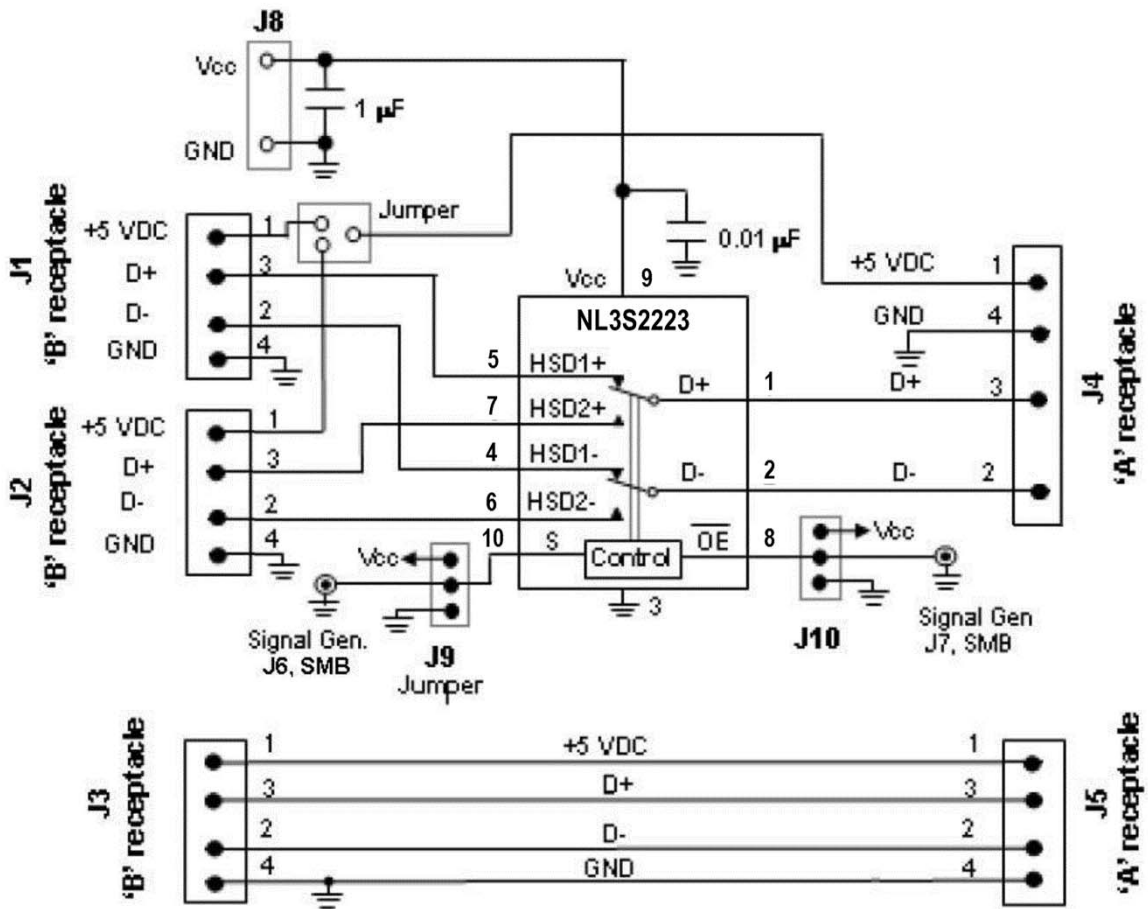


Figure 7. Board Schematic

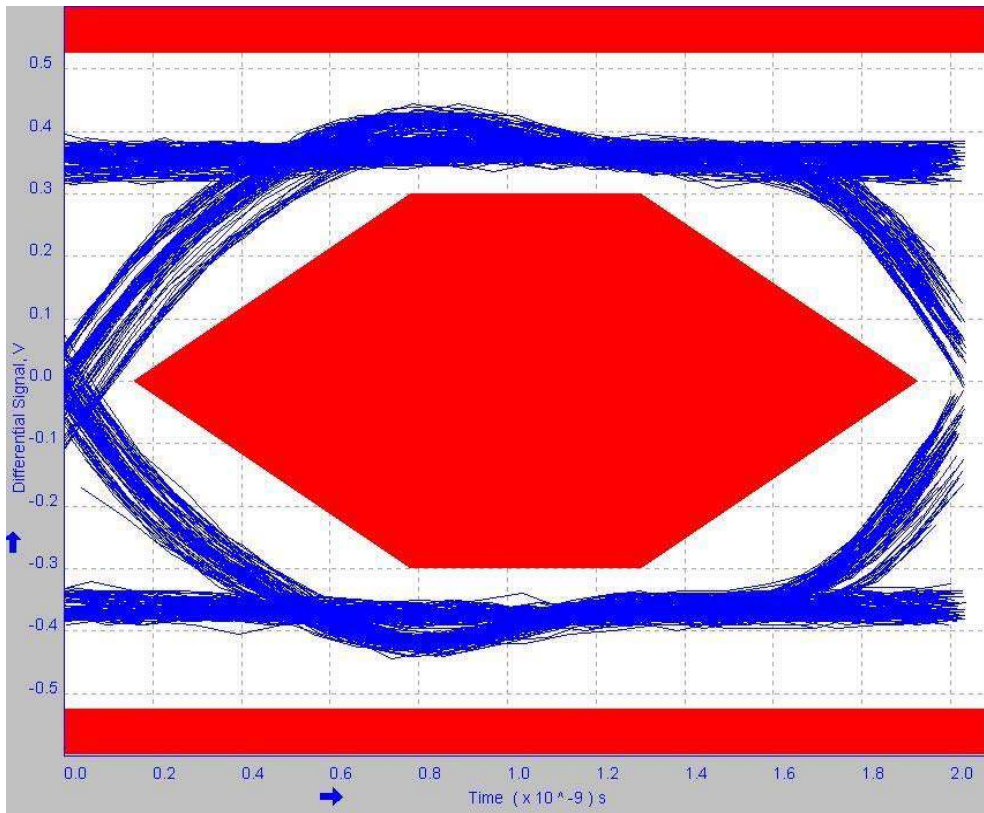


Figure 8. Signal Quality

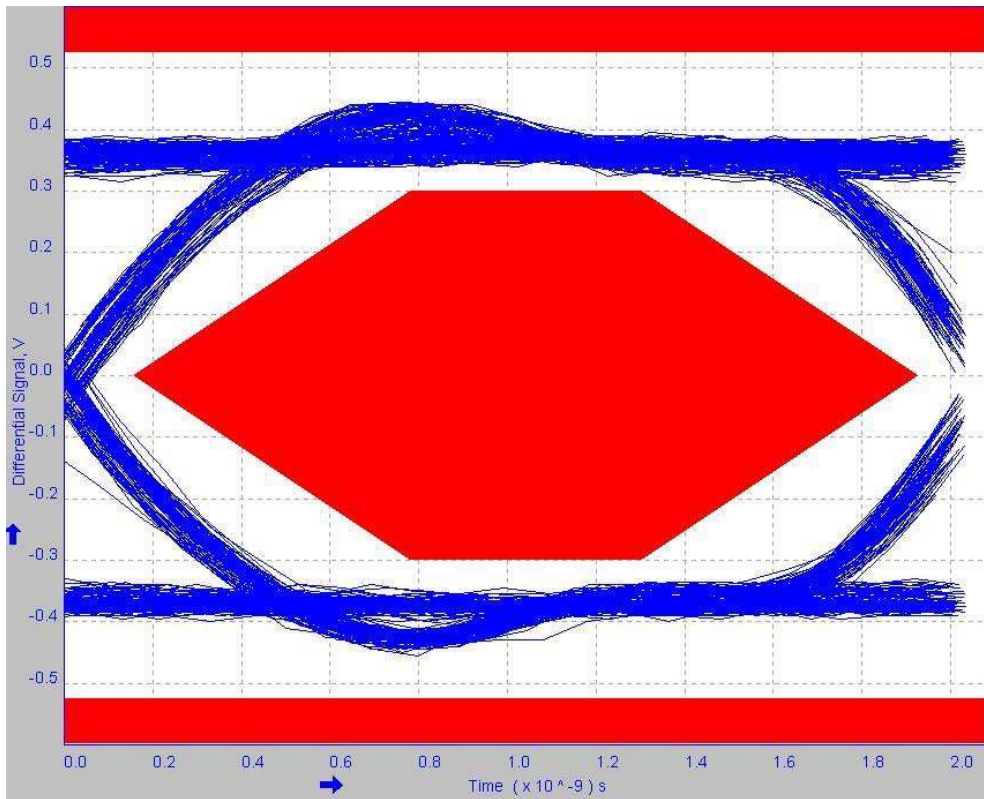
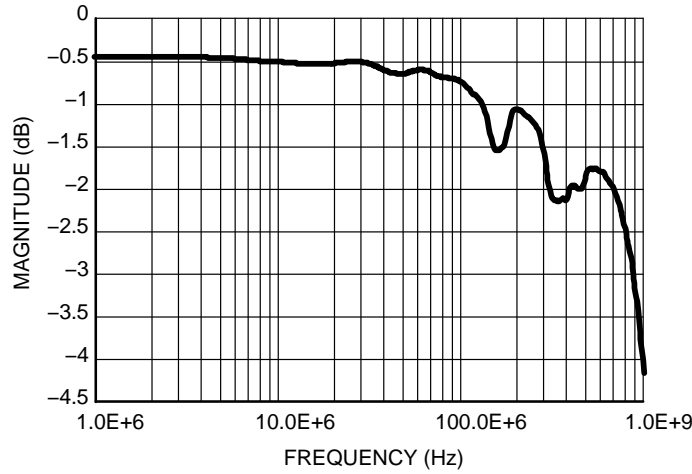


Figure 9. Near End Eye Diagram

NL3S2223

Near End Test Data:					Min	Max
Std.	Consecutive jitter range	-54.37	73.21	ps	-200 ps	+200 ps
	Paired JK jitter range	-59.14	59.56	ps		
	Paired KJ jitter range	-50.79	34.57	ps		
N.C.	Consecutive jitter range	-74.43	81.65	ps	-200 ps	+200 ps
	Paired JK jitter range	-61.60	58.55	ps		
	Paired KJ jitter range	-55.31	48.43	ps		
N.O.	Consecutive jitter range	-82.55	80.33	ps	-200 ps	+200 ps
	Paired JK jitter range	-53.50	71.65	ps		
	Paired KJ jitter range	-62.60	47.30	ps		



**Figure 10. Magnitude vs. Frequency
@ V_{CC} = 3.3 V, All Temperatures**

I_{CC} Leakage Current as a Function of V_{IN} Voltage (25°C)

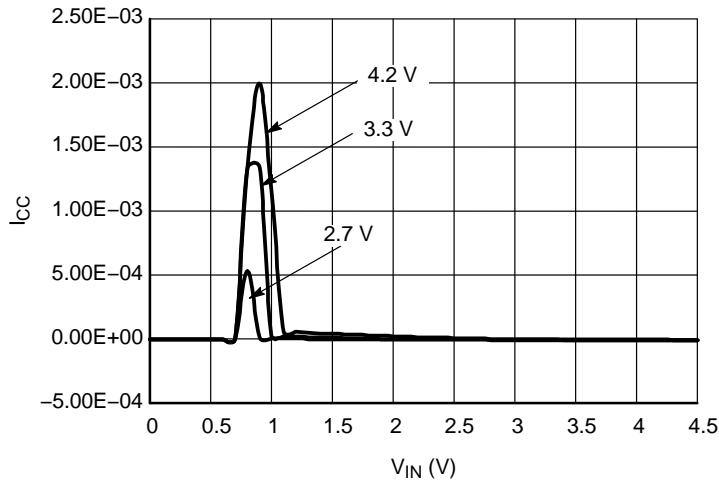


Figure 11. I_{CC} vs. V_{IN}, Select Pin, All V_{CC}'s, 25°C

MECHANICAL CASE OUTLINE

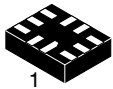
PACKAGE DIMENSIONS

ON Semiconductor®

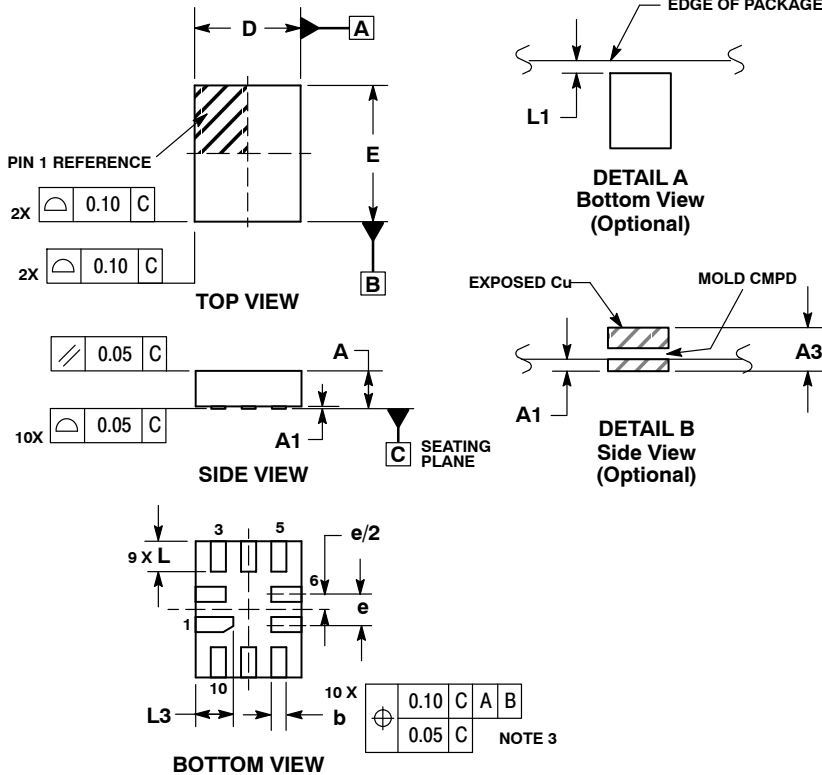


UQFN10 1.4x1.8, 0.4P CASE 488AT-01 ISSUE A

DATE 01 AUG 2007



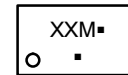
SCALE 5:1



- NOTES:
- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 - CONTROLLING DIMENSION: MILLIMETERS
 - DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
 - COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

MILLIMETERS		
DIM	MIN	MAX
A	0.45	0.60
A1	0.00	0.05
A3	0.127 REF	
b	0.15	0.25
D	1.40	BSC
E	1.80	BSC
e	0.40	BSC
L	0.30	0.50
L1	0.00	0.15
L3	0.40	0.60

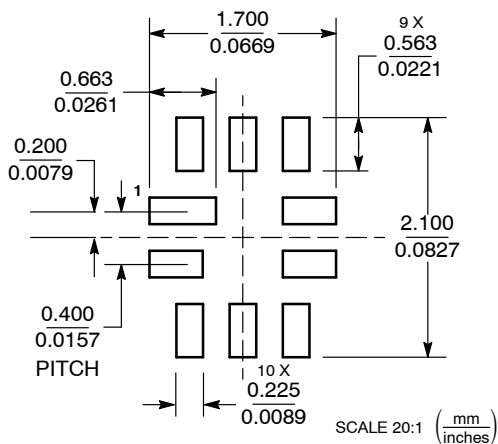
GENERIC MARKING DIAGRAM*



- XX = Specific Device Code
 M = Date Code
 ■ = Pb-Free Package
 (Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present.

MOUNTING FOOTPRINT



DOCUMENT NUMBER:	98AON22493D	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	10 PIN UQFN, 1.4 X 1.8, 0.4P	PAGE 1 OF 1

ON Semiconductor and ON are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales