KSZ8463ML/RL Evaluation Board User Guide

Preliminary Revision 1.1 / July 17, 2013

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Introduction

The KSZ8463ML/RL Evaluation Board provides a platform for testing or exploring the functionally of the KSZ8463ML and KSZ8463RL IEEE 1588 Precision Time Protocol (PTP) enabled switch products.

The KSZ8463ML, KSZ8463FML, KSZ8463RL and KSZ8463FRL devices are highly integrated 2-port 10BASE-T / 100BASE-TX/FX managed Ethernet switches with MII and RMII interface connectivity to a host on Port 3. They are the ideal solution in industrial applications where real time clock synchronization using Ethernet connectivity across a network is desired. The KSZ8463ML/RL includes all the functions of a 10/100BASE-T/TX/FX switch system that combines switch engine, frame buffers management, addresses look-up table, queue management, MIB counters, media access controllers (MAC) and PHY transceiver interfaces. The KSZ8463ML/RL is fully compliant with the IEEE 1588 (Version 2) Precision Time Protocol and IEEE 802.3 standards (10BASE-T and 100BASE-TX/FX). The KSZ8463ML/FML devices have Port 3 configured for MII mode, while the KSZ8463RL/FRL devices have Port 3 configured for RMII mode.

This KSZ8463ML/RL Evaluation Board User Guide provides the information necessary to configure and set up the board to evaluate or test the KSZ8463ML and KSZ8463RL devices in different environments.

1 Board Features

The KSZ8463ML/RL Evaluation Board encompasses the following features.

- Micrel's KSZ8463ML or KSZ8463RL Integrated 3-Port 10/100 Managed Ethernet Switch
- Fully compatible with the KSZ8463FML and KSZ8463FRL devices
- Two Ethernet LAN interfaces with RJ-45 jacks and isolation magnetics (Port 1 & 2)
- Auto MDI/MDI-X for automatic detection and correction for straight-through and crossover cables
- MII connector for Port 3 operating in PHY Mode
- Provisioning for MII / RMII connector for Port 3 operating in MAC Mode (optional)
- Provisioning for two 100BASE-FX fiber interfaces (optional)
- Provisioning for line side and chip side over-voltage protection (optional)
- On-board 3.3V and 1.8V/2.5V regulators
- Configurable for VDDIO of 3.3V, 2.5V, or 1.8V operation
- USB access to SPI or MIIM (MDIO/MDC) interface
- LED indicators for link status and activity of the RJ-45 ports
- On-board 25 MHz crystal
- Provisioning for on-board 50 MHz oscillator for RMII (optional)
- Jumpers for power up configuration of the device
- Jumpers for GPIO pins, I/O voltage selection and serial-port connections
- 5V DC voltage required for operation
- Reset switch
- Various test points

2 KSZ8463ML/RL Evaluation Board Kit

The KSZ8463ML/RL Evaluation Board kit includes the following:

- KSZ8463ML/RL Evaluation Board
- KSZ8463ML/RL Evaluation Board User Guide (This document, available in the eval kit, on the Micrel website)
- KSZ8463ML/RL Evaluation Board Schematic (Available in the eval kit, on the Micrel website)

3 Hardware Description

The KSZ8463ML/RL Evaluation board is a small form-factor board (5.2" x 4.75") with two10/100 RJ-45 ports and one MII/RMII port. There are two methods for configuring the KSZ8463: Strap-in configuration and serial interface.

Strap-in mode configuration occurs at power-on (and hardware reset) where the voltage level on certain pins is automatically sampled and used to configure various features in the device. This is accomplished with on-board jumper options, so that the KSZ8463 powers up in the desired modes. With no additional programming of registers, the device will start operation as an unmanaged 3-port switch.

The KSZ8463ML/RL has a serial interface which can be either SPI or MIIM (MDIO/MDC). Normally the SPI interface is used because it provides read/write access to all KSZ8463 registers. In comparison, the MIIM interface provides access only to the basic PHY registers in the KSZ8463. Full register access is required for managed operation of the switch, and to utilize the advanced features such as IEEE 1588 PTP. Access to the SPI interface is provided on the 6-pin header J5. SPI (or MIIM) access is also provided via the onboard USB port interface. An FT2232D chip is used for the USB-to-SPI/MIIM interface. Configuration options are explained in detail in the following sections. Figure 1 is a picture of the KSZ8463ML/RL Evaluation board.

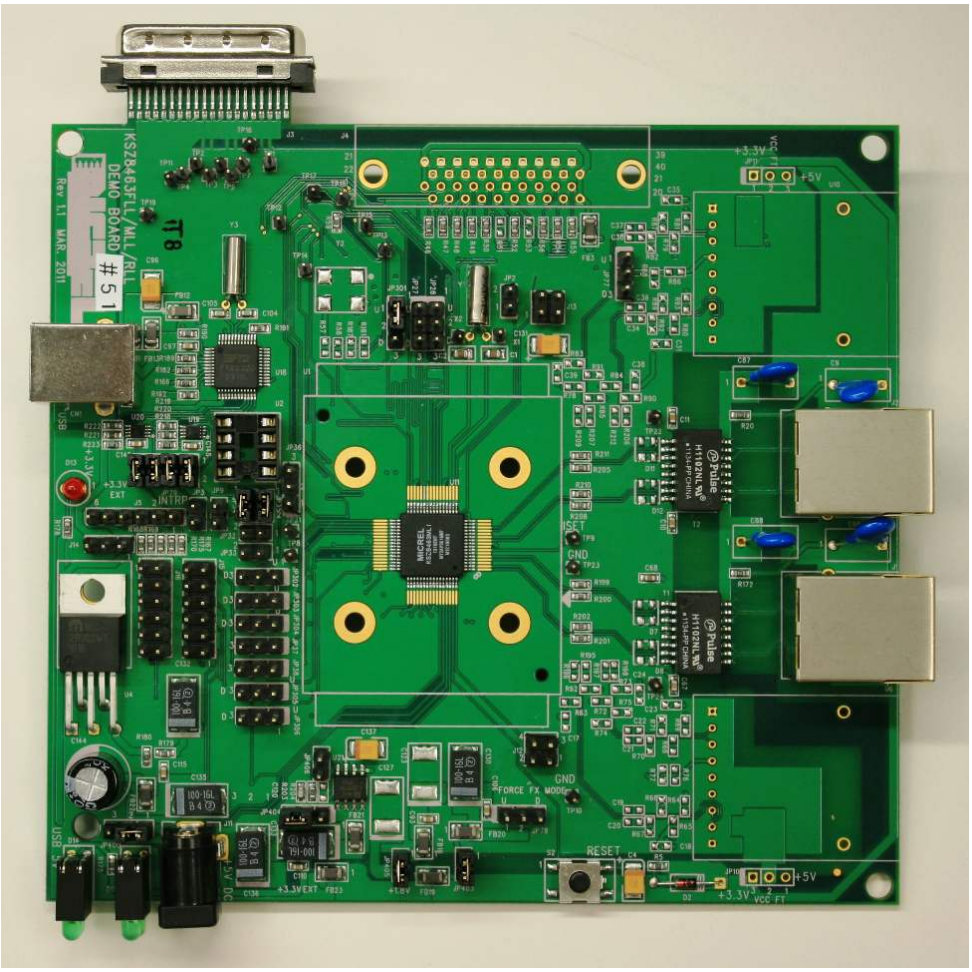

Figure 1 KSZ8463ML/RL Evaluation Board

3.1 Configuration Options

3.1.1 Strap-in Configuration

Strap-in configuration is used to set the basic modes of operation so that KSZ8463 powers up in the right modes. This is accomplished by setting available configuration jumpers which are used at device power-up. Simply set the board's configuration jumpers to the desired settings and apply power to the board. The configuration can be changed while power is applied to the board by changing the jumper settings and pressing the manual reset button for the new settings to take effect. Note that even if no external strap-in jumpers are set, internal pull-up and pull-down resistors will set the KSZ8463ML/RL to the default configuration. The following table covers each jumper used for the strap-in option and describes its function.

JUMPER	FUNCTION	SETTING	DEFAULT (no jumper)
JP301	PHY/MAC mode select for MII port[1]	Pins 1-2 closed: PHY MII mode Pins 2-3 closed: MAC MII mode	PHY MII

JUMPER	FUNCTION	SETTING		DEFAULT (no jumper)
JP302	High-speed/Low-speed SPI selection	Pins 1-2 closed: High speed (up to 50 MHz) Pins 2-3 closed: Low speed (up to 12.5 MHz)		High speed
	Serial Bus Mode Selection	**SPI Slave**	**MIIM (MDIO/MDC)**	SPI Slave
JP303		Pins 1-2 closed	Pins 1-2 closed	
JP304		Pins 2-3 closed	Pins 1-2 closed	
JP305	Input Clock Select[2]	Pins 1-2 closed: 25MHz from X1/X2 Pins 2-3 closed: 50MHz from REFCLK_I		25MHz

Table 1 Strap-In Configuration Jumpers

Notes:
1. This mode select applies only to the MII interface, and thus does not apply to the KSZ8463RL and KSZ8463FRL which have a RMII interface.
2. Mode "50MHz from REFCLK_I" is an option only for the KSZ8463RL and KSZ8463FRL. The KSZ8463ML and KSZ8463FML must use mode "25MHz from X1/X2."

3.1.2 USB Interface (SPI Slave or MDIO)

With the Micrel utility software that runs on a PC, it is possible to access the full register set of the device through the USB port provided on the evaluation board. Download and install the Windows based *MicrelSwitchPhyTools* software from the Micrel website. It includes two applications: MicrelSwitchConfigApp.exe and MicrelMDIOConfigApp.exe, plus associated DLL files. MicrelSwitchConfigApp has a graphical user interface (GUI) and provides access via USB to many of the KSZ8463 registers via the SPI interface. MicrelMDIOConfigApp and the MDIO interface are of limited use on the KSZ8463 and are not described further.

When using the USB-to-SPI interface, ensure that the following jumpers are installed: J14 (either pins 1-2 or 2-3), JP34, JP35 and JP79 (all four pairs). Do not install JP32 or JP33.

3.2 Power Supplies

The board requires a single 5V DC supply, which can be provided through a barrel power-supply jack (J11) or through the USB port. The current requirement is 200mA. When configured for fiber operation, expect the fiber modules to draw approximately 250mA of additional current per port.

The pin diameter of jack J11 is 2.5mm on early boards, and is 2.1mm on newer boards. 2.5mm plugs are recommended because they are generally compatible with both jack sizes. A 2.1mm plug, however, cannot be used with the 2.5mm jack.

JP400 is used for selecting the 5V source to the board. There is a 3.3V regulator on the board supplying power for the KSZ8463 and other components. A separate on-board voltage regulator is provided for the optional 2.5V and 1.8V supplies for KSZ8463's I/O interface (VDD_IO). JP404 and JP406 are used for VDD_IO selection. JP403 and JP405 must be in place and other options properly selected before powering up the board.

JUMPER	FUNCTION	SETTING		
JP400	+5V supply source selection	Pins 1-2 closed: Power connector (J11) Pins 2-3 closed: USB port		
JP403	+3.3V supply for KSZ8463 analog circuits	Must be closed		
JP405	+1.2V supply for KSZ8463 analog circuits	Must be closed		
	VDD_IO selection	**3.3V**	**2.5V**	**1.8V**
JP404		Pins 2-3 closed	Pins 1-2 closed	Pins 1-2 closed
JP406		X	open	closed

Table 2 Power Supply Related Jumpers

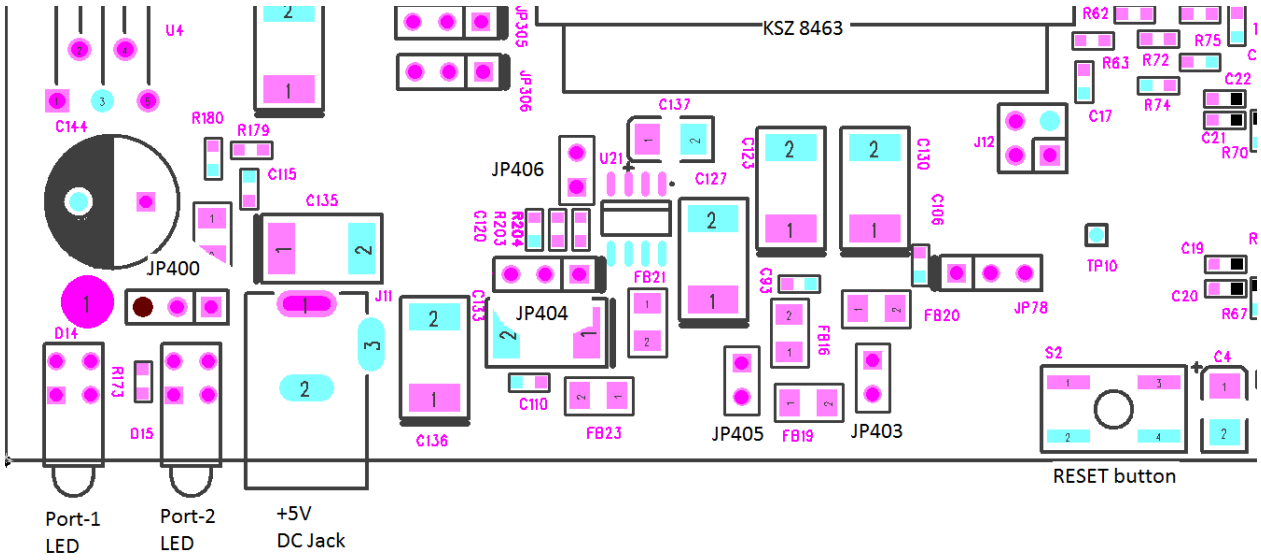

Figure 2 Power Supply Section and Related Jumper Locations

3.3 Port 3 Configuration

The board features two Media Independent Interface (MII) connectors, for interfacing the MAC of Port-3 on the KSZ8463ML/FML to either an external PHY or MAC.

The female MII connector (J4, not installed) is used for interfacing to a PHY. For example, it can be connected to a KSZ8081 eval board. When connecting to a PHY, the KSZ8463ML/FML must be set to MAC mode. A jumper is provided (JP301) to set Port-3 in PHY or MAC mode of operation at power-up.

The male MII connector (J3) is used for interfacing to any host processor's MAC interface. Normally this port connects to a Micrel KSZ9692MII-PTP-EV or KSZ9692PB-PTP-EVAL board for evaluation of the IEEE1588 PTP functionality. When connecting to an external MAC device such as the KSZ9692, the KSZ8463ML/FML must be set to PHY mode.

The KSZ8463ML/FML provides a bypass feature in the MII PHY mode. JP27 is used to enable the MII bypass mode. In the bypass mode, MII (port 3) is shut down and no new ingress frames from either Port 1 or Port 2 will be sent out through Port 3. Only the switch between Port 1 and Port 2 is active for all ingress packets, and the frames for Port 3 already in packet memory will be flushed out.

Whereas the KSZ8463ML/FML uses the full MII signaling pins of the connectors, the KSZ8463RL/FRL makes use of a subset of the available pins, as defined by the RMII standard. The RMII standard requires a 50 MHz clock which can be generated by the KSZ8463RL/FRL chip, or supplied externally. The KSZ8463ML/RL Evaluation board provides both options. JP28 is connected to EN_REFCLKO (pin 23), to enable or disable the generation of the 50 MHz clock by the KSZ8463RL/FRL on REFCLK_O (pin 32).

When REFCLKP_O (JP28) is enabled, the Input Clock Select option (JP305) must be set to “25MHz from X1/X2”.

An on-board 50 MHz oscillator (Y2, not installed) is also provided for the RMII devices. This oscillator drives a 50 MHz clock both to the J4 connector (pin 12) and to the KSZ8463RL/FRL (REFCLK_I, pin 27). In this configuration, REFCLK_O (JP28) must be disabled, and JP305 is used to select the “50MHz from REFCLK_I” option. When installing Y2, it is also necessary to install R181, R187, and to remove R51, R53 and R58.

JUMPER	FUNCTION	SETTING	DEFAULT (no jumper)
JP301	MAC/PHY mode selection for MII on Port-3[1]	Pins 1-2 closed: PHY mode Pins 2-3 closed: MAC mode	PHY mode
JP27	Bypass mode for MII PHY mode link[3]	Pins 1-2 closed: Bypass enabled Pins 2-3 closed: Normal operation	Normal operation
JP28	50 MHz Reference clock generation[4]	Pins 1-2 closed: REFCLK_O is enabled (EN_REFCLKO pin = 1) Pins 2-3 closed: REFCLK_O is disabled (EN_REFCLKO pin = 0)	REFCLK_O disabled
JP305	Input Clock Select[2]	Pins 1-2 closed: 25MHz from X1/X2 Pins 2-3 closed: 50MHz from REFCLK_I	25MHz

Table 3 MII / RMII Port Configuration Settings

Notes:

3. The Bypass mode option applies only when in MII PHY mode. When in MII MAC mode, do not install any jumper on JP27.
4. The 50 MHz reference option applies only to RMII devices (KSZ8463RL and KSZ8463FRL). For MII devices (KSZ8463ML and KSZ8463FML), do not install a jumper on JP28.

3.3.1 MII Port Configuration (KSZ8463ML, KSZ8463FML)

The Media Independent Interface (MII) is specified in Clause 22 of the IEEE 802.3 standard. It provides a common interface between PHY layer and MAC layer devices. The MII provided by the KSZ8463ML/FML is connected to the device’s third MAC (Port 3). The interface contains two distinct groups of signals, one for transmission and the other for reception. The following table describes the signals used by the MII interface to connect either external MAC or external PHY.

Signal Name on MII connectors	Description	Pin numbers	Signal direction in PHY mode: (Connector J3)	Signal direction in MAC mode: (Connector J4)	Test Points
TX_EN	Transmit enable	13	input	output	TP6
TX_ER	Transmit error	11	input	GND	TP15
TXD3	Transmit data bit 3	17	input	output	TP18
TXD2	Transmit data bit 2	16	Input	output	TP17
TXD1	Transmit data bit 1	15	Input	output	TP16
TXD0	Transmit data bit 0	14	input	output	TP7
TX_CLK	Transmit clock	12	output	input	TP5
COL	Collision detection	18	output	input	TP1
CRS	Carrier sense	19	output	input	-
RX_DV	Receive data valid	8	output	input	TP2
RX_ER	Receive error	10	GND	input	-
RXD3	Receive data bit 3	4	output	input	TP13
RXD2	Receive data bit 2	5	output	input	TP12
RXD1	Receive data bit 1	6	output	input	TP11
RXD0	Receive data bit 0	7	output	input	TP4
RX_CLK	Receive clock	9	output	input	TP3
MDIO	Data I/O		Bi-directional	Bi-directional	-
MDC	Clock		input	input	-
VCC		1, 20, 21, 40	No connection	VCC (+5V)	
GND		22 - 39	GND	GND	TP14, TP19

The KSZ8463ML/FML does not provide the RX_ER signal in PHY mode operation and the TX_ER signal in MAC mode operation. Normally, RX_ER indicates a receive error coming from the physical layer device and TX_ER indicates a transmit error from the MAC device. Since the switch filters error frames, these MII error signals are not used by the KSZ8463ML/FML. So, for PHY mode operation, if the device interfacing with the KSZ8463ML/FML has an RX_ER input pin, it needs to be tied low. And, for MAC mode operation, if the device interfacing with the KSZ8463ML/FML has a TX_ER input pin, it also needs to be tied low.

3.3.2 RMII Port Configuration (KSZ8463RL and KSZ8463FRL)

The Reduced Media Independent Interface (RMII) specifies a low pin count Media Independent Interface (MII). RMII provides a common interface between physical layer and MAC layer devices, and has the following key characteristics:

- Supports data rate either 10Mbps or 100Mbps.
- Uses a single 50 MHz clock reference for both transmit and receive data.
- Provides independent 2-bit wide transmit and receive data paths.
- Contains two distinct groups of signals: one for transmission and the other for reception.

Connector J3 is not configured for use with RMII. RMII interfacing must use connector J4, for connection to an external RMII PHY such as the KSZ8081RNA, KSZ8081RNB or KSZ8081RND eval board.

As shown in Table 4 and Table 5, JP28 is used for enabling or disabling the generation of 50MHz reference clock from the REFCLK_O pin of the KSZ8463RL/FRL. The 50MHz reference clock is always provided to KSZ8463RL/FRL via REFCLK_I (pin 27).

JUMPER	FUNCTION	SETTING	DEFAULT (no jumper)
JP28	50 MHz Reference clock generation	Pins 1-2 closed: REFCLK_O is enabled (EN_REFCLKO pin = 1) Pins 2-3 closed: REFCLK_O is disabled (EN_REFCLKO pin = 0)	REFCLK_O disabled

Table 4 MII Port Configuration Settings

JP28 Setting (EN_REFCLKO pin)	Clock Source	Note
Pins 2-3 closed (EN_REFCLKO = 0, REFCLK_O is off)	External 50MHz Ref Clock from oscillator (or J4 pin 9) is input to REFCLK_I.	X1/X2 25MHz clock is not used.
Pins 1-2 closed (EN_REFCLKO = 1, REFCLK_O is on)	REFCLK_O output must connect to REFCLK_I, and also drives to J4 pin 12.	X1/X2 25MHz clock is required.

Table 5 RMII Clock Setting

The RMII provided by the KSZ8463RL/FRL is connected to the device's third MAC. It complies with the RMII Specification. The following table describes the signals used by the RMII interface. Refer to RMII Specification for full detail on the signal description.

RMII Signal Name	RMII Signal Description	Pin number on MII connectors	Direction (with respect to the PHY)	Direction (with respect to the MAC)	Test Points
REFCLK	Synchronous 50 MHz clock reference for receive, transmit and control interface	12	Input	Input or Output	TP5
CRS_DV	Carrier sense/ Receive data valid	8	Output	Input	TP6
RXD0	Receive data bit 0	7	Output	Input	TP4
RXD1	Receive data bit 1	6	Output	Input	TP11
TX_EN	Transmit enable	13	Input	Output	TP6
TXD0	Transmit data bit 0	14	Input	Output	TP7
TXD1	Transmit data bit 1	15	Input	Output	TP16
RX_ER	Receive error	10	Output	Input or not required	TP15

Table 6 RMII Signal Description

The KSZ8463RL/FRL filters error frames, and thus does not implement the RX_ER output signal. To detect error frames from RMII PHY devices, the TX_ER input signal of the KSZ8463RL/FRL is connected to the RX_ER output signal of the RMII PHY device.

Collision detection is implemented in accordance with the RMII Specification.

In RMII mode, tie MII signals (TXD [3:2], RXD [3:2] and TX_ER) to ground if they are not used.

The KSZ8463RL/FRL can interface to either RMII PHY or RMII MAC devices. The RMII MAC device allows two KSZ8463RL/FRL devices to be connected back-to-back.

3.4 GPIO pins

The KSZ8463 has up to 12 General Purpose I/O (GPIO) pins which are available on the evaluation board at connectors J15 and J16. The KSZ8463RL has all 12 GPIO pins available. Three GPIO pins of the KSZ8463ML are shared with Port1/2 LED activity signals and are user programmable. By default the LED signals are enabled, therefore 9 GPIO pins are available. If more than 9 GPIO pins are required, the user needs to program IOMXSEL register (0x0D6) as follows:

IOMXSEL register (0x0D6)	Description	Setting
Bit 10	Selection of P2LED1 or GPIO9	1 = This pin is used for P2LED1 (default) 0 = This pin is used for GPIO9
Bit 9	Selection of P2LED0 or GPIO10	1 = This pin is used for P2LED0 (default) 0 = This pin is used for GPIO10
Bit 8	Selection of P1LED1 or GPIO7	1 = This pin is used for P1LED1 (default) 0 = This pin is used for GPIO7

Table 7 GPIO pin selection for KSZ8463ML

GPIO signals are on the odd numbered pins of connectors J15 and J16. All even numbered pins are GND connections. GPIO7, 9 and 10 pins are connected to jumpers JP36, 37 and 38 respectfully.

For the KSZ8463RL device, pins 1 and 2 of all three jumpers need to be closed in order to make GPIO7, 9 and 10 available at the GPIO headers. In case of KSZ8463ML, GPIO7, 9 and 10 are Port1/2 LED activity signals by default and no strapping is needed. If the user enables GPIO functionality instead, pins 2 and 3 of the corresponding jumpers have to be closed.

The GPIO pins can be used for any general purpose I/O as well as to support IEEE1588 PTP functionality.

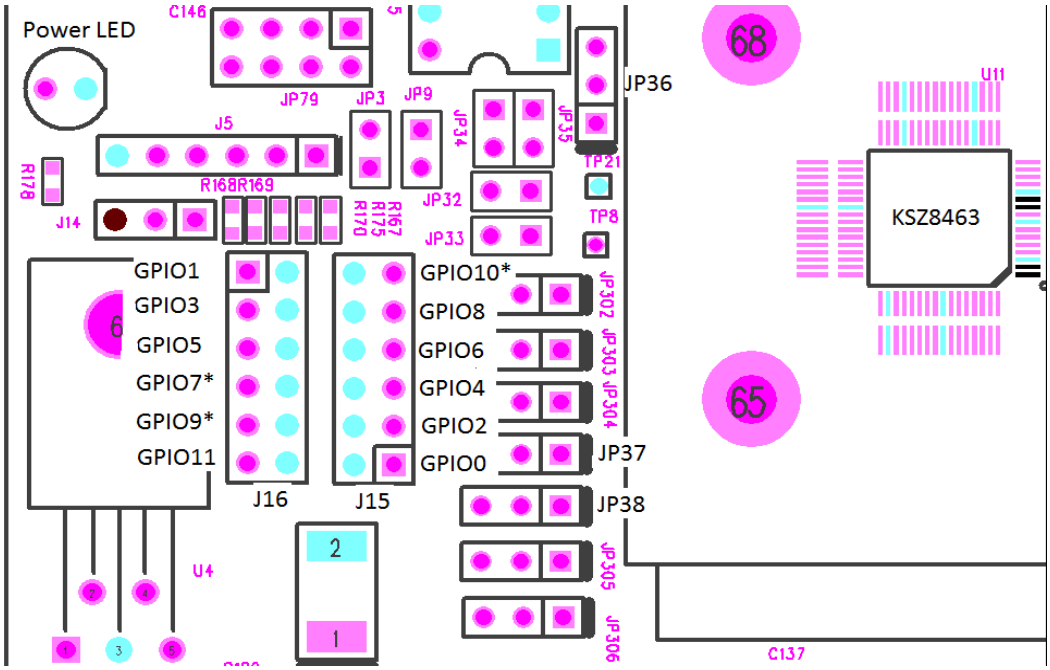

Figure 3 GPIO Connectors and Related Jumper Locations

3.5 10/100 Ethernet PHY Ports

There are two 10/100 Ethernet PHY ports on the KSZ8463ML/RL evaluation board. The ports can be connected to an Ethernet traffic generator or analyzer via standard RJ-45 connectors using CAT-5 (or better) UTP cables. Both ports support auto MDI/MDI-X, eliminating the need for cross-over cables.

Transformers are utilized for proper interfacing to an Ethernet network. In addition, optional over-voltage protection devices D5 thru D12 may be installed to protect the KSZ8463 in the event of an over-voltage condition.

For 10/100 Ethernet, the FXSD1 and FXSD2 pins should be pulled low by installing jumpers on pins 3 & 4 of J12 and J13.

3.6 100BASE-FX Fiber Port Option

There are two 100BASE-FX PHY ports on the KSZ8463ML/RL evaluation board, which are not populated with necessary components. The ports can be connected to an Ethernet traffic generator or analyzer via fiber transceiver and fiber cable. In 100BASE-FX operation, both fiber signal detect input FXSD1 and FXSD2 are usually connected to the fiber transceiver SD (signal detect) output pin. This is done by jumpering pins 1 & 2 of J12 (Port 1) and J13 (Port 2). No jumpers are required on JP77 and JP78 except as noted below. Capacitors C5 and C6 are also generally not required.

100BASE-FX is supported by the KSZ8463FML and KSZ8463FRL devices. All KSZ8463 devices power up in copper mode. Fiber Mode is selected by clearing the appropriate bits in the GFCR register (0x0D8 – 0x0D9).

The fiber signal detect threshold is set to 1.7V internally, When FXSD is less than the threshold, no fiber signal is detected and a far-end fault (FEF) is generated. When FXSD is over the threshold, the fiber signal is detected. To ensure proper operation, a resistive voltage divider is recommended to adjust the fiber transceiver SD output voltage swing to match the FXSD pin's input voltage threshold.

Alternatively, the user may choose not to implement the FEF feature. In this case, the FXSD input pin may be pulled high via jumpers JP77 and JP78.

3.7 LED Indicators

The KSZ8463ML/RL evaluation board provides two LEDs (PxLED1, PxLED0) for each PHY port. The LED indicators are programmable to four different states. LED mode is selected through bits [9:8] of the SGCR7 register (0x00E-0x00F).

The LED mode definitions are specified in Table 7. See Figure 2 for the LEDs' orientation on the KSZ8463ML/RL evaluation board in the power supply section.

SGCR7 Control Register (0x00E-0x00F) Bits[9:8]			
00 (default)	**01**	**10**	**11**
PxLED1 = Speed	PxLED1 = Active	PxLED1 = Duplex	PxLED1 = Duplex
PxLED0 = Link/Active	PxLED0 = Link	PxLED0 = Link/Active	PxLED0 = Link

Table 8 LED Functions

The KSZ8463ML/RL evaluation board also has a power LED (D3) for the 3.3V power supply. When D3 is illuminated, the board's 3.3V power supply is "on".

The activity LED indicators for Port-1 and Port-2 are powered by VDD_IO, which can be set to 3.3V, 2.5V or 1.8V. In the case of 2.5V and 1.8V selection, these LED indicators will be dimly lit or not illuminated because of inadequate voltage across the LED.

3.8 List of Jumpers and Connectors

Jumper	Description	Setting
J12-13	FXSD pin connections	Pins 1-2 closed: connect to SD signal from fiber module Pins 3-4 closed: ground the FXSD pins, for copper mode
J14	USB IO voltage selection	Close pins 1-2 or 2-3 to power USB to serial interface. Either setting will work.
JP2	PWRDN Chip Power-down	Place Jumper for full chip power-down
JP3, 9	Factory Usage	Install no jumpers
JP10, 11	Power selection for the Fiber module	Leave open when no Fiber Module present
JP27	MII bypass	Pins 1-2 closed: Enable MII bypass mode Pins 2-3 closed: MII PHY mode normal operation
JP28	Enable RMII mode reference clock output from REFCLK_O pin	Pins 1-2 closed: Enable Pins 2-3 closed: Disable
JP32, 33	Enable MDIO interface through MII connector	Place both jumpers to connect MDIO signals from MII connector to KSZ8463 serial port. When using SPI, do not install jumpers.
JP34, 35	KSZ8463 serial port connections	Place both jumpers for USB port access and SPI interface
JP36-38	GPIO7, GPIO9 and GPIO10 pin source selection on GPIO Headers	Pins 1-2 closed for KSZ8463RL/FRL Pins 2-3 closed for KSZ8463ML/FML
JP77, 78	FXSD1, FXSD2 Fiber signal detect input for Port 1 and Port 2 (not used)	
JP79	Enable USB controller interface	Close pins 1-2, 3-4, 5-6 and 7-8 to connect USB controller to serial bus
JP301-305	Strapping options	See Table 1
JP306	Not used	
JP400	5V DC input selection	See Table 2
JP403-406	Power-supply strapping options	See Table 2

Table 9 List of Jumpers and Connectors

3.9 Board Layout

The layout of the board is shown in Figure 3. The key areas are indicated.

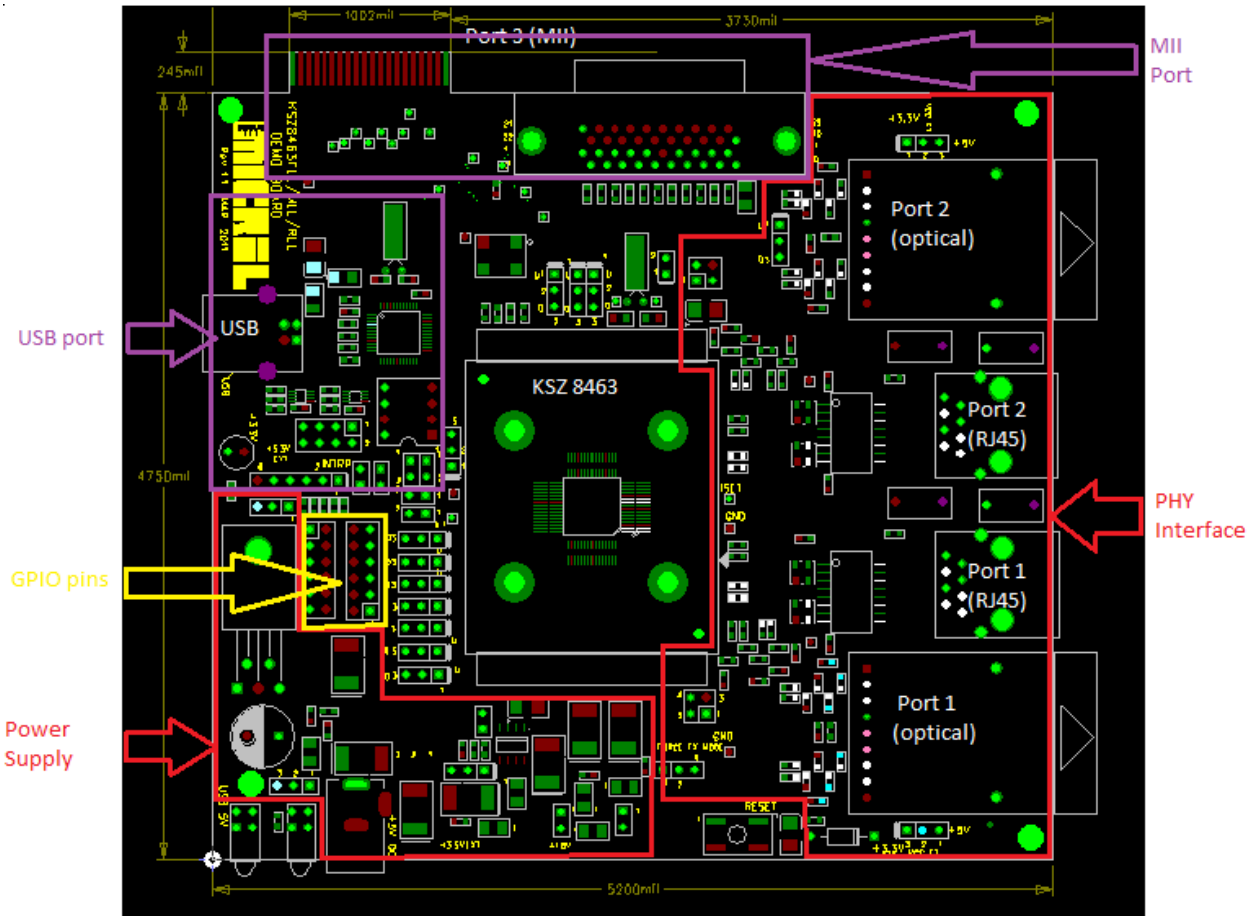

Figure 4 Topside Layout of the Board

The KSZ8463ML/RL Evaluation board, together with the KSZ9692PB SOC board (KSZ9692-MII-PTP-EV), provides a complete evaluation platform for the IEEE1588 PTP functionality. In this setup, Port 3 of the KSZ8463 evaluation board is configured in PHY mode and connected to the SOC board through its MII port. In addition to the MII connection, the SOC accesses the KSZ8463 through the SPI port. An interrupt line is also used for PTP software functionality. For more details on this configuration, refer to the KSZ8463ML Evaluation Kit User Guide.

4 Using the KSZ8463ML/RL Evaluation Board

The Evaluation Kit is intended to provide a platform that enables designers to investigate and evaluate the capabilities of the KSZ8463 device. It is not intended to be a complete development system to be used for an entire product design effort.

5 Reference Documents

KSZ8463ML/RL Datasheet (Contact Micrel for latest Datasheet)
KSZ8463ML/RL Evaluation Board Schematic (Contact Micrel for latest Schematic)
KSZ8463ML/RL Evaluation Board Gerber files
IEEE802.3 Specification
RMII Specification by RMII Consortium
KSZ8463ML Evaluation Kit User Guide

6 Revision History

Revision	Date	Summary of Changes
1.00	06/16/11	- Initial Release
1.01	08/30/11	- Removed eval kit information
1.02	09/19/11	- Updated text. - Added new board Figure 1.
1.03	09/23/11	- Changed MLLRLL to MLI/RLI, MLL to MLI, RLL to RLI
1.1	7/17/13	- Changed MLI/RLI to ML/RL, MLI to ML, RLI to RL - Added FML and FRL device suffixes - General overhaul