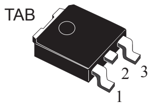
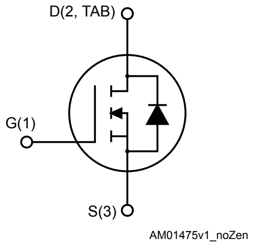
STD10NM65N

Datasheet

N-channel 650 V, 0.43 Ω typ., 9 A MDmesh™ II Power MOSFET in a DPAK package



DPAK



Features

Order code	V_{DS} @ $T_{jmax.}$	$R_{DS(on)}$ max.	I_D
STD10NM65N	710 V	0.48 Ω	9 A

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using the second generation of MDmesh™ technology. This revolutionary Power MOSFET associates a vertical structure to the company’s strip layout to yield one of the world’s lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.

Product status
STD10NM65N

Product summary	
Order code	STD10NM65N
Marking	10NM65N
Package	DPAK
Packing	Tape and reel

1 Electrical ratings

Table 1. **Absolute maximum ratings**

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	650	V
V_{GS}	Gate-source voltage	±25	V
I_D	Drain current (continuous) at T_C = 25 °C	9	A
I_D	Drain current (continuous) at T_C = 100 °C	5.7	A
I_{DM} (1)	Drain current (pulsed)	36	A
P_{TOT}	Total dissipation at T_C = 25 °C	90	W
dv/dt (2)	Peak diode recovery voltage slope	15	V/ns
dv/dt	Drain-source voltage slope (V_{DD} = 520 V, I_D = 9 A, V_{GS} = 10 V)	25	
T_j	Operating junction temperature range	-55 to 150	°C
T_{stg}	Storage temperature range		

1. *Pulse width limited by safe operating area.*
2. *$I_{SD} \leq 9$ A, di/dt ≤ 400 A/μs, $V_{DSpeak} \leq V_{(BR)DSS}$, V_{DD} = 80% $V_{(BR)DSS}$.*

Table 2. **Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	1.39	°C/W
$R_{thj\text{-}pcb}$ (1)	Thermal resistance junction-pcb	50	°C/W

1. *When mounted on 1inch² FR-4, 2 Oz copper board.*

Table 3. **Avalanche characteristics**

Symbol	Parameter	Value	Unit
I_{AS}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j Max)	2.5	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25 °C, I_D = I_{AS}, V_{DD} = 50 V)	200	mJ

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4. **On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0 V	650			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 650 V			1	µA
		V_{GS} = 0 V, V_{DS} = 650 V, T_C = 125 °C (1)			100	µA
I_{GSS}	Gate body leakage current	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 4.5 A		0.43	0.48	Ω

1. *Defined by design, not subject to production test.*

Table 5. **Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 50 V, f = 1 MHz, V_{GS} = 0 V	-	850	-	pF
C_{oss}	Output capacitance			53		
C_{rss}	Reverse transfer capacitance			4		
$C_{oss\ eq.}$ (1)	Equivalent output capacitance	V_{DS} = 0 to 520 V, V_{GS} = 0 V	-	90	-	pF
Q_g	Total gate charge	V_{DD} = 520 V, I_D = 9 A, V_{GS} = 0 to 10 V (see Figure 13. Test circuit for gate charge behavior)	-	25	-	nC
Q_{gs}	Gate-source charge			4		
Q_{gd}	Gate-drain charge			14		

1. *$C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.*

Table 6. **Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 325 V, I_D = 4.5 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 12. Test circuit for resistive load switching times and Figure 17. Switching time waveform)	-	12	-	ns
t_r	Rise time			8		
$t_{d(off)}$	Turn-off delay time			50		
$t_{f(i)}$	Fall time			20		

Table 7. **Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		9	A
I_{SDM} (1)	Source-drain current (pulsed)				36	
V_{SD} (2)	Forward on voltage	I_{SD} = 9 A, V_{GS} = 0 V	-		1.3	V
t_{rr}	Reverse recovery time	I_{SD} = 9 A, di/dt = 100 A/µs V_{DD} = 100 V (see Figure 14. Test circuit for inductive load switching and diode recovery times)	-	330		ns
Q_{rr}	Reverse recovery charge			3		µC
I_{RRM}	Reverse recovery current			19		A
t_{rr}	Reverse recovery time	I_{SD} = 9 A, di/dt = 100 A/µs V_{DD} = 100 V (see Figure 14. Test circuit for inductive load switching and diode recovery times)	-	430		ns
Q_{rr}	Reverse recovery charge			4		µC
I_{RRM}	Reverse recovery current			19		A

1. *Pulse width limited by safe operating area.*
2. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%.*

2.1 Electrical characteristics curves

Figure 1. Safe operating area

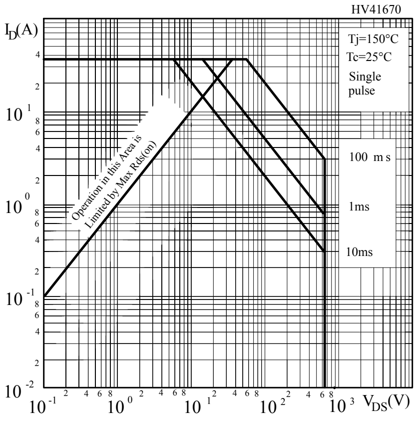


Figure 2. Thermal impedance

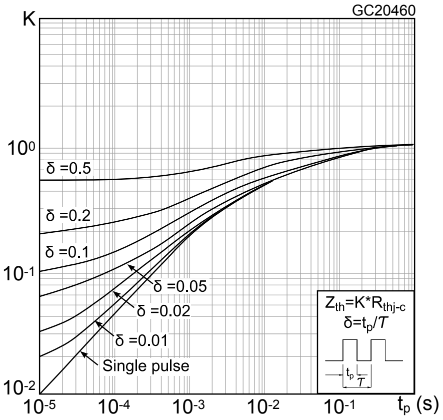


Figure 3. Output characterisics

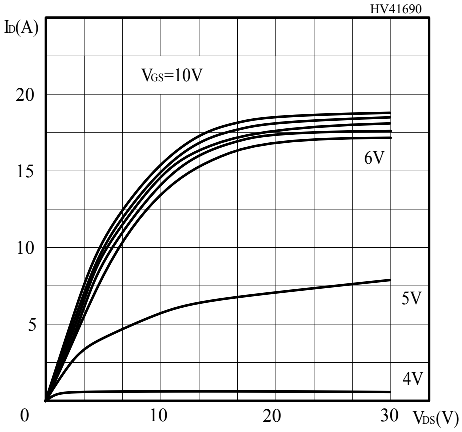


Figure 4. Transfer characteristics

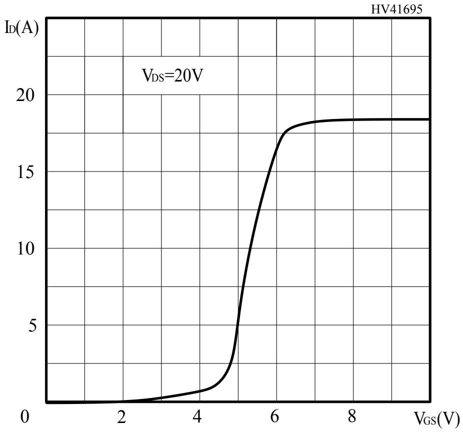


Figure 5. Static drain-source on resistance

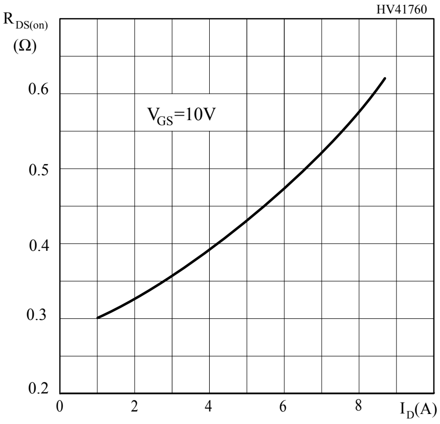


Figure 6. Gate charge vs gate-source voltage

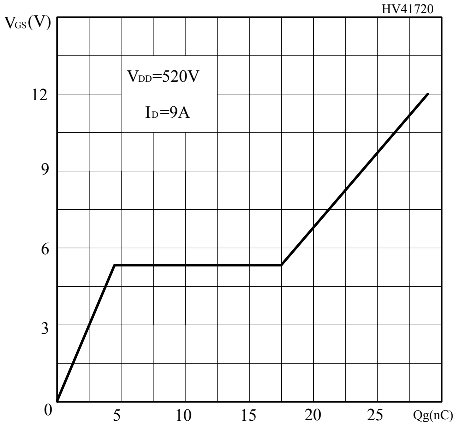


Figure 7. **Capacitance variations**

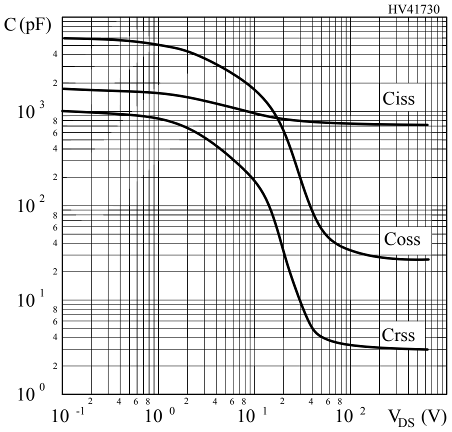


Figure 8. **Normalized gate threshold voltage vs temperature**

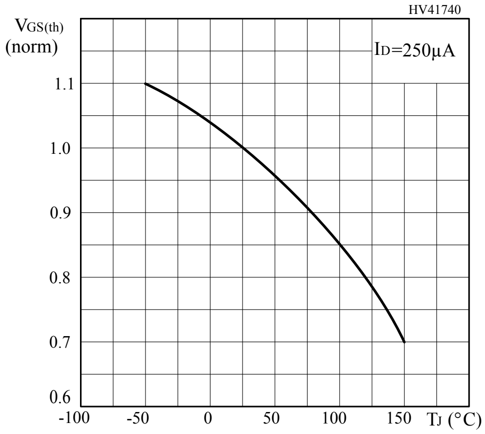


Figure 9. **Normalized on resistance vs temperature**

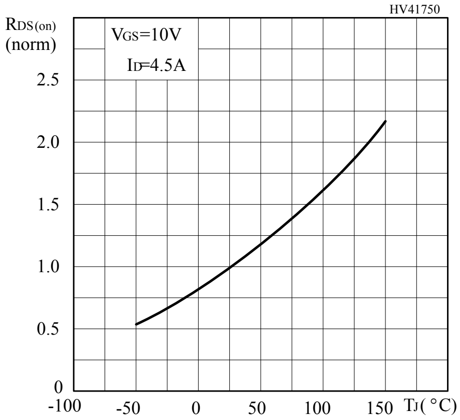


Figure 10. **Source-drain diode forward characteristic**

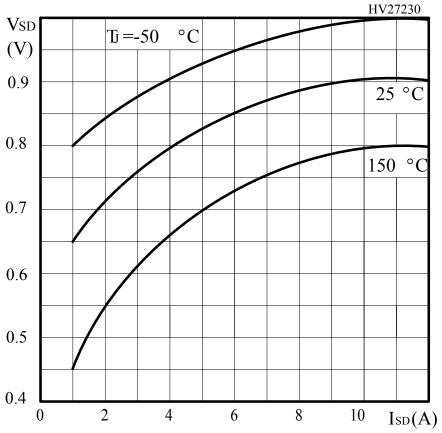
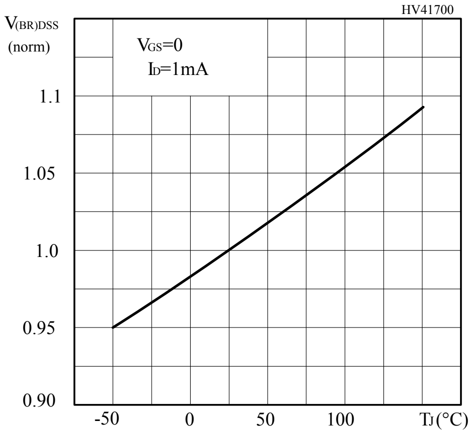


Figure 11. **Normalized $V_{(BR)DSS}$ vs temperature**



3 Test circuits

Figure 12. Test circuit for resistive load switching times

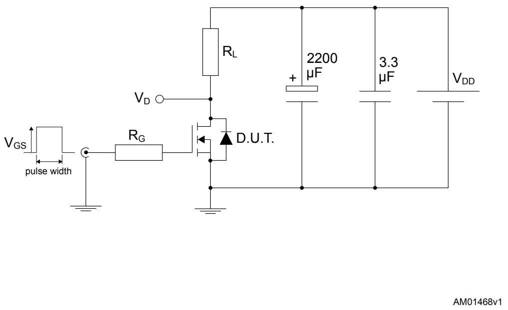


Figure 13. Test circuit for gate charge behavior

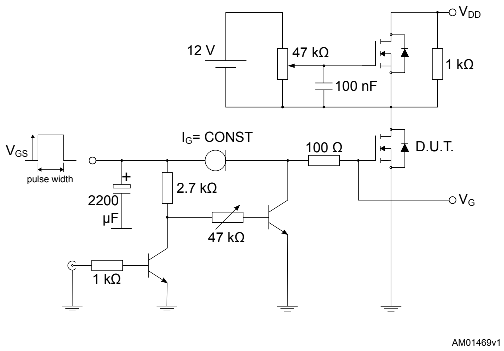


Figure 14. Test circuit for inductive load switching and diode recovery times

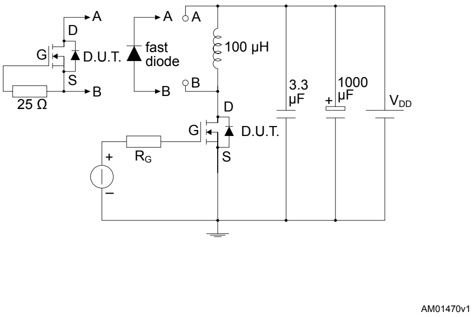


Figure 15. Unclamped inductive load test circuit

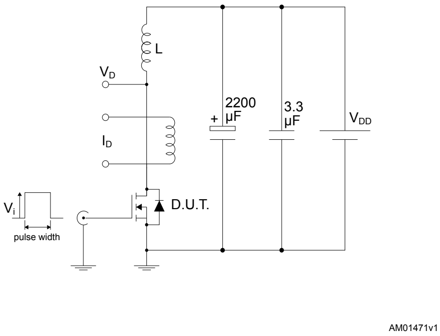


Figure 16. Unclamped inductive waveform

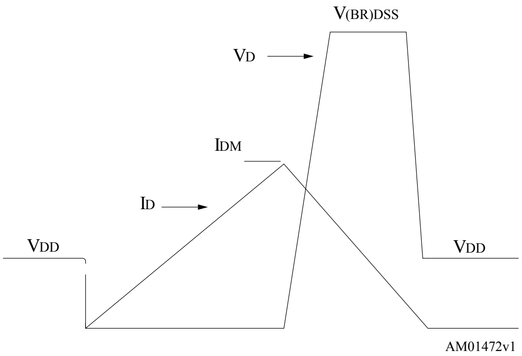
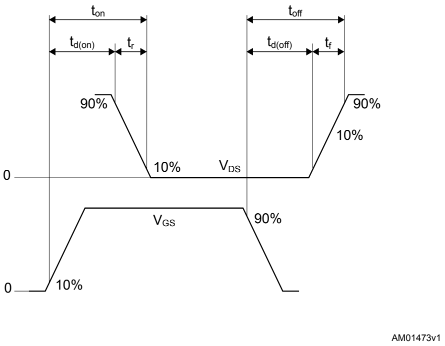


Figure 17. Switching time waveform

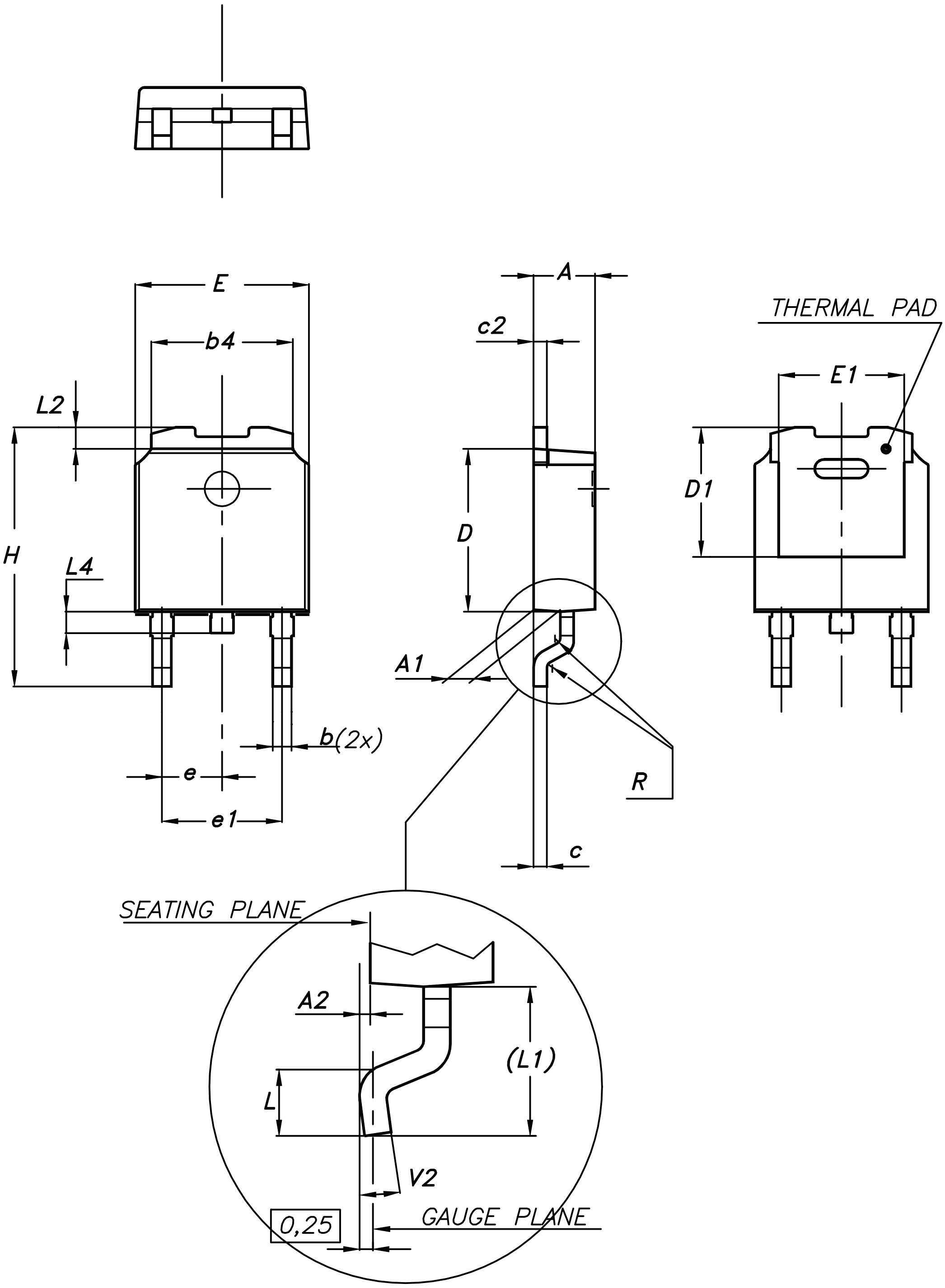


4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 DPAK (TO-252) type A2 package information

Figure 18. **DPAK (TO-252) type A2 package outline**



0068772_type-A2_rev25

Table 8. **DPAK (TO-252) type A2 mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	5.10	5.20	5.30
e	2.159	2.286	2.413
e1	4.445	4.572	4.699
H	9.35		10.10
L	1.00		1.50
L1	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

4.2 DPAK (TO-252) type C2 package information

Figure 19. DPAK (TO-252) type C2 package outline

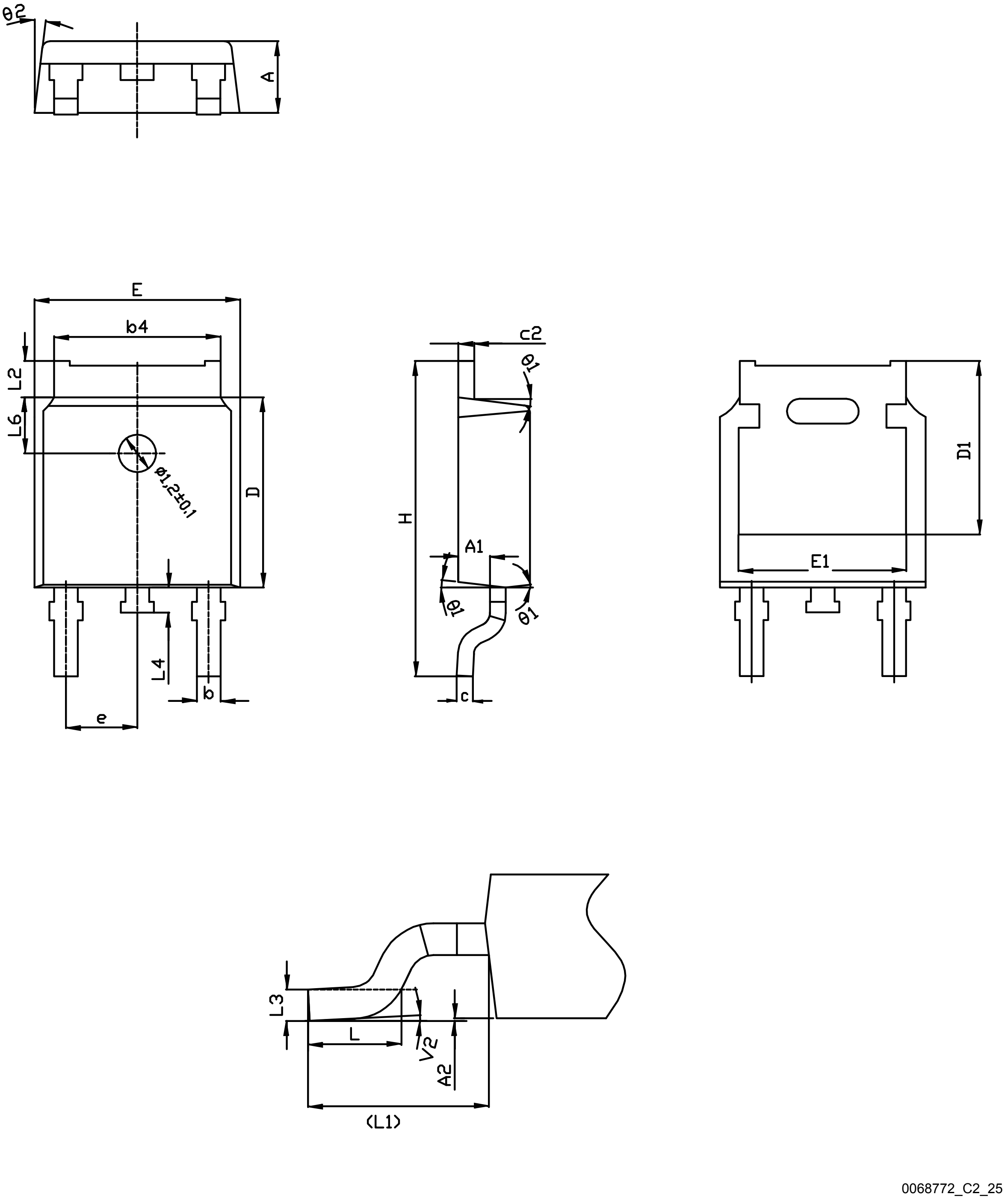
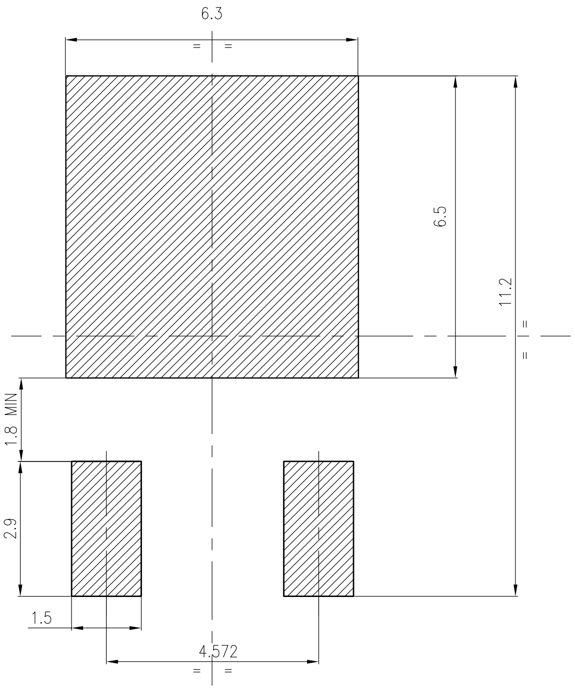


Table 9. **DPAK (TO-252) type C2 mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.20	2.30	2.38
A1	0.90	1.01	1.10
A2	0.00		0.10
b	0.72		0.85
b4	5.13	5.33	5.46
c	0.47		0.60
c2	0.47		0.60
D	6.00	6.10	6.20
D1	5.10		5.60
E	6.50	6.60	6.70
E1	5.20		5.50
e	2.186	2.286	2.386
H	9.80	10.10	10.40
L	1.40	1.50	1.70
L1		2.90 REF	
L2	0.90		1.25
L3		0.51 BSC	
L4	0.60	0.80	1.00
L6		1.80 BSC	
θ1	5°	7°	9°
θ2	5°	7°	9°
V2	0°		8°

Figure 20. **DPAK (TO-252) recommended footprint (dimensions are in mm)**



FP_0068772_25

4.3 DPAK (TO-252) packing information

Figure 21. DPAK (TO-252) tape outline

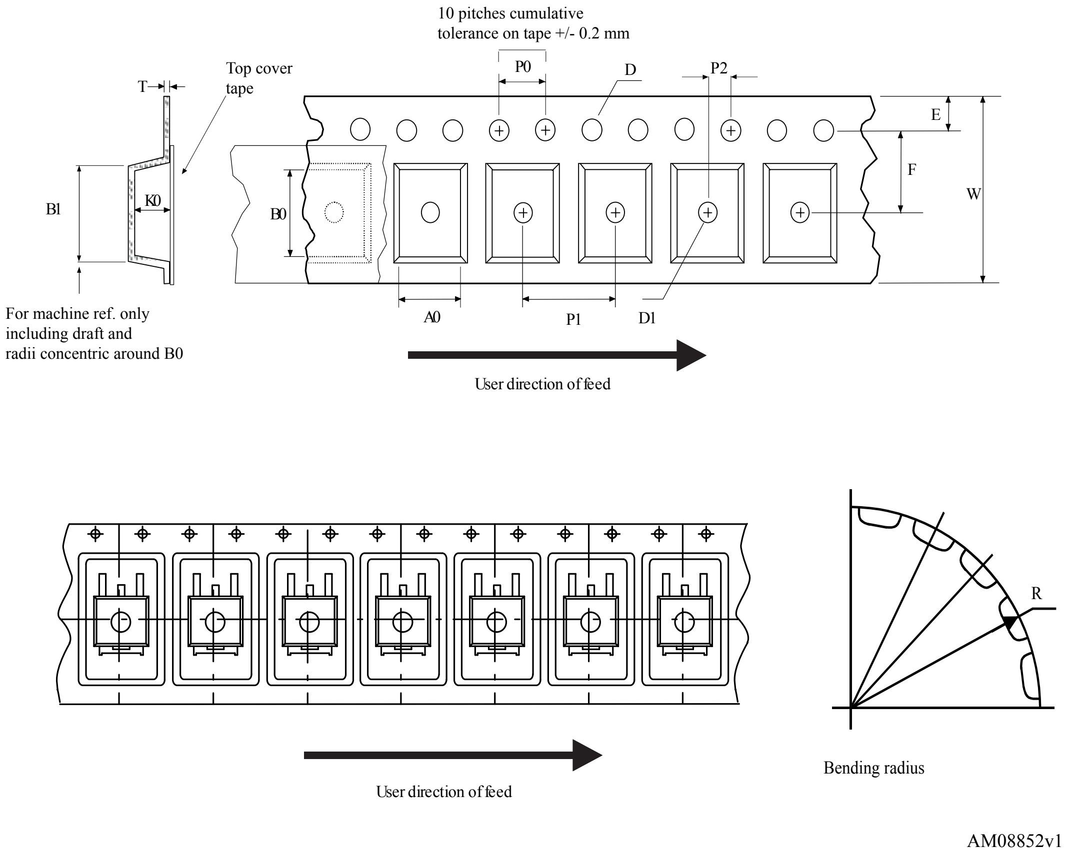
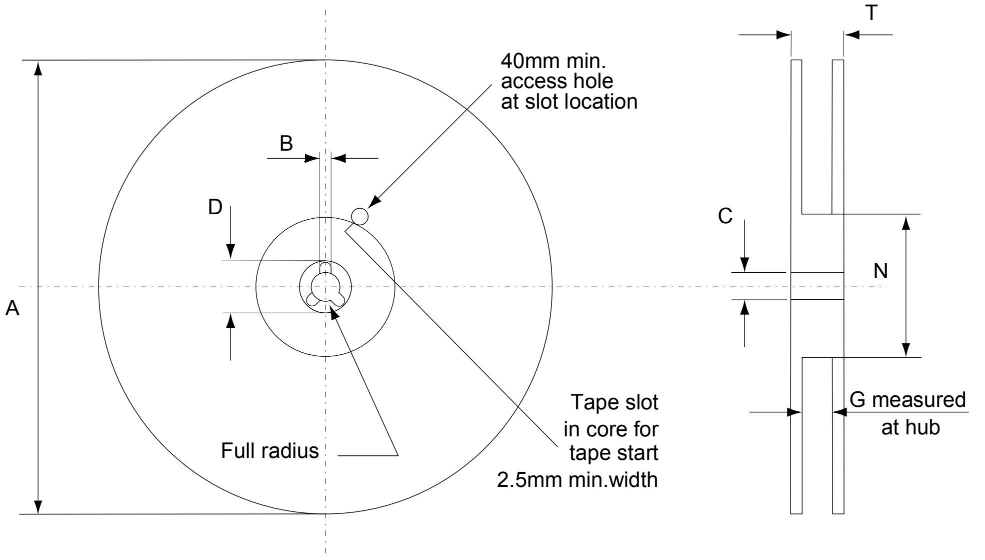


Figure 22. **DPAK (TO-252) reel outline**



AM06038v1

Table 10. **DPAK (TO-252) tape and reel mechanical data**

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

Revision history

Table 11. **Document revision history**

Date	Version	Changes
26-Oct-2007	1	Initial release.
07-Feb-2008	2	Document status promoted from preliminary data to datasheet.
14-Oct-2008	3	*Table 4: Avalanche characteristics* has been corrected.
16-May-2018	4	The part numbers STF10NM65N, STP10NM65N and STU10NM65N have been moved to a separate datasheet. Removed maturity status indication from cover page. The document status is production data. Updated features and description in cover page, Section 1 Electrical ratings, Section 2 Electrical characteristics, Section 2.1 Electrical characteristics curves and Section 4 Package information. Minor text changes.

Contents