74LVC3G14

Triple inverting Schmitt trigger with 5 V tolerant input

Rev. 17 — 2 August 2023 Product data sheet

1. General description

The 74LVC3G14 provides three inverting buffers with Schmitt trigger input. It is capable of transforming slowly changing input signals into sharply defined, jitter-free output signals.

The inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of this device in a mixed 3.3 V and 5 V environment. Schmitt trigger action at the inputs makes the circuit tolerant of slower input rise and fall time. This device is fully specified for partial power-down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

2. Features and benefits

- Wide supply voltage range from 1.65 V to 5.5 V
- 5 V tolerant input/output for interfacing with 5 V logic
- High noise immunity
- ±24 mA output drive (V_{CC} = 3.0 V)
- CMOS low power consumption
- Latch-up performance exceeds 250 mA
- Direct interface with TTL levels
- Unlimited rise and fall times
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Multiple package options
- Specified from -40 °C to +85 °C and -40 °C to +125 °C.

3. Applications

- Wave and pulse shaper for highly noisy environment
- Astable multivibrator
- Monostable multivibrator.

nexperia

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVC3G14DP	-40 °C to +125 °C	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm	SOT505-2
74LVC3G14DC	-40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	SOT765-1
74LVC3G14GT	-40 °C to +125 °C	XSON8	plastic extremely thin small outline package; no leads; 8 terminals; body 1 × 1.95 × 0.5 mm	SOT833-1
74LVC3G14GF	-40 °C to +125 °C	XSON8	extremely thin small outline package; no leads; 8 terminals; body 1.35 × 1 × 0.5 mm	SOT1089
74LVC3G14GN	-40 °C to +125 °C	XSON8	extremely thin small outline package; no leads; 8 terminals; body 1.2 × 1.0 × 0.35 mm	SOT1116
74LVC3G14GS	-40 °C to +125 °C	XSON8	extremely thin small outline package; no leads; 8 terminals; body 1.35 × 1.0 × 0.35 mm	SOT1203

5. Marking

Table 2. Marking codes

Type number	Marking code [1]
74LVC3G14DP	V14
74LVC3G14DC	V14
74LVC3G14GT	V14
74LVC3G14GF	VK
74LVC3G14GN	VK
74LVC3G14GS	VK

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

6. Functional diagram

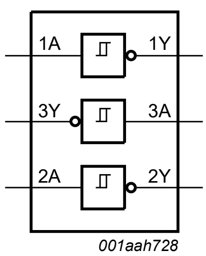


Fig. 1. Logic symbol

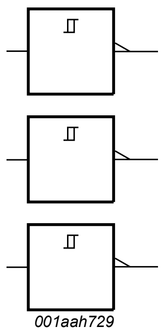


Fig. 2. IEC logic symbol

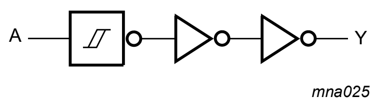


Fig. 3. Logic diagram (one Schmitt trigger)

7. Pinning information

7.1. Pinning

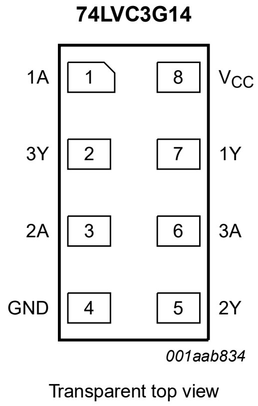
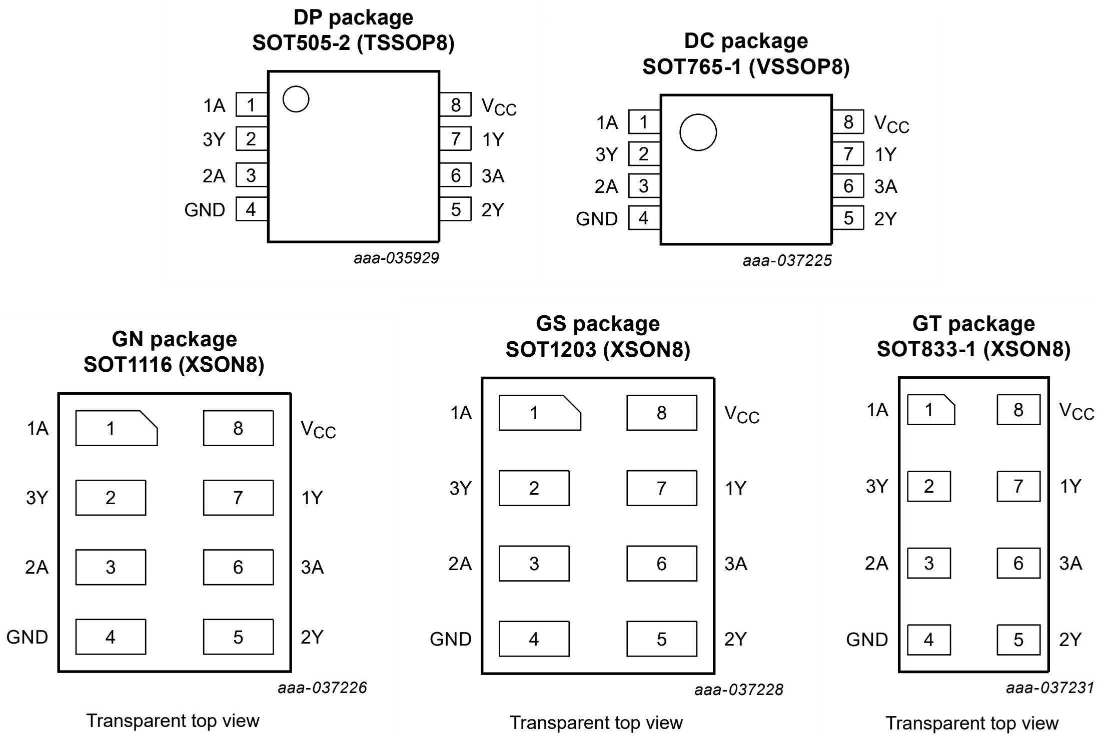


Fig. 4. Pin configuration SOT1089 (XSON8)



7.2. Pin description

Table 3. Pin description

Symbol	Pin	Description
1A, 2A, 3A	1, 3, 6	data input
1Y, 2Y, 3Y	7, 5, 2	data output
GND	4	ground (0 V)
V_{CC}	8	supply voltage

8. Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level

Input nA	Output nY
L	H
H	L

9. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			-0.5	+6.5	V
I_{IK}	input clamping current	$V_I < 0$ V		-50	-	mA
V_I	input voltage		[1]	-0.5	+6.5	V
I_{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V		-	±50	mA
V_O	output voltage	Active mode	[1]	-0.5	V_{CC} + 0.5	V
		Power-down mode; V_{CC} = 0 V	[1]	-0.5	+6.5	V
I_O	output current	V_O = 0 V to V_{CC}		-	±50	mA
I_{CC}	supply current			-	100	mA
I_{GND}	ground current			-100	-	mA
P_{tot}	total power dissipation	T_{amb} = -40 °C to +125 °C	[2]	-	250	mW
T_{stg}	storage temperature			-65	+150	°C

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT505-2 (TSSOP8) package: P_{tot} derates linearly with 4.6 mW/K above 96 °C.
For SOT765-1 (VSSOP8) package: P_{tot} derates linearly with 4.9 mW/K above 99 °C.
For SOT833-1 (XSON8) package: P_{tot} derates linearly with 3.1 mW/K above 68 °C.
For SOT1089 (XSON8) package: P_{tot} derates linearly with 4.0 mW/K above 88 °C.
For SOT1116 (XSON8) package: P_{tot} derates linearly with 4.2 mW/K above 90 °C.
For SOT1203 (XSON8) package: P_{tot} derates linearly with 3.6 mW/K above 81 °C.

10. Recommended operating conditions

Table 6. Operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		1.65	5.5	V
V_I	input voltage		0	5.5	V
V_O	output voltage	Active mode	0	V_{CC}	V
		Power-down mode; V_{CC} = 0 V	0	5.5	V
T_{amb}	ambient temperature		-40	+125	°C

11. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
V_{OH}	HIGH-level output voltage	$V_I = V_{T+}$ or V_{T-}						
		I_O = -100 μA; V_{CC} = 1.65 V to 5.5 V	V_{CC} - 0.1	-	-	V_{CC} - 0.1	-	V
		I_O = -4 mA; V_{CC} = 1.65 V	1.2	-	-	0.95	-	V
		I_O = -8 mA; V_{CC} = 2.3 V	1.9	-	-	1.7	-	V
		I_O = -12 mA; V_{CC} = 2.7 V	2.2	-	-	1.9	-	V
		I_O = -24 mA; V_{CC} = 3.0 V	2.3	-	-	2.0	-	V
		I_O = -32 mA; V_{CC} = 4.5 V	3.8	-	-	3.4	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{T+}$ or V_{T-}						
		I_O = 100 μA; V_{CC} = 1.65 V to 5.5 V	-	-	0.1	-	0.1	V
		I_O = 4 mA; V_{CC} = 1.65 V	-	-	0.45	-	0.7	V
		I_O = 8 mA; V_{CC} = 2.3 V	-	-	0.3	-	0.45	V
		I_O = 12 mA; V_{CC} = 2.7 V	-	-	0.4	-	0.6	V
		I_O = 24 mA; V_{CC} = 3.0 V	-	-	0.55	-	0.8	V
		I_O = 32 mA; V_{CC} = 4.5 V	-	-	0.55	-	0.8	V
I_I	input leakage current	V_I = 5.5 V or GND; V_{CC} = 0 V to 5.5 V	-	±0.1	±1	-	±1	μA
I_{OFF}	power-off leakage current	V_I or V_O = 5.5 V; V_{CC} = 0 V	-	±0.1	±2	-	±2	μA
I_{CC}	supply current	V_I = 5.5 V or GND; I_O = 0 A; V_{CC} = 1.65 V to 5.5 V	-	0.1	4	-	4	μA
ΔI_{CC}	additional supply current	$V_I = V_{CC}$ - 0.6 V; I_O = 0 A; V_{CC} = 2.3 V to 5.5 V	-	5	500	-	500	μA
C_I	input capacitance	V_{CC} = 3.3 V; V_I = GND to V_{CC}	-	3.5	-	-	-	pF

[1] All typical values are measured at maximum V_{CC} and T_{amb} = 25 °C.

11.1. Transfer characteristics

Table 8. Transfer characteristics

Voltages are referenced to GND (ground = 0 V; for test circuit see Fig. 9.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
V_{T+}	positive-going threshold voltage	see Fig. 5 and Fig. 6						
		V_{CC} = 1.8 V	0.70	1.10	1.50	0.70	1.70	V
		V_{CC} = 2.3 V	1.00	1.40	1.80	1.00	2.00	V
		V_{CC} = 3.0 V	1.30	1.76	2.20	1.30	2.40	V
		V_{CC} = 4.5 V	1.90	2.47	3.10	1.90	3.30	V
		V_{CC} = 5.5 V	2.20	2.91	3.60	2.20	3.80	V

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
V_{T-}	negative-going threshold voltage	see Fig. 5 and Fig. 6						
		V_{CC} = 1.8 V	0.25	0.61	0.90	0.25	1.10	V
		V_{CC} = 2.3 V	0.40	0.80	1.15	0.40	1.35	V
		V_{CC} = 3.0 V	0.60	1.04	1.50	0.60	1.70	V
		V_{CC} = 4.5 V	1.00	1.55	2.00	1.00	2.20	V
		V_{CC} = 5.5 V	1.20	1.86	2.30	1.20	2.50	V
V_H	hysteresis voltage	(V_{T+} - V_{T-}); see Fig. 5, Fig. 6 and Fig. 7						
		V_{CC} = 1.8 V	0.15	0.49	1.00	0.15	1.20	V
		V_{CC} = 2.3 V	0.25	0.60	1.10	0.25	1.30	V
		V_{CC} = 3.0 V	0.40	0.73	1.20	0.40	1.40	V
		V_{CC} = 4.5 V	0.60	0.92	1.50	0.60	1.70	V
		V_{CC} = 5.5 V	0.70	1.02	1.70	0.70	1.90	V

[1] All typical values are measured at T_{amb} = 25 °C

11.2. Waveforms transfer characteristics

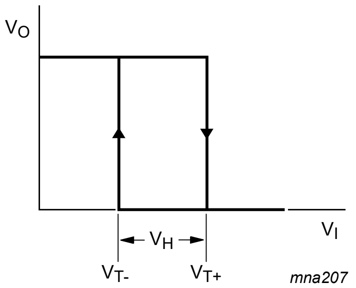
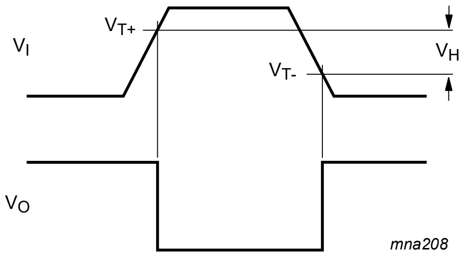
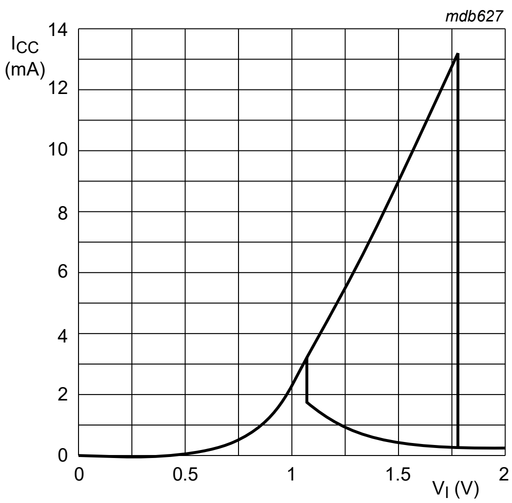


Fig. 5. Transfer characteristic



V_{T+} and V_{T-} limits at 70 % and 20 %.

Fig. 6. Definition of V_{T+}, V_{T-} and V_H



V_{CC} = 3.0 V

Fig. 7. Typical transfer characteristics

12. Dynamic characteristics

Table 9. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see Fig. 9.

Symbol	Parameter	Conditions		-40 °C to +85 °C			-40 °C to +125 °C		Unit
				Min	Typ [1]	Max	Min	Max	
t_{pd}	propagation delay	nA to nY; see Fig. 8	[2]						
		V_{CC} = 1.65 V to 1.95 V		1.0	4.2	11.0	1.0	12.0	ns
		V_{CC} = 2.3 V to 2.7 V		0.5	3.0	6.5	0.5	7.2	ns
		V_{CC} = 2.7 V		0.5	3.8	7.0	0.5	7.7	ns
		V_{CC} = 3.0 V to 3.6 V		0.5	3.2	6.0	0.5	6.7	ns
		V_{CC} = 4.5 V to 5.5 V		0.5	2.4	4.3	0.5	4.7	ns
C_{PD}	power dissipation capacitance	V_I = GND to V_{CC}; V_{CC} = 3.3 V	[3]	-	18.1	-	-	-	pF

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.8 V, 2.5 V, 2.7 V, 3.3 V and 5.0 V respectively.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

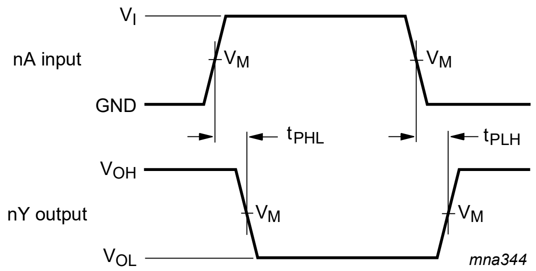
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

12.1. Waveforms and test circuit



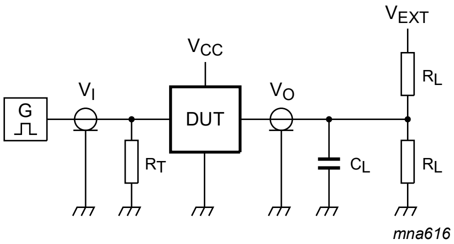
Measurement points are given in Table 10.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 8. The data input (nA) to output (nY) propagation delays

Table 10. Measurement points

V_{CC}	Input V_M	Output V_M
1.65 V to 1.95 V	0.5 × V_{CC}	0.5 × V_{CC}
2.3 V to 2.7 V	0.5 × V_{CC}	0.5 × V_{CC}
2.7 V	1.5 V	1.5 V
3.0 V to 3.6 V	1.5 V	1.5 V
4.5 V to 5.5 V	0.5 × V_{CC}	0.5 × V_{CC}



Test data is given in Table 11.

Definitions for test circuit:

R_L = Load resistance;

C_L = Load capacitance including jig and probe capacitance;

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator;

V_{EXT} = External voltage for measuring switching times.

Fig. 9. Test circuit for measuring switching times

Table 11. Test data

Supply voltage	Input		Load		V_{EXT}
V_{CC}	V_I	$t_r = t_f$	C_L	R_L	t_{PLH}, t_{PHL}
1.65 V to 1.95 V	V_{CC}	≤ 2.0 ns	30 pF	1 kΩ	open
2.3 V to 2.7 V	V_{CC}	≤ 2.0 ns	30 pF	500 Ω	open
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open
4.5 V to 5.5 V	V_{CC}	≤ 2.5 ns	50 pF	500 Ω	open

13. Application information

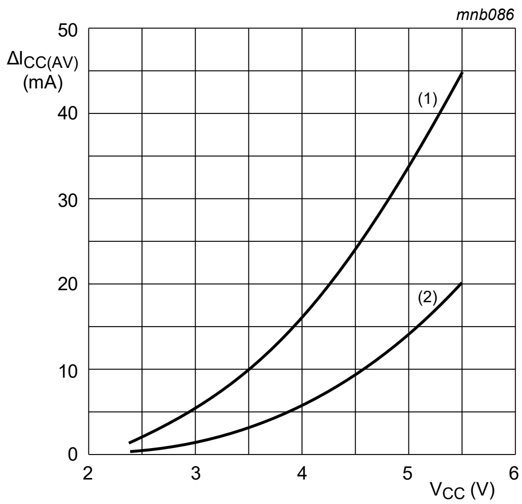
The slow input rise and fall times cause additional power dissipation, this can be calculated using the following formula:

$P_{add} = f_i \times (t_r \times \Delta I_{CC(AV)} + t_f \times \Delta I_{CC(AV)}) \times V_{CC}$ where:

P_{add} = additional power dissipation (μW);
f_i = input frequency (MHz);
t_r = input rise time (ns); 10 % to 90 %;
t_f = input fall time (ns); 90 % to 10 %;
$\Delta I_{CC(AV)}$ = average additional supply current (μA).

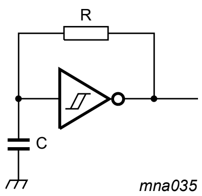
$\Delta I_{CC(AV)}$ differs with positive or negative input transitions, as shown in Fig. 10.

An example of a relaxation circuit using the 74LVC3G14 is shown in Fig. 11.



Linear change of V_I between 0.8 V to 2.0 V. All values given are typical unless otherwise specified.
(1) Positive-going edge.
(2) Negative-going edge.

Fig. 10. $\Delta I_{CC(AV)}$ as a function of V_{CC}



$$f = \frac{1}{T} \approx \frac{1}{K \times RC}$$

For K-factor, see Fig. 12

Fig. 11. Relaxation oscillator

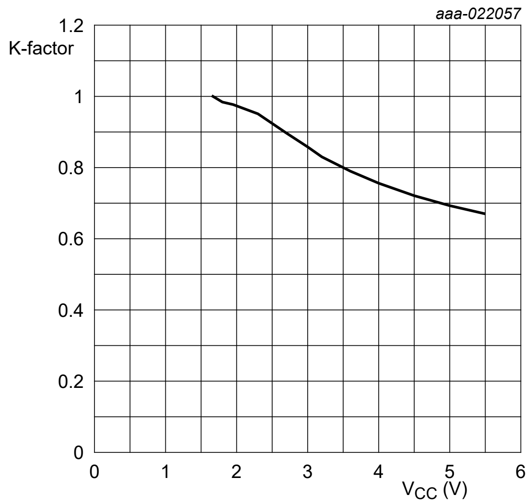
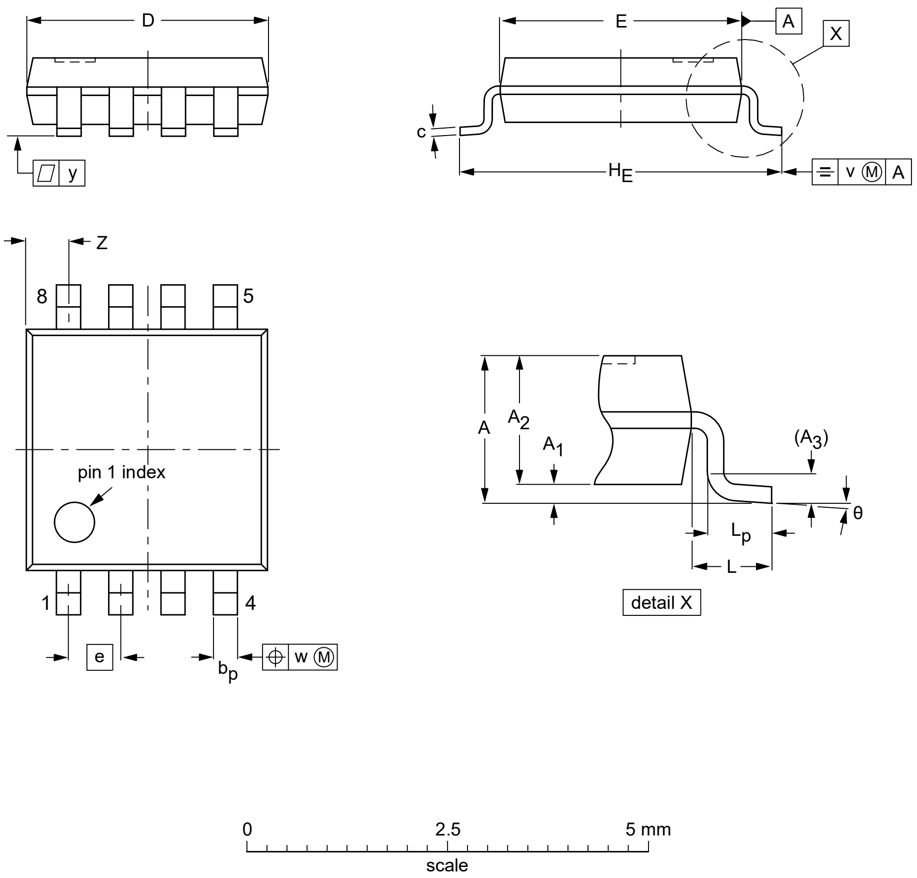


Fig. 12. Typical K-factor for relaxation oscillator

14. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	v	w	y	Z(1)	θ
mm	1.1	0.15 0.00	0.95 0.75	0.25	0.38 0.22	0.18 0.08	3.1 2.9	3.1 2.9	0.65	4.1 3.9	0.5	0.47 0.33	0.2	0.13	0.1	0.70 0.35	8° 0°

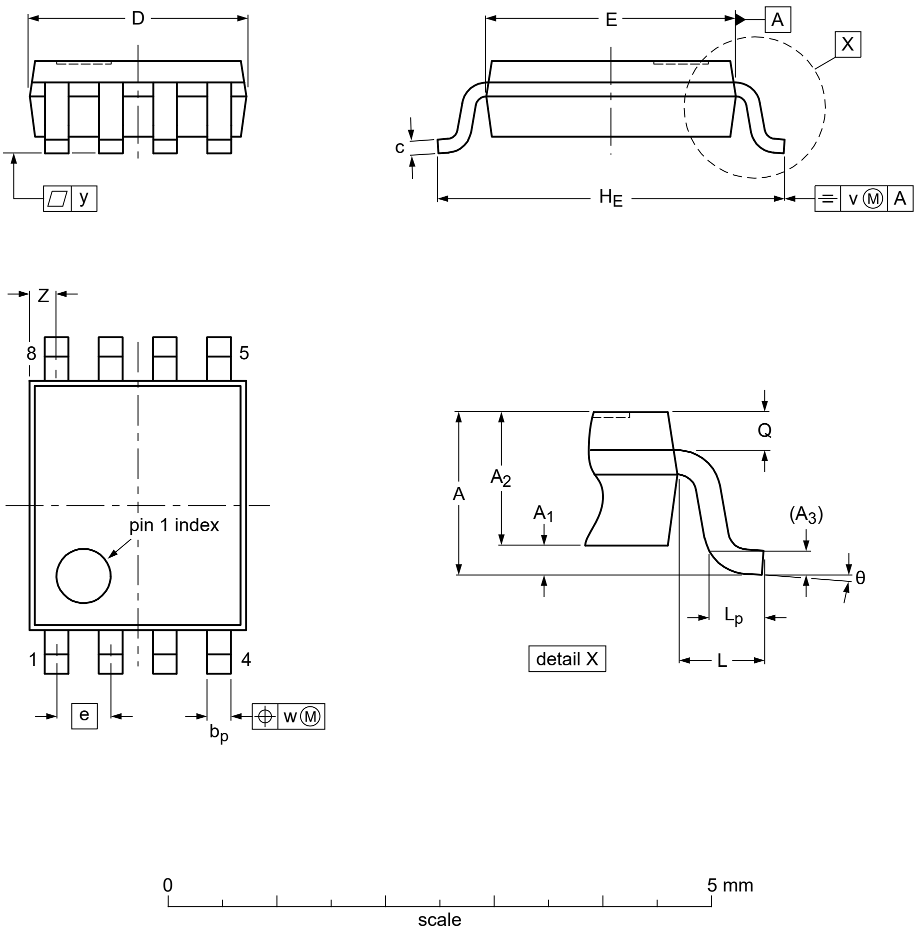
Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT505-2		- - -				02-01-16

Fig. 13. Package outline SOT505-2 (TSSOP8)

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm **SOT765-1**



Dimensions (mm are the original dimensions)

Unit		A max.	A_1	A_2	A_3	b_p	c	D(1)	E(2)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	max		0.15	0.85		0.27	0.23	2.1	2.4		3.2		0.40	0.21				0.4	8°
	nom	1			0.12					0.5		0.4			0.2	0.08	0.1		
	min		0.00	0.60		0.17	0.08	1.9	2.2		3.0		0.15	0.19				0.1	0°

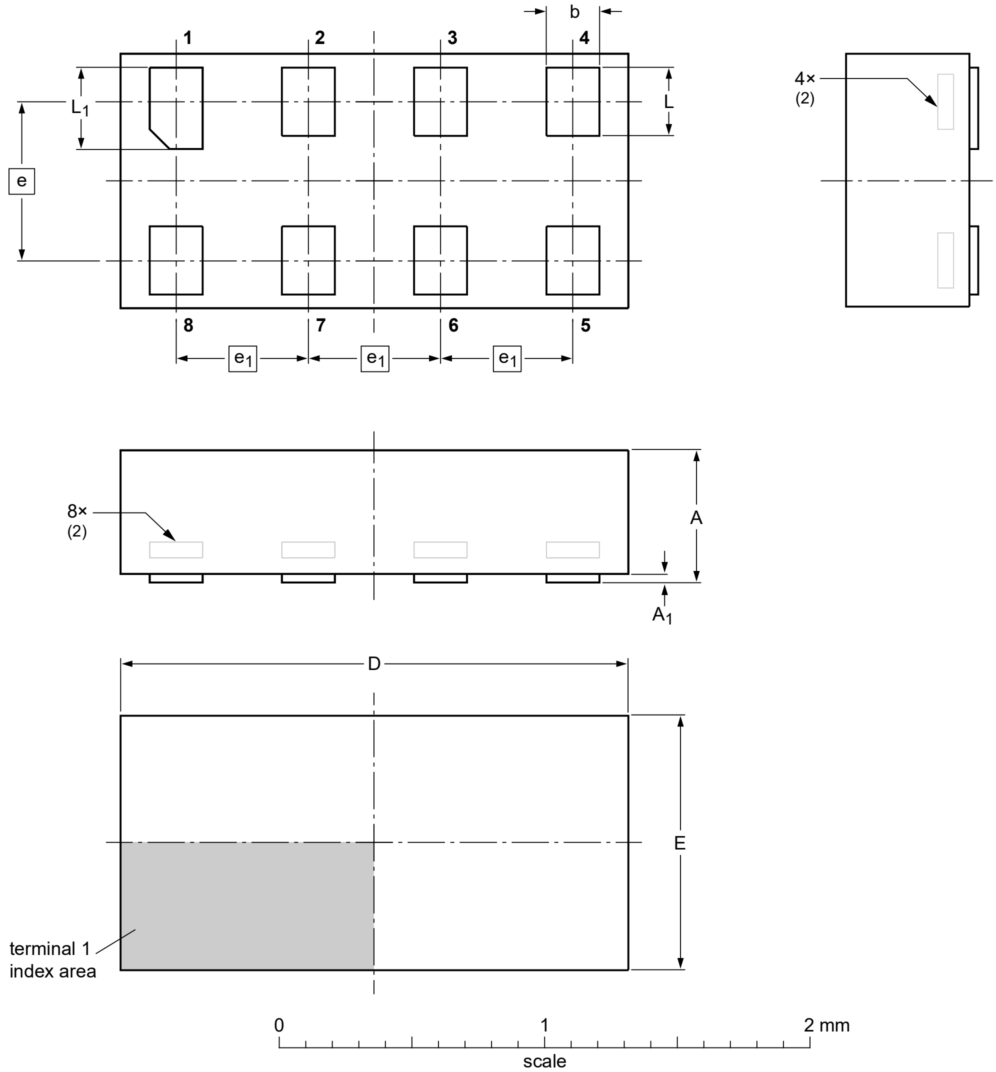
Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

sot765-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT765-1		MO-187				~~07-06-02~~ 16-05-31

Fig. 14. Package outline SOT765-1 (VSSOP8)

XSON8: plastic extremely thin small outline package; no leads; 8 terminals; body 1 x 1.95 x 0.5 mm **SOT833-1**



DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max	A_1 max	b	D	E	e	e_1	L	L_1
mm	0.5	0.04	0.25 0.17	2.0 1.9	1.05 0.95	0.6	0.5	0.35 0.27	0.40 0.32

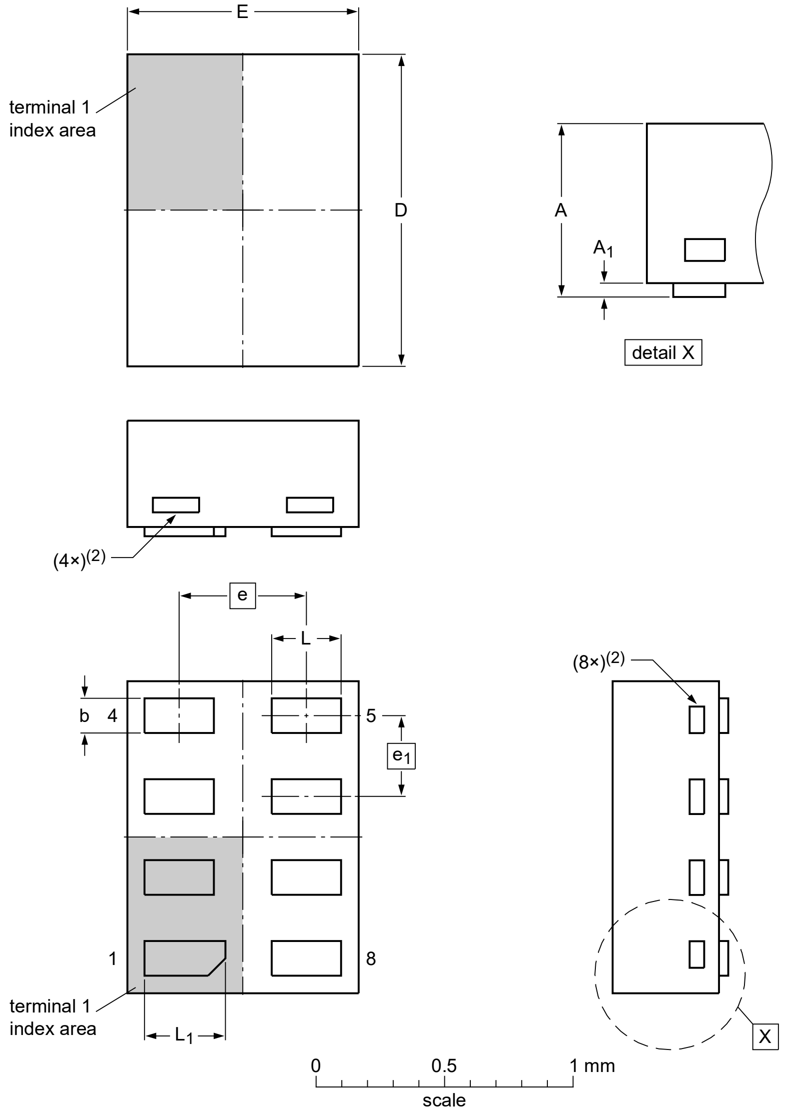
Notes

1. Including plating thickness.
2. Can be visible in some manufacturing processes.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT833-1	- - -	MO-252	- - -			~~07-11-14~~ 07-12-07

Fig. 15. Package outline SOT833-1 (XSON8)

XSON8: extremely thin small outline package; no leads;
8 terminals; body 1.35 x 1 x 0.5 mm **SOT1089**



Dimensions

Unit		A(1)	A_1	b	D	E	e	e_1	L	L_1
	max	0.5	0.04	0.20	1.40	1.05			0.35	0.40
mm	nom			0.15	1.35	1.00	0.55	0.35	0.30	0.35
	min			0.12	1.30	0.95			0.27	0.32

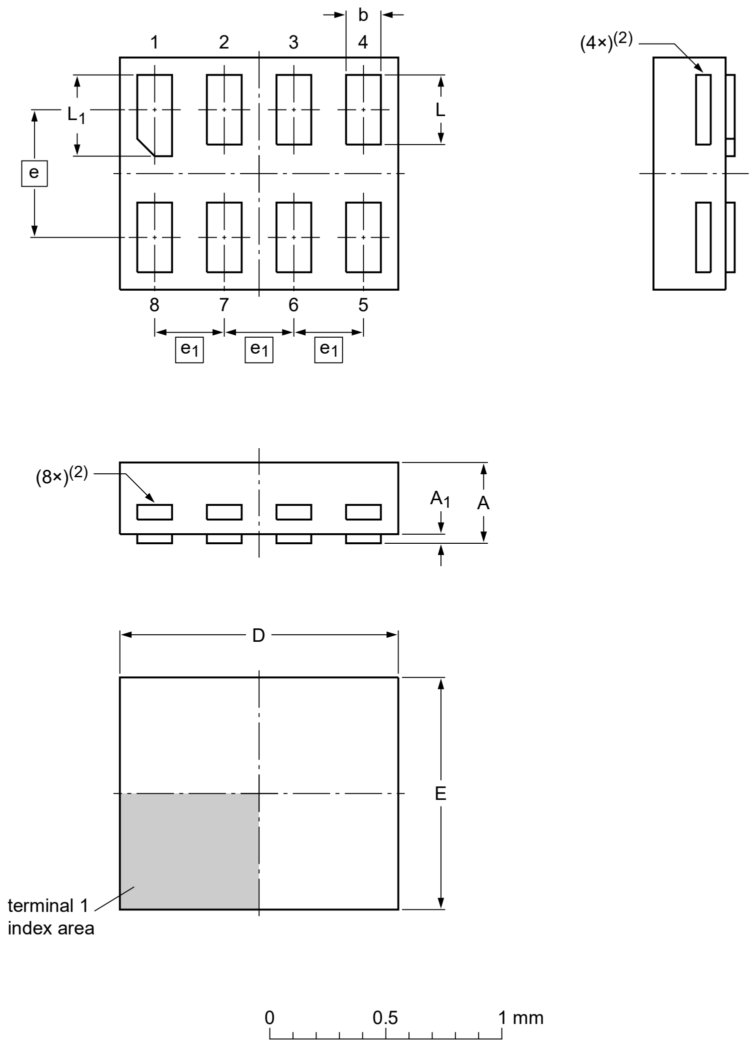
Note
1. Including plating thickness.
2. Visible depending upon used manufacturing technology.

sot1089_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1089		MO-252				~~10-04-09~~ 10-04-12

Fig. 16. Package outline SOT1089 (XSON8)

XSON8: extremely thin small outline package; no leads;
8 terminals; body 1.2 x 1.0 x 0.35 mm **SOT1116**



Dimensions

Unit		A(1)	A_1	b	D	E	e	e_1	L	L_1
mm	max	0.35	0.04	0.20	1.25	1.05			0.35	0.40
	nom			0.15	1.20	1.00	0.55	0.3	0.30	0.35
	min			0.12	1.15	0.95			0.27	0.32

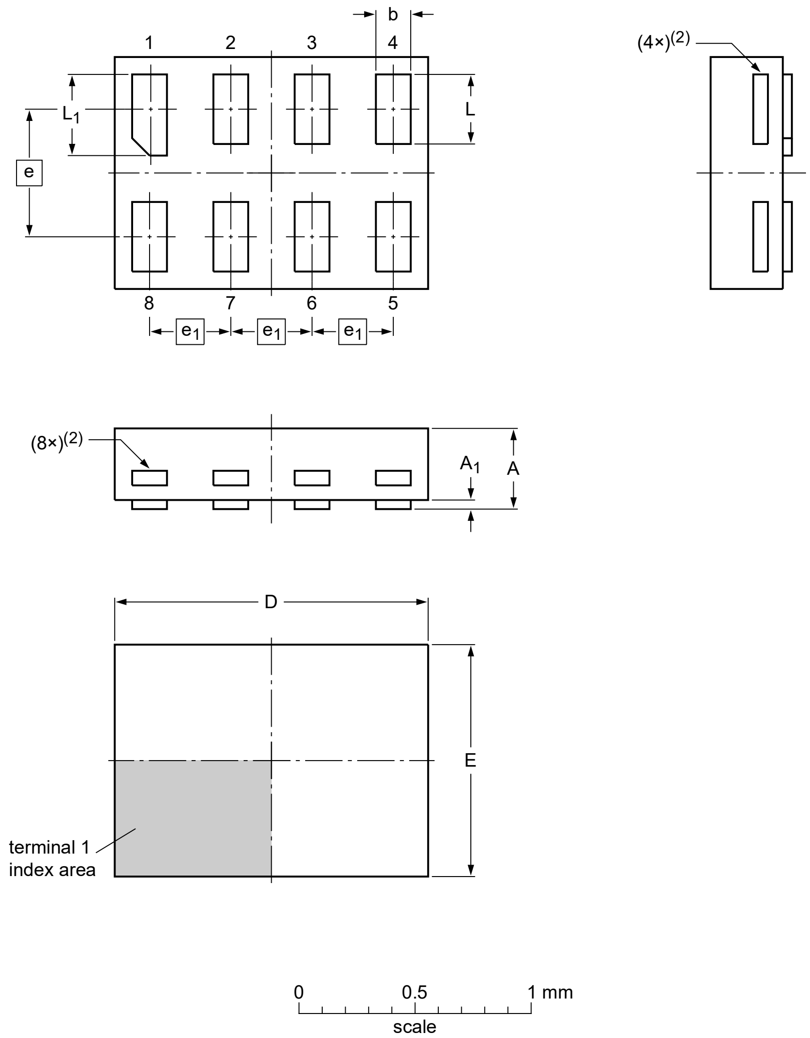
Note
1. Including plating thickness.
2. Visible depending upon used manufacturing technology.

sot1116_po

Outline version	References: IEC	References: JEDEC	References: JEITA		European projection	Issue date
SOT1116						~~10-04-02~~ 10-04-07

Fig. 17. Package outline SOT1116 (XSON8)

XSON8: extremely thin small outline package; no leads;
8 terminals; body 1.35 x 1.0 x 0.35 mm **SOT1203**



Dimensions

Unit		A(1)	A1	b	D	E	e	e1	L	L1
mm	max	0.35	0.04	0.20	1.40	1.05			0.35	0.40
	nom			0.15	1.35	1.00	0.55	0.35	0.30	0.35
	min			0.12	1.30	0.95			0.27	0.32

Note
1. Including plating thickness.
2. Visible depending upon used manufacturing technology.

sot1203_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1203						~~10-04-02~~ 10-04-06

Fig. 18. Package outline SOT1203 (XSON8)

15. Abbreviations

Table 12. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

16. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC3G14 v.17	20230802	Product data sheet	-	74LVC3G14 v.16
Modifications:	• Section 2: ESD specification updated according to the latest JEDEC standard.			
74LVC3G14 v.16	20190731	Product data sheet	-	74LVC3G14 v.15
Modifications:	• Type number 74LVC3G14GM (SOT902-2/XQFN8) removed. • Table 5: Derating values for P_{tot} total power dissipation updated.			
74LVC3G14 v.15	20190103	Product data sheet	-	74LVC3G14 v.14
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Type number 74LVC3G14GD (SOT996-2) removed.			
74LVC3G14 v.14	20161215	Product data sheet	-	74LVC3G14 v.13
Modifications:	• Table 7: The maximum limits for leakage current and supply current have changed.			
74LVC3G14 v.13	20160315	Product data sheet	-	74LVC3G14 v.12
Modifications:	• Fig. 12 added (typical K-factor for relaxation oscillator).			
74LVC3G14 v.12	20130409	Product data sheet	-	74LVC3G14 v.11
Modifications:	• For type number 74LVC3G14GD XSON8U has changed to XSON8.			
74LVC3G14 v.11	20120706	Product data sheet	-	74LVC3G14 v.10
Modifications:	• For type number 74LVC3G14GM the SOT code has changed to SOT902-2.			
74LVC3G14 v.10	20111123	Product data sheet	-	74LVC3G14 v.9
Modifications:	• Legal pages updated.			
74LVC3G14 v.9	20110922	Product data sheet	-	74LVC3G14 v.8
74LVC3G14 v.8	20100819	Product data sheet	-	74LVC3G14 v.7
74LVC3G14 v.7	20080612	Product data sheet	-	74LVC3G14 v.6
74LVC3G14 v.6	20080207	Product data sheet	-	74LVC3G14 v.5
74LVC3G14 v.5	20071005	Product data sheet	-	74LVC3G14 v.4
74LVC3G14 v.4	20070314	Product data sheet	-	74LVC3G14 v.3
74LVC3G14 v.3	20050131	Product data sheet	-	74LVC3G14 v.2
74LVC3G14 v.2	20041027	Product data sheet	-	74LVC3G14 v.1
74LVC3G14 v.1	20040510	Product data sheet	-	-

17. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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