

STF19NM50N, STP19NM50N, STW19NM50N

N-channel 500 V, 0.2 Ω typ., 14 A MDmesh™ II Power MOSFETs in TO-220FP, TO-220 and TO-247 packages

Datasheet - production data

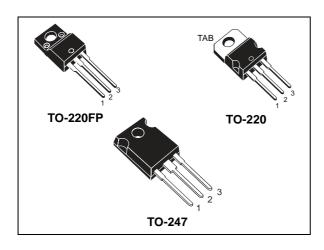
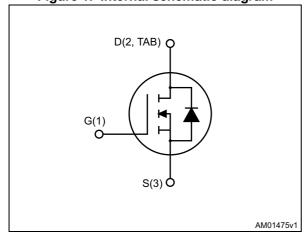


Figure 1. Internal schematic diagram



Features

Order codes	V _{DS @} T _{Jmax}	R _{DS(on)} max	I _D
STF19NM50N			
STP19NM50N	550 V	$0.25~\Omega$	14 A
STW19NM50N			

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

Applications

• Switching applications

Description

These devices are N-channel Power MOSFETs developed using the second generation of MDmesh™ technology. This revolutionary Power MOSFET associates a vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.

Table 1. Device summary

Order codes	Marking	Packages	Packaging
STF19NM50N		TO-220FP	
STP19NM50N	19NM50N	TO-220	Tube
STW19NM50N		TO-247	

Contents

1	Electrical ratings
2	Electrical characteristics
	2.1 Electrical characteristics (curves)
3	Test circuits
4	Package mechanical data
5	Revision history

1 Electrical ratings

Table 2. Absolute maximum ratings

Comple of	Boundary		Value		l lm!r
Symbol	Parameter	TO-220	TO-247	TO-220FP	Unit
V _{DS}	Drain-source voltage		500		V
V _{GS}	Gate-source voltage		± 25		V
I _D	Drain current (continuous) at T _C = 25 °C	14		14 ⁽¹⁾	Α
I _D	Drain current (continuous) at T _C = 100 °C	10		10 ⁽¹⁾	Α
I _{DM} ⁽²⁾	Drain current (pulsed)	56		56 ⁽¹⁾	Α
P _{TOT}	Total dissipation at T _C = 25 °C	110		30	W
dv/dt ⁽³⁾	Peak diode recovery voltage slope		15		V/ns
V _{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s; Tc = 25 °C)	250		2500	V
T _{stg}	Storage temperature	- 55 to 150		°C	
Tj	Max. operating junction temperature		150		°C

- 1. Limited by maximum junction temperature
- 2. Pulse width limited by safe operating area
- 3. $I_{SD} \leq$ 14 A, di/dt \leq 400 A/ μ s, V_{DS} peak \leq $V_{(BR)DSS}$, V_{DD} = 80% $V_{(BR)DSS}$.

Table 3. Thermal data

Symbol Parameter			Unit		
Symbol	r ai ailletei	TO-220	TO-247	TO-220FP	o iii
R _{thj-case}	Thermal resistance junction-case max	1.14		4.17	°C/W
R _{thj-amb}	Thermal resistance junction-ambient max	62.5	50	62.5	°C/W

Table 4. Avalanche characteristics

Symbol	Parameter	Value	Unit
I _{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	6	А
E _{AS}	Single pulse avalanche energy (starting $T_j = 25$ °C, $I_D = I_{AR}$, $V_{DD} = 50$ V)	208	mJ

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 5. On /off states

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	I _D = 1 mA, V _{GS} = 0	500			V
I _{DSS}	Zero gate voltage drain current (V _{GS} = 0)	V _{DS} = 500 V V _{DS} = 500 V, T _C =125 °C			1 100	μA μA
I _{GSS}	Gate-body leakage current (V _{DS} = 0)	V _{GS} = ± 25 V			±100	nA
V _{GS(th)}	Gate threshold voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	2	3	4	V
R _{DS(on)}	Static drain-source on- resistance	$V_{GS} = 10 \text{ V}, I_D = 7 \text{ A}$		0.2	0.25	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
C _{iss}	Input capacitance		-	1000	-	pF
C _{oss}	Output capacitance	$V_{DS} = 50 \text{ V, f} = 1 \text{ MHz,}$	-	72	-	pF
C _{rss}	Reverse transfer capacitance	$V_{GS} = 0$	-	3	-	pF
C _{oss eq} ⁽¹⁾	Equivalent output capacitance	$V_{DS} = 0$ to 400 V, $V_{GS} = 0$	-	202	-	pF
R_{G}	Intrinsic gate resistance	f = 1 MHz, I _D =0	-	4.4	-	Ω
Qg	Total gate charge	V _{DD} = 400 V, I _D = 14 A,	-	34	-	nC
Q _{gs}	Gate-source charge	V _{GS} = 10 V	-	5	-	nC
Q _{gd}	Gate-drain charge	(see Figure 17)	-	18	-	nC

^{1.} $C_{\rm oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as $C_{\rm oss}$ when $V_{\rm DS}$ increases from 0 to 80% $V_{\rm DS}$

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Тур.	Max	Unit
t _{d(on)}	Turn-on delay time		-	12	-	ns
t _r	Rise time	$V_{DD} = 250 \text{ V}, I_D = 7 \text{ A},$ $R_G = 4.7 \Omega, V_{GS} = 10 \text{ V}$	-	16	-	ns
t _{d(off)}	Turn-off-delay time	(see <i>Figure 18</i>)	-	61	-	ns
t _f	Fall time	,	-	17	ı	ns





Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
I _{SD}	Source-drain current		-		14	Α
I _{SDM} ⁽¹⁾	Source-drain current (pulsed)		-		56	Α
V _{SD} (2)	Forward on voltage	I _{SD} = 14 A, V _{GS} = 0	-		1.5	V
t _{rr}	Reverse recovery time	1. 1.1. 1.1. 1.00. 1.1	-	296		ns
Q _{rr}	Reverse recovery charge	$I_{SD} = 14 \text{ A}, \text{ di/dt} = 100 \text{ A/}\mu\text{s}$ $V_{DD} = 60 \text{ V (see } Figure 21)$	-	3.5		μC
I _{RRM}	Reverse recovery current	100 = 33 1 (333 1 igal 2 1)	-	23		Α
t _{rr}	Reverse recovery time	I _{SD} = 14 A, di/dt = 100 A/μs	-	346		ns
Q _{rr}	Reverse recovery charge	$V_{DD} = 60 \text{ V}, T_j = 150 ^{\circ}\text{C}$	-	4		μC
I _{RRM}	Reverse recovery current	(see Figure 21)	-	24		Α

^{1.} Pulse width limited by safe operating area



^{2.} Pulsed: pulse duration = $300 \mu s$, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-220FP Figure 3. T

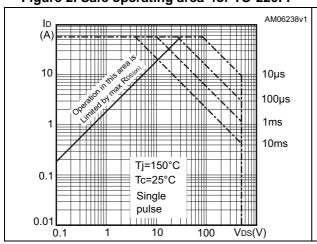


Figure 3. Thermal impedance for TO-220FP

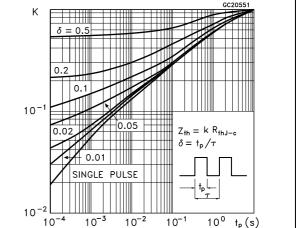
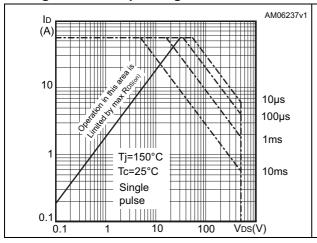


Figure 4. Safe operating area for TO-220

Figure 5. Thermal impedance for TO-220



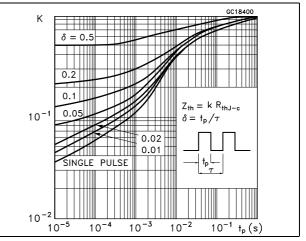
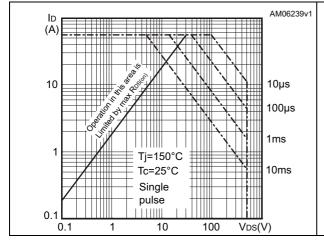
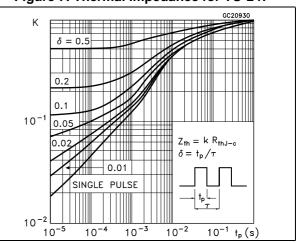


Figure 6. Safe operating area for TO-247

Figure 7. Thermal impedance for TO-247





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Figure 8. Output characteristics

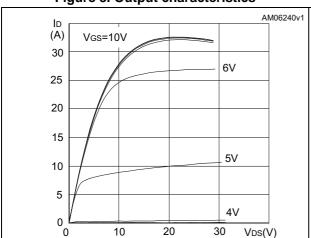


Figure 9. Transfer characteristics

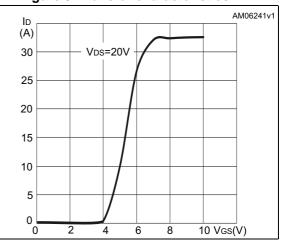
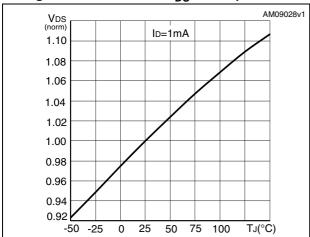


Figure 10. Normalized V_{DS} vs temperature

Figure 11. Static drain-source on resistance



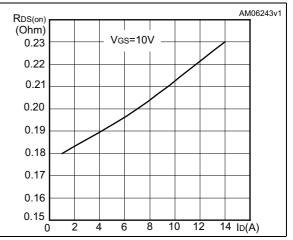
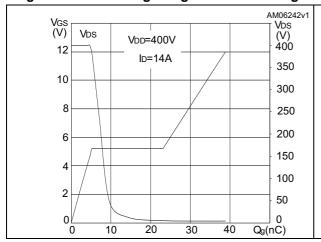


Figure 12. Gate charge vs gate-source voltage

Figure 13. Capacitance variations



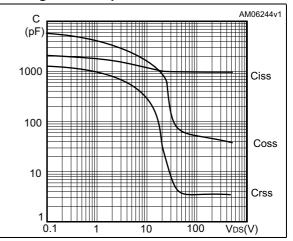
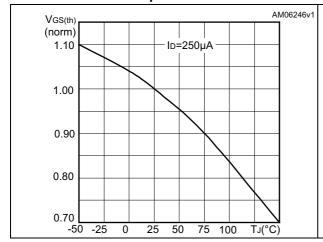
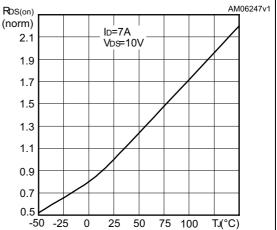


Figure 14. Normalized gate threshold voltage vs temperature

Figure 15. Normalized on-resistance vs temperature RDS(on) (norm) ID=7A VDS=10V 2.1





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3 Test circuits

Figure 16. Switching times test circuit for resistive load

Figure 17. Gate charge test circuit

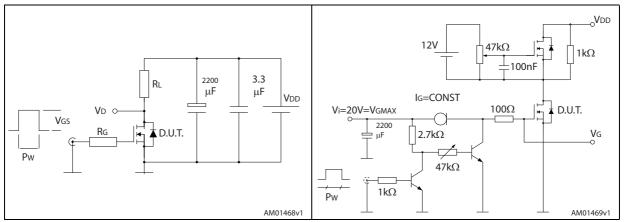


Figure 18. Test circuit for inductive load switching and diode recovery times

Figure 19. Unclamped inductive load test circuit

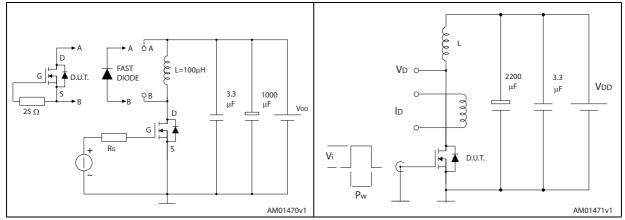
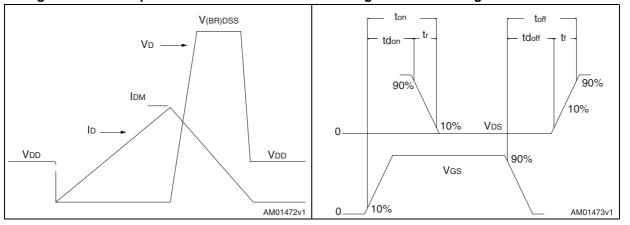


Figure 20. Unclamped inductive waveform

Figure 21. Switching time waveform





4 Package mechanical data

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Table 9. TO-220FP mechanical data

Dim	mm				
Dim.	Min.	Тур.	Max.		
А	4.4		4.6		
В	2.5		2.7		
D	2.5		2.75		
E	0.45		0.7		
F	0.75		1		
F1	1.15		1.70		
F2	1.15		1.70		
G	4.95		5.2		
G1	2.4		2.7		
Н	10		10.4		
L2		16			
L3	28.6		30.6		
L4	9.8		10.6		
L5	2.9		3.6		
L6	15.9		16.4		
L7	9		9.3		
Dia	3		3.2		



-*B*-Dia L6 *L2 L7* L3 F1 **L4** F2 Ε -G1_ 7012510_Rev_K_B

Figure 22. TO-220FP drawing

Table 10. TO-220 type A mechanical data

Dim	10010 101 10 ==	mm	
Dim.	Min.	Тур.	Max.
А	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
С	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
е	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
ØP	3.75		3.85
Q	2.65		2.95



øΡ Ε H1 D <u>D1</u> L20 L30 b1(X3) b (X3) 0015988_typeA_Rev_T

Figure 23. TO-220 type A drawing

Table 11. TO-247 mechanical data

Tubio 11. 10 247 incondinadi data				
Dim.	mm.			
	Min.	Тур.	Max.	
А	4.85		5.15	
A1	2.20		2.60	
b	1.0		1.40	
b1	2.0		2.40	
b2	3.0		3.40	
С	0.40		0.80	
D	19.85		20.15	
Е	15.45		15.75	
е	5.30	5.45	5.60	
L	14.20		14.80	
L1	3.70		4.30	
L2		18.50		
ØP	3.55		3.65	
ØR	4.50		5.50	
S	5.30	5.50	5.70	



HEAT-SINK PLANE

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Figure 24. TO-247 drawing

5 Revision history

Table 12. Document revision history

Date	Revision	Changes	
09-Feb-2010	1	First release	
03-Sep-2013	2	 Updated: Section 2.1: Electrical characteristics (curves) Updated: Section 4: Package mechanical data Minor text changes. 	



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