



ATP113

P-Channel Power MOSFET -60V, -35A, 29.5mΩ, Single ATPAK

ON Semiconductor®

<http://onsemi.com>

Features

- ON-resistance $R_{DS(on)1}=22.5m\Omega$ (typ.)
- 4V drive
- Protection diode in
- Input Capacitance $C_{iss}=2400pF$ (typ.)
- Halogen free compliance

Specifications

Absolute Maximum Ratings at $T_a=25^\circ C$

| Parameter | Symbol | Conditions | Ratings | Unit |
|-------------------------------------|-----------|---|-------------|------------|
| Drain-to-Source Voltage | V_{DSS} | | -60 | V |
| Gate-to-Source Voltage | V_{GSS} | | ± 20 | V |
| Drain Current (DC) | I_D | | -35 | A |
| Drain Current ($PW \leq 10\mu s$) | I_{DP} | $PW \leq 10\mu s$, duty cycle $\leq 1\%$ | -105 | A |
| Allowable Power Dissipation | P_D | $T_c=25^\circ C$ | 50 | W |
| Channel Temperature | T_{ch} | | 150 | $^\circ C$ |
| Storage Temperature | T_{stg} | | -55 to +150 | $^\circ C$ |
| Avalanche Energy (Single Pulse) *1 | E_{AS} | | 95 | mJ |
| Avalanche Current *2 | I_{AV} | | -18 | A |

Note : *1 $V_{DD}=-10V$, $L=500\mu H$, $I_{AV}=-18A$

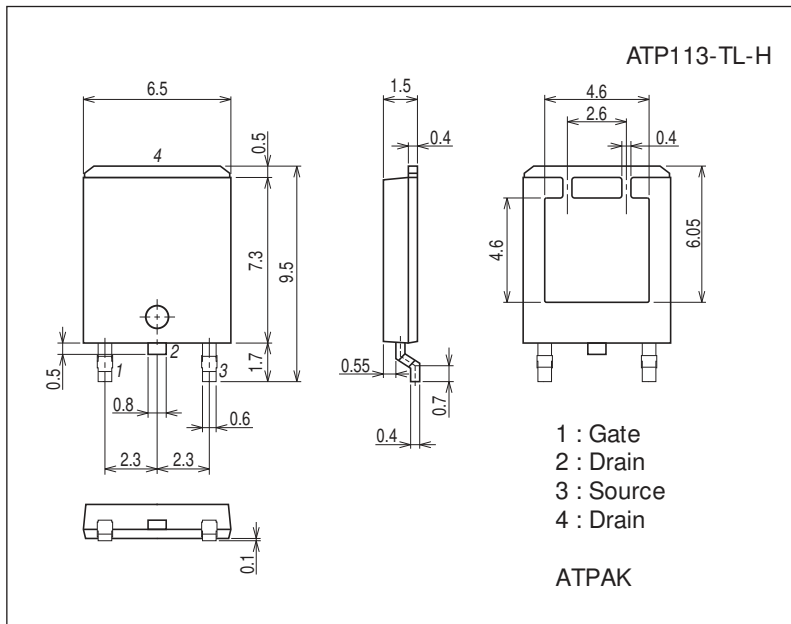
*2 $L \leq 500\mu H$, Single pulse

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Package Dimensions

unit : mm (typ)

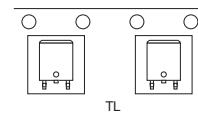
7057-001



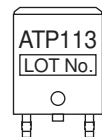
Product & Package Information

- Package : ATPAK
- JEITA, JEDEC : -
- Minimum Packing Quantity : 3,000 pcs./reel

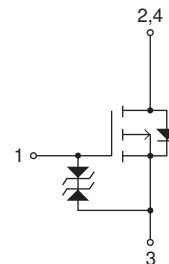
Packing Type: TL



Marking



Electrical Connection

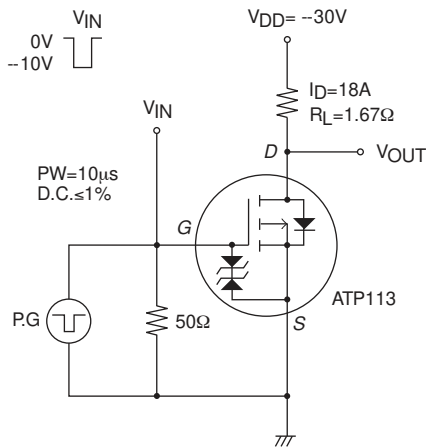


ATP113

Electrical Characteristics at Ta=25°C

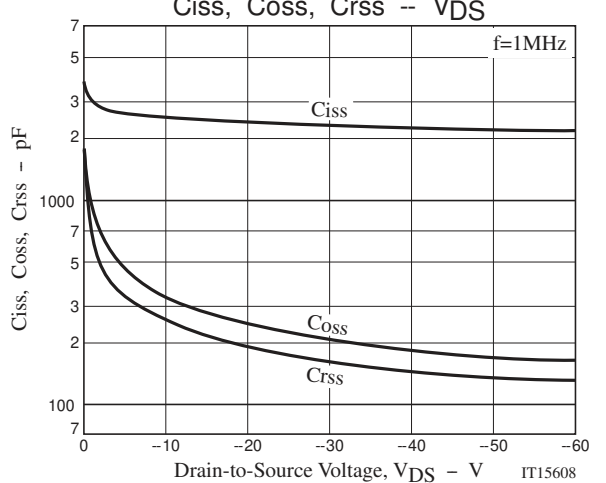
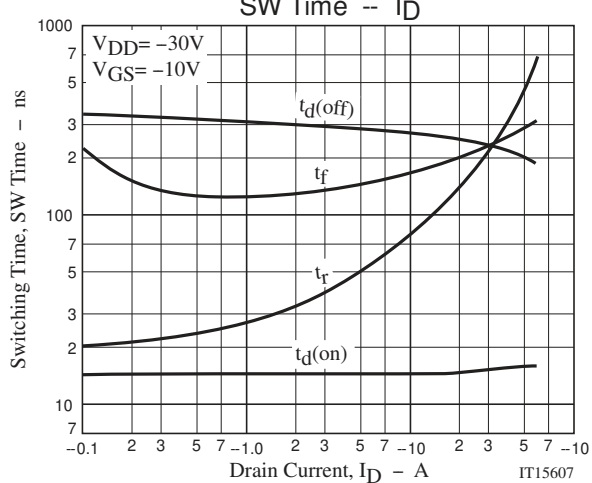
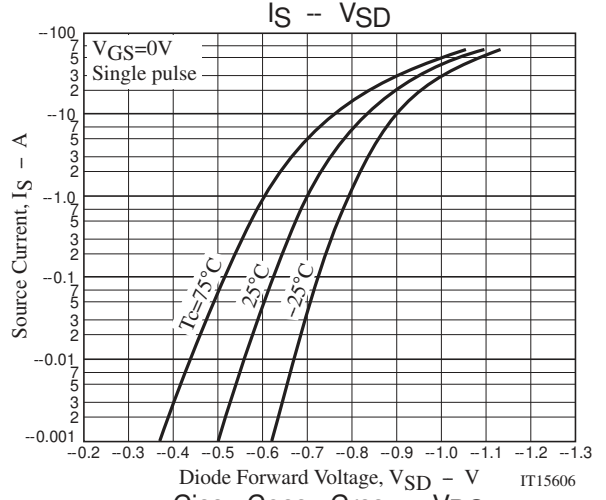
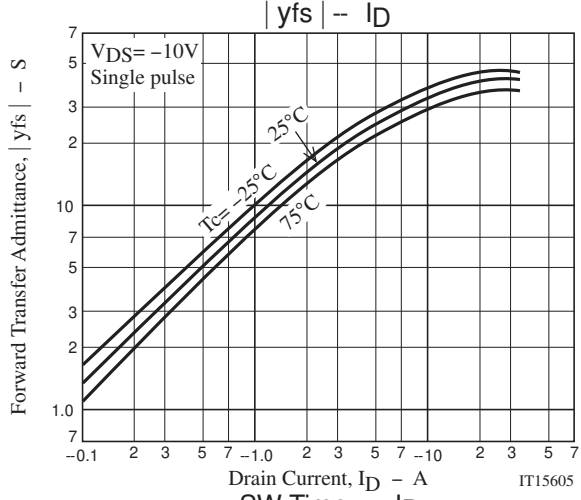
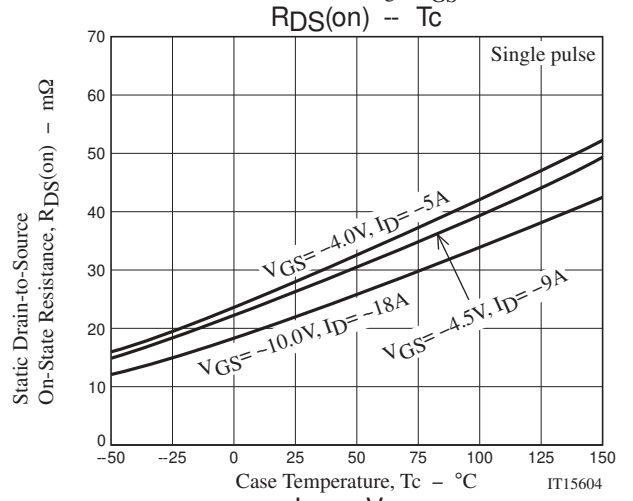
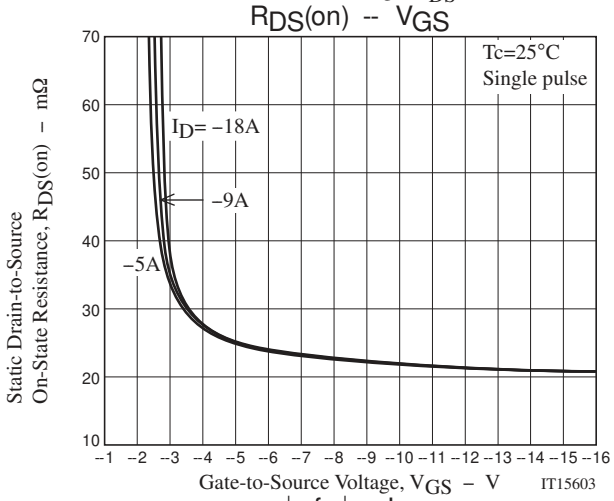
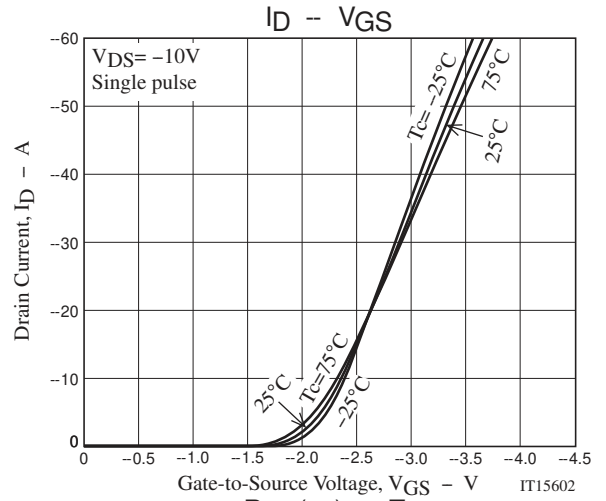
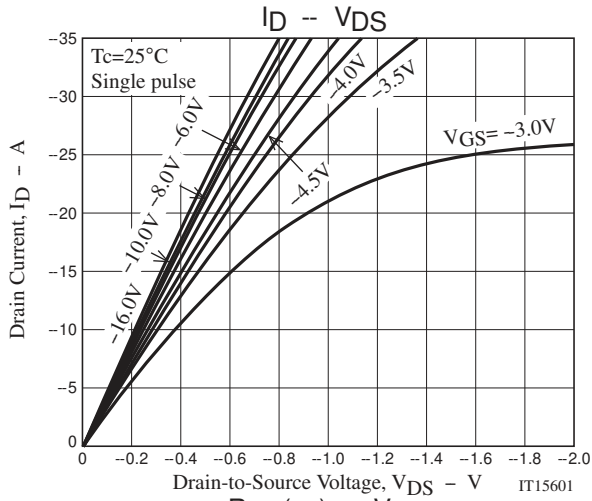
| Parameter | Symbol | Conditions | Ratings | | | Unit |
|--|----------|-----------------------------|---------|-------|------|------|
| | | | min | typ | max | |
| Drain-to-Source Breakdown Voltage | V(BR)DSS | ID=-1mA, VGS=0V | -60 | | | V |
| Zero-Gate Voltage Drain Current | IDSS | VDS=-60V, VGS=0V | | | -1 | μA |
| Gate-to-Source Leakage Current | IGSS | VGS=±16V, VDS=0V | | | ±10 | μA |
| Cutoff Voltage | VGS(off) | VDS=-10V, ID=-1mA | -1.2 | | -2.6 | V |
| Forward Transfer Admittance | yfs | VDS=-10V, ID=-18A | | 37 | | S |
| Static Drain-to-Source On-State Resistance | RDS(on)1 | ID=-18A, VGS=-10V | | 22.5 | 29.5 | mΩ |
| | RDS(on)2 | ID=-9A, VGS=-4.5V | | 27 | 38 | mΩ |
| | RDS(on)3 | ID=-5A, VGS=-4V | | 29 | 44 | mΩ |
| Input Capacitance | Ciss | VDS=-20V, f=1MHz | | 2400 | | pF |
| Output Capacitance | Coss | | | 250 | | pF |
| Reverse Transfer Capacitance | Crss | | | 195 | | pF |
| Turn-ON Delay Time | td(on) | | | 15 | | ns |
| Rise Time | tr | See specified Test Circuit. | | 125 | | ns |
| Turn-OFF Delay Time | td(off) | | | 250 | | ns |
| Fall Time | tf | | | 200 | | ns |
| Total Gate Charge | Qg | VDS=-30V, VGS=-10V, ID=-35A | | 55 | | nC |
| Gate-to-Source Charge | Qgs | | | 7.5 | | nC |
| Gate-to-Drain "Miller" Charge | Qgd | | | 12 | | nC |
| Diode Forward Voltage | VSD | IS=-35A, VGS=0V | | -0.98 | -1.5 | V |

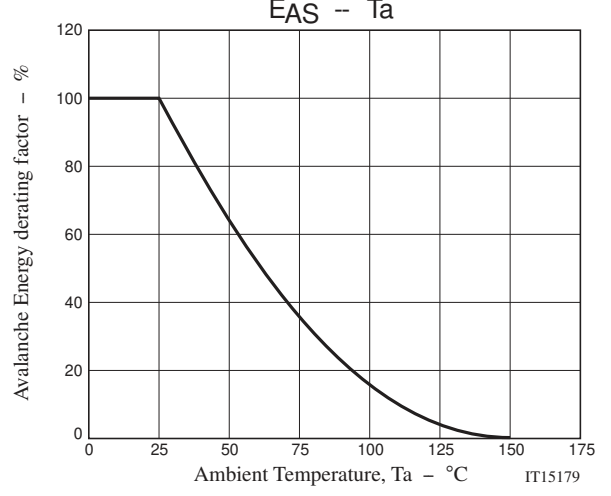
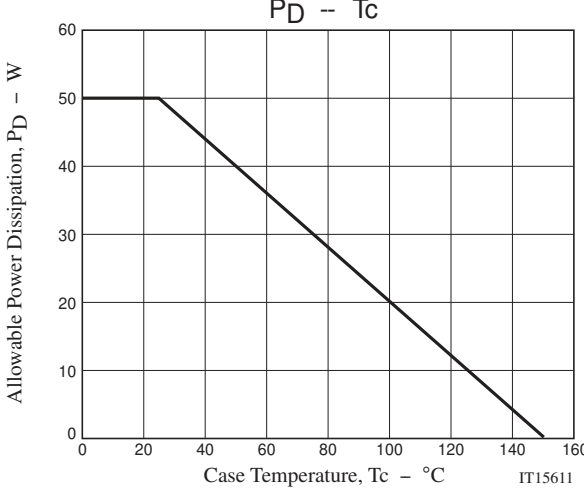
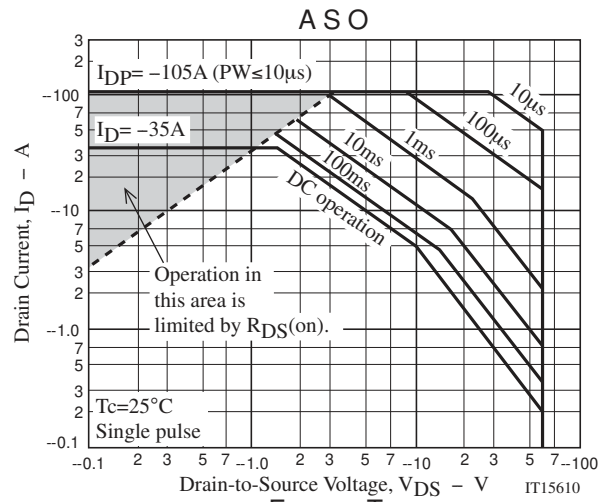
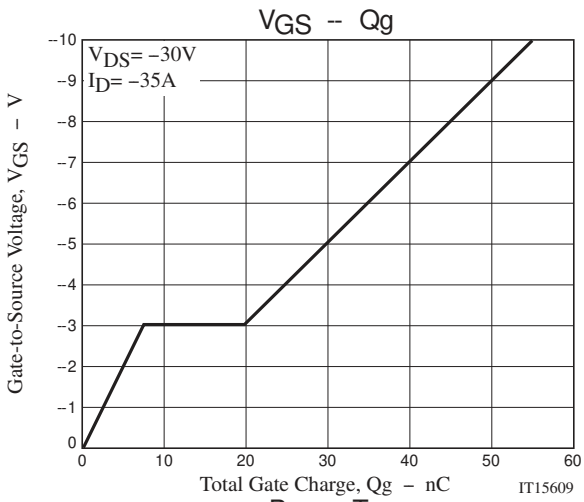
Switching Time Test Circuit



Ordering Information

| Device | Package | Shipping | memo |
|-------------|---------|----------------|--------------------------|
| ATP113-TL-H | ATPAK | 3,000pcs./reel | Pb Free and Halogen Free |





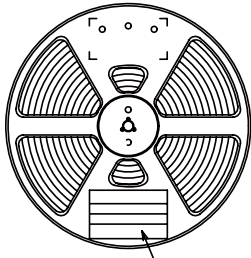
Taping Specification

ATP113-TL-H

1. Packing Format (TL)

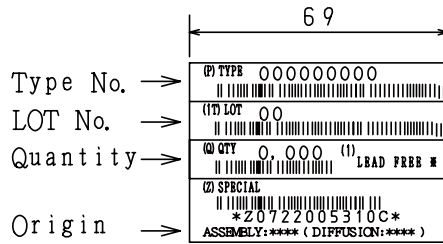
| Package Name | Carrier Tape Type | Maximum Number of devices contained (pcs) | | | Packing format | |
|--------------|-------------------|---|-----------|-----------|---|--|
| | | Reel | Inner box | Outer box | INNER BOX SD-C-18 | OUTER BOX SD-A-18 |
| ATPAK | ATP | 3,000 | 3,000 | 15,000 | 1 reels contained Dimensions:mm (external) 340×340×28 | 5 inner boxes contained Dimensions:mm (external) 355×355×165 |

Packing method



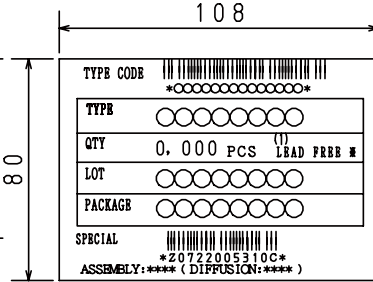
Reel label

Reel label, Inner box label
(unit:mm)



Outer box label

It is a label at the time of factory shipments. The form of a label may change in physical distribution process.



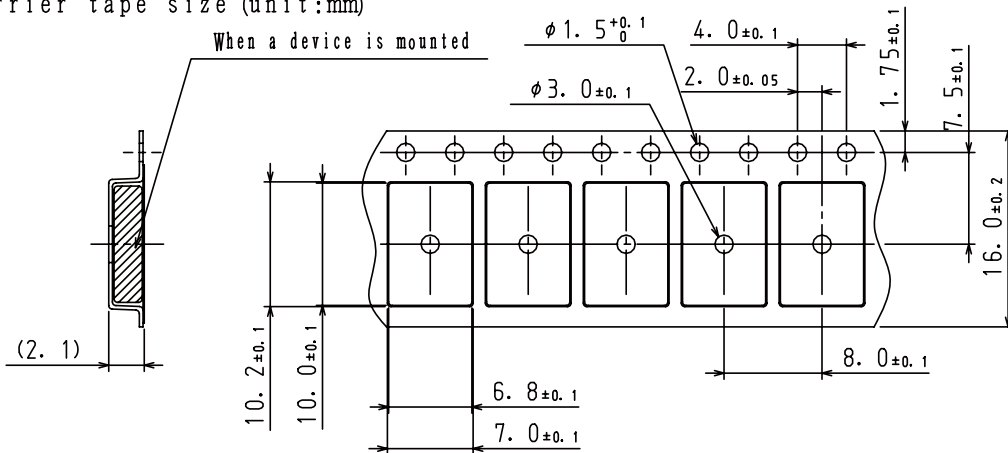
NOTE (1)

The LEAD FREE * description shows that the surface treatment of the terminal is lead free.

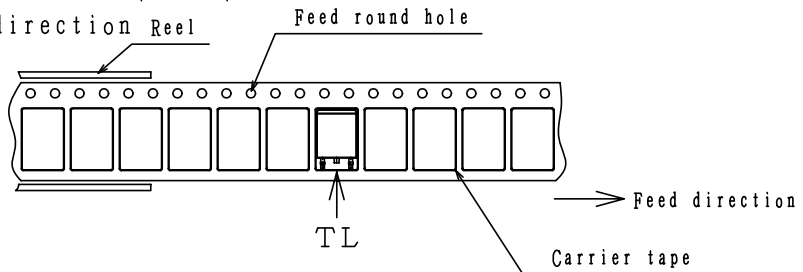
| Label | JEITA Phase |
|-------------|----------------|
| LEAD FREE 3 | JEITA Phase 3A |
| LEAD FREE 4 | JEITA Phase 3 |

2. Taping configuration

2-1. Carrier tape size (unit:mm)



2-2. Device placement direction Reel

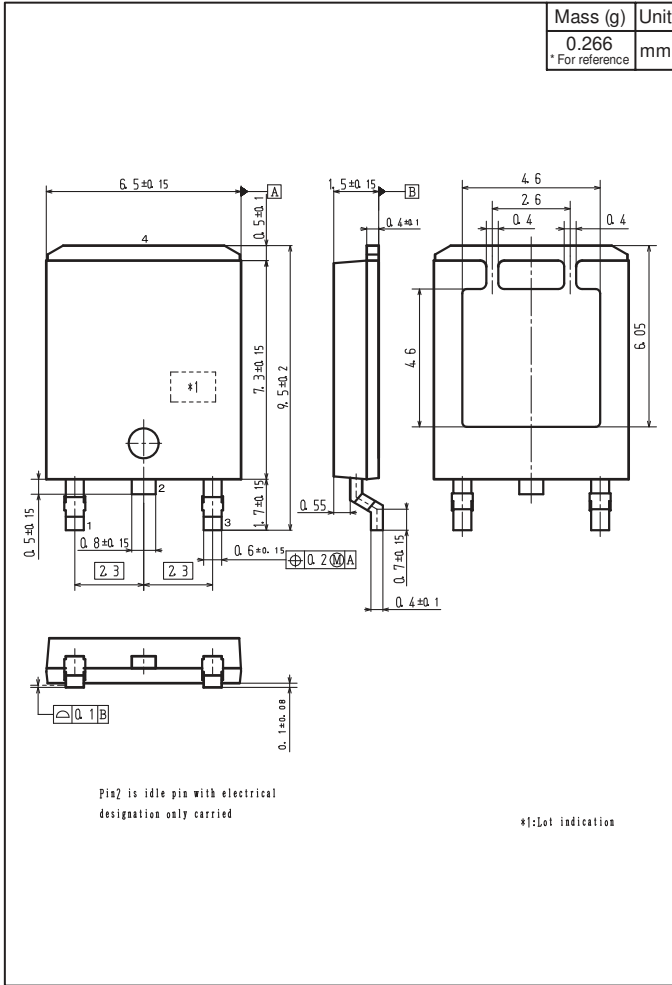


The one electrode terminals on feed hole side...TL

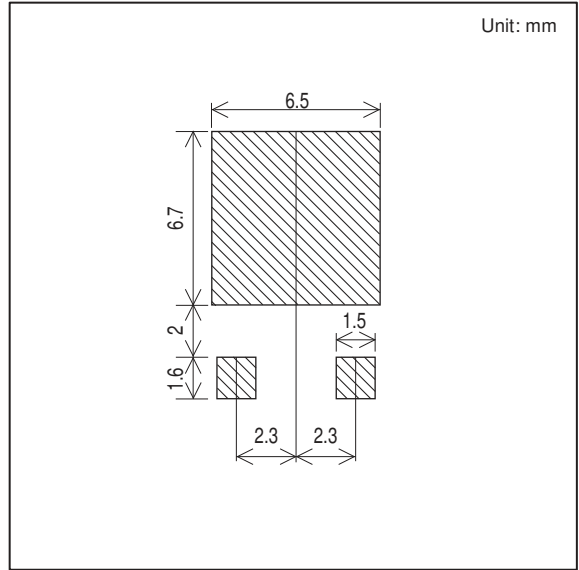
ATP113

Outline Drawing

ATP113-TL-H



Land Pattern Example



Note on usage : Since the ATP113 is a MOSFET product, please avoid using this device in the vicinity of highly charged objects.

ON Semiconductor and the ON logo are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.