

## Dual Channel USB3.0 Redriver/Equalizer

Check for Samples: [SN65LVPE502](#)

### FEATURES

- Single Lane USB 3.0 Equalizer/Redriver
- Selectable Equalization, De-emphasis and Output Swing Control
- Integrated Termination
- Hot-Plug Capable
- Receiver Detect
- Low Power:
  - 315mW(TYP),  $V_{CC} = 3.3V$
- Auto Low Power Modes:
  - 5mW (TYP) When no Connection Detected
  - 70mW (TYP) When in U2/U3 Mode
- Excellent Jitter and Loss Compensation Capability: to 24"
  - 24" of 6 mil Stripline on FR4
  - 12" on Input and 4m, 26AWG USB 3.0 Cable on Output
- Small foot print – 24 Pin (4mm × 4mm) QFN Package
- High Protection Against ESD Transient
  - HBM: 5,000 V
  - CDM: 1,500 V
  - MM: 200 V

### APPLICATIONS

- Notebooks, Desktops, Docking Stations, Backplane and Cabled Application

### DESCRIPTION

The SN65LVPE502 is a dual channel, single lane USB 3.0 redriver and signal conditioner supporting data rates of 5.0Gbps. The device complies with USB 3.0 spec revision 1.0, supporting electrical idle condition and low frequency periodic signals (LFPS) for USB 3.0 power management modes.

#### Programmable EQ, De-Emphasis and Amplitude Swing

The SN65LVPE502 is designed to minimize signal degradation effects such as crosstalk and inter-symbol interference (ISI) that limits the interconnect distance between two devices. The input stage of each channel offers selectable equalization settings that can be programmed to match loss in the channel. The differential outputs provide selectable de-emphasis to compensate for the anticipated distortion USB 3.0 signal will experience. Level of de-emphasis will depend on the length of interconnect and its characteristics. The SN65LVPE502 provides a unique way to tailor output de-emphasis on a per channel basis with use of DE and OS pins. All Rx and Tx equalization settings supported by the device are programmed by six 3-state pins as shown in [Table 2](#).

#### Low Power Modes

The device supports three low power modes as described below.

##### 1. Sleep Mode

Initiated anytime EN\_RXD undergoes a high to low transition or when device powers up with EN\_RXD set low. In sleep mode both input and output terminations are held at HiZ and device ceases operation to conserve power. Sleep mode max power consumption is 1mW, entry time is 2 $\mu$ s, device exits sleep mode to Rx.Detect mode after EN\_RXD is driven to  $V_{CC}$ , exit time is 100 $\mu$ s max.

##### 2. RX Detect Mode – When no remote device is connected

Anytime SN65LVPE502 detects a break in link (i.e., when upstream device is disconnected) or after powerup fails to find a remote device, SN65LVPE502 goes to Rx Detect mode and conserves power by shutting down majority of the internal circuitry. In this mode, input termination for both channels are driven to Hi-Z. In Rx Detect mode device power is <10mW(TYP) or less than 5% of its normal operating power This feature is useful in saving system power in mobile applications like notebook PC where battery life is critical.

Anytime an upstream device gets reconnected the redriver automatically senses the connection and goes to normal operating mode. This operation requires no setting to the device.



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### 3. U2/U3 Mode

With the help of internal timers the device tracks when link enters USB 3.0 low power modes U2 and U3, in these modes link is in electrical idle state. SN65LVPE502 will selectively turn-off internal circuitry to save on power. Typical power saving is about 75% lower than normal operating mode. The device will automatically revert to active mode when signaling activity (LFPS) is detected.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## DESCRIPTION CONTINUED

### Receiver Detection

RX.Detect cycle is performed by first setting Rx termination for each channel to Hi-Z, device then starts sensing for receiver termination that may be attached at the other end of each TX.

If receiver is detected on both channel:

- The TX and RX terminations are switched to  $Z_{DIFF-TX}$ ,  $Z_{DIFF-RX}$ , respectively

If no receiver is detected on one or both channels:

- The transmitter is pulled to Hi-Z
- The channel is put in low power mode
- Device attempts to detect Rx termination in 12 ms (TYP) interval until termination is found or the device is put in sleep mode.

### USB Compliance Mode

The device enters USB compliance mode when both EN\_RXD and CM pins are set H. This mode is used to test the transmitter for compliance to voltage and timing specifications per USB 3.0 compliance specs. In this mode each channel will maintain its low-impedance termination  $R_{DC-RX}$ , while auto Rx detect operation in the device is disabled.

### Electrical Idle Support

The electrical idle support is needed for low frequency periodic signaling (LFPS) used in USB 3.0 side band communication. A link is in an electrical idle state when the TX± voltage is held at a steady constant value like the common mode voltage. SN65LVPE502 detects an electrical idle state when RX± voltage at the device pin falls below  $V_{RX\_IDLE\_DIFFpp}$  min. After detection of an idle state in a given channel the device asserts electrical idle state in its corresponding TX. When RX± voltage exceeds  $V_{RX\_IDLE\_DIFFpp}$  max normal operation is restored and output start passing input signal. The electrical idle exit and entry time is specified at  $\leq 6$  ns.

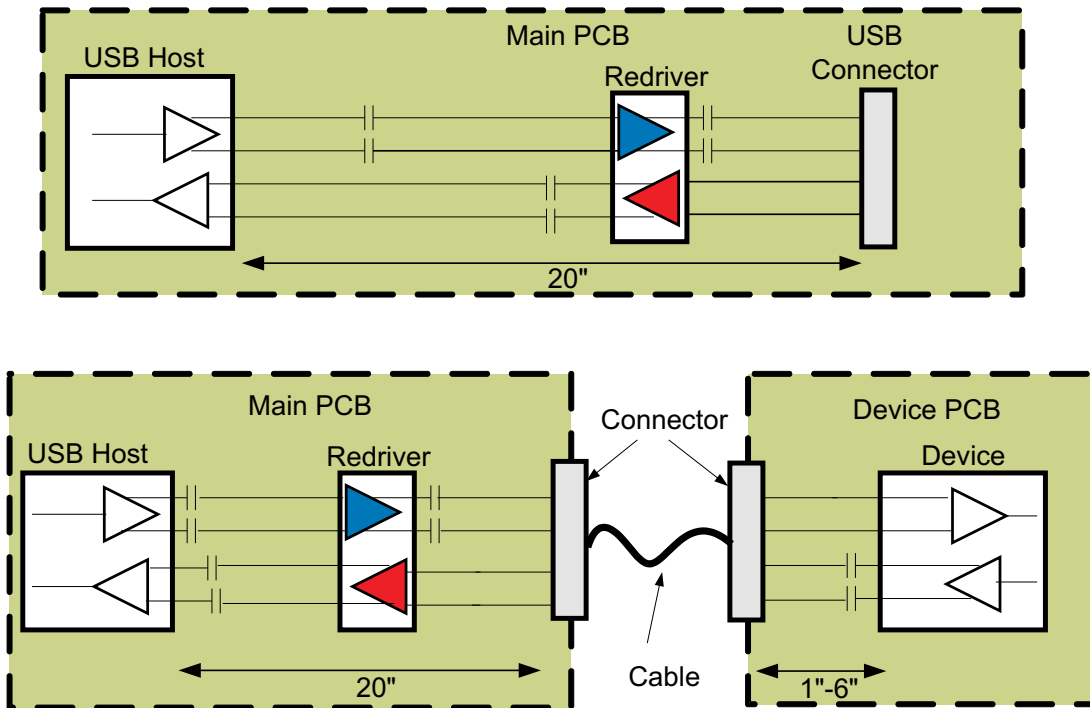


Figure 1. Typical Application

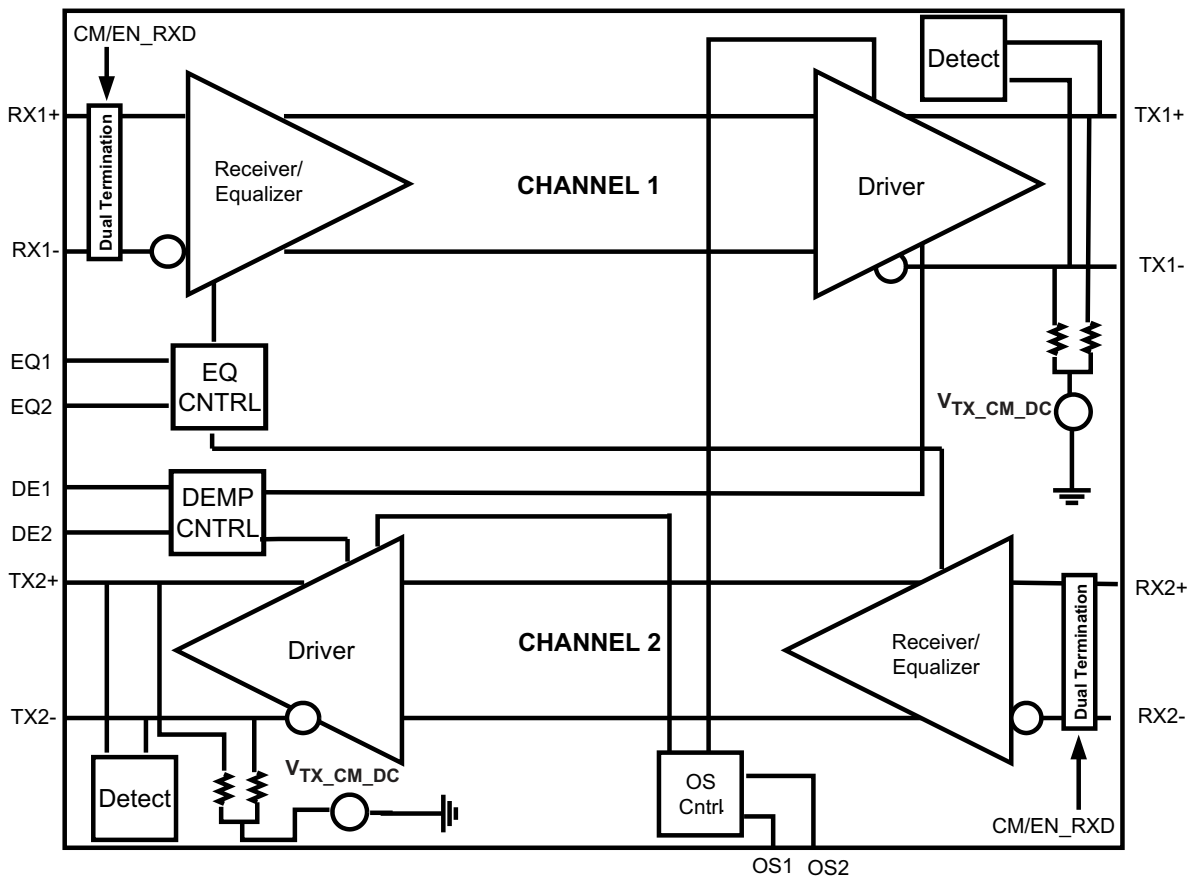


Figure 2. Data Flow Block Diagram

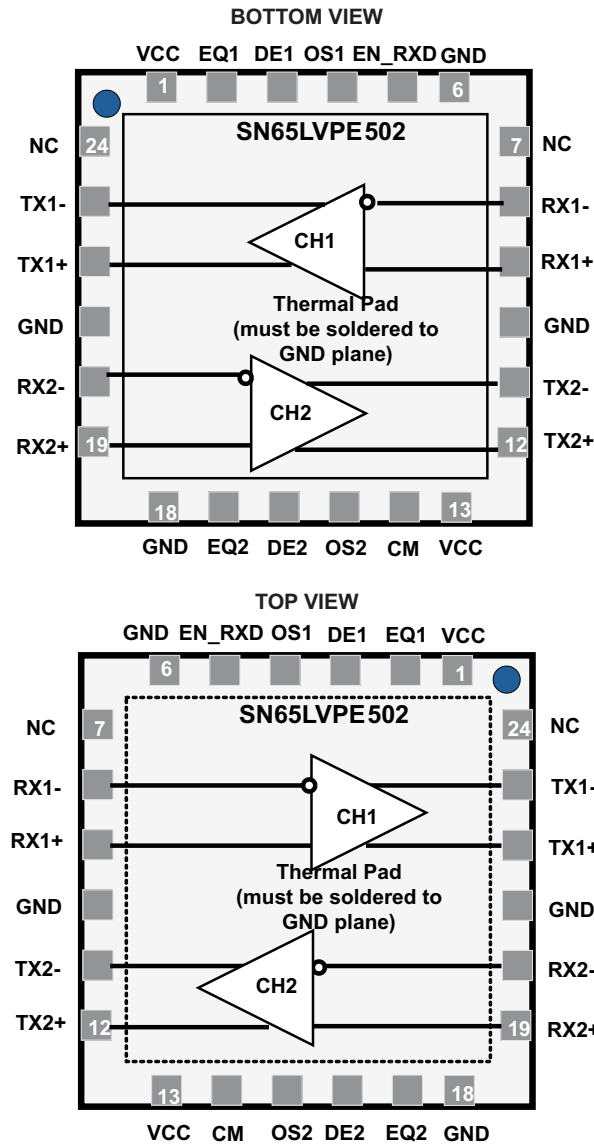


Figure 3. Flow-Through Pin-Out

Table 1. Pin Description

| PIN                                     |      |          | DESCRIPTION  |
|---|------|----------|--|
| NUMBER                                  | NAME | I/O TYPE |  |
| <b>HIGH SPEED DIFFERENTIAL I/O PINS</b> |      |          |  |
| 8                                       | RX1- | I, CML   | Non-inverting and inverting CML differential input for CH 1 and CH 2. These pins are tied to an internal voltage bias by dual termination resistor circuit |
| 9                                       | RX1+ | I, CML   |  |
| 20                                      | RX2- | I, CML   |  |
| 19                                      | RX2+ | I, CML   |  |
| 23                                      | TX1- | O, VML   | Non-inverting and inverting VML differential output for CH 1 and CH 2. These pins are internally tied to voltage bias by termination resistors             |
| 22                                      | TX1+ | O, VML   |  |
| 11                                      | TX2- | O, VML   |  |
| 12                                      | TX2+ | O, VML   |  |

**Table 1. Pin Description (continued)**

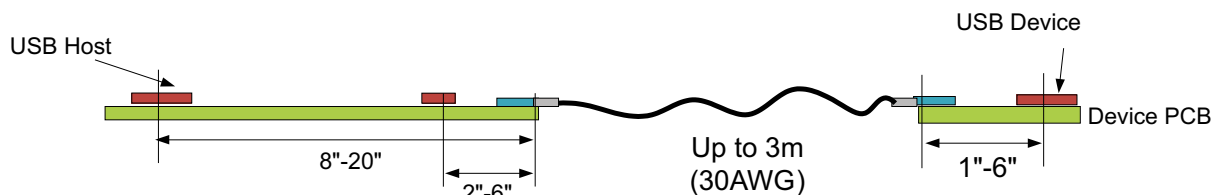
| PIN                                  |          |           |  |
|--------------------------------------|----------|-----------|--|
| <b>DEVICE CONTROL PIN</b>            |          |           |  |
| 5                                    | EN_RXD   | I, LVCMOS | Sets device operation modes per Table 2. Internally pulled to VCC                          |
| 14                                   | CM       | I, LVCMOS | Sets device in compliance mode when pulled to VCC, internally pulled to GND                |
| 7,24                                 | NC       |           | Pads not internally connected  |
| <b>EQ CONTROL PINS<sup>(1)</sup></b> |          |           |  |
| 3,16                                 | DE1, DE2 | I, LVCMOS | Selects de-emphasis settings for CH 1 and CH 2 per Table 2. Internally tied to $V_{CC}/2$  |
| 2,17                                 | EQ1, EQ2 | I, LVCMOS | Selects equalization settings for CH 1 and CH 2 per Table 2. Internally tied to $V_{CC}/2$ |
| 4, 15                                | OS1, OS2 | I, LVCMOS | Selects output amplitude for CH 1 and CH 2 per Table 2. Internally tied to $V_{CC}/2$      |
| <b>POWER PINS</b>                    |          |           |  |
| 1,13                                 | VCC      | Power     | Positive supply should be $3.3V \pm 10\%$  |
| 6,10,18,21                           | GND      | Power     | Supply ground  |

(1) Internally biased to  $V_{CC}/2$  with  $>200k\Omega$  pull-up/pull-down. When pins are left as NC board leakage at this pin pad must be  $< 1 \mu A$  otherwise drive to  $V_{CC}/2$  to assert mid-level state.

**Table 2. Signal Control Pin Setting**

| OS <sub>x</sub> <sup>(1)</sup> |                                     | TRANSITION BIT AMPLITUDE<br>(TYP mVpp) |                                    |
|--------------------------------|-------------------------------------|--|------------------------------------|
| NC (default)                   |                                     | 1000                                   |                                    |
| 0                              |                                     | 870                                    |                                    |
| 1                              |                                     | 1085                                   |                                    |
| EQ <sub>x</sub> <sup>(1)</sup> |                                     | EQUALIZATION dB                        |                                    |
| NC (default)                   |                                     | 0                                      |                                    |
| 0                              |                                     | 7                                      |                                    |
| 1                              |                                     | 15                                     |                                    |
| DE <sub>x</sub> <sup>(1)</sup> | OS <sub>x</sub> <sup>(1)</sup> = NC | OS <sub>x</sub> <sup>(1)</sup> = 0     | OS <sub>x</sub> <sup>(1)</sup> = 1 |
| NC                             | -3.5 dB                             | -2.2 dB                                | -4.4 dB                            |
| 0                              | -6.0 dB                             | -5.2 dB                                | -6.0 dB                            |
| 1                              | -8.5 dB                             | -8.9 dB                                | -7.6 dB                            |
| EN_RXD                         |                                     | DEVICE FUNCTION                        |                                    |
| 1 (default)                    |                                     | Normal operating mode                  |                                    |
| 0                              |                                     | Sleep mode                             |                                    |
| CM                             |                                     | DEVICE FUNCTION                        |                                    |
| 0 (default)                    |                                     | Normal Mode                            |                                    |
| 1                              |                                     | Compliance mode                        |                                    |

(1) Applies to Channel 1 and Channel 2 at 2.5 GHz.



**Figure 4. Redriver Placement Example**

**ORDERING INFORMATION<sup>(1)</sup>**

| PART NUMBER     | PART MARKING | PCAKAGE                 |
|-----------------|--------------|-------------------------|
| SN65LVPE502RGER | LVPE502      | 24-pin RGE Reel (large) |
| SN65LVPE502RGET | LVPE502      | 24-pin RGE Reel (small) |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).

**ABSOLUTE MAXIMUM RATINGS**

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                                     |                                     | UNITS / VALUES                   |
|-------------------------------------|-------------------------------------|----------------------------------|
| Supply Voltage Range <sup>(2)</sup> | V <sub>CC</sub>                     | –0.5 V to 4 V                    |
| Voltage Range                       | Differential I/O                    | –0.5 V to 4 V                    |
|                                     | Control I/O                         | –0.5 V to V <sub>CC</sub> + 0.5V |
| Electrostatic discharge             | Human Body Model <sup>(3)</sup>     | ±5000V                           |
|                                     | Charged Device Model <sup>(4)</sup> | ±1500V                           |
|                                     | Machine Model <sup>(5)</sup>        | ±200V                            |
| Continuous power dissipation        |                                     | See Dissipation Rating Table     |

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values, except differential voltages, are with respect to network ground terminal.

(3) Tested in accordance with JEDEC Standard 22, Test Method A114-B.

(4) Tested in accordance with JEDEC Standard 22, Test Method C101-A.

(5) Tested in accordance with JEDEC Standard 22, Test Method A115-A.

**PACKAGE CHARACTERIZATION**

over operating free-air temperature range (unless otherwise noted)

| PARAMETER       |   | TEST CONDITIONS  | MIN | TYP | MAX | UNIT |
|-----------------|---|--|-----|-----|-----|------|
| P <sub>D</sub>  | Device power dissipation                      | CM, EN_RXD, EQ cntrl pins = NC, K28.5 pattern at 5 Gbps, V <sub>ID</sub> = 1000 mVpp |     | 330 | 450 | mW   |
| P <sub>SD</sub> | Device power dissipation under low power mode | EN_RXD= GND  |     | 0.3 | 1   | mW   |

**THERMAL INFORMATION**

| THERMAL METRIC <sup>(1)</sup> |  | SN65LVPE502 | UNITS |
|-------------------------------|--|-------------|-------|
|                               |  | RGE         |       |
|                               |  | 24 PINS     |       |
| θ <sub>JA</sub>               | Junction-to-ambient thermal resistance       | 46          | °C/W  |
| θ <sub>JC(TOP)</sub>          | Junction-to-case(top) thermal resistance     | 42          |       |
| θ <sub>JB</sub>               | Junction-to-board thermal resistance         | 13          |       |
| ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 0.5         |       |
| ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 9           |       |
| θ <sub>JC(BOTTOM)</sub>       | Junction-to-case(bottom) thermal resistance  | 4           |       |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](http://SPRA953).

## RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

|                       |                                | MIN | TYP | MAX | UNIT |
|-----------------------|--------------------------------|-----|-----|-----|------|
| V <sub>CC</sub>       | Supply Voltage                 | 3   | 3.3 | 3.6 | V    |
| C <sub>COUPLING</sub> | AC Coupling Capacitor          | 75  |     | 200 | nF   |
|                       | Operating free-air temperature | 0   |     | 85  | °C   |

## DEVICE POWER

The SN65LVPE502 is designed to operate from a single 3.3 V supply.

## ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

| PARAMETER   |   | TEST CONDITIONS   | MIN  | TYP | MAX             | UNIT |
|---|---|---|------|-----|-----------------|------|
| <b>DEVICE PARAMETERS</b>                                      |   |   |      |     |                 |      |
| I <sub>CC</sub>   | Supply Current  | EN_RXD, CM, EQ cntrl = NC,<br>K28.5 pattern at 5 Gbps, V <sub>ID</sub> = 1000 mV <sub>pp</sub>                |      | 100 | 120             | mA   |
| I <sub>CC</sub> <sub>Rx.Detect</sub>                          |   | In Rx.Detect mode   |      | 2   | 5               |      |
| I <sub>CC</sub> <sub>sleep</sub>                              |   | EN_RXD = GND  |      |     | 0.1             |      |
| I <sub>CC</sub> <sub>U2-U3</sub>                              |   | Link in USB low power state   |      | 21  |                 |      |
|   | Maximum Data Rate   |   |      |     | 5               | Gbps |
| t <sub>ENB</sub>  | Device Enable Time  | Sleep mode exit time EN_RXD L→H With<br>Rx termination present  |      |     | 100             | μs   |
| t <sub>DIS</sub>  | Device Disable Time                                       | Sleep mode entry time EN_RXD H→L  |      |     | 2               | μs   |
| T <sub>RX.DETECT</sub>  | Rx.Detect Start Event                                     | Power-up time   |      |     | 100             | μs   |
| <b>CONTROL LOGIC (under recommended operating conditions)</b> |   |   |      |     |                 |      |
| V <sub>IH</sub>   | High level Input Voltage                                  |   | 1.4  |     | V <sub>CC</sub> | V    |
| V <sub>IL</sub>   | Low Level Input Voltage                                   |   | -0.3 |     | 0.5             | V    |
| V <sub>HYS</sub>  | Input Hysteresis  |   |      | 150 |                 | mV   |
| I <sub>IH</sub>   | High Level Input Current                                  | OSx, EQx, DEx = V <sub>CC</sub>   |      |     | 30              | μA   |
|   |   | EN_RXD = V <sub>CC</sub>  |      |     | 1               |      |
|   |   | CM = V <sub>CC</sub>  |      |     | 30              |      |
| I <sub>IL</sub>   | Low Level Input Current                                   | OSx, EQx, DEx = GND   | -30  |     |                 | μA   |
|   |   | EN_RXD = GND  | -30  |     |                 |      |
|   |   | CM = GND  | -1   |     |                 |      |
| <b>RECEIVER AC/DC</b>   |   |   |      |     |                 |      |
| V <sub>in</sub> <sub>diff_pp</sub>                            | RX1, RX2 Input Voltage Swing                              | AC coupled differential RX peak to peak<br>signal   | 100  |     | 1200            | mVpp |
| V <sub>CM_RX</sub>  | RX1, RX2 Common Mode Voltage                              |   |      | 3.3 |                 | V    |
| V <sub>in</sub> <sub>COM_P</sub>                              | RX1, RX2 AC Peak common mode<br>voltage                   | Measured at Rx pins with termination<br>enabled   |      |     | 150             | mVP  |
| Z <sub>DC_RX</sub>  | DC common mode impedance                                  |   | 18   | 26  | 30              | Ω    |
| Z <sub>diff_RX</sub>  | DC differential input impedance                           |   | 72   | 80  | 120             | Ω    |
| Z <sub>RX_High_IMP+</sub>                                     | DC Input High Impedance                                   | Device in sleep mode Rx termination not<br>powered. Measured with respect to GND<br>over 500mV max            | 50   | 85  |                 | kΩ   |
| V <sub>RX-LFPS-DETpp</sub>                                    | Low Voltage Periodic Signaling (LFPS)<br>Detect Threshold | Measured at receiver pin, below minimum<br>output is squelched, above max input signal<br>is passed to output | 100  |     | 300             | mVpp |
| RL <sub>RX-DIFF</sub>   | Differential Return Loss                                  | 50 MHz – 1.25 GHz   | 10   | 11  |                 | dB   |
|   |   | 1.25 GHz – 2.5 GHz  | 6    | 7   |                 |      |
| RL <sub>RX-CM</sub>   | Common Mode Return Loss                                   | 50 MHz – 2.5 GHz  | 11   | 13  |                 | dB   |

## ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER                                    |   | TEST CONDITIONS  | MIN  | TYP  | MAX  | UNIT                |
|--|---|--|------|------|------|---------------------|
| <b>TRANSMITTER AC/DC</b>                     |   |  |      |      |      |                     |
| V <sub>TXDIFF_TB_PP</sub>                    | Differential peak-to-peak Output Voltage<br>(VID = 800, 1200 mVpp, 5Gbps) | R <sub>L</sub> = 100Ω +1%, DEX, OS <sub>x</sub> = NC, <b>Transition Bit</b>                                | 800  | 1000 | 1200 | mV                  |
|  |   | R <sub>L</sub> = 100Ω +1%, DEX, OS <sub>x</sub> = GND<br><b>Transition Bit</b>                             | 870  |      |      |                     |
|  |   | R <sub>L</sub> = 100Ω +1%, DEX, OS <sub>x</sub> = VCC<br><b>Transition Bit</b>                             | 1085 |      |      |                     |
| V <sub>TXDIFF_NTBP_PP</sub>                  |   | R <sub>L</sub> = 100Ω +1%, DEX=NC,<br>OS <sub>x</sub> = 0,1,NC <b>Non-Transition Bit</b>                   | 665  |      |      |                     |
|  |   | R <sub>L</sub> = 100Ω +1%, DEX=0,<br>OS <sub>x</sub> = 0,1,NC <b>Non-Transition Bit</b>                    | 510  |      |      |                     |
|  |   | R <sub>L</sub> = 100Ω +1%, DEX=1<br>OS <sub>x</sub> = 0,1,NC <b>Non-Transition Bit</b>                     | 375  |      |      |                     |
| De-Emphasis Level                            |   | OS <sub>1,2</sub> = NC (for OS <sub>1,2</sub> = 1 and 0 see<br>Table 2)                                    | -3.0 | -3.5 | -4.0 | dB                  |
|  |   |  | -6.0 |      |      |                     |
|  |   |  | -8.5 |      |      |                     |
| T <sub>DE</sub>                              | De-Emphasis Width   |  | 0.85 |      |      | UI                  |
| Z <sub>diff_TX</sub>                         | DC Differential Impedance   |  | 72   | 90   | 120  | Ω                   |
| Z <sub>CM_TX</sub>                           | DC Common Mode Impedance  | Measured w.r.t to AC ground over 0-500mV   | 18   | 23   | 30   | Ω                   |
| R <sub>Ldiff_TX</sub>                        | Differential Return Loss  | f = 50 MHz – 1.25 GHz  | 9    | 10   |      | dB                  |
|  |   | f = 1.25 GHz – 2.5 GHz   | 6    | 7    |      |                     |
| R <sub>Lcm_TX</sub>                          | Common Mode Return Loss   | f = 50 MHz – 2.5 GHz   | 11   | 12   |      | dB                  |
| I <sub>TX_SC</sub>                           | TX short circuit current  | TX± shorted to GND   |      |      | 60   | mA                  |
| V <sub>TX_CM_DC</sub>                        | Transmitter DC common-mode voltage  |  | 2.0  | 2.6  | 3.0  | V                   |
| V <sub>TX_CM_AC_Active</sub>                 | TX AC common mode voltage active  |  |      | 30   | 100  | mVpp                |
| V <sub>TX_idle_diff-AC-pp</sub>              | Electrical idle differential peak to peak output voltage                  | HPF to remove DC   | 0    |      | 10   | mV                  |
| V <sub>TX_CM_DeltaU1-U0</sub>                | Absolute delta of DC CM voltage during active and idle states             |  |      | 35   | 200  | mV                  |
| V <sub>TX_idle_diff-DC</sub>                 | DC Electrical idle differential output voltage                            | Voltage must be low pass filtered to remove any AC component   | 0    |      | 10   | mV                  |
| V <sub>detect</sub>                          | Voltage change to allow receiver detect                                   | Positive voltage to sense receiver termination   |      |      | 600  | mV                  |
| t <sub>R</sub> , t <sub>F</sub>              | Output Rise/Fall time   | 20%-80% of differential voltage measure 1" from the output pin   | 30   | 50   |      | ps                  |
| t <sub>RF_MM</sub>                           | Output Rise/Fall time mismatch  |  |      |      | 20   | ps                  |
| T <sub>diff_LH</sub> , T <sub>diff_HL</sub>  | Differential Propagation Delay  | De-Emphasis = -3.5dB (CH 0 and CH 1). Propagation delay between 50% level at input and output See Figure 5 |      | 290  | 350  | ps                  |
| t <sub>idleEntry</sub> t <sub>idleExit</sub> | Idle entry and exit times   | See Figure 6   |      | 4    | 6    | ns                  |
| C <sub>TX</sub>                              | Tx input capacitance to GND   | At 2.5 GHz   |      | 1.25 |      | pF                  |
| <b>EQUALIZATION</b>                          |   |  |      |      |      |                     |
| T <sub>TX-EYE</sub> <sup>(1)(2)</sup>        | <b>Total Jitter (Tj) at point A</b>                                       | Device setting: OS1 = L, DE1 = H, EQ1 = L  |      | 0.14 | 0.5  | Ulpp <sup>(3)</sup> |
| DJ <sub>TX</sub> <sup>(2)</sup>              | Deterministic Jitter (Dj)   |  |      | 0.06 | 0.3  |                     |
| RJ <sub>TX</sub> <sup>(2)(4)</sup>           | Random Jitter (Rj)  |  |      | 0.08 | 0.2  |                     |
| T <sub>TX-EYE</sub> <sup>(1)(2)</sup>        | <b>Total Jitter (Tj) at point B</b>                                       | Device setting: OS2 = H, DE2 = H, EQ2 = L  |      | 0.14 | 0.5  | Ulpp <sup>(3)</sup> |
| DJ <sub>TX</sub> <sup>(2)</sup>              | Deterministic Jitter (Dj)   |  |      | 0.06 | 0.3  |                     |
| RJ <sub>TX</sub> <sup>(2)(4)</sup>           | Random Jitter (Rj)  |  |      | 0.08 | 0.2  |                     |

(1) Includes Rj at 10<sup>-12</sup>

(2) Measured at the end of reference channel in Figure 8 with K28.5 pattern, V<sub>ID</sub>=1000mVpp, 5Gbps, -3.5dB DE from source.

(3) UI = 200ps

(4) Rj calculated as 14.069 times the RMS random jitter for 10<sup>-12</sup> BER



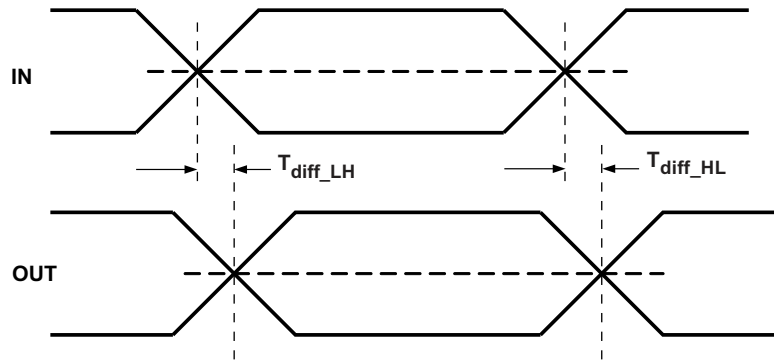


Figure 5. Propagation Delay

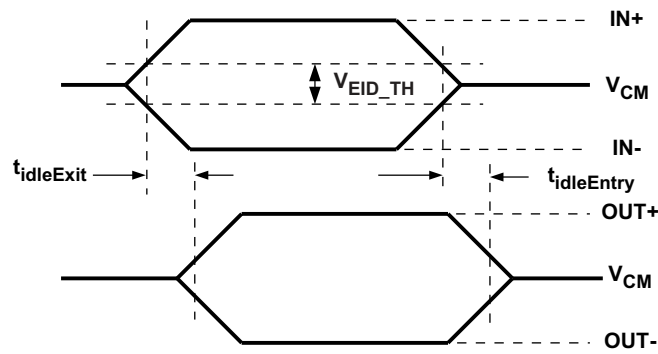


Figure 6. Electrical Idle Mode Exit and Entry Delay

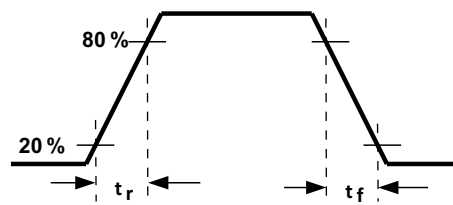


Figure 7. Output Rise and Fall Times

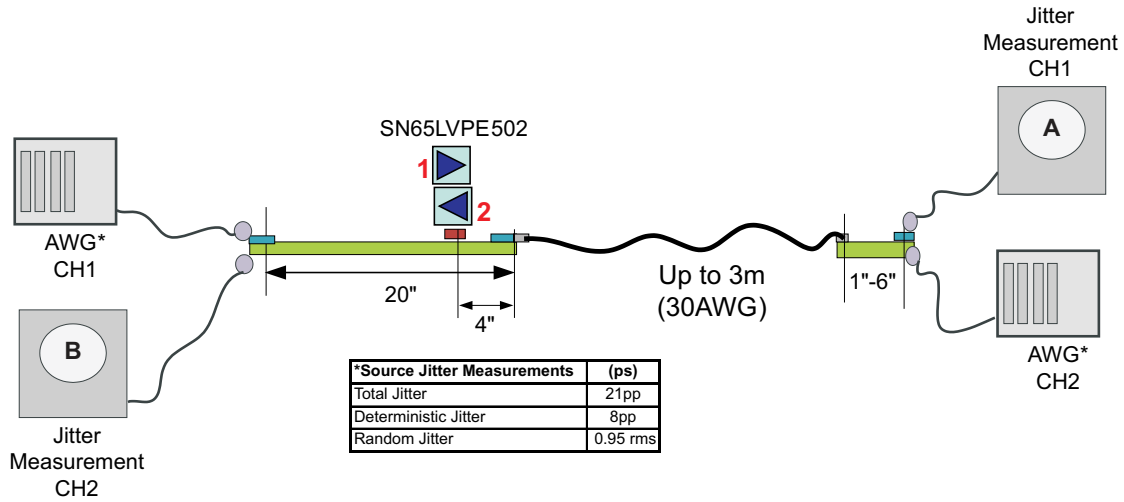


Figure 8. Jitter Measurement Setup

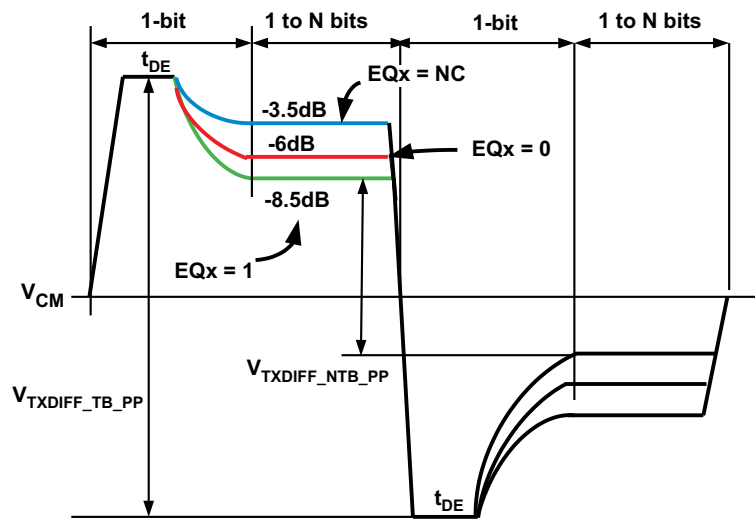


Figure 9. Output De-Emphasis Levels OSx = NC

### Typical Eye Diagram and Performance Curves

Input Signal Characteristics: Data Rate = 5 Gbps,  $V_{ID} = 1000$  mVpp, DE = -3.5 dB, Pattern = K28.5 Device  
 Operating Conditions: VCC = 3.3 V, Temp = 25°C

### Input Trace Length Held Constant and Output Cable Length Varied

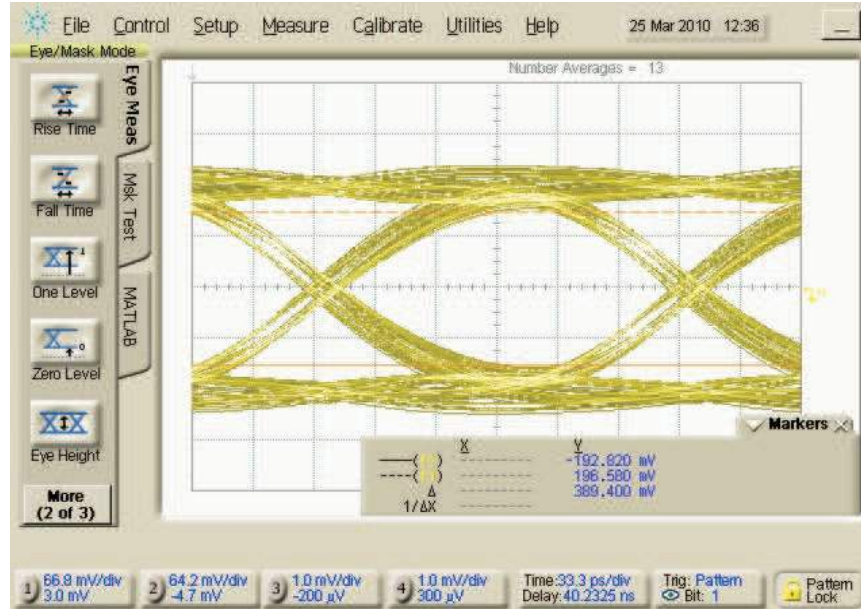


Figure 10. Input Trace = 12 Inches, 6 mil and Output USB 3 Cable Length = 1 M

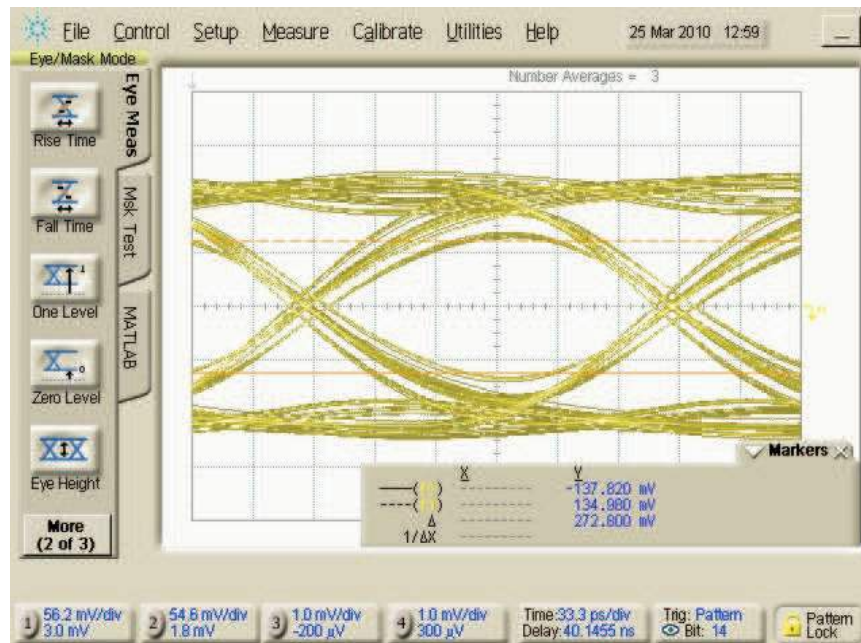


Figure 11. Input Trace = 12 Inches, 6 mil and Output USB 3 Cable Length = 2 M

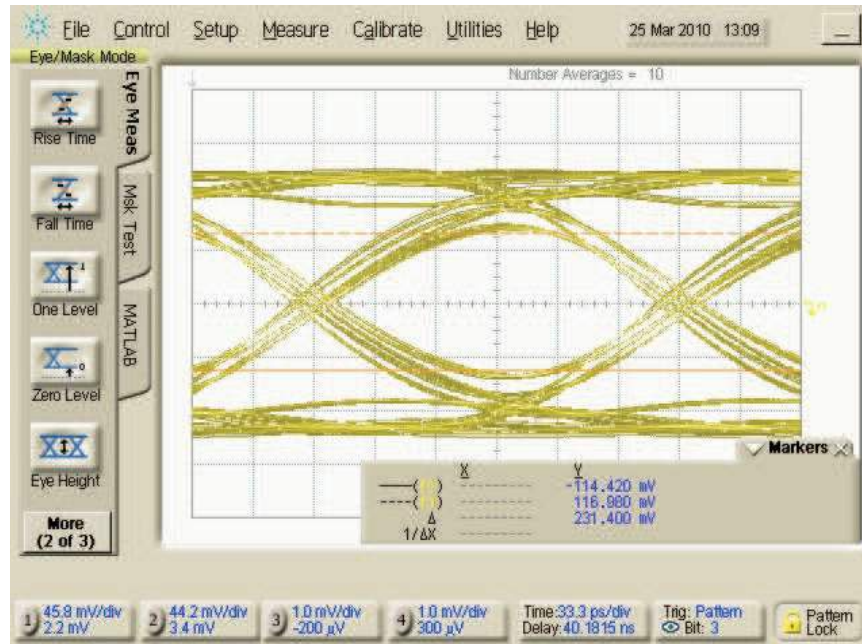


Figure 12. Input Trace = 12 Inches, 6 mil and Output USB 3 Cable Length = 3 M

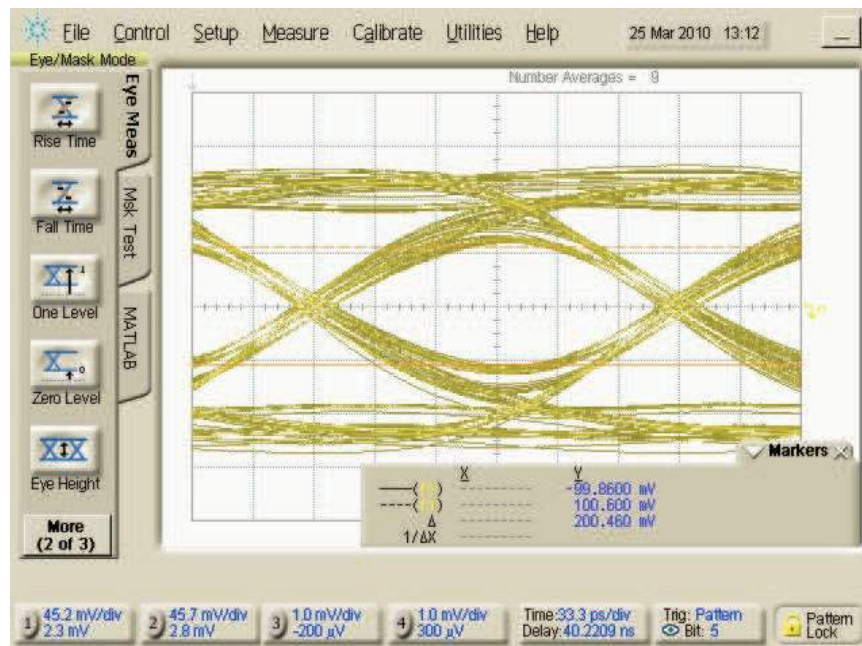


Figure 13. Input Trace = 12 Inches, 6 mil and Output USB 3 Cable Length = 4 M

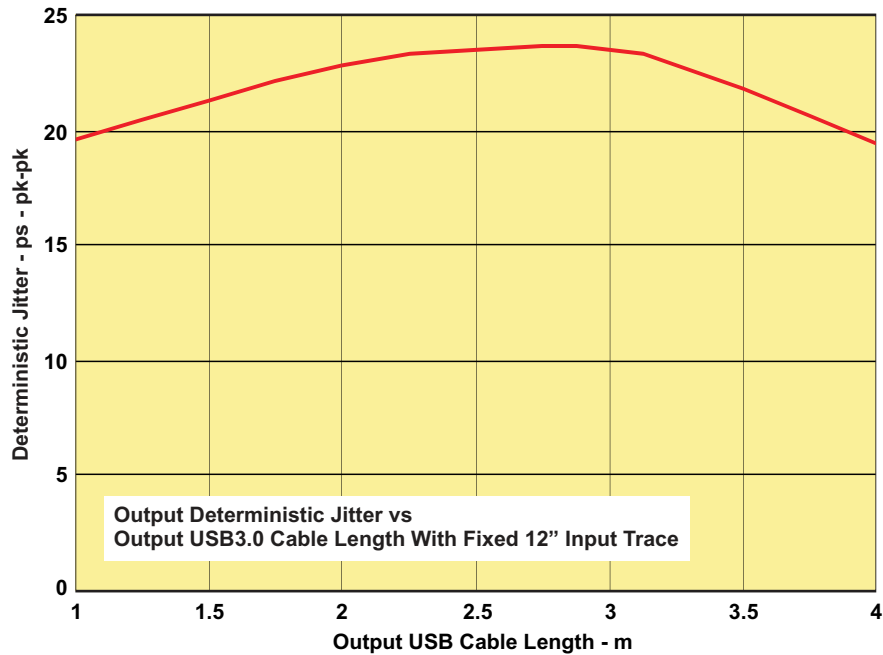


Figure 14. Jitter Performance Over Different Cable Lengths

Input Trace Length Held Constant and Output Trace Varied

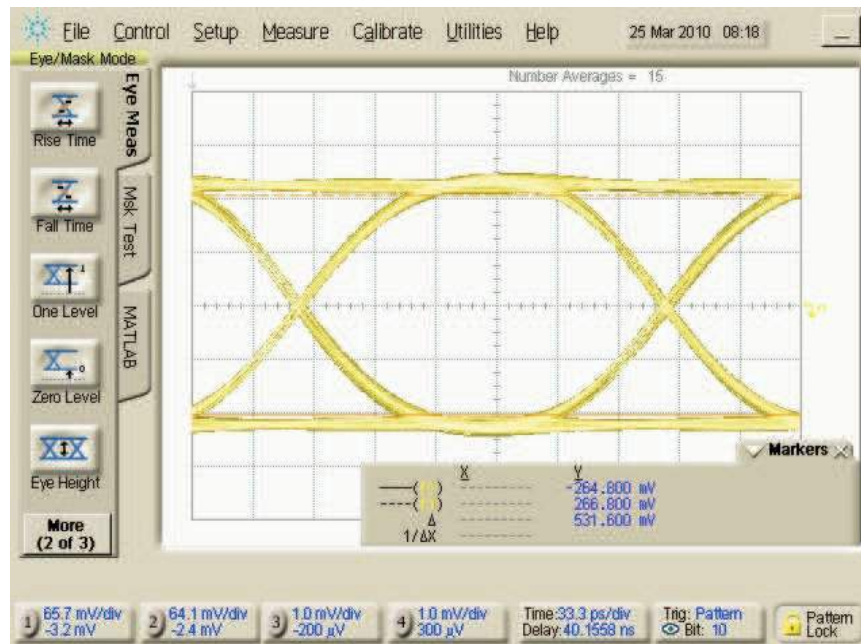


Figure 15. Input Trace = 4 Inches, 6 mil and Output Trace = 4 Inches, 6 mil



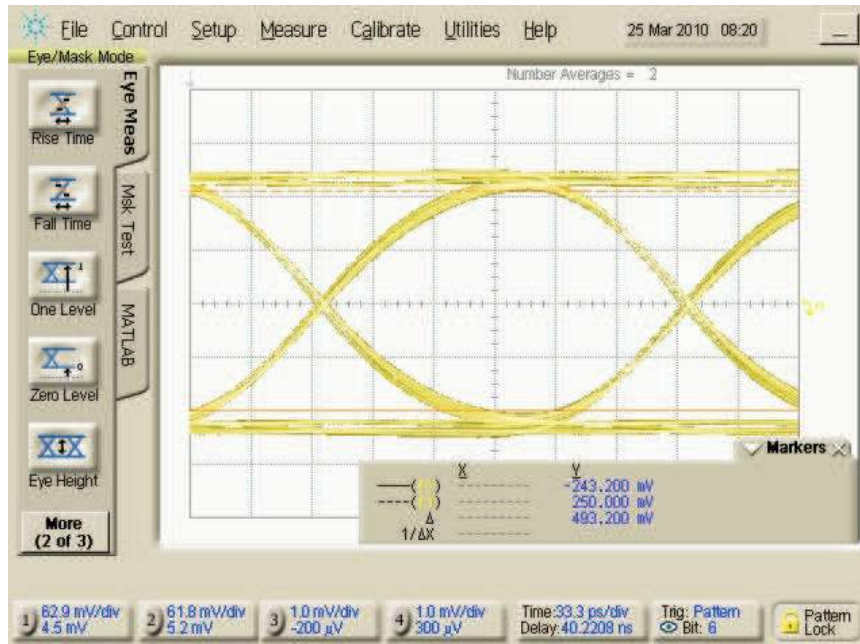


Figure 16. Input Trace = 4 Inches, 6 mil and Output Trace = 8 Inches, 6 mil

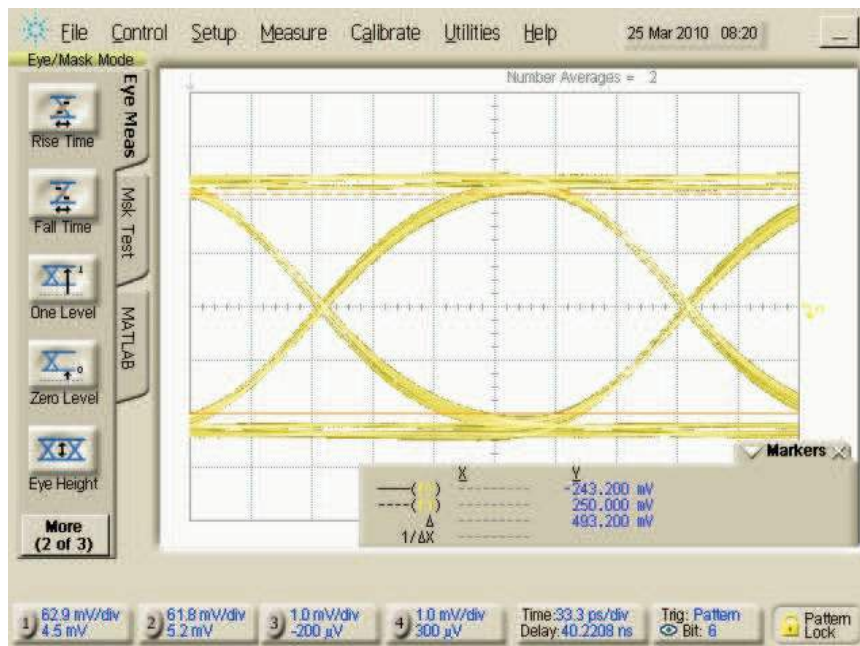


Figure 17. Input Trace = 4 Inches, 6 mil and Output Trace = 12 Inches, 6 mil

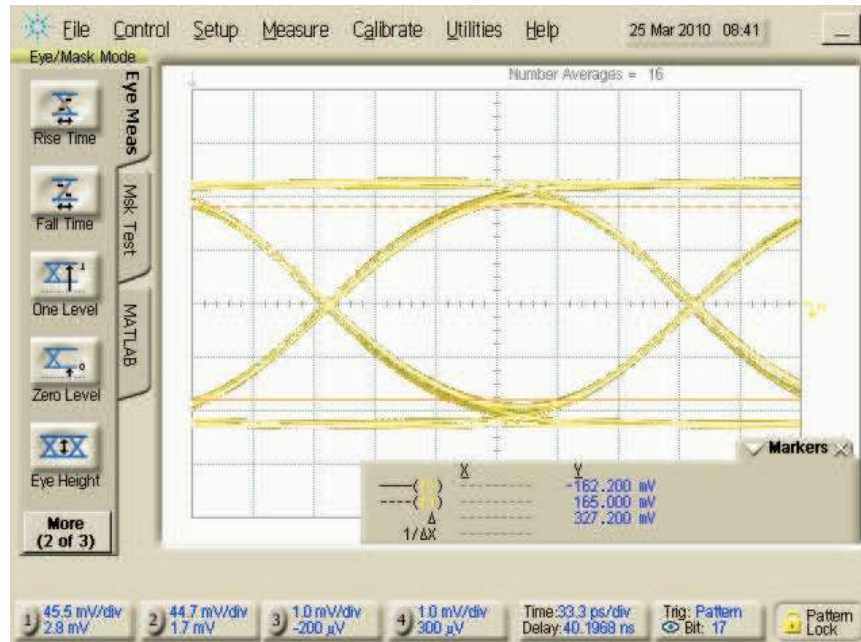


Figure 18. Input Trace = 4 Inches, 6 mil and Output Trace = 16 Inches, 6 mil

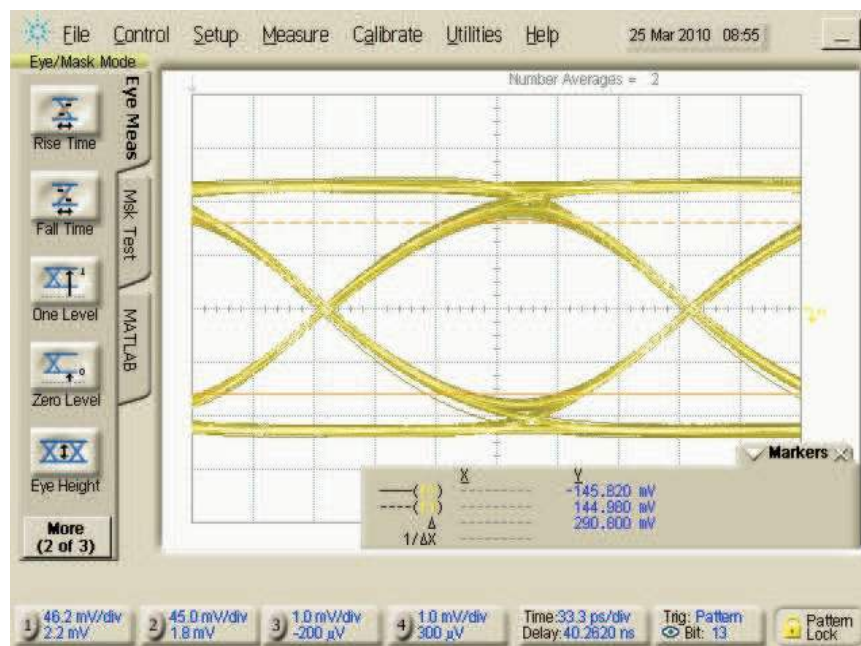


Figure 19. Input Trace = 4 Inches, 6 mil and Output Trace = 20 Inches, 6 mil

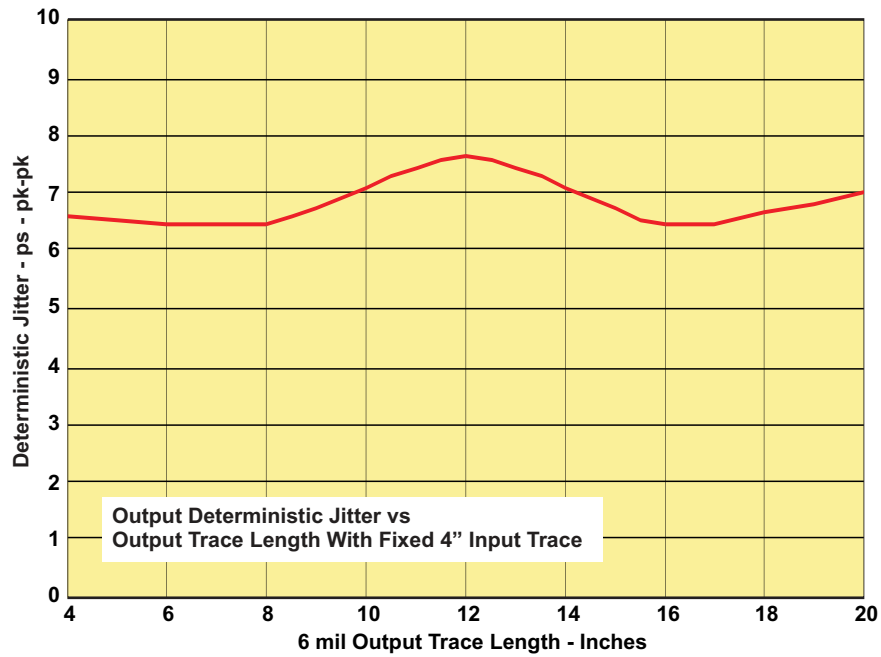


Figure 20. Jitter Performance Over Different Output Trace Lengths

Output Trace Length Held Constant and Input Trace Length Varied

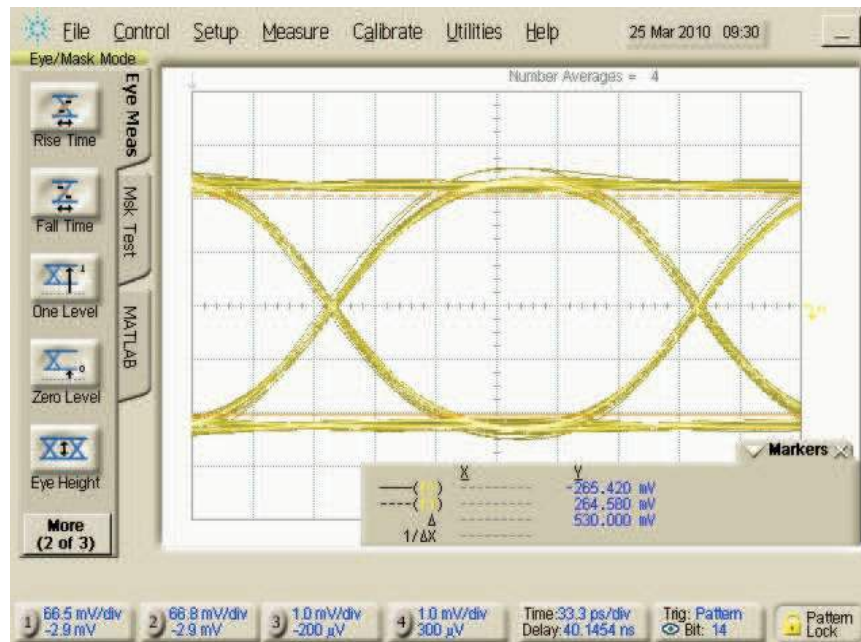


Figure 21. Input Trace = 4 Inches, 6 mil and Output Trace = 4 Inches, 6 mil



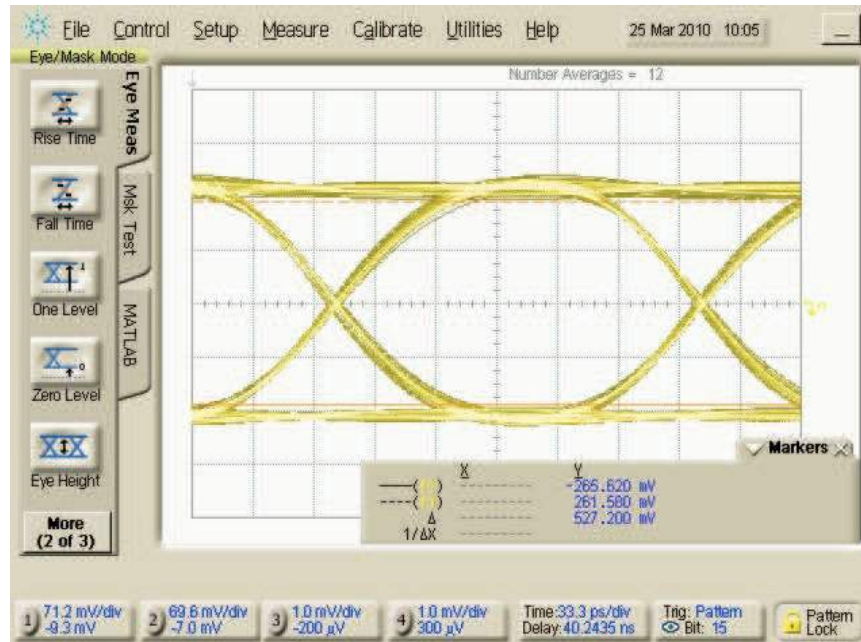


Figure 22. Input Trace = 8 Inches, 6 mil and Output Trace = 4 Inches, 6 mil

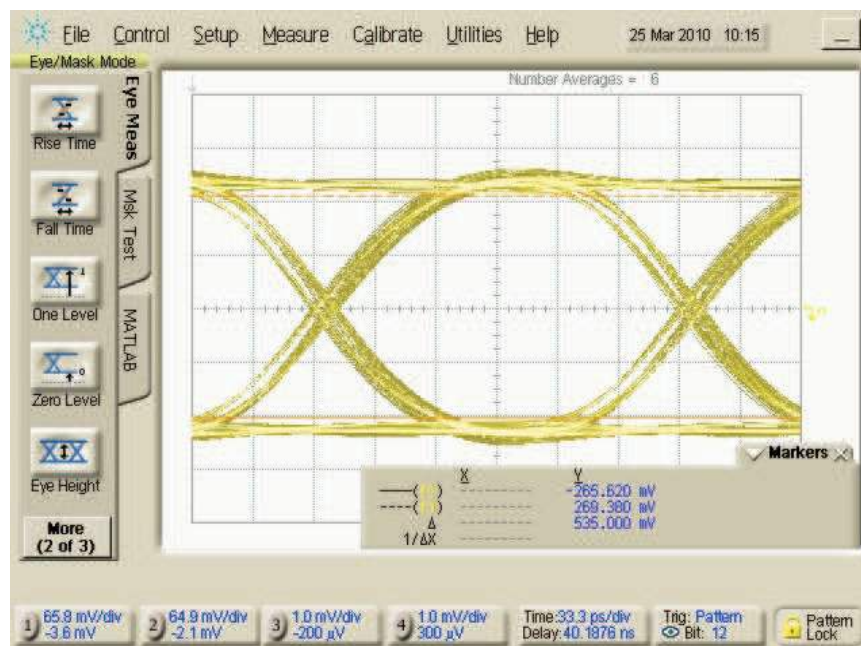


Figure 23. Input Trace = 12 Inches, 6 mil and Output Trace = 4 Inches, 6 mil

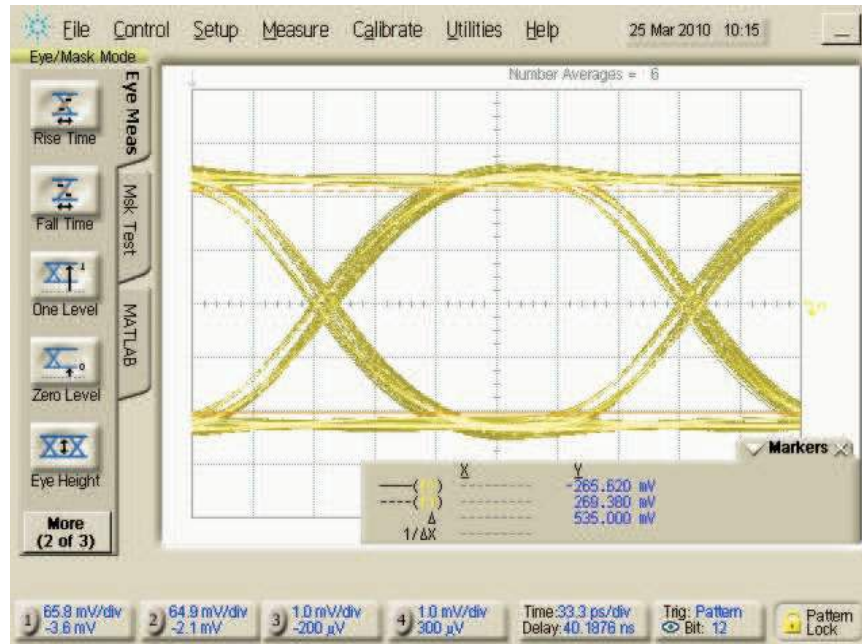


Figure 24. Input Trace = 16 Inches, 6 mil and Output Trace = 4 Inches, 6 mil

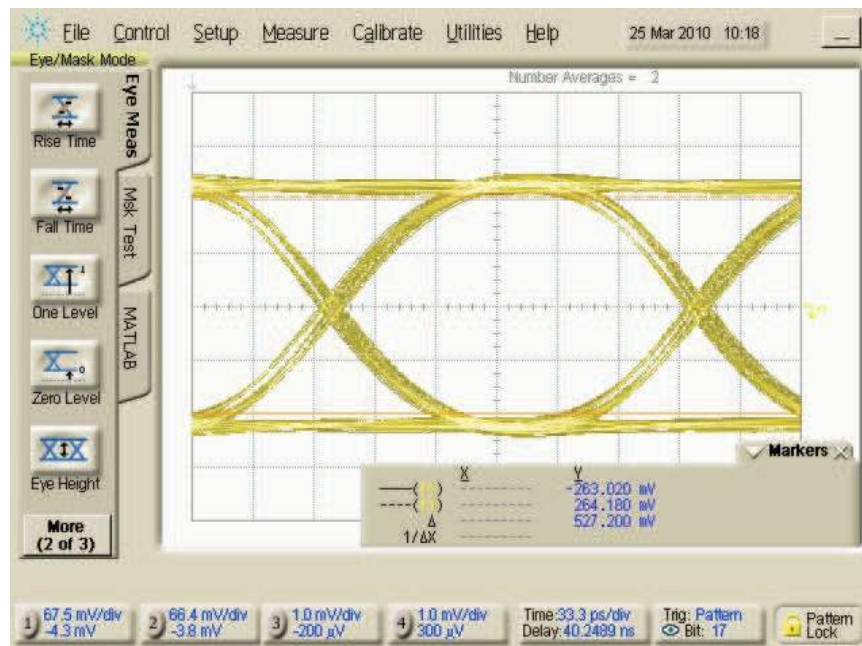


Figure 25. Input Trace = 20 Inches, 6 mil and Output Trace = 4 Inches, 6 mil

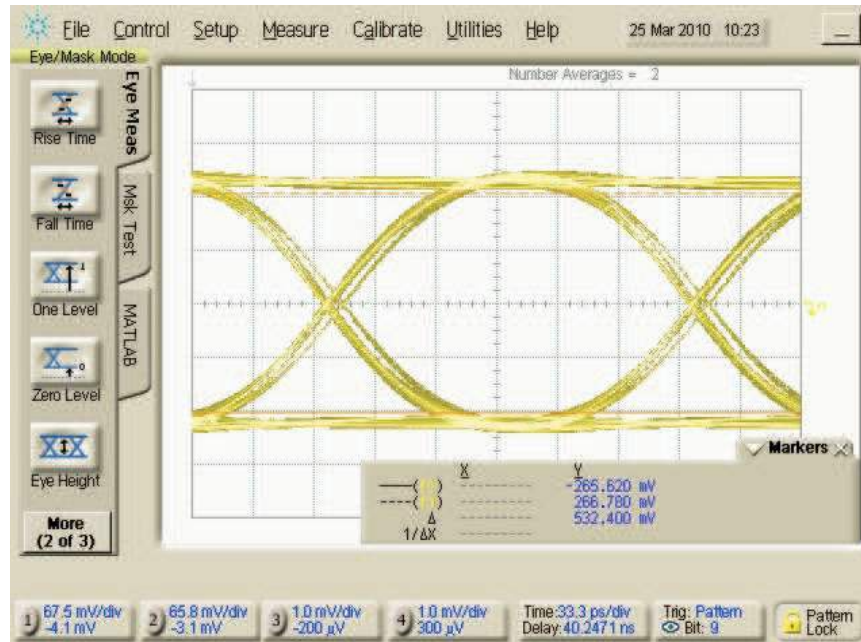


Figure 26. Input Trace = 28 Inches, 6 mil and Output Trace = 4 Inches, 6 mil

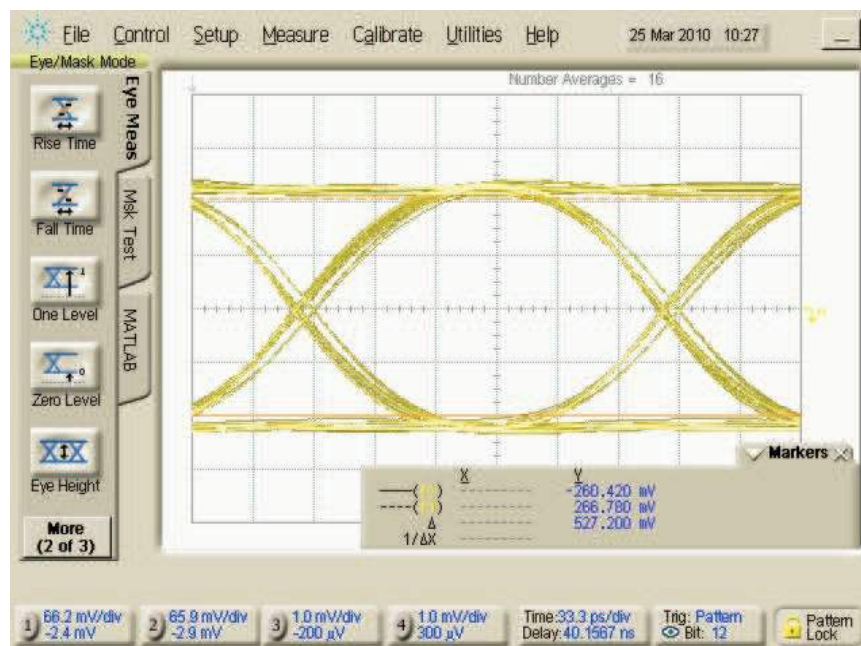


Figure 27. Input Trace = 32 Inches, 6 mil and Output Trace = 4 Inches, 6 mil

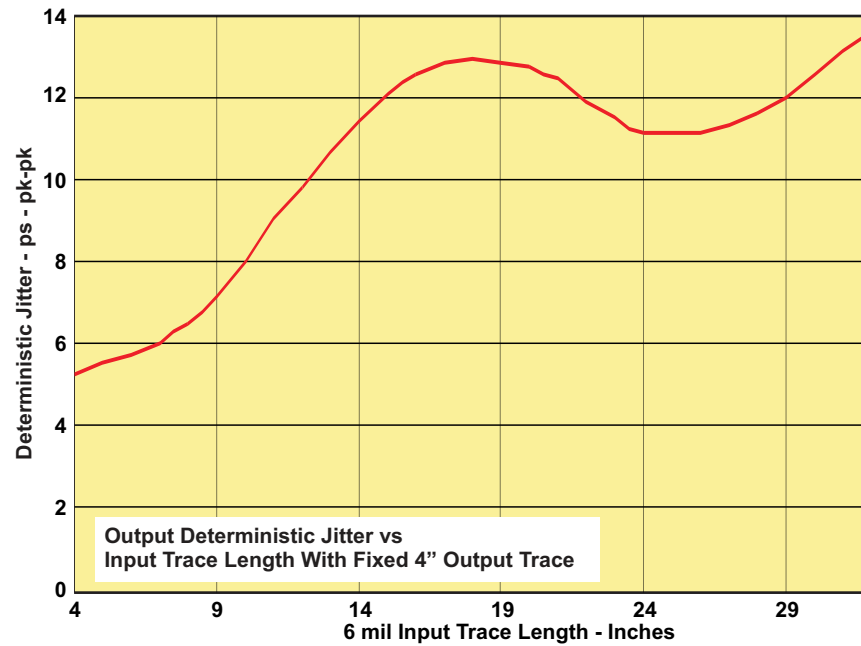


Figure 28. Jitter Performance Over Different Input Trace Lengths

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**REVISION HISTORY**

| <b>Changes from Original (April 2010 ) to Revision A</b>   | <b>Page</b>          |
|--|----------------------|
| <hr/> <ul style="list-style-type: none"><li>Changed in Table 1. Pin Description, signals: TX1+, TX1-, TX2+ and TX2- , I/O types changed from O, CML to O, VML also in Descripton, 'CML' to 'VML' .....</li></ul> <hr/> | <hr/> <b>4</b> <hr/> |



**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|---------|
| SN65LVPE502RGER  | NRND          | VQFN         | RGE                | 24   | 3000           | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | 0 to 85      | LVPE502                 |         |
| SN65LVPE502RGET  | NRND          | VQFN         | RGE                | 24   | 250            | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | 0 to 85      | LVPE502                 |         |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

| Device          | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN65LVPE502RGER | VQFN         | RGE             | 24   | 3000 | 330.0              | 12.4               | 4.25    | 4.25    | 1.15    | 8.0     | 12.0   | Q2            |
| SN65LVPE502RGET | VQFN         | RGE             | 24   | 250  | 180.0              | 12.4               | 4.25    | 4.25    | 1.15    | 8.0     | 12.0   | Q2            |

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device          | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN65LVPE502RGER | VQFN         | RGE             | 24   | 3000 | 356.0       | 356.0      | 35.0        |
| SN65LVPE502RGET | VQFN         | RGE             | 24   | 250  | 210.0       | 185.0      | 35.0        |

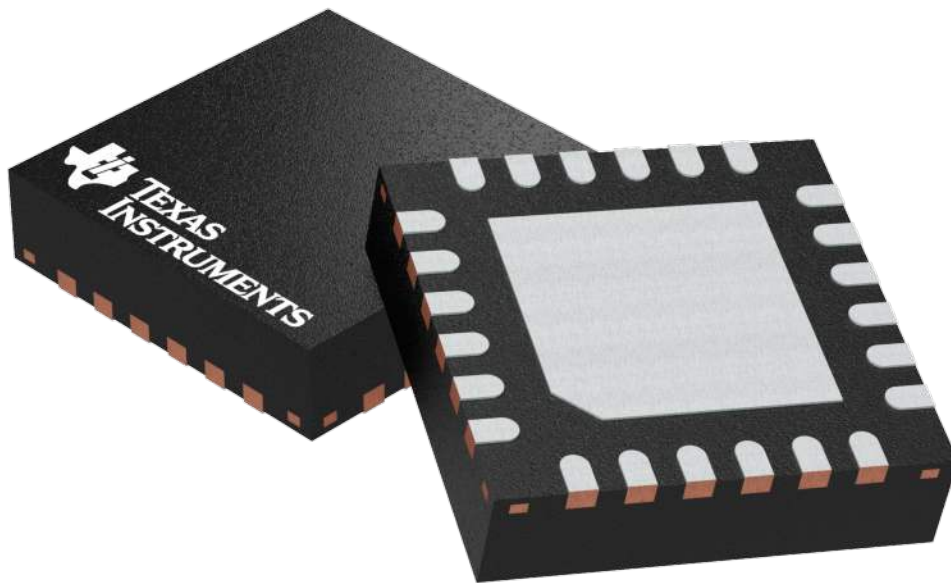


**RGE 24**

**GENERIC PACKAGE VIEW**

**VQFN - 1 mm max height**

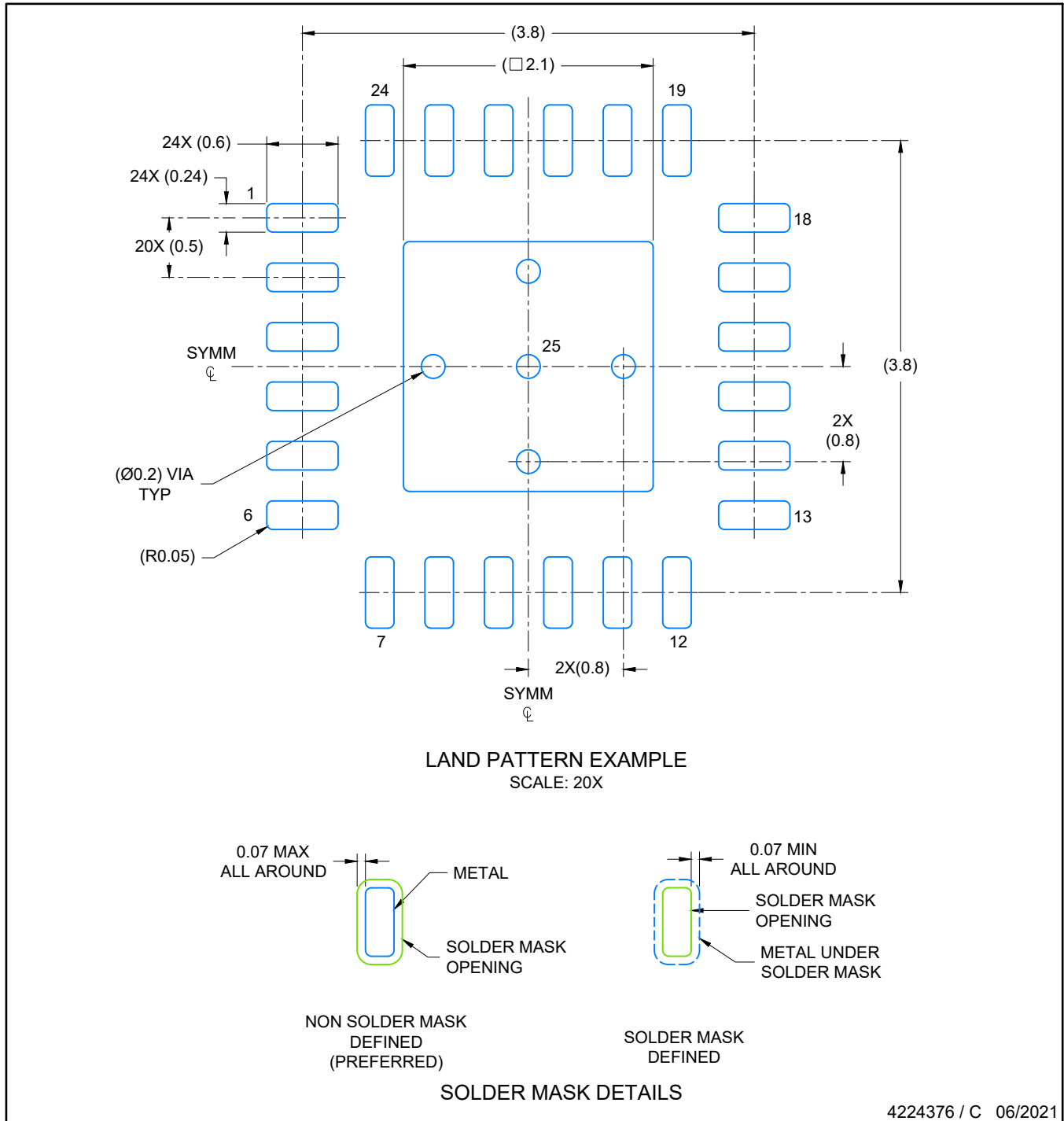
PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4204104/H





NOTES: (continued)

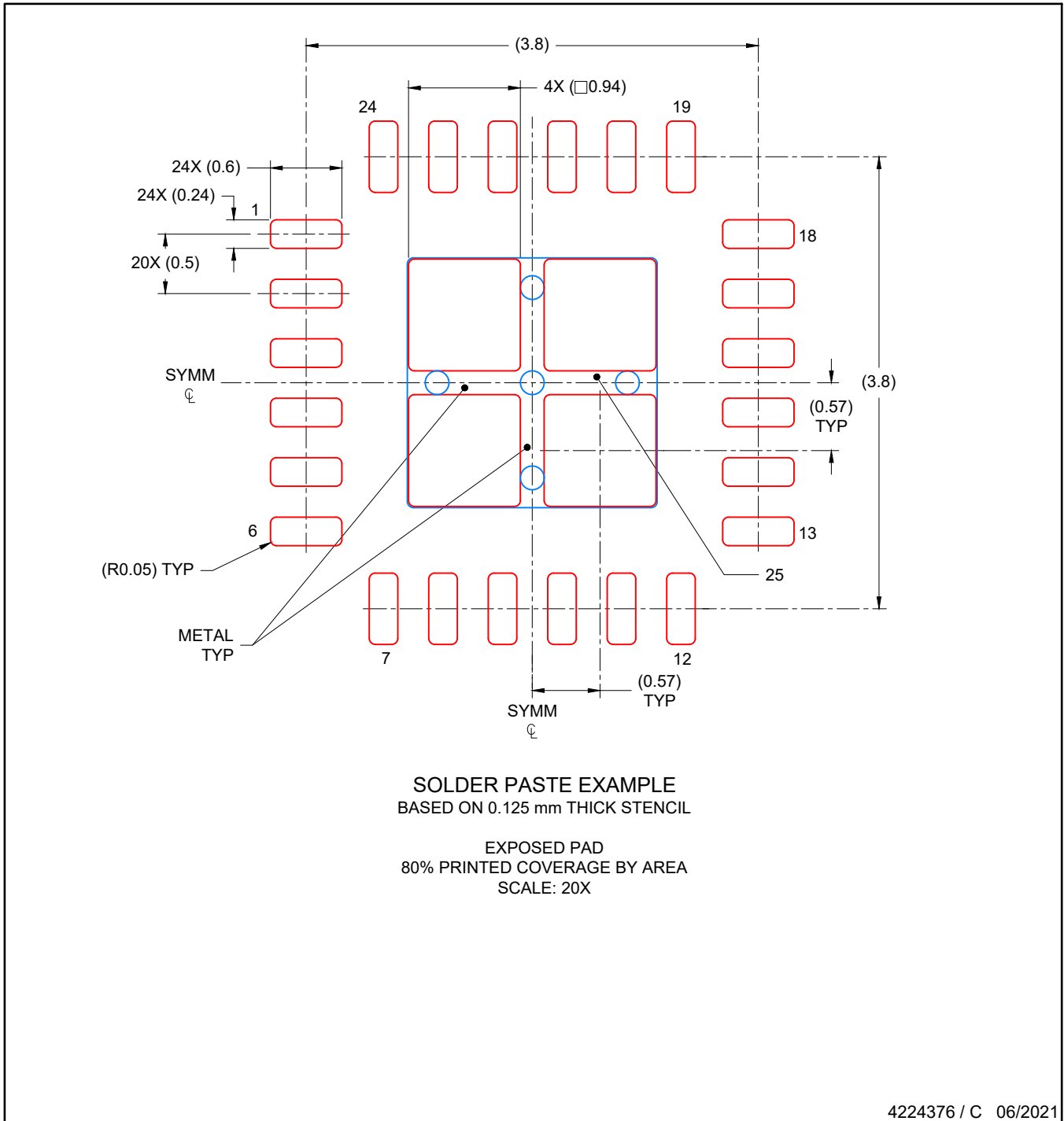
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

RGE0024C

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK- NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

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