ADC0844/ADC0848 8-Bit µP Compatible A/D Converters with Multiplexer Options

Check for Samples: ADC0844, ADC0848

FEATURES

- **Easy Interface to All Microprocessors**
- **Operates Ratiometrically or with 5 V_{DC} Voltage Reference**
- **No Zero or Full-Scale Adjust Required**
- **4-Channel or 8-Channel Multiplexer with Address Logic**
- **Internal Clock**
- **0V to 5V Input Range with Single 5V Power Supply**
- **Standard Width 20-Pin or 24-Pin PDIP**
- **28 Pin PLCC Package**

KEY SPECIFICATIONS

- **Resolution: 8 Bits**
- **Total Unadjusted Error: ±½ LSB and ± 1 LSB**
- **Single Supply: 5 V_{DC}**
- **Low Power: 15 mW**
- **Conversion Time: 40 µs**

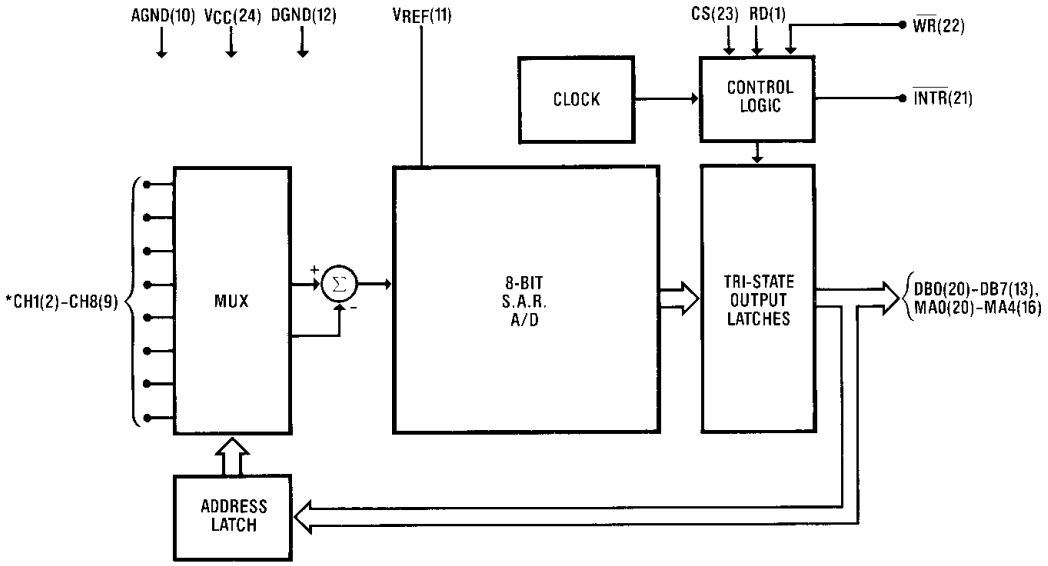
DESCRIPTION

The ADC0844 and ADC0848 are CMOS 8-bit successive approximation A/D converters with versatile analog input multiplexers. The 4-channel or 8-channel multiplexers can be software configured for single-ended, differential or pseudo-differential modes of operation.

The differential mode provides low frequency input common mode rejection and allows offsetting the analog range of the converter. In addition, the A/D's reference can be adjusted enabling the conversion of reduced analog ranges with 8-bit resolution.

The A/Ds are designed to operate from the control bus of a wide variety of microprocessors. TRI-STATE output latches that directly drive the data bus permit the A/Ds to be configured as memory locations or I/O devices to the microprocessor with no interface logic necessary.

Block Diagram



* ADC0848 shown in PDIP Package CH5-CH8 not included on the ADC0844

Connection Diagram

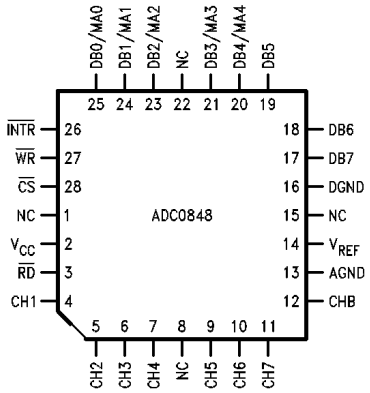


Figure 1. PLCC Package (Top View)

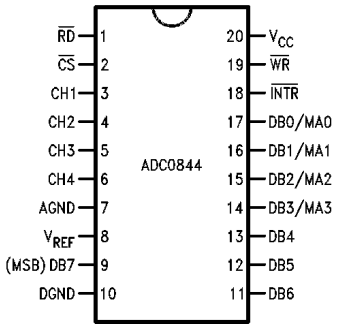


Figure 2. 20-Pin PDIP (Top View)

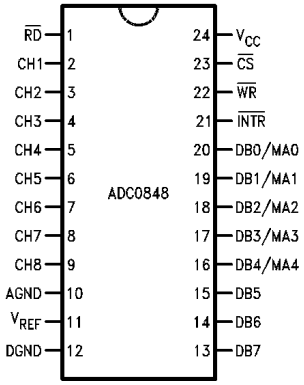


Figure 3. 28-Pin PDIP (Top View)

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[1][2][3]

Supply Voltage (V_{CC})			6.5V
Voltage	Logic Control Inputs		−0.3V to +15V
	At Other Inputs and Outputs		−0.3V to V_{CC}+0.3V
Input Current at Any Pin[4]			5 mA
Package Input Current[4]			20 mA
Storage Temperature			−65°C to +150°C
Package Dissipation at T_A=25°C			875 mW
ESD Susceptibility[5]			800V
Lead Temperature (Soldering, 10 seconds)	PDIP Package		260°C
	PLCC Package	Vapor Phase (60 seconds)	215°C
		Infrared (15 seconds)	220°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.
(2) All voltages are measured with respect to the ground pins.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(4) When the input voltage (V_{IN}) at any pin exceeds the power supply rails (V_{IN} < V^- or V_{IN} > V^+) the absolute value of the current at that pin should be limited to 5 mA or less. The 20 mA package input current limits the number of pins that can exceed the power supply boundaries with a 5 mA current limit to four.
(5) Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Operating Conditions[1][2]

Supply Voltage (V_{CC})		4.5 V_{DC} to 6.0 V_{DC}
Temperature Range ($T_{MIN} \le T_A \le T_{MAX}$)	ADC0844CCN, ADC0848BCN, ADC0848CCN	$0°C \le T_A \le 70°C$
	ADC0844BCJ[3], ADC0844CCJ[3], ADC0848BCV, ADC0848CCV	$-40°C \le T_A \le 85°C$

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.
(2) All voltages are measured with respect to the ground pins.
(3) Product/package combination obsolete; shown for reference only.

Electrical Characteristics

The following specifications apply for V_{CC} = 5 V_{DC} unless otherwise specified. **Boldface limits apply from T_{MIN} to T_{MAX};** all other limits $T_A = T_j$ = 25°C.

Parameter		Conditions	ADC0844BCJ[1] ADC0844CCJ[1]			ADC0844CCN, ADC0848BCN, ADC0848CCN, ADC0848BCV, ADC0848CCV			Limit Units
			Typ[2]	Tested Limit[3]	Design Limit[4]	Typ[2]	Tested Limit[3]	Design Limit[4]	
CONVERTER AND MULTIPLEXER CHARACTERISTICS									
Maximum Total Unadjusted Error	ADC0844BCN, ADC0848BCN, BCV	V_{REF} = 5.00 V_{DC}[5]					±½	**±½**	LSB
	ADC0844CCN, ADC0848CCN, CCV						±1	**±1**	LSB
	ADC0844CCJ[1]			**±1**					LSB
Minimum Reference Input Resistance			2.4	**1.1**		2.4	1.2	**1.1**	kΩ
Maximum Reference Input Resistance			2.4	**5.9**		2.4	5.4	**5.9**	kΩ
Maximum Common-Mode Input Voltage		See[6]		**V_{CC} + 0.05**			V_{CC} + 0.05	**V_{CC} + 0.05**	V
Minimum Common-Mode Input Voltage		See[6]		**GND − 0.05**			GND − 0.05	**GND − 0.05**	V
DC Common-Mode Error		Differential Mode	±1/16	**±¼**		±1/16	±¼	**±¼**	LSB
Power Supply Sensitivity		V_{CC} = 5V±5%	±1/16	**±⅛**		±1/16	±⅛	**±⅛**	LSB
Off Channel Leakage Current		On Channel = 5V, Off Channel = 0V[7]		**−1**			−0.1	**−1**	µA
		On Channel = 0V, Off Channel = 5V		**1**			0.1	**1**	µA
DIGITAL AND DC CHARACTERISTICS									
$V_{IN(1)}$, Logical "1" Input Voltage (Min)		V_{CC} = 5.25V		**2.0**			2.0	**2.0**	V
$V_{IN(0)}$, Logical "0" Input Voltage (Max)		V_{CC} = 4.75V		**0.8**			0.8	**0.8**	V
$I_{IN(1)}$, Logical "1" Input Current (Max)		V_{IN} = 5.0V	0.005	**1**		0.005		**1**	µA
$I_{IN(0)}$, Logical "0" Input Current (Max)		V_{IN} = 0V	−0.005	**−1**		−0.005		**−1**	µA

(1) This product/package combination is obsolete. Shown for reference only.
(2) Typical figures are at 25°C and represent most likely parametric norm.
(3) Tested limits are specified to TI's AOQL (Average Outgoing Quality Level).
(4) Design limits are specified by not 100% tested. These limits are not used to calculate outgoing quality levels.
(5) Total unadjusted error includes offset, full-scale, linearity, and multiplexer error.
(6) For V_{IN} (−) ≥ V_{IN}(+) the digital output code will be 0000 0000. Two on-chip diodes are tied to each analog input, which will forward-conduct for analog input voltages one diode drop below ground or one diode drop greater than V_{CC} supply. Be careful during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct, especially at elevated temperatures, and cause errors for analog inputs near full-scale. The spec allows 50 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.950 V_{DC} over temperature variations, initial tolerance and loading.
(7) Off channel leakage current is measured after the channel selection.

Electrical Characteristics (continued)

The following specifications apply for V_{CC} = 5 V_{DC} unless otherwise specified. **Boldface limits apply from T_{MIN} to T_{MAX};** all other limits $T_A = T_j$ = 25°C.

Parameter	Conditions	ADC0844BCJ[1] ADC0844CCJ[1]			ADC0844CCN, ADC0848BCN, ADC0848CCN, ADC0848BCV, ADC0848CCV			Limit Units
		Typ[2]	Tested Limit[3]	Design Limit[4]	Typ[2]	Tested Limit[3]	Design Limit[4]	
$V_{OUT(1)}$, Logical "1" Output Voltage (Min)	V_{CC} = 4.75V, I_{OUT} = −360 µA		**2.4**			2.8	**2.4**	V
	I_{OUT} = −10 µA		**4.5**			4.6	**4.5**	V
$V_{OUT(0)}$, Logical "0" Output Voltage (Max)	V_{CC} = 4.75V, I_{OUT} = 1.6 mA		**0.4**			0.34	**0.4**	V
I_{OUT}, TRI-STATE Output Current (Max)	V_{OUT} = 0V	−0.01	**−3**		−0.01	−0.3	**−3**	µA
	V_{OUT} = 5V	0.01	**3**		0.01	0.3	**3**	µA
I_{SOURCE}, Output Source Current (Min)	V_{OUT} = 0V	−14	**−6.5**		−14	−7.5	**−6.5**	mA
I_{SINK}, Output Sink Current (Min)	V_{OUT} = V_{CC}	16	**8.0**		16	9.0	**8.0**	mA
I_{CC}, Supply Current (Max)	$\overline{CS}$ = 1, V_{REF} Open	1	**2.5**		1	2.3	**2.5**	mA

AC Electrical Characteristics

The following specifications apply for V_{CC} = 5V_{DC}, $t_r = t_f$ = 10 ns unless otherwise specified. **Boldface limits apply from T_{MIN} to T_{MAX};** all other limits $T_A = T_j$ = 25°C.

Parameter	Conditions	Typ[1]	Tested Limit[2]	Design Limit[3]	Units
t_C, Maximum Conversion Time (See Figure 7)		30	40	**60**	µs
$t_{W(\overline{WR})}$, Minimum $\overline{WR}$ Pulse Width	See[4]	50	150		ns
t_{ACC}, Maximum Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Data Valid)	C_L = 100 pF[4]	145		225	ns
t_{1H}, t_{0H}, TRI-STATE Control (Maximum Delay from Rising Edge of $\overline{RD}$ to Hi-Z State)	C_L = 10 pF, R_L = 10k[4]	125		200	ns
t_{WI}, t_{RI}, Maximum Delay from Falling Edge of $\overline{WR}$ or $\overline{RD}$ to Reset of INTR	See[4]	200	400		ns
t_{DS}, Minimum Data Set-Up Time		50	100		ns
t_{DH}, Minimum Data Hold Time		0	50		ns
C_{IN}, Capacitance of Logic Inputs		5			pF
C_{OUT}, Capacitance of Logic Outputs		5			pF

(1) Typical figures are at 25°C and represent most likely parametric norm.
(2) Tested limits are specified to TI's AOQL (Average Outgoing Quality Level).
(3) Design limits are specified by not 100% tested. These limits are not used to calculate outgoing quality levels.
(4) The temperature coefficient is 0.3%/°C.

Typical Performance Characteristics

Logic Input Threshold Voltage vs. Supply Voltage

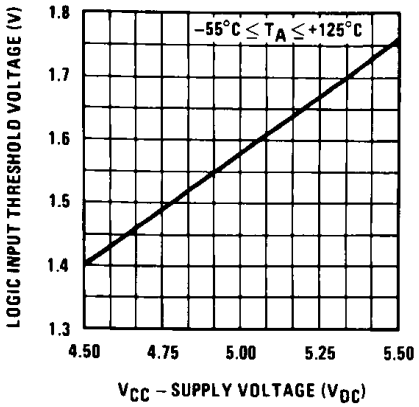


Figure 4.

Output Current vs. Temperature

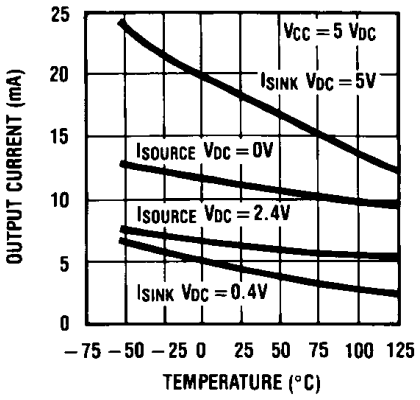


Figure 5.

Power Supply Current vs. Temperature

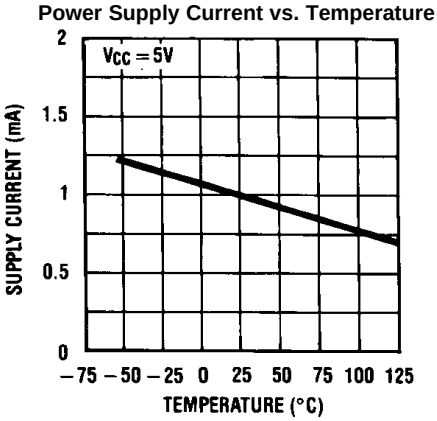


Figure 6.

Linearity Error vs. V_{REF}

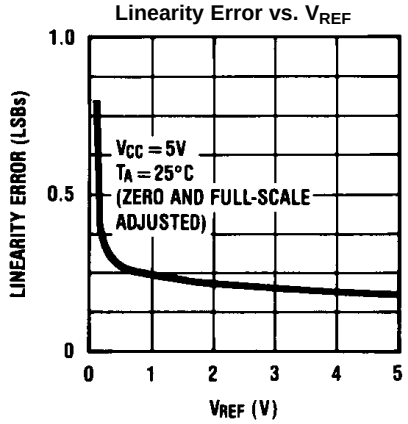


Figure 7.

Conversion Time vs. V_{SUPPLY}

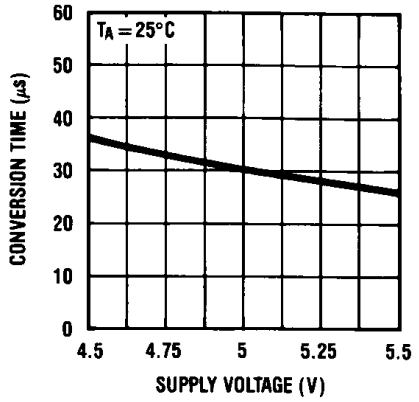


Figure 8.

Conversion Time vs.Temperature

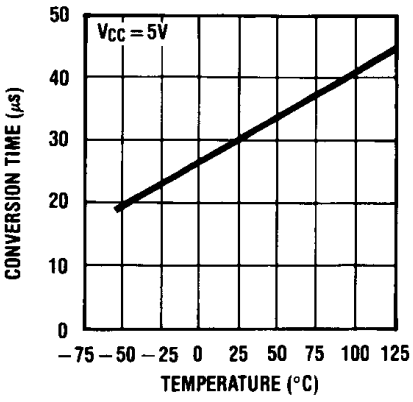


Figure 9.

Typical Performance Characteristics (continued)

Unadjusted Offset Error vs. V_{REF} Voltage

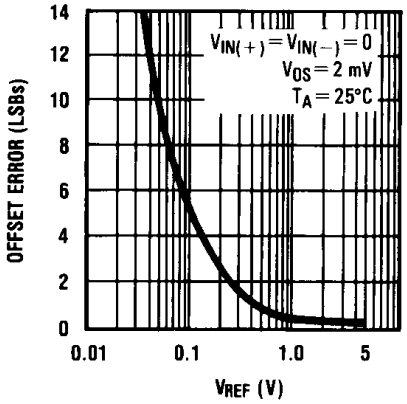
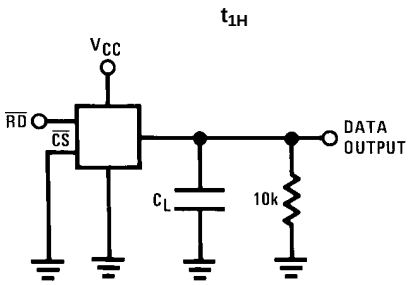
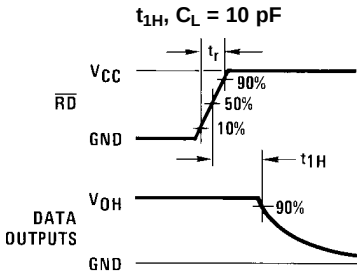
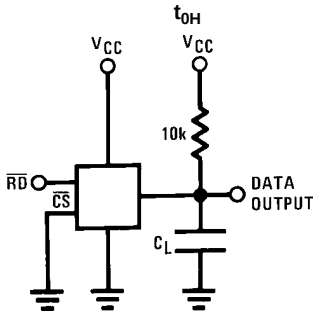


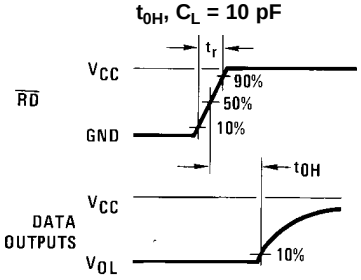
Figure 10.

TRI-STATE Test Circuits and Waveforms



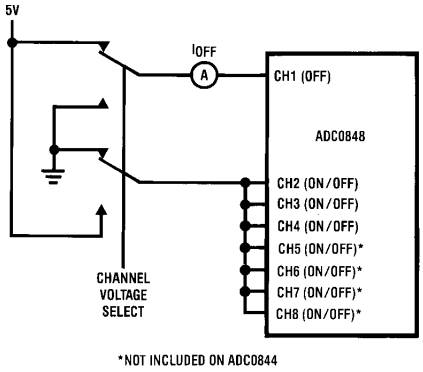






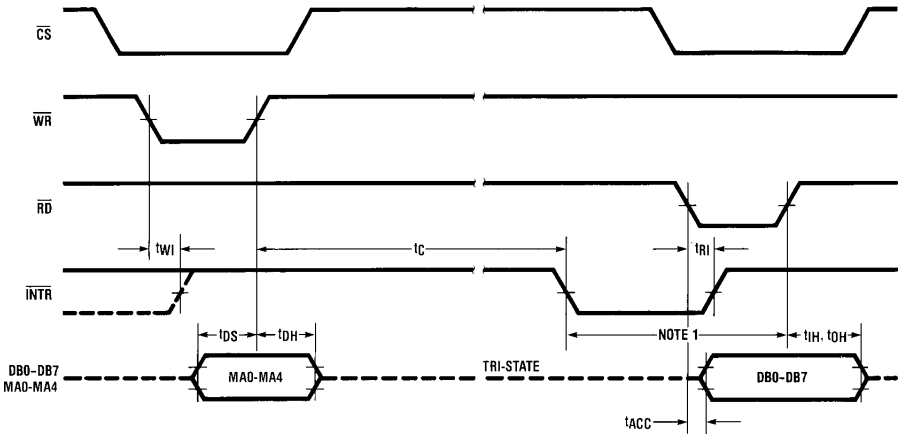
t_r = 20 ns

Leakage Current Test Circuit



*NOT INCLUDED ON ADC0844

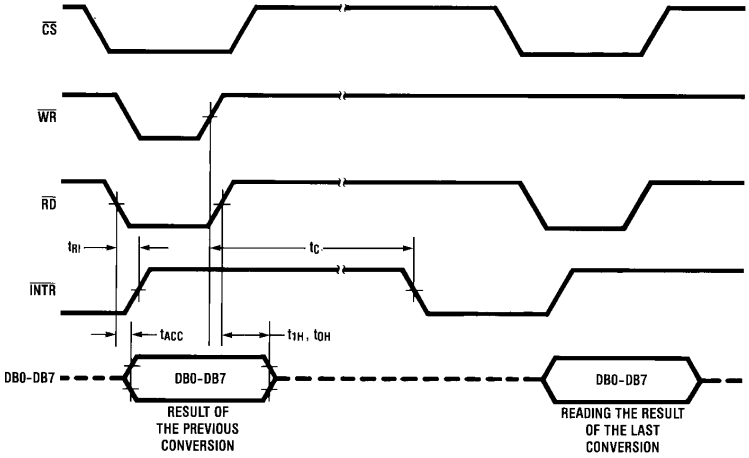
Timing Diagrams



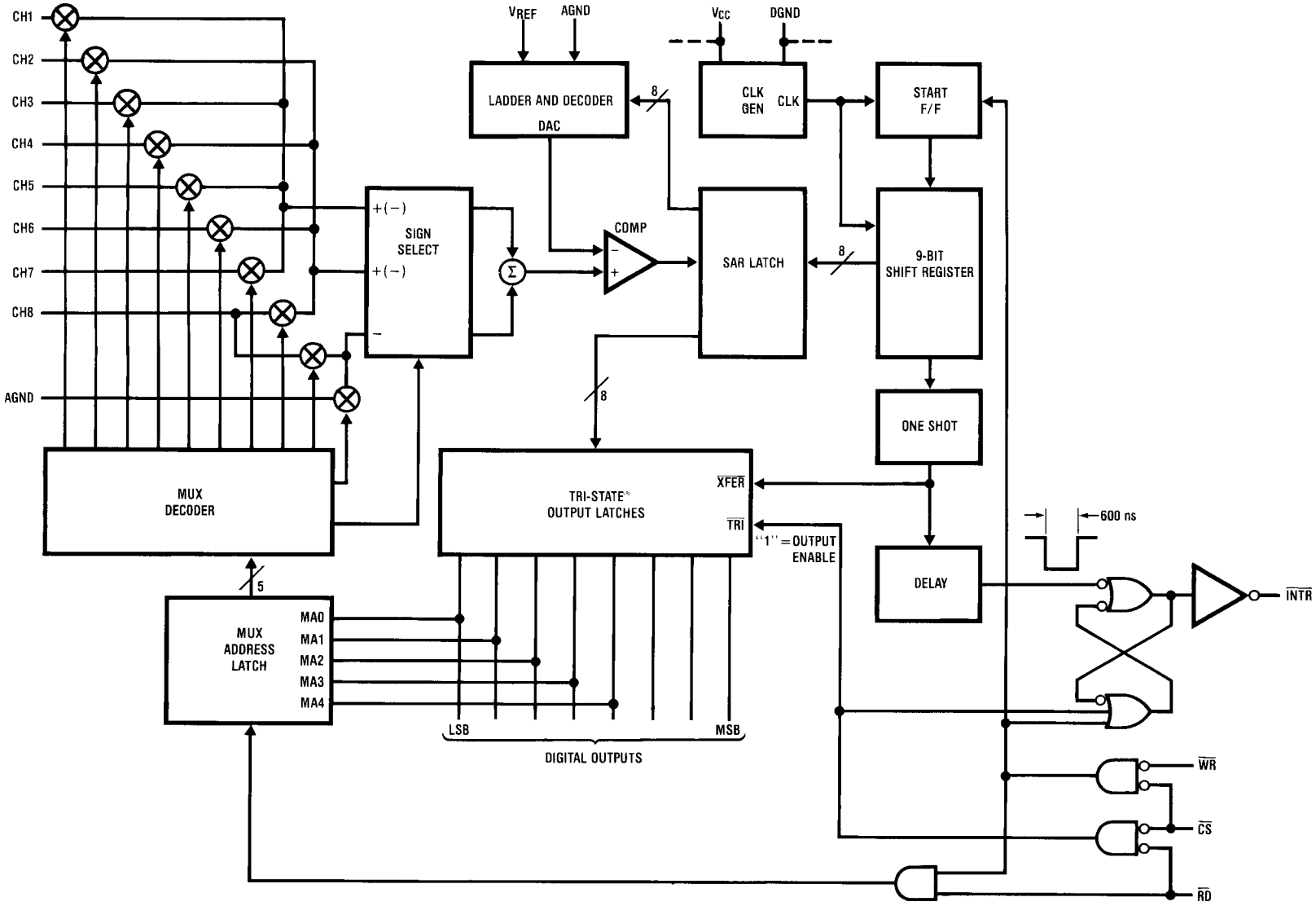
Read strobe must occur at least 600 ns after the assertion of interrupt to ensure reset of $\overline{INTR}$.

MA stands for MUX address.

Figure 11. Using the Previously Selected Channel Configuration and Starting a Conversion



ADC0848 Functional Block Diagram



Functional Description

The ADC0844 and ADC0848 contain a 4-channel and 8-channel analog input multiplexer (MUX) respectively. Each MUX can be configured into one of three modes of operation differential, pseudo-differential, and single ended. These modes are discussed in Applications Information. The specific mode is selected by loading the MUX address latch with the proper address (see Table 1 and Table 2). Inputs to the MUX address latch (MA0-MA4) are common with data bus lines (DB0-DB4) and are enabled when the $\overline{RD}$ line is high. A conversion is initiated via the $\overline{CS}$ and $\overline{WR}$ lines. If the data from a previous conversion is not read, the $\overline{INTR}$ line will be low. The falling edge of $\overline{WR}$ will reset the $\overline{INTR}$ line high and ready the A/D for a conversion cycle. The rising edge of $\overline{WR}$, with $\overline{RD}$ high, strobes the data on the MA0/DB0-MA4/DB4 inputs into the MUX address latch to select a new input configuration and start a conversion. If the $\overline{RD}$ line is held low during the entire low period of $\overline{WR}$ the previous MUX configuration is retained, and the data of the previous conversion is the output on lines DB0-DB7. After the conversion cycle ($t_C \leq 40$ µs), which is set by the internal clock frequency, the digital data is transferred to the output latch and the $\overline{INTR}$ is asserted low. Taking $\overline{CS}$ and $\overline{RD}$ low resets $\overline{INTR}$ output high and outputs the conversion result on the data lines (DB0-DB7).

APPLICATIONS INFORMATION

MULTIPLEXER CONFIGURATION

The design of these converters utilizes a sampled-data comparator structure which allows a differential analog input to be converted by a successive approximation routine.

The actual voltage converted is always the difference between an assigned “+” input terminal and a “−” input terminal. The polarity of each input terminal of the pair being converted indicates which line the converter expects to be the most positive. If the assigned “+” input is less than the “−” input the converter responds with an all zeros output code.

A unique input multiplexing scheme has been utilized to provide multiple analog channels. The input channels can be software configured into three modes: differential, single ended, or pseudo-differential. Figure 12 shows the three modes using the 4-channel MUX ADC0844. The eight inputs of the ADC0848 can also be configured in any of the three modes. In the differential mode, the ADC0844 channel inputs are grouped in pairs, CH1 with CH2 and CH3 with CH4. The polarity assignment of each channel in the pair is interchangeable. The single-ended mode has CH1–CH4 assigned as the positive input with the negative input being the analog ground (AGND) of the device. Finally, in the pseudo-differential mode CH1–CH3 are positive inputs referenced to CH4 which is now a pseudo-ground. This pseudo-ground input can be set to any potential within the input common-mode range of the converter. The analog signal conditioning required in transducer-based data acquisition systems is significantly simplified with this type of input flexibility. One converter package can now handle ground referenced inputs and true differential inputs as well as signals with some arbitrary reference voltage.

The analog input voltages for each channel can range from 50 mV below ground to 50 mV above V_{CC} (typically 5V) without degrading conversion accuracy.

Table 1. ADC0844 MUX ADDRESSING (1)

MUX Address				$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	Channel#					MUX Mode
MA3	MA2	MA1	MA0				CH1	CH2	CH3	CH4	AGND	
X	L	L	L	L		H	+	−				Differential
X	L	L	H	L	NP	H	−	+				
X	L	H	L	L		H			+	−		
X	L	H	H	L		H			−	+		
L	H	L	L	L		H	+				−	Single-Ended
L	H	L	H	L	NP	H		+			−	
L	H	H	L	L		H			+		−	
L	H	H	H	L		H				+	−	
H	H	L	L	L		H	+			−		Pseudo- Differential
H	H	L	H	L	NP	H		+		−		
H	H	H	L	L		H			+	−		
X	X	X	X	L	NP	L	Previous Channel Configuration					

(1) X = don't care, NP = negative pulse

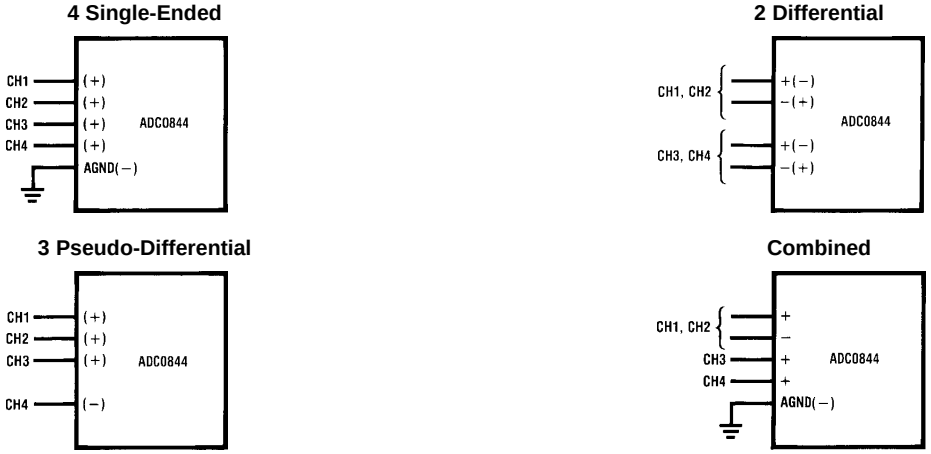


Figure 12. Analog Input Multiplexer Options

REFERENCE CONSIDERATIONS

The voltage applied to the reference input of these converters defines the voltage span of the analog input (the difference between $V_{IN(MAX)}$ and $V_{IN(MIN)}$) over which the 256 possible output codes apply. The devices can be used in either ratiometric applications or in systems requiring absolute accuracy. The reference pin must be connected to a voltage source capable of driving the minimum reference input resistance of 1.1 kΩ. This pin is the top of a resistor divider string used for the successive approximation conversion.

In a ratiometric system (Figure 13), the analog input voltage is proportional to the voltage used for the A/D reference. This voltage is typically the system power supply, so the V_{REF} pin can be tied to V_{CC}. This technique relaxes the stability requirements of the system reference as the analog input and A/D reference move together maintaining the same output code for a given input condition. For absolute accuracy (Figure 14), where the analog input varies between very specific voltage limits, the reference pin can be biased with a time and temperature stable voltage source. The LM385 and LM336 reference diodes are good low current devices to use with these converters.

The maximum value of the reference is limited to the V_{CC} supply voltage. The minimum value, however, can be quite small (see Typical Performance Characteristics) to allow direct conversions of transducer outputs providing less than a 5V output span. Particular care must be taken with regard to noise pickup, circuit layout and system error voltage sources when operating with a reduced span due to the increased sensitivity of the converter (1 LSB equals $V_{REF}/256$).

THE ANALOG INPUTS

Analog Differential Voltage Inputs and Common-Mode Rejection

The differential input of these converters actually reduces the effects of common-mode input noise, a signal common to both selected "+" and "−" inputs for a conversion (60 Hz is most typical). The time interval between sampling the "+" input and then the "−" inputs is ½ of a clock period. The change in the common-mode voltage during this short time interval can cause conversion errors. For a sinusoidal common-mode signal this error is:

$$V_{ERROR(MAX)} = V_{peak}\,(2\pi\, f_{CM}) \times 0.5 \times \left(\frac{t_C}{8}\right)$$

where

- f_{CM} is the frequency of the common-mode signal
- V_{peak} is its peak voltage value
- t_C is the conversion time

For a 60 Hz common-mode signal to generate a ¼ LSB error (≈5 mV) with the converter running at 40 µS, its peak value would have to be 5.43V. This large a common-mode signal is much greater than that generally found in a well designed data acquisition system.

Table 2. ADC0848 MUX Addressing(1)

MUX Address					$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	Channel									MUX Mode
MA4	MA3	MA2	MA1	MA0				CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8	AGND	
X	L	L	L	L	L		H	+	−								Differential
X	L	L	L	H	L		H	−	+								
X	L	L	H	L	L		H			+	−						
X	L	L	H	H	L	NP	H			−	+						
X	L	H	L	L	L		H					+	−				
X	L	H	L	H	L		H					−	+				
X	L	H	H	L	L		H							+	−		
X	L	H	H	H	L		H							−	+		
L	H	L	L	L	L		H	+								−	Single-Ended
L	H	L	L	H	L		H		+							−	
L	H	L	H	L	L		H			+						−	
L	H	L	H	H	L	NP	H				+					−	
L	H	H	L	L	L		H					+				−	
L	H	H	L	H	L		H						+			−	
L	H	H	H	L	L		H							+		−	
L	H	H	H	H	L		H								+	−	
H	H	L	L	L	L		H	+							−		Pseudo-Differential
H	H	L	L	H	L		H		+						−		
H	H	L	H	L	L		H			+					−		
H	H	L	H	H	L	NP	H				+				−		
H	H	H	L	L	L		H					+			−		
H	H	H	L	H	L		H						+		−		
H	H	H	H	L	L		H							+	−		
X	X	X	X	X	L		L	Previous Channel Configuration									

(1) X = don't care, NP = negative pulse

Input Current

Due to the sampling nature of the analog inputs, short duration spikes of current enter the "+" input and exit the "−" input at the clock edges during the actual conversion. These currents decay rapidly and do not cause errors as the internal comparator is strobed at the end of a clock period. Bypass capacitors at the inputs will average these currents and cause an effective DC current to flow through the output resistance of the analog signal source. Bypass capacitors should not be used if the source resistance is greater than 1 kΩ.

Input Source Resistance

The limitation of the input source resistance due to the DC leakage currents of the input multiplexer is important. A worst-case leakage current of ± 1 µA over temperature will create a 1 mV input error with a 1 kΩ source resistance. An op amp RC active low pass filter can provide both impedance buffering and noise filtering should a high impedance signal source be required.

OPTIONAL ADJUSTMENTS

Zero Error

The zero of the A/D does not require adjustment. If the minimum analog input voltage value, $V_{IN(MIN)}$, is not ground, a zero offset can be done. The converter can be made to output 0000 0000 digital code for this minimum input voltage by biasing any V_{IN} (−) input at this $V_{IN(MIN)}$ value. This is useful for either differential or pseudo-differential modes of input channel configuration.

The zero error of the A/D converter relates to the location of the first riser of the transfer function and can be measured by grounding the V^- input and applying a small magnitude positive voltage to the V^+ input. Zero error is the difference between actual DC input voltage which is necessary to just cause an output digital code transition from 0000 0000 to 0000 0001 and the ideal ½ LSB value (½ LSB=9.8 mV for V_{REF}=5.000 V_{DC}).

Full-Scale

The full-scale adjustment can be made by applying a differential input voltage which is 1 ½ LSB down from the desired analog full-scale voltage range and then adjusting the magnitude of the V_{REF} input for a digital output code changing from 1111 1110 to 1111 1111.

Adjusting for an Arbitrary Analog Input Voltage Range

If the analog zero voltage of the A/D is shifted away from ground (for example, to accommodate an analog input signal which does not go to ground), this new zero reference should be properly adjusted first. A V_{IN} (+) voltage which equals this desired zero reference plus ½ LSB (where the LSB is calculated for the desired analog span, 1 LSB = analog span/256) is applied to selected "+" input and the zero reference voltage at the corresponding "−" input should then be adjusted to just obtain the 00_{HEX} to 01_{HEX} code transition.

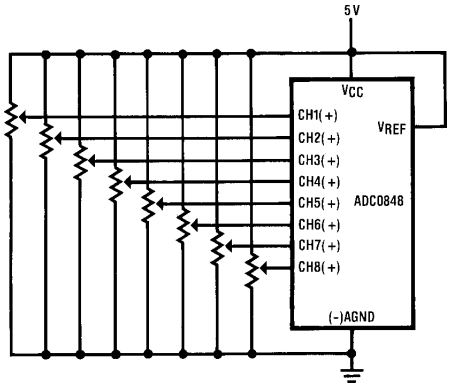


Figure 13. Referencing Examples - Ratiometric

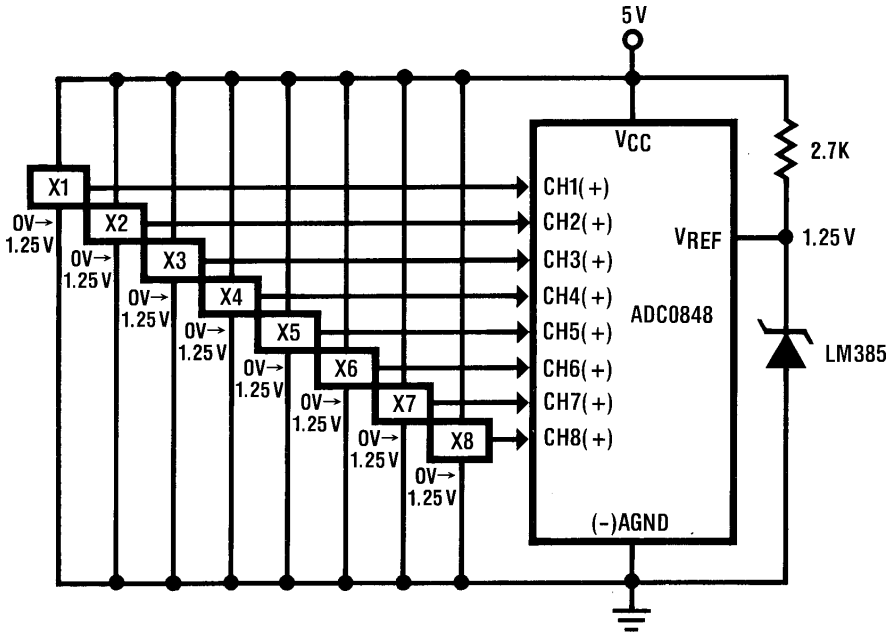


Figure 14. Referencing Examples - Absolute with a Reduced Span

The full-scale adjustment should be made [with the proper V_{IN} (−) voltage applied] by forcing a voltage to the V_{IN} (+) input which is given by:

$$V_{IN}(+)\ \text{fs adj} = V_{MAX} - 1.5\left[\frac{(V_{MAX} - V_{MIN})}{256}\right] \quad (1)$$

where

- V_{MAX} = the high end of the analog input range
- V_{MIN} = the low end (the offset zero) of the analog range. (Both are ground referenced.)

The V_{REF} (or V_{CC}) voltage is then adjusted to provide a code change from FE_{HEX} to FF_{HEX}. This completes the adjustment procedure.

For an example see the Zero-Shift and Span Adjust circuit below.

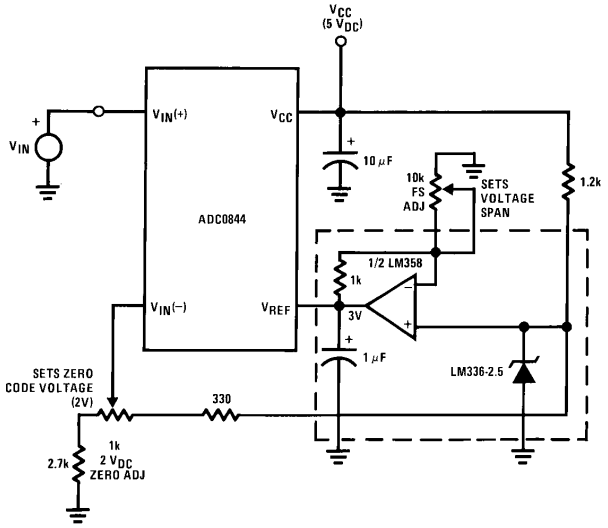


Figure 15. Zero-Shift and Span Adjust (2V ≤ V_{IN} ≤ 5V)

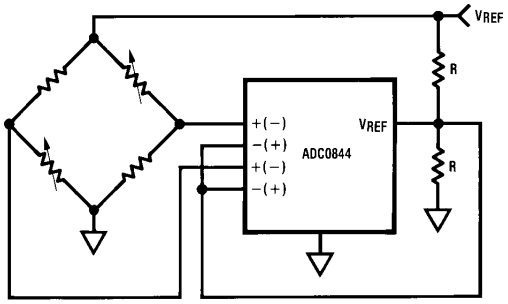


Figure 16. Differential Voltage Input 9-Bit A/D

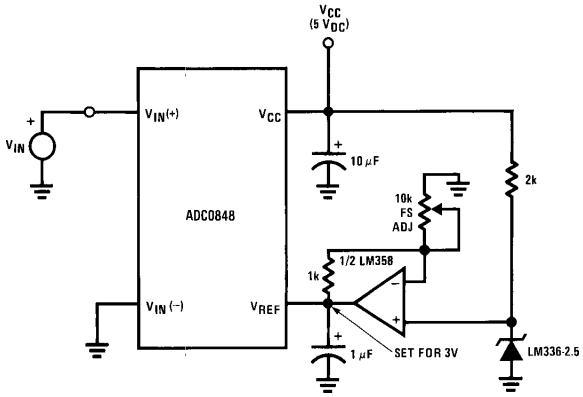


Figure 17. Span Adjust (0V ≤ V_{IN} ≤ 3V)

Diodes are 1N914

DO = all 1s if $V_{IN}(+) > V_{IN}(-)$
DO = all 0s if $V_{IN}(+) < V_{IN}(-)$

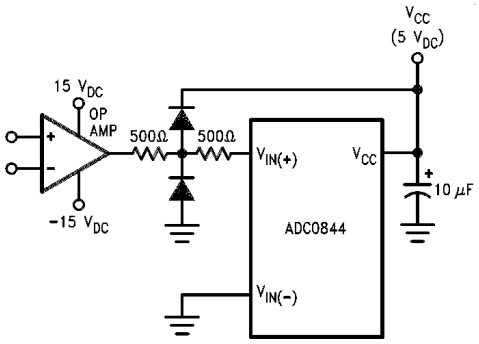


Figure 18. Protecting the Input

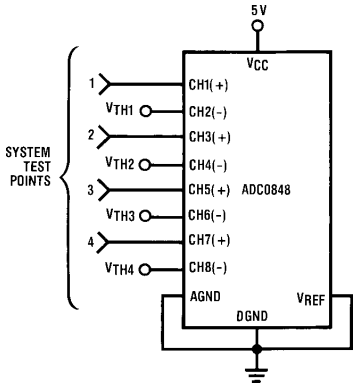


Figure 19. High Accuracy Comparators

* $V_{IN}(-) = 0.15\ V_{CC}$
15% of $V_{CC} \leq V_{XDR} \leq 85\%$ of V_{CC}

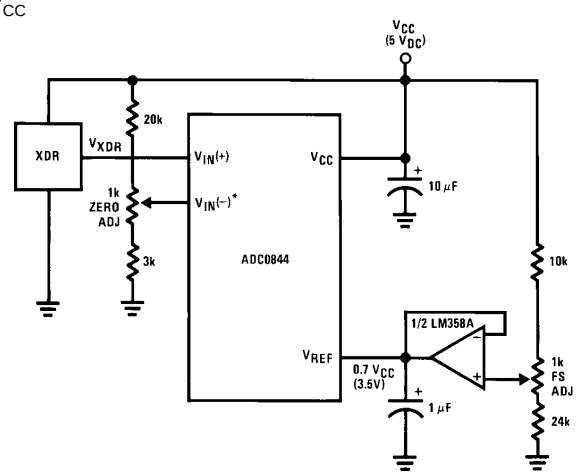
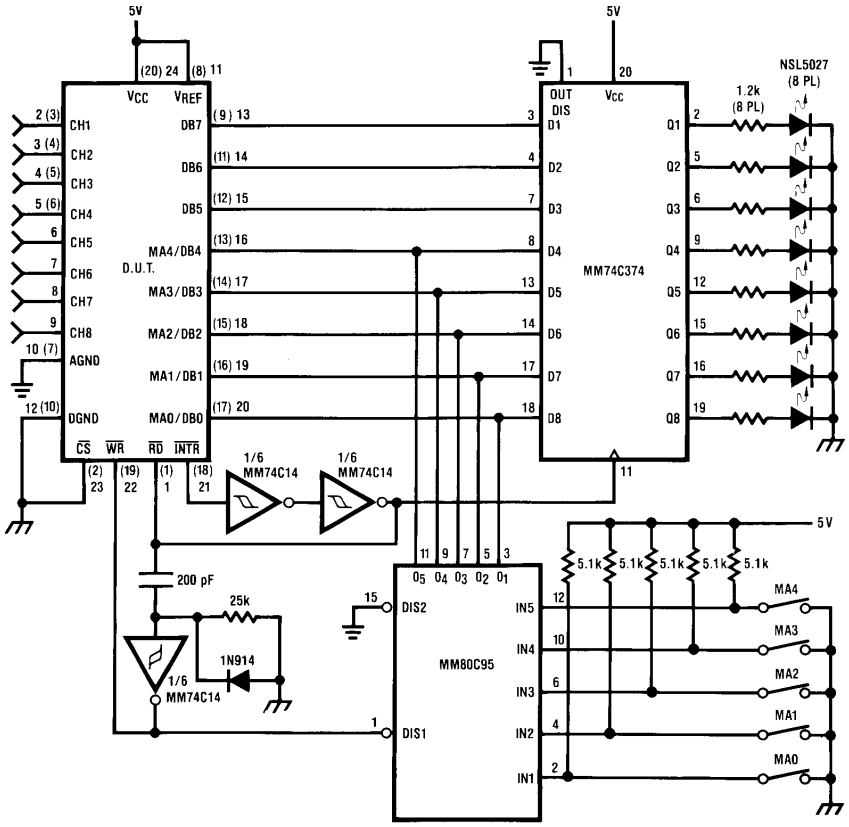
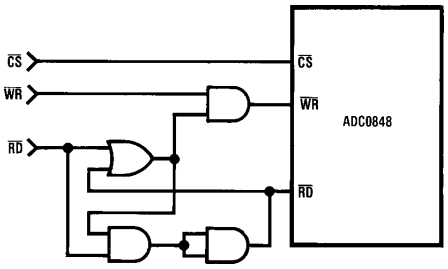


Figure 20. Operating with Automotive Ratiometric Transducers



Note: DUT pin numbers in parentheses are for ADC0844, others are for ADC0848.

Figure 21. A Stand Alone Circuit



$\overline{CS}$ •$\overline{WR}$ will update the channel configuration and start a conversion.
$\overline{CS}$ •$\overline{RD}$ will read the conversion data and start a new conversion without updating the channel configuration. Waiting for the end of this conversion is not necessary. A $\overline{CS}$ •$\overline{WR}$ can immediately follow the $\overline{CS}$•$\overline{RD}$.

Figure 22. Start a Conversion without Updating the Channel Configuration

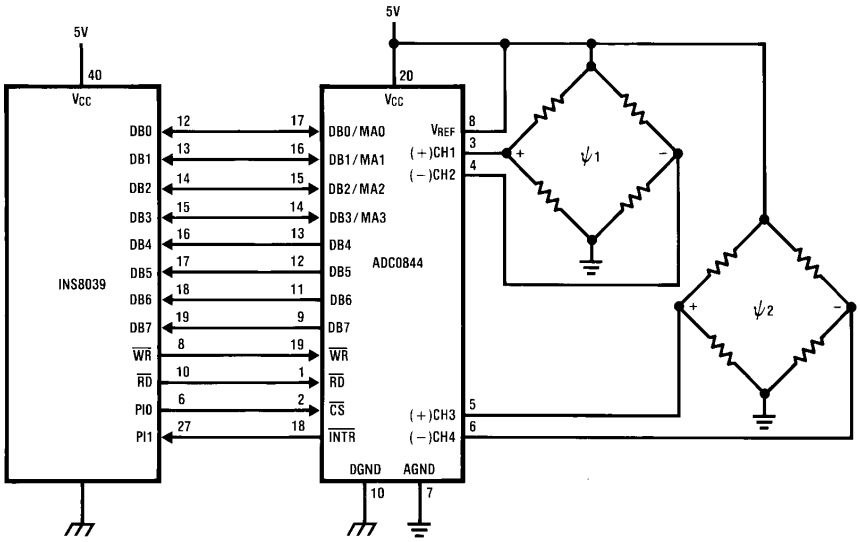


Figure 23. ADC0844—INS8039 Interface

Sample Program for ADC0844 - INS8039 Interface Converting Two Ratiometric Differential Signals

```
                          ORG    0H
0000   04 10              JMP    BEGIN            ;START PROGRAM AT ADDR 10
                          ORG    10H              ;MAIN PROGRAM
0010   B9 FF    BEGIN:    MOV    R1,#0FFH         ;LOAD R1 WITH AN UNUSED ADDR
                                                  ;LOCATION
0012   B8 20              MOV    R0,#20H          ;A/D DATA ADDRESS
0014   89 FF              ORL    P1,#0FFH         ;SET PORT 1 OUTPUTS HIGH
0016   23 00              MOV    A,00H            ;LOAD THE ACC WITH A/D MUX DATA
                                                  ;CH1 AND CH2 DIFFERENTIAL
0018   14 50              CALL   CONV             ;CALL THE CONVERSION SUBROUTINE
001A   23 02              MOV    A,#02H           ;LOAD THE ACC WITH A/D MUX DATA
                                                  ;CH3 AND CH4 DIFFERENTIAL
001C   18                INC    R0               ;INCREMENT THE A/D DATA ADDRESS
001D   14 50              CALL   CONV             ;CALL THE CONVERSION SUBROUTINE

                          ;CONTINUE MAIN PROGRAM

                          ;CONVERSION SUBROUTINE
                          ;ENTRY:ACC-A/D MUX DATA
                          ;EXIT:ACC-CONVERTED DATA

                          ORG    50H
0050   99 FE    CONV:     ANL    P1#0FEH          ;CHIP SELECT THE A/D
0052   91                MOVX   @R1,A            ;LOAD A/D MUX & START CONVERSION
0053   09       LOOP:     IN     A,P1             ;INPUT INTR STATE
0054   32 53              JB1    LOOP             ;IF INTR = 1 GOTO LOOP
0056   81                MOVX   A,@R1            ;IF INTR = 0 INPUT A/D DATA
0057   89 01              ORL    P1,&01H          ;CLEAR THE A/D CHIP SELECT
0059   A0                MOV    @R0,A            ;STORE THE A/D DATA
005A   83                RET                     ;RETURN TO MAIN PROGRAM
```

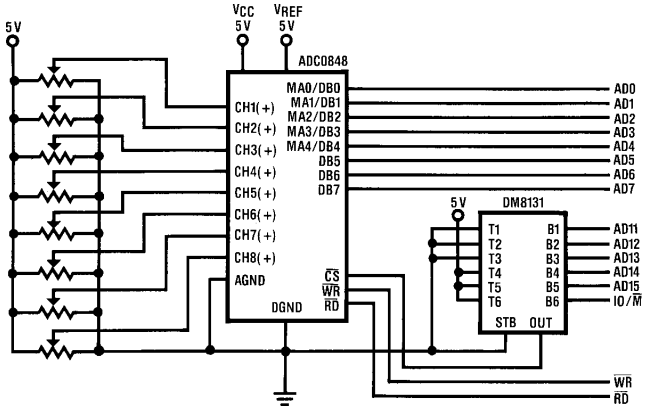


Figure 24. I/O Interface to NSC800

Sample Program for ADC0848 - NSC800 Interface

```
0008                NCONV    EQU    16
000F                DEL      EQU    15              ;DELAY 50 µSEC CONVERSION
001F                CS       EQU    1FH             ;THE BOARD ADDRESS
3C00                ADDTA    EQU    003CH           ;START OF RAM FOR A/D
                                                    ;DATA
0000'   08 09 0A 0B MUXDTA:  DB     08H,09H,0AH,0BH ;MUX DATA
0004'   0C 0D 0E 0F         DB     0CH,0DH,0EH,0FH
0008'   0E 1F       START:   LD     C,CS
000A'   06 16                LD     B,NCONV
000C'   21 0000'             LD     HL,MUXDTA
000F'   11 003C              LD     DE,ADDTA
0012'   ED A3       STCONV:  OUTI                   ;LOAD A/D'S MUX DATA
                                                    ;AND START A CONVERSION
0014'   EB                   EX     DE,HL           ;HL=RAM ADDRESS FOR THE
                                                    ;A/D DATA
0015'   3E 0F                LD     A,DEL
0017'   3D          WAIT:    DEC    A               ;WAIT 50 µSEC FOR THE
0018'   C2 0013'             JP     NZ,WAIT         ;CONVERSION TO FINISH
001B'   ED A2                INI                    ;STORE THE A/D'S DATA
                                                    ;CONVERTED ALL INPUTS?
001D'   EB                   EX     DE,HL
001E'   C2 000E'             JP     NZ,STCONV       ;IF NOT GOTO STCONV

                             END
```

Note: This routine sequentially programs the MUX data latch in the signal-ended mode. For CH1-CH8 a conversion is started, then a 50 µs wait for the A/D to complete a conversion and the data is stored at address ADDTA for CH1, ADDTA + 1 for CH2, etc.

REVISION HISTORY

Changes from Revision C (March 2013) to Revision D	Page
• Changed layout of National Data Sheet to TI format	17

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADC0844CCN/NOPB	ACTIVE	PDIP	NFH	20	18	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	0 to 70	ADC0844CCN	Samples
ADC0848BCV	NRND	PLCC	FN	28	35	TBD	Call TI	Call TI	-40 to 85	ADC0848 BCV	
ADC0848BCV/NOPB	ACTIVE	PLCC	FN	28	35	Green (RoHS & no Sb/Br)	CU SN	Level-2A-245C-4 WEEK	-40 to 85	ADC0848 BCV	Samples
ADC0848BCVX/NOPB	ACTIVE	PLCC	FN	28	750	Green (RoHS & no Sb/Br)	CU SN	Level-2A-245C-4 WEEK	-40 to 85	ADC0848 BCV	Samples
ADC0848CCN	NRND	PDIP	NAM	24	15	TBD	Call TI	Call TI	-40 to 85	ADC0848CCN	
ADC0848CCV	NRND	PLCC	FN	28	35	TBD	Call TI	Call TI	-40 to 85	ADC0848 CCV	
ADC0848CCV/NOPB	ACTIVE	PLCC	FN	28	35	Green (RoHS & no Sb/Br)	CU SN	Level-2A-245C-4 WEEK	-40 to 85	ADC0848 CCV	Samples
ADC0848CCVX	NRND	PLCC	FN	28	750	TBD	Call TI	Call TI	-40 to 85	ADC0848 CCV	
ADC0848CCVX/NOPB	ACTIVE	PLCC	FN	28	750	Green (RoHS & no Sb/Br)	CU SN	Level-2A-245C-4 WEEK	-40 to 85	ADC0848 CCV	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

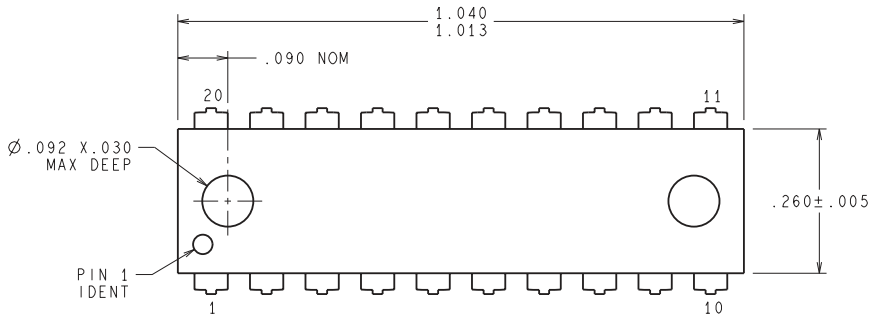
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

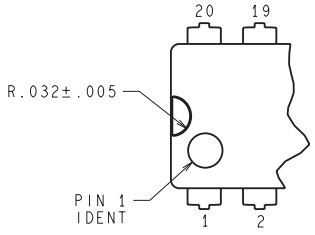
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

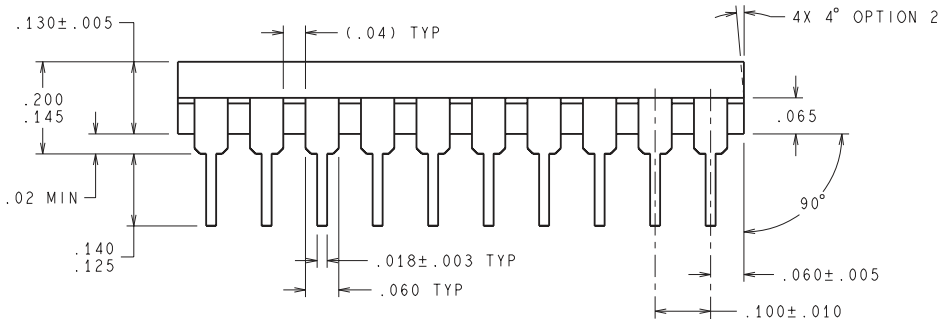
NFH0020A

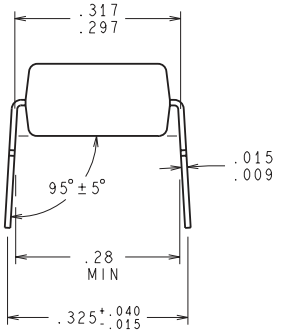


OPTION 1



OPTION 2

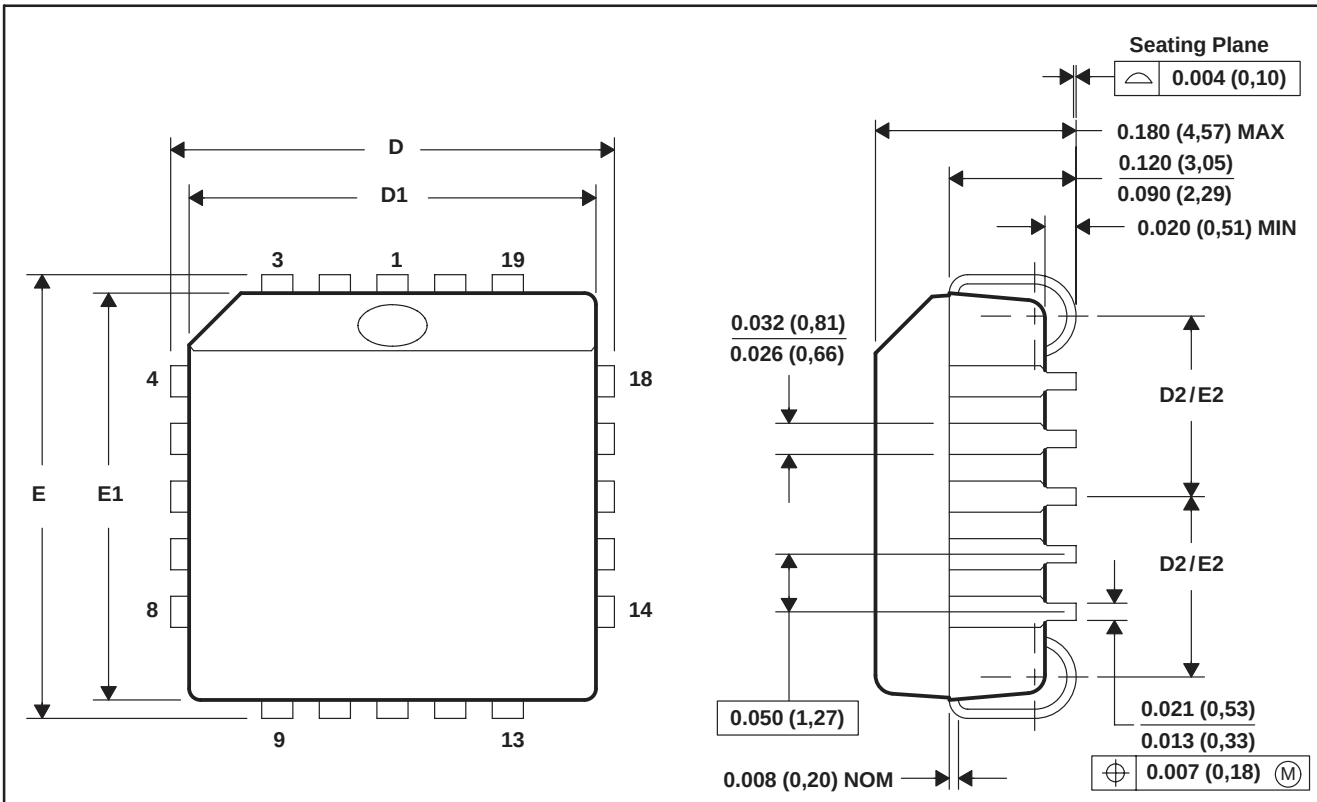




N20A (Rev G)

FN (S-PQCC-J)** **PLASTIC J-LEADED CHIP CARRIER**

20 PIN SHOWN

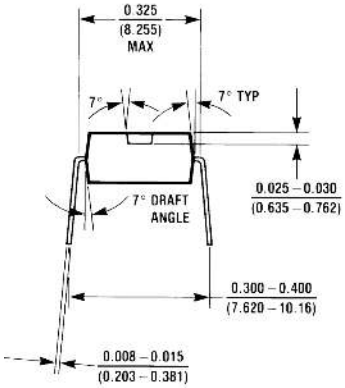


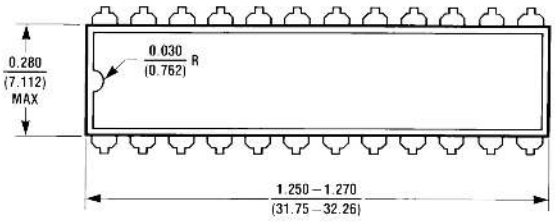
NO. OF PINS **	D/E		D1/E1		D2/E2	
	MIN	MAX	MIN	MAX	MIN	MAX
20	0.385 (9,78)	0.395 (10,03)	0.350 (8,89)	0.356 (9,04)	0.141 (3,58)	0.169 (4,29)
28	0.485 (12,32)	0.495 (12,57)	0.450 (11,43)	0.456 (11,58)	0.191 (4,85)	0.219 (5,56)
44	0.685 (17,40)	0.695 (17,65)	0.650 (16,51)	0.656 (16,66)	0.291 (7,39)	0.319 (8,10)
52	0.785 (19,94)	0.795 (20,19)	0.750 (19,05)	0.756 (19,20)	0.341 (8,66)	0.369 (9,37)
68	0.985 (25,02)	0.995 (25,27)	0.950 (24,13)	0.958 (24,33)	0.441 (11,20)	0.469 (11,91)
84	1.185 (30,10)	1.195 (30,35)	1.150 (29,21)	1.158 (29,41)	0.541 (13,74)	0.569 (14,45)

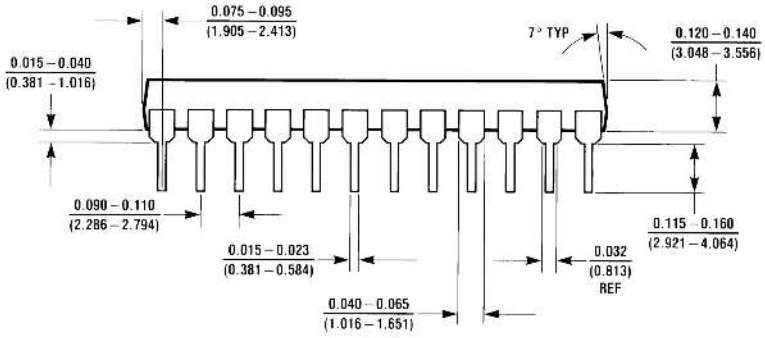
4040005/B 03/95

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-018

NAM0024D







N24D (Rev B)

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