CS4353

3.3 V Stereo Audio DAC with 2 V_{RMS} Line Output

Features

- Multi-bit Delta-Sigma Modulator
- 106 dB A-wt Dynamic Range
- -93 dB THD+N
- Single-ended Ground Centered Analog Architecture
  - No DC-blocking Capacitors Required
  - Integrated Step-up/Inverting Charge Pump
  - Filtered Line-level Outputs
  - Selectable 1 or 2 V_{RMS} Full-scale Output
- Low Clock-jitter Sensitivity
- Low-latency Digital Filtering
- Supports Sample Rates up to 192 kHz
- 24-bit Resolution
- +3.3 V Charge Pump and Core Logic, +3.3 V Analog, and +0.9 to 3.3 V Interface Power Supplies
- Low Power Consumption
- 24-pin QFN, Lead-free Assembly

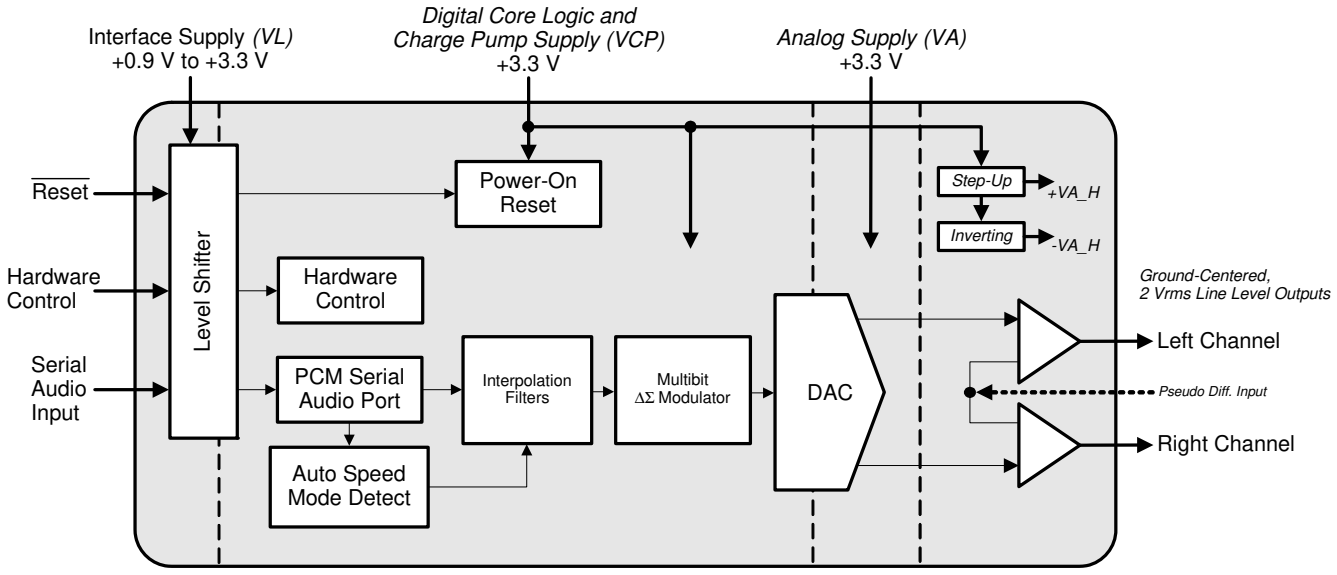
Description

The CS4353 is a complete stereo digital-to-analog system including digital interpolation, fifth-order multi-bit delta-sigma digital-to-analog conversion, digital de-emphasis, analog filtering, and on-chip 2 V_{RMS} line-level driver from a 3.3 V supply.

The advantages of this architecture include ideal differential linearity, no distortion mechanisms due to resistor matching errors, no linearity drift over time and temperature, high tolerance to clock jitter, and a minimal set of external components.

The CS4353 is available in a 24-pin QFN package in Commercial (-40°C to +85°C) grade. The CDB4353 Customer Demonstration Board is also available for device evaluation and implementation suggestions. Please see "Ordering Information" on page 25 for complete details.

These features are ideal for cost-sensitive, 2-channel audio systems including video game consoles, DVD players and recorders, A/V receivers, set-top boxes, digital TVs, mini-component systems, and mixing consoles.



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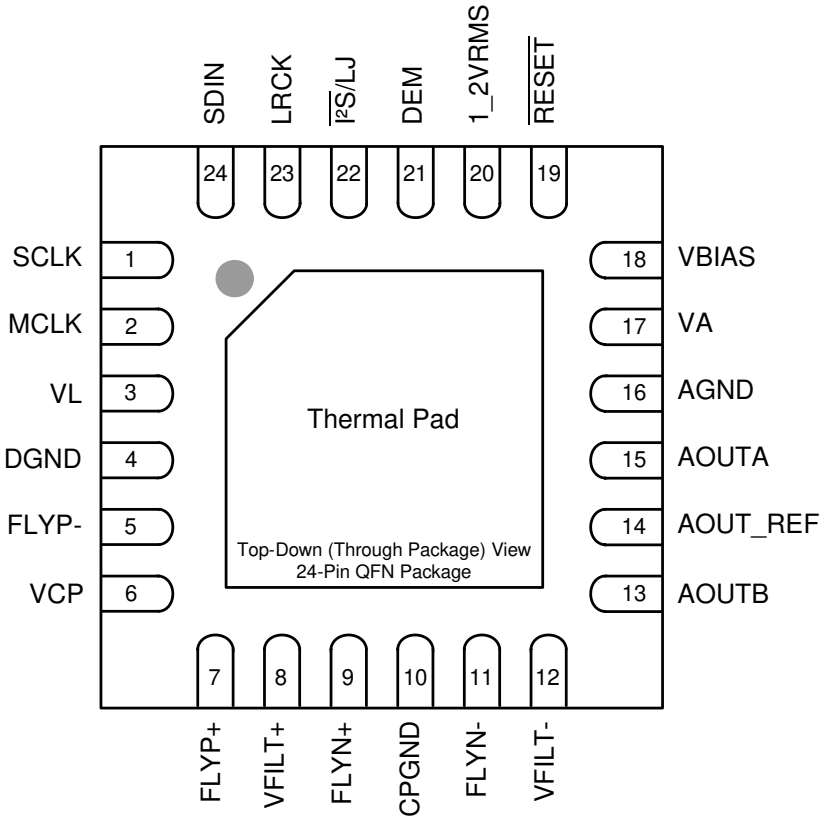
1. PIN DESCRIPTIONS



Pin Name	Pin #	Pin Description
SCLK	1	**Serial Clock** (*Input*) - Serial clock for the serial audio interface.
MCLK	2	**Master Clock** (*Input*) - Clock source for the delta-sigma modulator and digital filters.
VL	3	**Serial Audio Interface Power** (*Input*) **-** Positive power for the serial audio interface
DGND	4	**Digital Ground** (*Input*) - Ground reference for the digital section.
FLYP+ FLYP-	7 5	**Step-up Charge Pump Cap Positive/Negative Nodes** *(Output)* - Positive and Negative nodes for the step-up charge pump's flying capacitor.
VCP	6	**Charge Pump and Digital Core Logic Power** (*Input*) **-** Positive power supply for the step-up and inverting charge pumps as well as the digital core logic sections.
VFILT+	8	**Step-up Charge Pump Filter Connection** *(Output)* - Power supply from the step-up charge pump that provides the positive rail for the output amplifiers
FLYN+ FLYN-	9 11	**Inverting Charge Pump Cap Positive/Negative Nodes** *(Output)* - Positive and Negative nodes for the inverting charge pump's flying capacitor.
CPGND	10	**Charge Pump Ground** (*Input*) - Ground reference for the Charge Pump section.
VFILT-	12	**Inverting Charge Pump Filter Connection** *(Output)* - Power supply from the inverting charge pump that provides the negative rail for the output amplifiers.
AOUTB AOUTA	13 15	**Analog Outputs** (*Output*) - The full-scale analog line output level is specified in the Analog Characteristics table.
AOUT_REF	14	**Pseudo Diff. Analog Output Reference** (*Input*) **-** Ground reference for the analog output amplifiers. This pin must be at the same nominal DC voltage as the AGND pin.
AGND	16	**Analog Ground** (*Input*) - Ground reference for the low voltage analog section.

VA	17	**Low Voltage Analog Power** (*Input*) **-** Positive power supply for the analog section.
VBIAS	18	**Positive Voltage Reference** (*Output*) **-** Positive reference voltage for the internal DAC.
$\overline{\text{RESET}}$	19	**Reset** (*Input*) - Optional connection for an external reset control. The device enters a powered-down state when this pin is set low (GND) OR when the VCP supply falls below the V_{off} threshold (see See "Internal Power-on Reset Threshold Voltages" on page 10.). This pin should be set high (VL) during normal operation.
1_2VRMS	20	**1 or 2 V_{RMS} Select** (*Input*) - Selects the analog output full-scale voltage. Setting this pin low (GND) selects 1 V_{RMS}, while setting it high (VL) selects 2 V_{RMS}.
DEM	21	**De-emphasis** (*Input*) - Selects the standard 50 µs/15 µs digital de-emphasis filter response for 44.1 kHz sample rates when enabled.
$\overline{\text{I}^2\text{S}}$/LJ	22	**Digital Interface Format** (*Input*) - Selects the serial audio interface format. Setting this pin low (GND) selects I²S, while setting it high (VL) selects Left-Justified.
LRCK	23	**Left** / **Right Clock** (*Input*) - Determines which channel, Left or Right, is currently active on the serial audio data line.
SDIN	24	**Serial Audio Data Input** (*Input*) - Input for two's complement serial audio data.
Thermal Pad	-	**Thermal Relief Pad** - This pad may be soldered to the board, however it MUST be electrically isolated from all board connections.

2. CHARACTERISTICS AND SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

AGND = DNGD = CPGND = 0 V; all voltages with respect to ground.

Parameters		Symbol	Min	Typ	Max	Units
DC Power Supply	Charge Pump and Digital Core power (Note 1)	VCP	3.13	3.3	3.47	V
	Low Voltage Analog power (Note 1)	VA	3.13	3.3	3.47	V
	Interface power	VL	0.85	0.9 to 3.3	3.47	V
Ambient Operating Temperature (Power Applied)		T_A	-40	-	+85	°C

Notes: 1. VCP and VA must be supplied with the same nominal voltage. Additional current draw will occur if the supply voltages applied to VCP and VA differ by more than 0.5 V.

ABSOLUTE MAXIMUM RATINGS

AGND = DNGD = CPGND = 0 V; all voltages with respect to ground.

Parameters		Symbol	Min	Max	Units
DC Power Supply	Charge Pump and Digital Core Logic Power	VCP	-0.3	3.63	V
	Low Voltage Analog Power	VA	-0.3	3.63	V
	Supply Voltage Difference	|VCP - VA|	-	0.5	V
	Interface Power	VL	-0.3	3.63	V
Input Current, Any Pin Except Supplies		I_{in}	-	±10	mA
Digital Input Voltage	Digital Interface	V_{IN-L}	-0.3	V_L+ 0.4	V
Analog Input Voltage	AOUT_REF	V_{IN-A}	-0.3	0.5	V
Ambient Operating Temperature (Power Applied)		T_A	-55	+125	°C
Storage Temperature		T_{stg}	-65	+150	°C

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

DAC ANALOG CHARACTERISTICS

Test conditions (unless otherwise specified): T_A = 25 °C; VCP = VA = 3.3 V; AOUT_REF = AGND = DGND = CPGND = 0 V; VBIAS, VFILT+/-, and FLYP/N+/- capacitors as shown in Figure 3 on page 12; input test signal is a 997 Hz sine wave at 0 dBFS; measurement bandwidth 10 Hz to 20 kHz.

Parameter			Symbol	1_2VRMS = 0 Min	1_2VRMS = 0 Typ	1_2VRMS = 0 Max	1_2VRMS = 1 Min	1_2VRMS = 1 Typ	1_2VRMS = 1 Max	Unit
Dynamic Performance, Fs = 48, 96, and 192 kHz (Notes 2, 3, 4)										
Dynamic Range	24-bit	A-Weighted		94	100	-	100	106	-	dB
		unweighted		91	97	-	97	103	-	dB
	16-bit	A-Weighted		-	92	-	-	98	-	dB
		unweighted		-	89	-	-	95	-	dB
Total Harmonic Distortion + Noise				-			-			
	24-bit	0 dB		-	-93	-87	-	-93	-87	dB
		-20 dB		-	-77	-71	-	-83	-77	dB
		-60 dB	THD+N	-	-37	-31	-	-43	-37	dB
	16-bit	0 dB		-	-93	-	-	-93	-	dB
		-20 dB		-	-75	-	-	-75	-	dB
		-60 dB		-	-29	-	-	-35	-	dB
Idle Channel Noise / Signal-to-Noise Ratio		(A-wt)		-	100	-	-	106	-	dB
Interchannel Isolation		(1 kHz)		-	115	-	-	115	-	dB
Analog Output (Note 5)										
Full Scale AOUTx Output Voltage		(Notes 4, 6, 7)		1.02 2.89	1.08 3.05	1.13 3.20	2.04 5.78	2.15 6.09	2.26 6.40	V_{RMS} V_{pp}
Max Current Draw from an AOUTx Pin			I_{OUTmax}	-	575	-	-	575	-	µA
Interchannel Gain Mismatch				-	0.1	-	-	0.1	-	dB
Output Offset				-	±5	±8	-	±5	±8	mV
Gain Drift				-	100	-	-	100	-	ppm/°C
Output Impedance			Z_{OUT}	-	100	-	-	100	-	Ω
AC-Load Resistance			R_L	5	-	-	5	-	-	kΩ
Load Capacitance			C_L	-	-	1000	-	-	1000	pF
AOUT_REF Rejection		(Notes 8, 9)	AOR	-	40	-	-	40	-	dB
Analog Reference Input										
AOUT_REF Input Voltage		(Note 10)		-	-	0.2	-	-	0.2	Vpp

Notes: 2. Measured at the output of the external LPF on AOUTx as shown in Figure 3 on page 12.

3. One-half LSB of triangular PDF dither is added to data.
4. Measured with the specified minimum AC-Load Resistance present on the AOUTx pins.
5. Measured between the AOUTx and AOUT_REF pins.
6. External impedance between the AOUTx pin and the load will lower the voltage delivered to the load.
7. V_{PP} is the controlling specification. V_{RMS} specification valid for sine wave signals only.

   Note that for sine wave signals: $V_{RMS} = \frac{V_{pp}}{2\sqrt{2}}$
8. Measured with AOUT_REF connected directly to ground. External impedance between AOUT_REF and ground will lower the AOUT_REF rejection.

9. SDIN = 0. AOUT_REF input test signal is a 60 Hz, 50 mVpp sine wave. Measured by applying the test signal into the AOUT_REF pin and measuring the resulting output amplitude on the AOUTx pin. Specification calculated by: $AOR_{dB} = 20 \cdot log_{10}\left(\frac{AOUT\_REF}{AOUT\_REF - AOUTx}\right)$

10. Applying a DC voltage on the AOUT_REF pin will cause a DC offset on the DAC output. See Section 4.1.3 for more information.

COMBINED INTERPOLATION & ON-CHIP ANALOG FILTER RESPONSE

The filter characteristics have been normalized to the sample rate (Fs) and can be referenced to the desired sample rate by multiplying the given characteristic by Fs.

Parameter		Min	Typ	Max	Unit
Single-Speed Mode - 48 kHz					
Passband (Note 11)	to -0.01 dB corner to -3 dB corner	0 0	- -	.454 .499	Fs Fs
Frequency Response 10 Hz to 20 kHz		-0.01	-	+0.01	dB
StopBand		0.547	-	-	Fs
StopBand Attenuation	(Note 12)	102	-	-	dB
Total Group Delay (Fs = Sample Rate)		-	9.4/Fs	-	s
Intra-channel Phase Deviation		-	-	±0.56/Fs	s
Inter-channel Phase Deviation		-	-	0	s
De-emphasis Error (Note 13)(Relative to 1 kHz)	Fs = 44.1 kHz	-	-	±0.14	dB
Double-Speed Mode - 96 kHz					
Passband (Note 11)	to -0.01 dB corner to -3 dB corner	0 0	- -	.430 .499	Fs Fs
Frequency Response 10 Hz to 20 kHz		-0.01	-	0.01	dB
StopBand		.583	-	-	Fs
StopBand Attenuation	(Note 12)	80	-	-	dB
Total Group Delay (Fs = Sample Rate)		-	4.6/Fs	-	s
Intra-channel Phase Deviation		-	-	±0.03/Fs	s
Inter-channel Phase Deviation		-	-	0	s
Quad-Speed Mode - 192 kHz					
Passband (Note 11)	to -0.01 dB corner to -3 dB corner	0 0	- -	.105 .490	Fs Fs
Frequency Response 10 Hz to 20 kHz		-0.01	-	0.01	dB
StopBand		.635	-	-	Fs
StopBand Attenuation	(Note 12)	90	-	-	dB
Total Group Delay (Fs = Sample Rate)		-	4.7/Fs	-	s
High-Pass Filter Characteristics					
Passband (Note 11)	to -0.05 dB corner to -3 dB corner	9.00×10^{-5} 9.74×10^{-6}	- -	- -	Fs Fs
Passband Ripple		-	-	0.01	dB
Phase Deviation @ 20 Hz		-	-	1.34	Deg
Filter Settling Time (input signal goes to 95% of its final value)		-	5×10^{4}/Fs	-	s

Notes: 11. Response is clock-dependent and will scale with Fs.

12. For Single- and Double-Speed Mode, the Measurement Bandwidth is from stopband to 3 Fs. For Quad-Speed Mode, the Measurement Bandwidth is from stopband to 1.34 Fs.

13. De-emphasis is available only in Single-Speed Mode.

14. Amplitude vs. Frequency plots of this data are available in "Digital Filter Response Plots" on page 21.

SWITCHING SPECIFICATIONS - SERIAL AUDIO INTERFACE

Parameters		Symbol	Min	Max	Units
MCLK Frequency			2.048	51.2	MHz
MCLK Duty Cycle			45	55	%
Input Sample Rate (Auto selection)	Single-Speed Mode	Fs	8	54	kHz
	Double-Speed Mode	Fs	84	108	kHz
	Quad-Speed Mode	Fs	170	216	kHz
LRCK Duty Cycle			40	60	%
SCLK Pulse Width Low		t_{sclkl}	20	-	ns
SCLK Pulse Width High		t_{sclkh}	20	-	ns
SCLK Period	Single-Speed Mode		$\frac{1}{(128)Fs}$	-	s
	Double-Speed Mode		$\frac{1}{(64)Fs}$	-	s
	Quad-Speed Mode		$\frac{1}{(64)Fs}$	-	s
SCLK rising to LRCK edge delay		t_{slrd}	20	-	ns
SCLK rising to LRCK edge setup time		t_{slrs}	20	-	ns
SDIN valid to SCLK rising setup time		t_{sdlrs}	20	-	ns
SCLK rising to SDIN hold time		t_{sdh}	20	-	ns

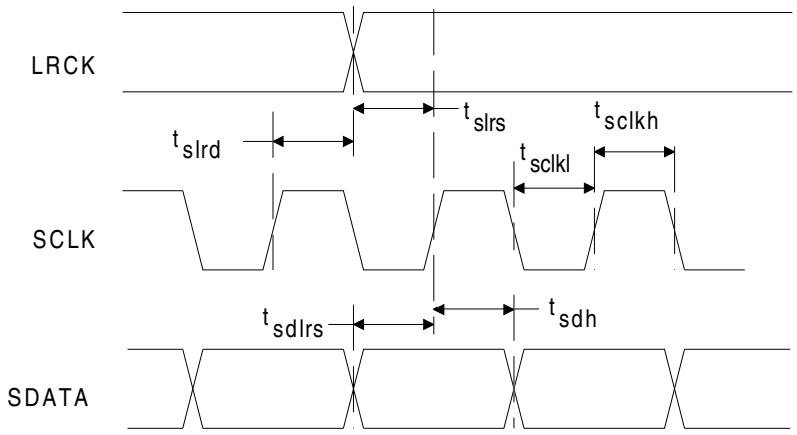


Figure 1. Serial Input Timing

DIGITAL INTERFACE CHARACTERISTICS

Test conditions (unless otherwise specified): AGND = DGND = CPGND = 0 V; all voltages with respect to ground.

Parameters		Symbol	Min	Typ	Max	Units
High-Level Input Voltage	1.2 V < VL ≤ 3.3 V	V_{IH}	0.7xVL	-	-	V
	0.9 V ≤ VL ≤ 1.2 V	V_{IH}	0.9xVL	-	-	V
Low-Level Input Voltage	1.2 V < VL ≤ 3.3 V	V_{IL}	-	-	0.3xVL	V
	0.9 V ≤ VL ≤ 1.2 V	V_{IL}	-	-	0.1xVL	V
Input Leakage Current		I_{in}	-	-	±10	µA
Input Capacitance			-	8	-	pF

INTERNAL POWER-ON RESET THRESHOLD VOLTAGES

Test conditions (unless otherwise specified): AGND = DGND = CPGND = 0 V; all voltages with respect to ground.

Parameters	Symbol	Min	Typ	Max	Units
Internal Reset Asserted at Power-On	V_{on1}	-	1.00	-	V
Internal Reset Released at Power-On	V_{on2}	-	2.36	-	V
Internal Reset Asserted at Power-Off	V_{off}	-	2.22	-	V

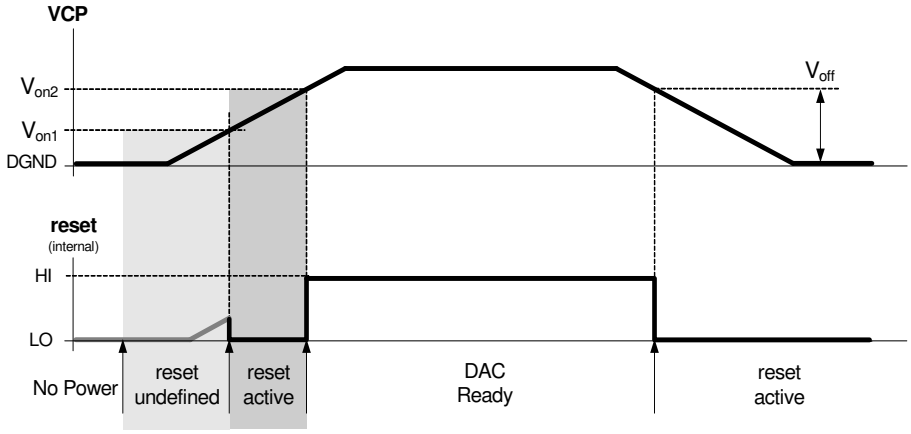


Figure 2. Power-on Reset Threshold Sequence

DC ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise specified): VCP = VA = VL = 3.3 V; AGND = DGND = CPGND = 0 V; SDIN = 0; all voltages with respect to ground.

Parameters		Symbol	Min	Typ	Max	Units
Power Supplies						
Power Supply Current (Note 15)						
	Normal Operation	I_{VCP}	-	36	43	mA
		I_{VA}	-	2.4	3	mA
		I_{VL}	-	0.1	0.2	mA
	Power-Down, All Supplies (Note 16)	I_{PD}	-	65	-	µA
Power Dissipation (All Supplies) (Note 15)	Normal Operation, 1_2VRMS = 0		-	127	152	mW
	Power-Down (Note 16)		-	1	-	mW
Power Supply Rejection Ratio (Note 17)	(1 kHz)	PSRR	-	60	-	dB
	(60 Hz)		-	60	-	dB
DC Output Voltages						
Pin Voltage	FLYP+ to FLYP-		-	3.3	-	V
	VFILT+ to GND (Note 18)		-	6.6	-	V
	FLYN+ to FLYN-		-	6.6	-	V
	GND to VFILT- (Note 18)		-	6.6	-	V
	VA to VBIAS		-	2.1	-	V

Notes: 15. Current consumption increases with increasing sample rate and increasing MCLK frequency. Typical values are based on Fs = 48 kHz and MCLK = 12.288 MHz. Maximum values are based on highest sample rate and highest MCLK frequency; see Switching Specifications - Serial Audio Interface. Variance between speed modes is small.

16. Power-down is defined as $\overline{\text{RESET}}$ pin = Low with all clock and data lines held static low. All digital inputs have a weak pull-down (approximately 50 kΩ) which is only present during reset. Opposing this pull-down will slightly increase the power-down current.

17. Valid with the recommended capacitor value on VBIAS as shown in the typical connection diagram in Section 3.

18. Typical voltage shown for “Initialization State”, see Section 4.8. Typical voltage may be up to 1.5 V lower during normal operation.

2.1 Digital I/O Pin Characteristics

Input and output levels and associated power supply voltage are shown in Table 1. Logic levels should not exceed the corresponding power supply voltage.

Pin Name	Power Supply	I/O	Driver	Receiver
$\overline{\text{RESET}}$	VL	Input	-	0.9 V - 3.3 V, with Hysteresis
MCLK		Input	-	0.9 V - 3.3 V
LRCK		Input	-	0.9 V - 3.3 V
SCLK		Input	-	0.9 V - 3.3 V
SDIN		Input	-	0.9 V - 3.3 V
DEM		Input	-	0.9 V - 3.3 V
$\overline{\text{I²S}}$/LJ		Input	-	0.9 V - 3.3 V
1_2VRMS		Input	-	0.9 V - 3.3 V

Table 1. Digital I/O Pin Characteristics

3. TYPICAL CONNECTION DIAGRAM

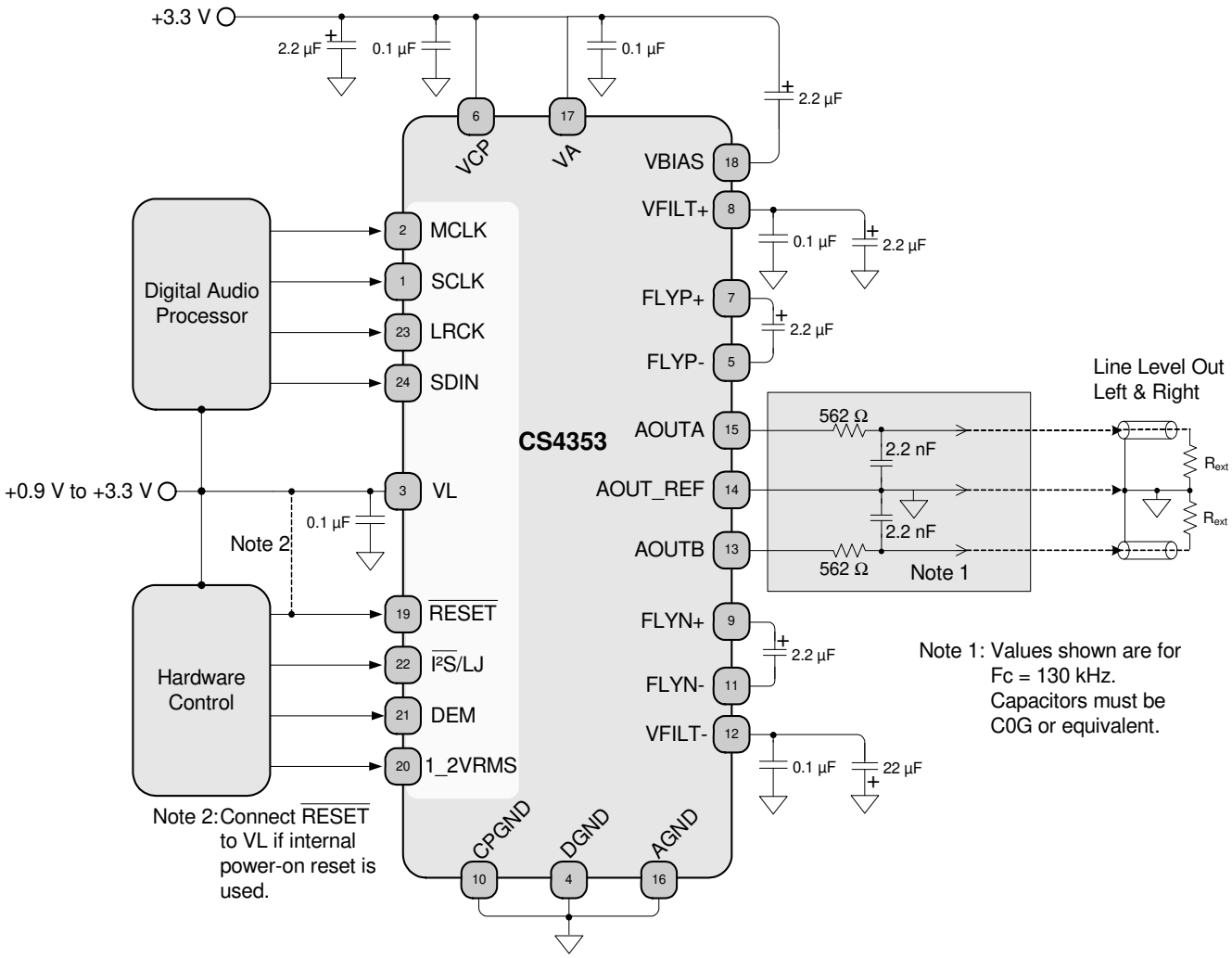


Figure 3. Typical Connection Diagram

4. APPLICATIONS

4.1 Line Outputs

4.1.1 Ground-centered Outputs

An on-chip charge pump creates both positive and negative high-voltage supplies, which allows the full-scale output swing to be centered around ground. This eliminates the need for large DC-blocking capacitors which create audible pops at power-on, allows the CS4353 to deliver a larger full-scale output at lower supply voltages, and provides improved bandwidth frequency response.

4.1.2 Full-scale Output Amplitude Control

The full-scale output voltage amplitude is selected via the 1_2VRMS pin. When the pin is connected to VL, the full-scale output voltage at the AOUTx pins is approximately 2 V_{RMS}. When the pin is connected to GND, the full-scale output voltage at the AOUTx pins is approximately 1 V_{RMS}. Additional impedance between the AOUTx pin and the load will lower the voltage delivered to the load. See the DAC Analog Characteristics table for the complete specifications of the full-scale output voltage.

4.1.3 Pseudo-differential Outputs

The CS4353 implements a pseudo-differential output stage. The AOUT_REF input is intended to be used as a pseudo-differential reference signal. This feature provides common mode noise rejection with single-ended signals. Figure 4 shows a basic diagram outlining the internal implementation of the pseudo-differential output stage, including a recommended stereo pseudo-differential output topology. If pseudo-differential output functionality is not required, simply connect the AOUT_REF pin to ground next to the CS4353. If a split-ground design is used, the AOUT_REF pin should be connected to AGND. See the Absolute Maximum Ratings table for the maximum allowable voltage on the AOUT_REF pin. Applying a DC voltage on the AOUT_REF pin will cause a DC offset on the DAC output.

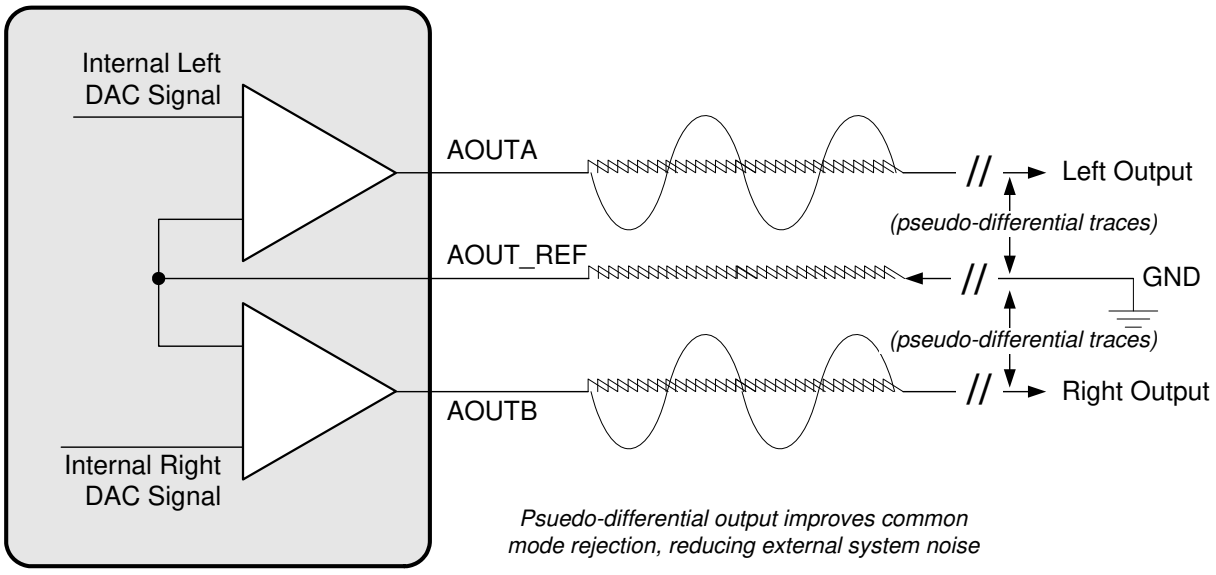


Figure 4. Stereo Pseudo-differential Output

4.2 Sample Rate Range/Operational Mode Detect

The CS4353 operates in one of three operational modes. The device will auto-detect the correct mode when the input sample rate (Fs), defined by the LRCK frequency, falls within one of the ranges illustrated in Table 2. Sample rates outside the specified range for each mode are not supported. In addition to a valid LRCK frequency, a valid serial clock (SCLK) and master clock (MCLK) must also be applied to the device for speed mode auto-detection; see Figure 9.

Input Sample Rate (Fs)	Mode
8 kHz - 54 kHz	Single-Speed Mode
84 kHz - 108 kHz	Double-Speed Mode
170 kHz - 216 kHz	Quad-Speed Mode

Table 2. CS4353 Operational Mode Auto-Detect

4.3 System Clocking

The device requires external generation of the master (MCLK), left/right (LRCK) and serial (SCLK) clocks. The left/right clock, defined also as the input sample rate (Fs), must be synchronously derived from the MCLK signal according to specified ratios. The specified ratios of MCLK to LRCK, along with several standard audio sample rates and the required MCLK frequency, are illustrated in Tables 3-5.

Refer to Section 4.4 for the required SCLK timing associated with the selected Digital Interface Format and to "Switching Specifications - Serial Audio Interface" on page 9 for the maximum allowed clock frequencies.

Sample Rate (kHz)	MCLK (MHz)				
	256x	384x	512x	768x	1024x
32	8.1920	12.2880	16.3840	24.5760	32.7680
44.1	11.2896	16.9344	22.5792	33.8688	45.1584
48	12.2880	18.4320	24.5760	36.8640	49.1520

Table 3. Single-speed Mode Standard Frequencies

Sample Rate (kHz)	MCLK (MHz)				
	128x	192x	256x	384x	512x
88.2	11.2896	16.9344	22.5792	33.8688	45.1584
96	12.2880	18.4320	24.5760	36.8640	49.1520

Table 4. Double-speed Mode Standard Frequencies

Sample Rate (kHz)	MCLK (MHz)		
	128x	192x	256x
176.4	22.5792	33.8688	45.1584
192	24.5760	36.8640	49.1520

Table 5. Quad-speed Mode Standard Frequencies

4.4 Digital Interface Format

The device will accept audio samples in either I²S or Left-Justified digital interface formats, as illustrated in Table 6.

The desired format is selected via the $\overline{\text{I²S}}$/LJ pin. For an illustration of the required relationship between the LRCK, SCLK and SDIN, see Figures 5-6. For all formats, SDIN is valid on the rising edge of SCLK. Also, SCLK must have at least 32 cycles per LRCK period in the Left-Justified format.

For more information about serial audio formats, refer to Cirrus Logic Application Note AN282: *The 2-Channel Serial Audio Interface: A Tutorial*, available at http://www.cirrus.com.

$\overline{\text{I²S}}$/LJ	Description	Figure
0	I²S, up to 24-bit Data	5
1	Left-Justified, up to 24-bit Data	6

Table 6. Digital Interface Format

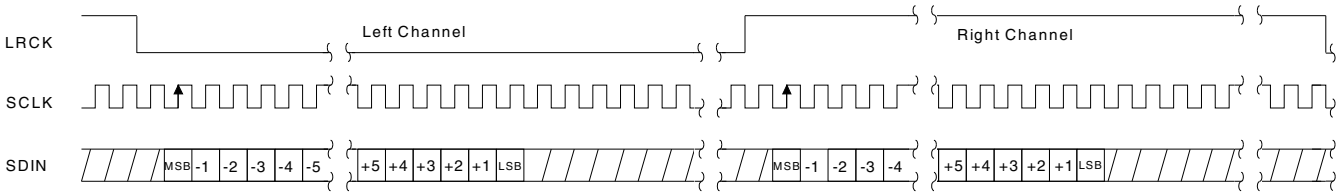


Figure 5. I²S, up to 24-bit Data

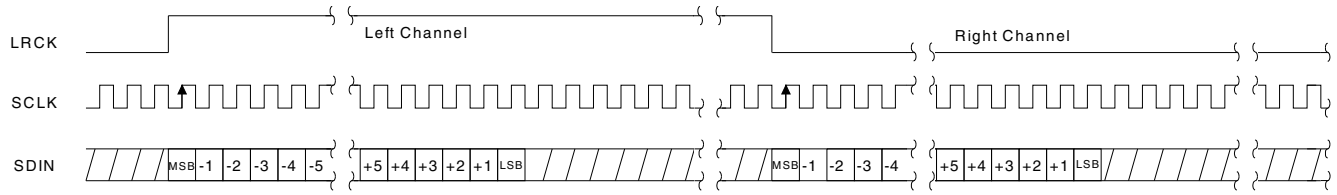


Figure 6. Left-justified up to 24-bit Data

4.5 Internal High-Pass Filter

The device includes an internal digital high-pass filter. This filter prevents a constant digital offset from creating a DC voltage on the analog output pins. The filter's corner frequency is well below the audio band; see the Combined Interpolation & On-Chip Analog Filter Response table for filter specifications.

4.6 De-emphasis Control

The device includes on-chip digital de-emphasis. Figure 7 shows the de-emphasis curve for Fs equal to 44.1 kHz. The frequency response of the de-emphasis curve scales with changes in the sample rate, Fs. The de-emphasis error will increase for sample rates other than 44.1 kHz.

When the DEM pin is connected to VL, the 44.1 kHz de-emphasis filter is activated. When the DEM pin is connected to GND, the de-emphasis filter is turned off.

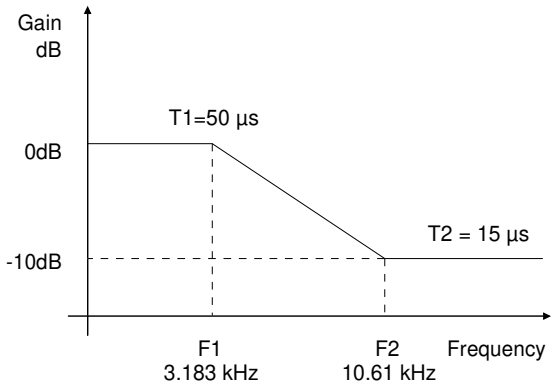


Figure 7. De-emphasis Curve, Fs = 44.1 kHz

Note: De-emphasis is only available in Single-Speed Mode.

4.7 Internal Power-on Reset

The CS4353 features an internal power-on reset (POR) circuit. The POR circuit allows the $\overline{\text{RESET}}$ pin to be connected to VL during power-up and power-down sequences if the external reset function is not needed. This circuit monitors the VCP supply and automatically asserts or releases an internal reset of the DAC's digital circuitry when the supply reaches defined thresholds (see "Internal Power-on Reset Threshold Voltages" on page 10). No external clocks are required for the POR circuit to function.

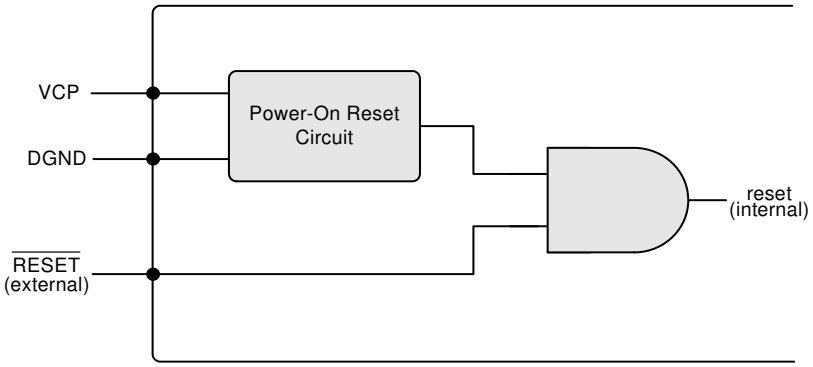


Figure 8. Internal Power-on Reset Circuit

When power is first applied, the POR circuit monitors the VCP supply voltage to determine when it reaches a defined threshold, V_{on1}. At this time, the POR circuit asserts the internal reset low, resetting all of the digital circuitry. Once the VCP supply reaches the secondary threshold, V_{on2}, the POR circuit releases the internal reset.

Note: For correct operation of the internal POR circuit, the voltage on VL must rise before or simultaneously with VCP.

When power is removed and the VCP voltage reaches a defined threshold, V_{off}, the POR circuit asserts the internal reset low, resetting all of the digital circuitry.

4.8 Initialization

When power is first applied, the DAC enters a reset (low power) state at the beginning of the initialization sequence. In this state, the AOUTx pins are weakly pulled to ground and VBIAS is connected to VA.

The device will remain in the reset state until the $\overline{\text{RESET}}$ pin is brought high. Once the $\overline{\text{RESET}}$ pin is high, the internal digital circuitry is reset and the DAC enters a power-down state until MCLK is applied. Alternatively, if no external reset control is required, the internal power-on reset can be used by tying the $\overline{\text{RESET}}$ pin to VL (see Section 4.7).

Once MCLK is valid, the device enters an initialization state in which the charge pump powers up and charges the capacitors for both the positive and negative high-voltage supplies.

Once LRCK and SCLK are valid, the number of MCLK cycles is counted relative to the LRCK period to determine the MCLK/LRCK frequency ratio. Next, the device enters the power-up state in which the interpolation and decimation filters and delta-sigma modulators are turned on, the internal voltage reference, VBIAS, powers up to normal operation, the analog output pull-down resistors are removed, and power is applied to the output amplifiers.

After this power-up state sequence is complete, normal operation begins and analog output is generated.

If valid MCLK, LRCK, and SCLK are applied to the DAC before $\overline{\text{RESET}}$ is set high, the total time from $\overline{\text{RESET}}$ being set high to the analog audio output from AOUTx is less than 50 ms.

See Figure 9 for a diagram of the device's states and transition conditions.

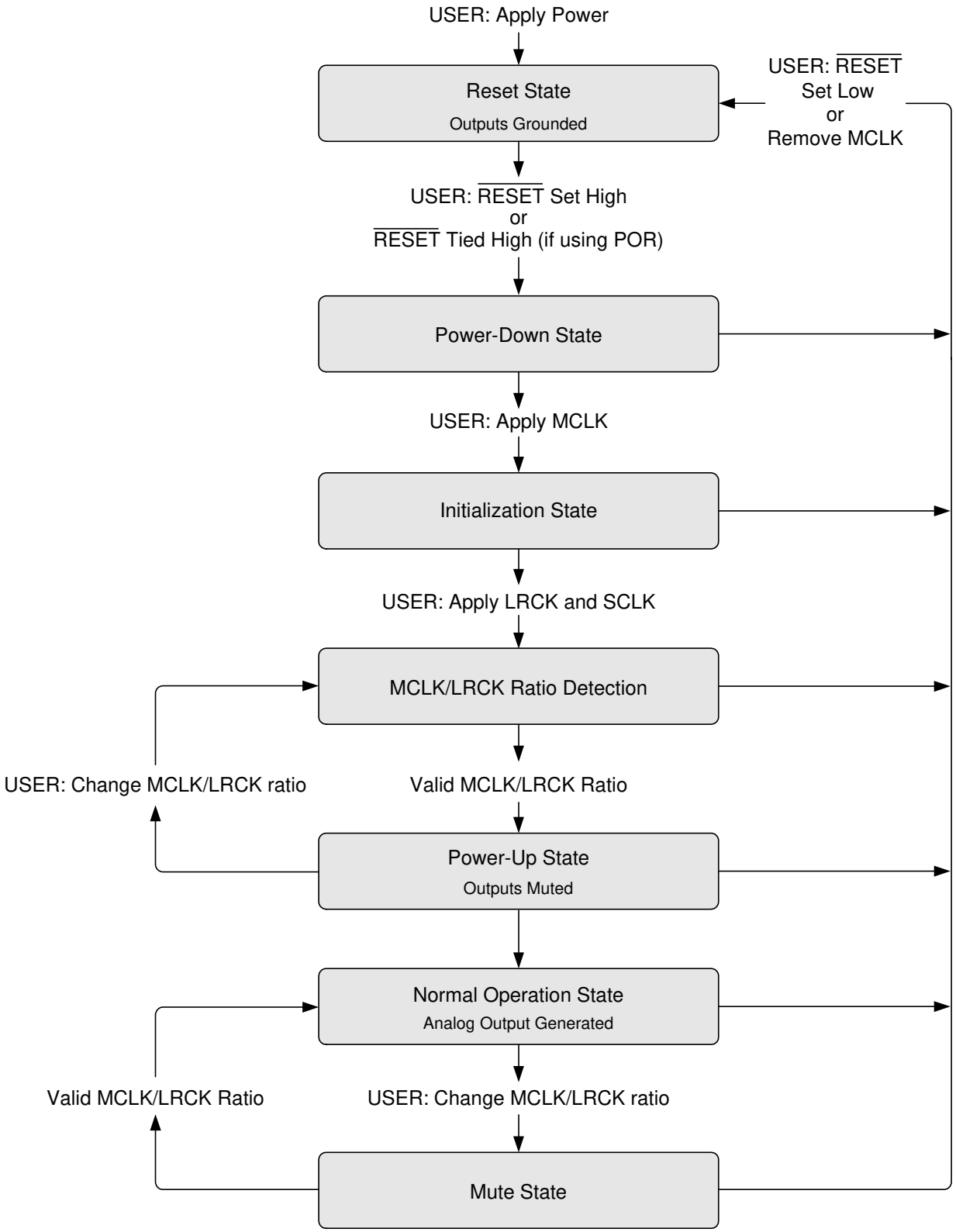


Figure 9. Initialization and Power-down Sequence Diagram

4.9 Recommended Power-up and Power-down Sequences

4.9.1 Power-up Sequences

4.9.1.1 External $\overline{\text{RESET}}$ Power-up Sequence

Follow the power-up sequence below if the external $\overline{\text{RESET}}$ pin is used:

1. Hold $\overline{\text{RESET}}$ low while the power supplies are turned on.
2. Set the $\overline{\text{I}^2\text{S}}$/LJ, 1_2VRMS, and DEM configuration pins to the desired state.
3. Provide the correct MCLK, LRCK, and SCLK signals locked to the appropriate frequencies as discussed in Section 4.3.
4. After the power supplies, configuration pins, and clock signals are stable, bring $\overline{\text{RESET}}$ high. The device will initiate the power-up sequence seen in Figure 9. The sequence will complete and audio will be output from AOUTx within 50 ms after $\overline{\text{RESET}}$ is set high.

4.9.1.2 Internal Power-on Reset Power-up Sequence

Follow the power-up sequence below if the internal power-on reset is used:

1. Hold $\overline{\text{RESET}}$ high (connected to VL) while the power supplies are turned on. The power-on reset circuitry will function as described in Section 4.7.
2. Set the $\overline{\text{I}^2\text{S}}$/LJ, 1_2VRMS, and DEM configuration pins to the desired state.
3. After the power supplies and configuration pins are stable, provide the correct MCLK, LRCK, and SCLK signals to progress from the 'Power-Down State' in the power-up sequence seen in Figure 9. The sequence will complete and audio will be output from the AOUTx pins within 50 ms after valid clocks are applied.

4.9.2 Power-down Sequences

4.9.2.1 External $\overline{\text{RESET}}$ Power-down Sequence

Follow the power-down sequence below if the external $\overline{\text{RESET}}$ pin is used:

1. For minimal pops, set the input digital data to zero for at least 8192 consecutive samples.
2. Bring $\overline{\text{RESET}}$ low.
3. Remove the power supply voltages.

4.9.2.2 Internal Power-on Reset Power-down Sequence

Follow the power-down sequence below if the internal power-on reset is used:

1. For minimal pops, set the input digital data to zero for at least 8192 consecutive samples.
2. Remove the MCLK signal without applying any glitched pulses to the MCLK pin.
3. Remove the power supply voltages.

Note: A glitched pulse is any pulse that is shorter than the period defined by the minimum/maximum MCLK signal duty cycle specification and the nominal frequency of the input MCLK signal. A transient may occur on the analog outputs if the MCLK signal duty cycle specification is violated when the MCLK signal is removed during normal operation; see "Switching Specifications - Serial Audio Interface" on page 9.

4.10 Grounding and Power Supply Arrangements

As with any high-resolution converter, the CS4353 requires careful attention to power supply and grounding arrangements if its potential performance is to be realized. Figure 3 shows the recommended power arrangements, with VCP, VA, and VL connected to clean supplies. It is strongly recommended that a single ground plane be used, with the DGND, CPGND, and AGND pins all connected to this common plane. Should it be necessary to split the ground planes, the DGND and CPGND pins should be connected to the digital ground plane and the AGND pin should be connected to the analog ground plane. In this configuration, it is critical that the digital and analog ground planes be tied together with a low-impedance connection, ideally a strip of copper on the printed circuit board, at a single point near the CS4353.

All signals, especially clocks, should be kept away from the VBIAS pin in order to avoid unwanted coupling into the DAC.

4.10.1 Capacitor Placement

Decoupling capacitors should be placed as close to the device as possible, with the low-value ceramic capacitor being the closest. To further minimize impedance, these capacitors should be located on the same PCB layer as the device. If desired, all supply pins may be connected to the same supply, but a decoupling capacitor should still be placed on each supply pin. See DC Electrical Characteristics for the voltage present across pin pairs. This is useful for choosing appropriate capacitor voltage ratings and orientation if electrolytic capacitors are used.

The CDB4353 evaluation board demonstrates the optimum layout and power supply arrangements.

5. DIGITAL FILTER RESPONSE PLOTS

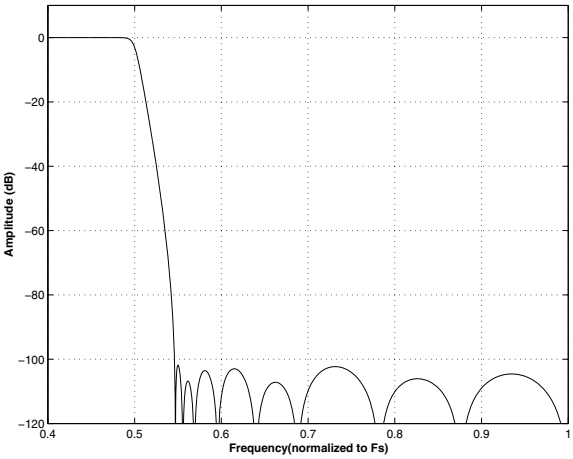


Figure 10. Single-speed Stopband Rejection

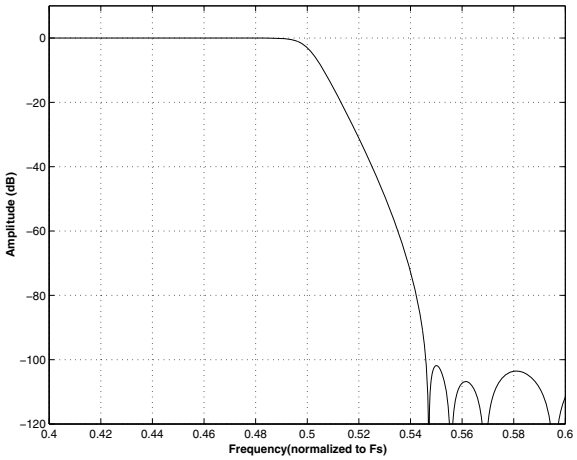


Figure 11. Single-speed Transition Band

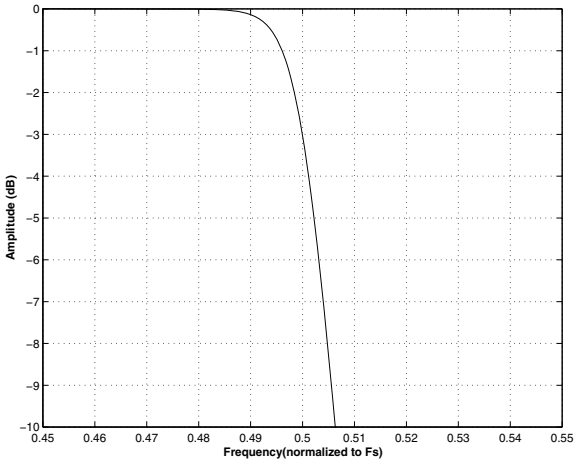


Figure 12. Single-speed Transition Band (detail)

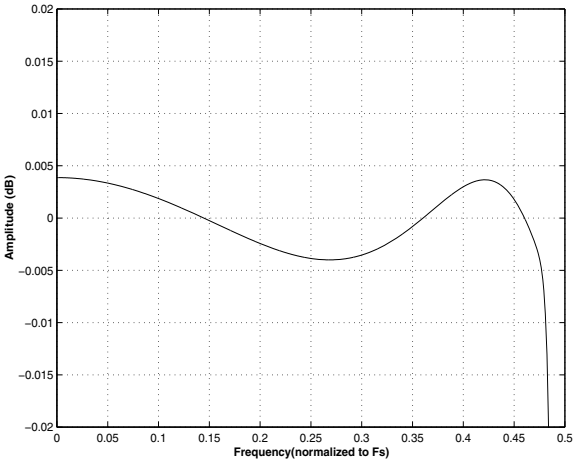


Figure 13. Single-speed Passband Ripple

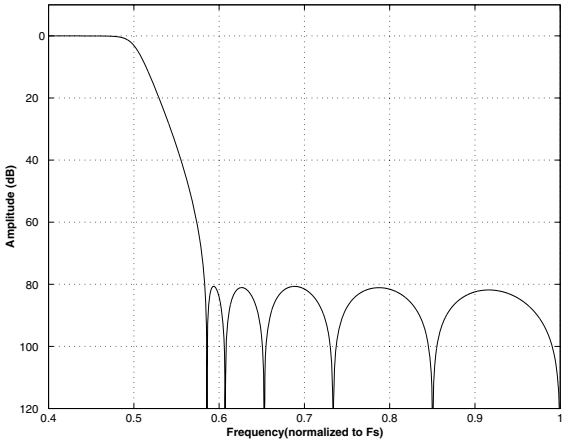


Figure 14. Double-speed Stopband Rejection

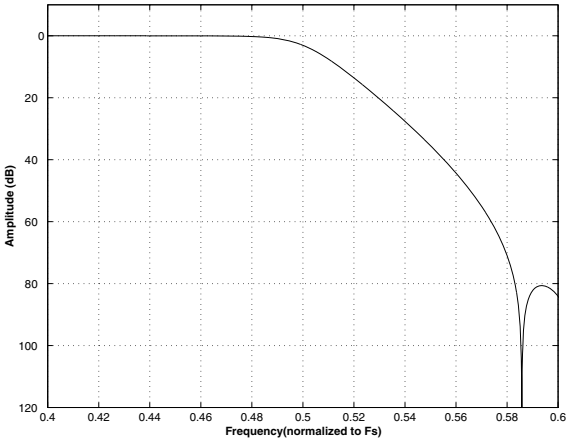


Figure 15. Double-speed Transition Band

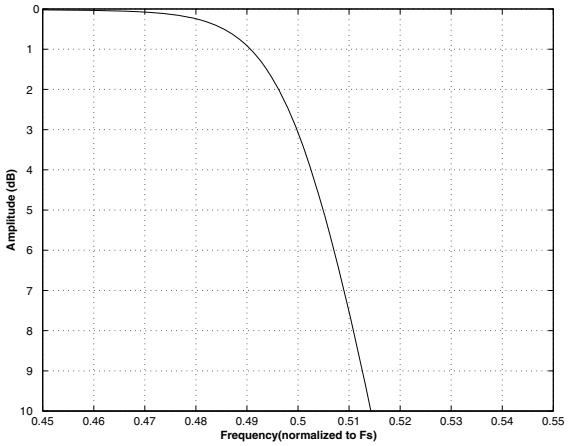


Figure 16. Double-speed Transition Band (detail)

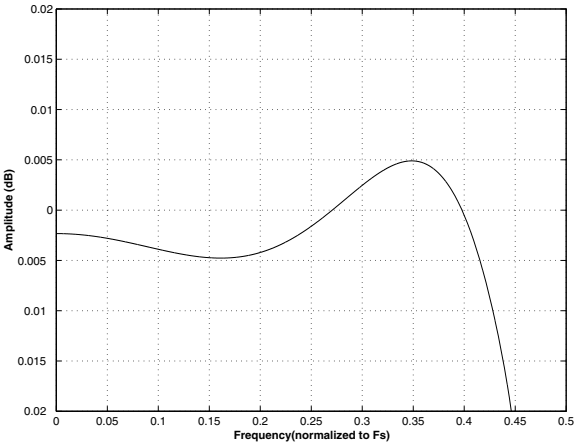


Figure 17. Double-speed Passband Ripple

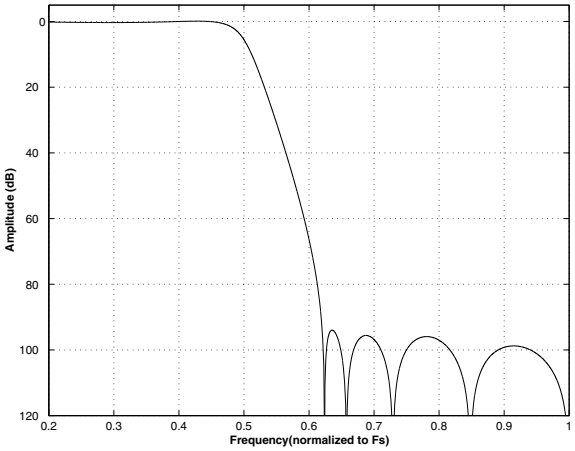


Figure 18. Quad-speed Stopband Rejection

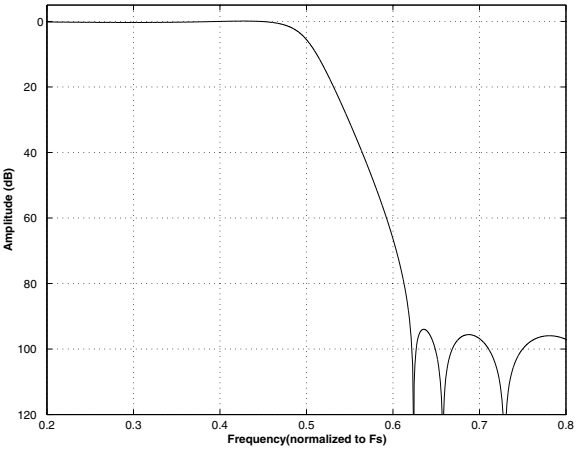


Figure 19. Quad-speed Transition Band

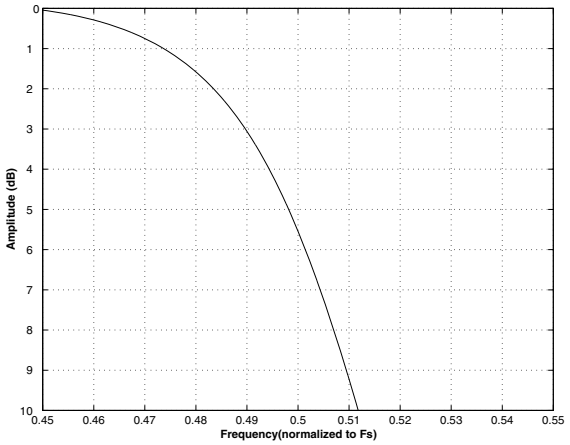


Figure 20. Quad-speed Transition Band (detail)

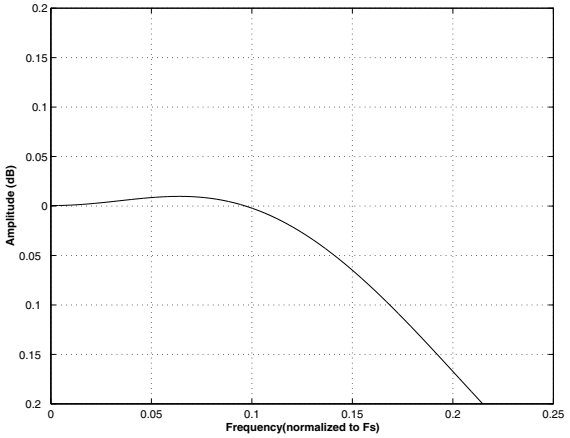


Figure 21. Quad-speed Passband Ripple

6. PARAMETER DEFINITIONS

Total Harmonic Distortion + Noise (THD+N)

The ratio of the RMS value of the signal to the RMS sum of all other spectral components over the specified bandwidth (typically 10 Hz to 20 kHz), including distortion components. Expressed in decibels.

Dynamic Range

The ratio of the full-scale RMS value of the signal to the RMS sum of all other spectral components over the specified bandwidth. Dynamic range is a signal-to-noise measurement over the specified bandwidth made with a -60 dBFS signal. 60 dB is then added to the resulting measurement to refer the measurement to full scale. This technique ensures that the distortion components are below the noise level and do not affect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-1991, and the Electronic Industries Association of Japan, EIAJ CP-307.

Interchannel Isolation

A measure of crosstalk between the left and right channels. Measured for each channel at the converter's output with all zeros to the input under test and a full-scale signal applied to the other channel. Units in decibels.

Interchannel Gain Mismatch

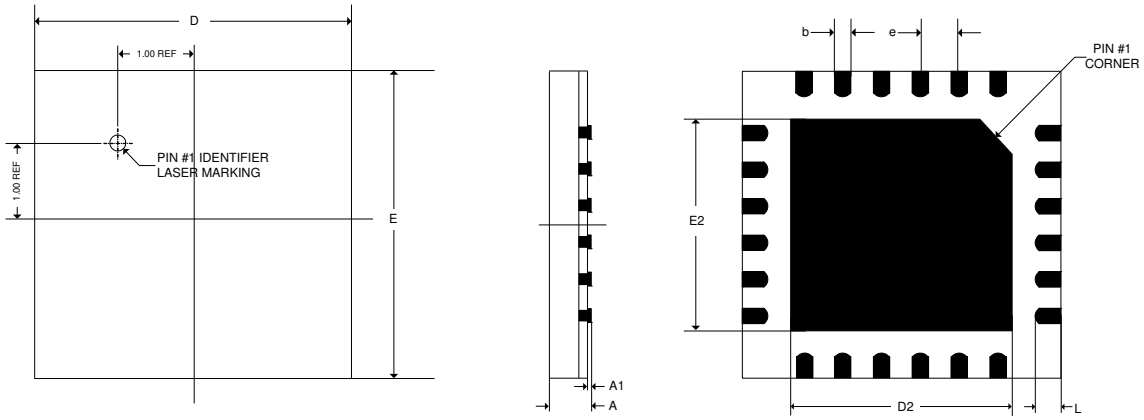
The gain difference between left and right channels. Units in decibels.

Gain Drift

The change in gain value with temperature. Units in ppm/°C.

7. PACKAGE DIMENSIONS

24L QFN (4.00 mm BODY) PACKAGE DRAWING



TOP VIEW SIDE VIEW BOTTOM VIEW

	INCHES			MILLIMETERS			NOTE
DIM	MIN	NOM	MAX	MIN	NOM	MAX	
A	-	-	0.03937	-	-	1.00	1
A1	0.00000	-	0.00197	0.00	-	0.05	1
b	0.00787	0.00984	0.01181	0.20	0.25	0.30	1, 2
e	0.01772	0.01969	0.02165	0.45	0.50	0.55	1
D		0.15748 BSC			4.00 BSC		1
D2	0.10433	0.10630	0.10827	2.65	2.70	2.75	1
E		0.15748 BSC			4.00 BSC		1
E2	0.10433	0.10630	0.10827	2.65	2.70	2.75	1
L	0.01181	0.01575	0.01969	0.30	0.40	0.50	1
Controlling Dimension is Millimeters							

Notes: 1. Dimensioning and tolerance per ASME Y 14.5M-1994.

2. Dimensioning lead width applies to the metallized terminal and is measured between 0.15 mm and 0.30 mm from the terminal tip.

Parameter		Symbol	Min	Typ	Max	Units
Junction to Ambient Thermal Impedance	2 Layer Board	θ_{JA}	-	68	-	°C/Watt
	4 Layer Board	θ_{JA}	-	28	-	°C/Watt

8. ORDERING INFORMATION

Product	Description	Package	Pb-Free	Grade	Temp Range	Container	Order #
CS4353	3.3 V Stereo Audio DAC with 2 V_{RMS} Line Output	24-pin QFN	YES	Commercial	-40° to +85° C	Rail	CS4353-CNZ
						Tape & Reel	CS4353-CNZR
CDB4353	CS4353 Evaluation Board		-	-	-	-	CDB4353

9. REVISION HISTORY

Release	Changes
PP1	– Updated interchannel isolation specification in the DAC Analog Characteristics specification table. – Updated minimum Quad-Speed Mode SCLK period in the Switching Specifications - Serial Audio Interface table. – Updated power supply current and power dissipation specifications in the DC Electrical Characteristics table. – Updated the FLYN+ to FLYN- DC voltage in the DC Electrical Characteristics table. – Added “SDIN = 0” to the test conditions in the DC Electrical Characteristics table. – Updated Section 4.9.1.1 on page 19. – Updated output impedance specification in the DAC Analog Characteristics specification table.
PP2	– Removed Automotive Grade.
F1	– Added Note 2 and reference to Note 4 in the Dynamic Performance section of the DAC Analog Characteristics table. – Changed “additional” to “external” in Note 6 and 8 on page 7. – Updated full scale output specification in the DAC Analog Characteristics table. – Updated Von2 and Voff specifications in the Internal Power-on Reset Threshold Voltages table. – Added HPF data to Combined Interpolation & On-Chip Analog Filter Response table. – Added Section 4.5 Internal High-Pass Filter.

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
To find one nearest you, go to www.cirrus.com.