- **Color or Gray Scale Operation**
- **Signals Processed in the Digital Domain**
- **Differential RGB Input Multiplexer**
- **Three 8-bit DACs for CCD Offset Level Shifting With Bipolar Correction Range**
- **Two Sampling Modes:**
  - **DAC Referenced**
  - **Correlated Double Sampling (CDS)**
- **12-Bit ADC with 6 MSPS Operation**
- **Digital dc Restoration**
- **Pixel-By-Pixel Offset and Shading (Gain) Compensation**
- **Global Gain Adjust for Each Color (Channel)**
- **Compatible with 600 dpi CCD Image Sensors**
- **Global Offset Adjust for Each Color (Channel)**
- **Output Word Length Programmable to 8, 10, 12, or 16 Bits**
- **Programmable Threshold Detector for Each Color (Channel)**
- **Dual Internal Default Registers for Even/Odd Pixel Offset Correction**
- **68-Terminal PLCC Package**

applications

- **Handy Scanners**
- **Flatbed Scanners**

description

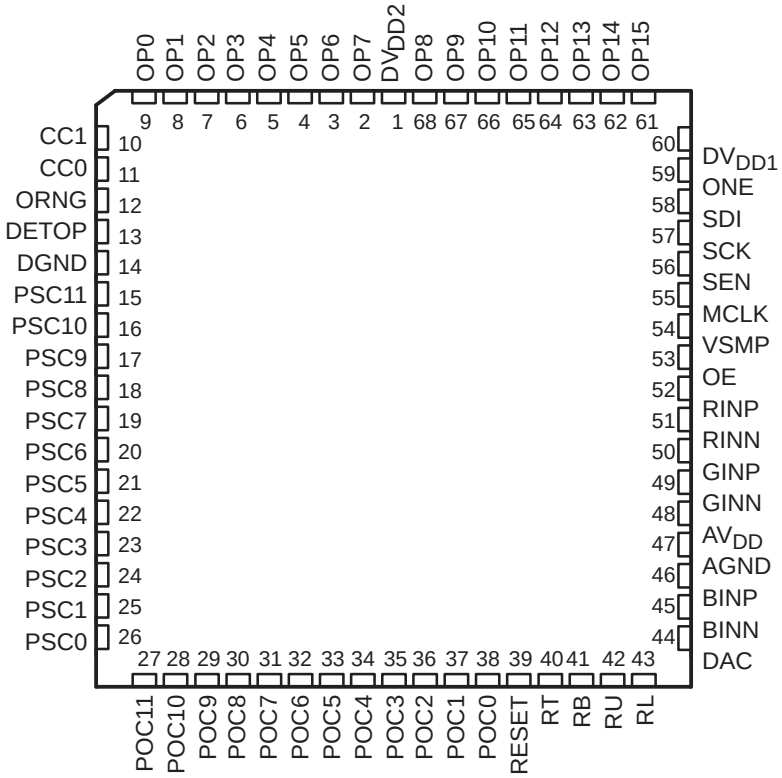
The TLC8044 is a 12-bit analog-to-digital interface subsystem for charge-coupled device (CCD) image sensors and scanners. An input multiplexer allows color operation with a single on-chip 12-bit ADC. The TLC8044 uses DSP circuits to correct for nonideal CCD image sensor and scanning system characteristics. Cost effective gray scale operation is obtained using a single multiplexer input. The TLC8044 three-channel input multiplexer and sampling function has two basic modes of operation: normal sampling and correlated double sampling. The internal sample and hold allows all three channels to be sampled simultaneously in color operation. Three DACs (8 bits + sign) are provided to allow bipolar adjustment of the dc level of the signal at the ADC input. Digital dc restoration is provided following the ADC. Variations in offset and luminance across a scan are dynamically corrected on a pixel-by-pixel basis, using calibration data provided by an external data store. Provisions are made for global adjustments of gain, contrast and color balance, and offset for brightness. The output word length can be programmed to 8, 10, 12, or 16 bits, and a programmable threshold detector is provided for use during calibration and OCR applications. The TLC8044 is characterized for operation from 0°C to 70°C.

AVAILABLE OPTIONS

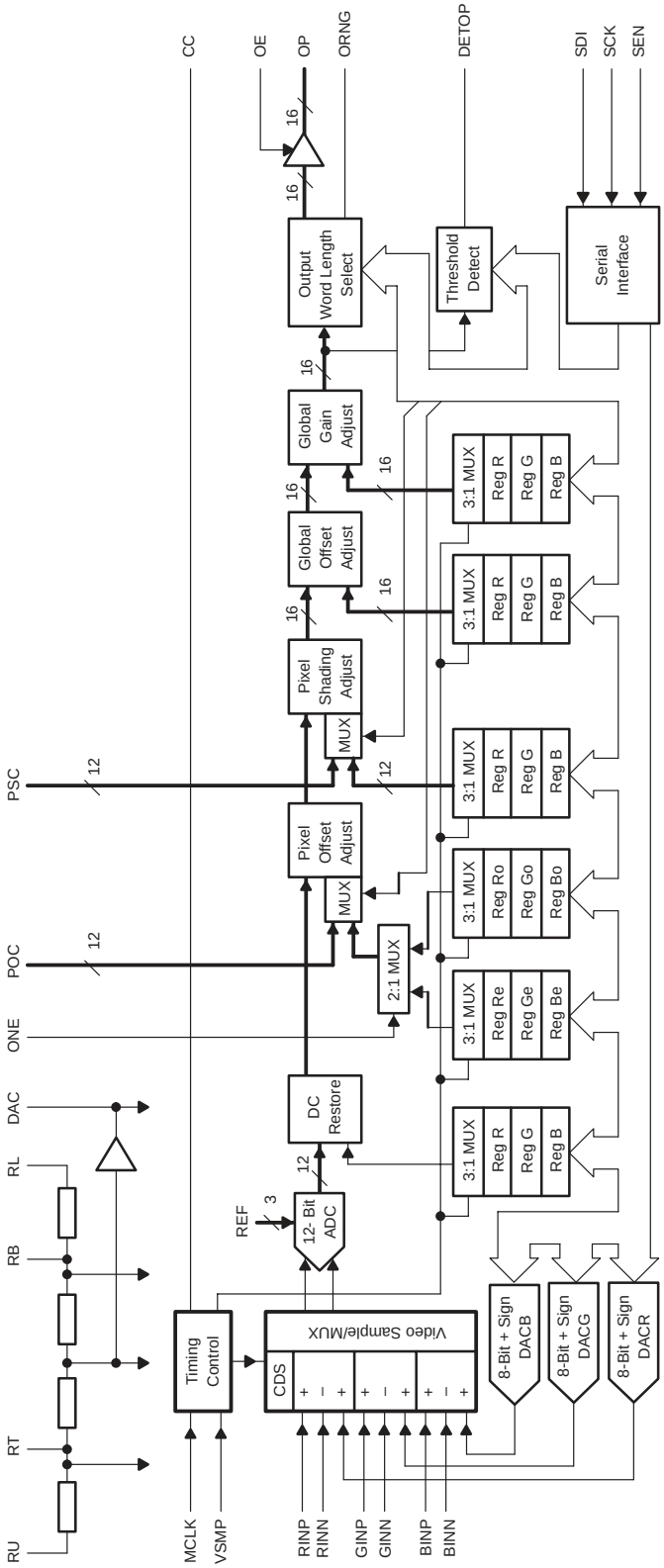
T_A	PACKAGE
	CHIP CARRIER (FN)
0°C to 70°C	TLC8044FN

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

FN PACKAGE
(TOP VIEW)



functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	TYPE	I/O	DESCRIPTION
AGND	47	Analog	I	Analog ground (0 V)
AV_{DD}	48	Analog		Positive analog supply (5 V)
BINN	45	Analog	I	Negative blue channel input video
BINP	46	Analog	I	Positive blue channel input video
CC1,0	10, 11	Digital	O	Color code outputs. CC0 and CC1 indicate which channel the current output sample was taken from (R = 00, G = 01, B = 10).
DAC	44	Analog	O	Buffered midpoint of ADC reference string. DAC is used internally to set DAC reference voltages.
DETOP	13	Digital	O	Threshold detector output (active high). DETOP indicates that the current output pixel has exceeded the internally programmed threshold for that channel.
DGND	14	Digital	I	Digital ground (0 V)
$DV_{DD}1,2$	60, 1	Digital	I	Positive digital supply (5 V)
GINN	49	Analog	I	Negative green channel input video
GINP	50	Analog	I	Positive green channel input video
MCLK	55	Digital	I	Master clock. MCLK is applied at either six times or twice the input pixel rate for color and monochrome operation, respectively. MCLK is divided by two internally to define the ADC sample rate and to provide the clock source for the DSP section.
OE	53	Digital	I	Output 3-state control. Outputs are enabled when OE = 0.
ONE	59	Digital	I	Odd not even. ONE defines the even and odd pixels when the internal pixel offset correction registers are in use (even = 0, odd = 1).
OP15–OP0	61-68, 2-9	Digital	O	Digital 16-bit output (3-state). In 8-, 10-, and 12-bit output modes, OP15 is used to indicate that the output pixel is negative; i.e., OP15 can be used as an under range indicator. OP15 is active high when indicating under range.
ORNG	12	Digital	O	Over range signal (active high). In 8-, 10-, and 12-bit output modes, this signal indicates that the current output pixel has exceeded the maximum achievable for the output word length in use.
POC11–POC0	27-38	Digital	I	Pixel offset coefficient input. The POC11–POC0 12-bit word is applied at the multiplexed pixel rate (i.e., three samples per pixel period in color mode) to correct offset errors in a pixel-by-pixel fashion.
PSC11–PSC0	15-26	Digital	I	Pixel shading coefficient input. The PSC11–PSC0 12-bit quantity is applied at the multiplexed pixel rate (i.e., three samples per pixel period in color mode) to correct shading effects in a pixel-by-pixel fashion.
RESET	39	Digital	I	Reset input (active high). RESET forces a reset of all internal registers in the TLC8044.
RINN	51	Analog	I	Negative red channel input video
RINP	52	Analog	I	Positive red channel input video
RU, RT, RB, RL	42, 40, 41, 43	Analog	I	ADC reference terminals. The voltage applied between RT (full scale) and RB (zero level). define the ADC reference range. RU and RL, upper and lower resistor terminals, are used to derive optimum reference voltages from an external 5-V reference.
SCK	57	Digital	I	Serial clock. Serial interface clock signal.
SDI	58	Digital	I	Serial data in. Serial interface input data signal.
SEN	56	Digital	I	Serial enable
VSMP	54	Digital	I	Video sample synchronization pulse. VSMP applied synchronously with MCLK specifies the point in time that the input is sampled. The timing of internal multiplexing between the R, G, and B channels is derived from this signal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, DV_{DD1}, DV_{DD2}, AV_{DD}, V_{DD} (see Note 1) . . . . . 7 V
Digital inputs (see Note 1) . . . . . – 0.3 V to V_{DD} + 0.3 V
Analog inputs (see Note 1) . . . . . – 0.3 V to V_{CC} + 0.3 V
Digital outputs, maximum external voltage applied (see Note 1) . . . . . – 0.3 V to V_{CC} + 0.3 V
Reference input (see Note 1) . . . . . – 0.3 V to V_{DD} + 0.3 V
Operating temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . –50°C to 150°C
Lead temperature, soldering, 10 sec . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Voltages applied to $DV_{DD}1$ and $DV_{DD}2$ are measured with respect to the DGND terminal. AV_{DD} is measured with respect to the AGND terminal. For the following specifications, unless otherwise noted, AGND and DGND are tied togather (and represent 0 volts) and are referred to simply as GND. When the voltages applied to $DV_{DD}1$, $DV_{DD}2$, and AV_{DD} are equal, they are referred to simply as V_{DD}, unless otherwise noted.

recommended operating conditions

total device

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75		5.25	V

digital inputs

	MIN	NOM	MAX	UNIT
High-level input voltage, V_{IH}	0.9 V_{DD}			V
Low-level input voltage, V_{IL}			0.1 V_{DD}	V

input multiplexer

	TEST CONDITIONS	MIN	NOM	MAX	UNIT
Setup time, input video before MCLK↑, $t_{su(V)}$		10			ns
Hold time, input video after MCLK↑, $t_{h(V)}$		25			ns
Setup time, reset video before MCLK↑, $t_{su(R)}$	CDS mode only	10			ns
Hold time, reset video after MCLK↑, $t_{h(R)}$	CDS mode only	25			ns

serial interface

	MIN	NOM	MAX	UNIT
Cycle time, MCLK, t_{cyc1}	83.3			ns
Pulse duration, MCLK high, $t_{w1(MCLKH)}$	37.5			ns
Pulse duration, MCLK low, $t_{w2(MCLKL)}$	37.5			ns
Setup time, VSMP↑ to MCLK↑, $t_{su(D)}$	10			ns
Hold time, MCLK↑ to VSMP↓, $t_{h(D)}$	10			ns
Setup time, POC/PCS to MCLK↓, $t_{su(P)}$	10			ns
Hold time, MCLK↓ to POC/PCS, $t_{h(P)}$	30			ns
Cycle time, SCK, t_{cyc2}	83.3			ns
Pulse duration, SCK high, $t_{w3(SCKH)}$	37.5			ns
Pulse duration, SCK low, $t_{w4(SCKL)}$	37.5			ns
Setup time, SDI to MCLK↑, $t_{su(S)}$	10			ns
Hold time, MCLK↑ to SDI change, $t_{h(S)}$	10			ns
Setup time, SCK↑ to SEN↑, $t_{su(SCE)}$	20			ns
Setup time, SEN↓ to SCK↑, $t_{su(SEC)}$	20			ns
Pulse duration, SEN high, $t_{w(SEN)}$	50			ns

electrical characteristics, V_{DD} = 5 V, AGND = DGND = 0 V, T_A = full range (unless otherwise noted)

total device

PARAMETER		MIN	TYP	MAX	UNIT
I_{CC}	Supply current, active		80	130	mA
I_{CC}	Supply current, standby		8	10	mA

digital inputs

PARAMETER		MIN	TYP	MAX	UNIT
I_{IH}	High-level input current			1	μA
I_{IL}	Low-level input current			1	μA
C_i	Input capacitance		10		pF

digital outputs

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –1 mA	V_{DD} - 0.75			V
V_{OL}	Low-level output voltage	I_{OL} = 1 mA			0.75	V
I_{OZ}	High-impedance output current				1	μA

input multiplexer

PARAMETER		MIN	TYP	MAX	UNIT
	Channel-to-channel gain matching		0.5%	5%	
V_{ICR}	Common mode input voltage	0.5		4.5	V

reference string

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Z	Impedance, RT to RB		595	850	1105	Ω
Z	Impedance, RU to RL		1190	1700	2210	Ω
$V_{ref(RT)}$	Reference voltage, top	$V_{I(RU)}$ = 5 V, $V_{I(RL)}$ = 0 V	3.7125	3.75	3.7875	V
$V_{ref(RB)}$	Reference voltage, bottom	$V_{I(RU)}$ = 5 V, $V_{I(RL)}$ = 0 V	1.2375	1.25	1.2625	V
$V_{ref(DAC)}$	DAC reference voltage	$V_{I(RU)}$ = 5 V, $V_{I(RL)}$ = 0 V	2.475	2.5	2.525	V

8-bit DACs

PARAMETER	MIN	TYP	MAX	UNIT
Resolution	8			Bits
Zero-scale voltage	0		10	mV
Full-scale voltage	$V_{ref(DAC)}$ -10		$V_{ref(DAC)}$ +10	mV
Differential nonlinearity (DNL)		0.1	<1	LSB
Integral nonlinearity (INL)		0.4	1	LSB

electrical characteristics, V_{DD} = 5 V, AGND = DGND = 0 V, T_A = full range (unless otherwise noted) (continued)

12-bit ADC

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution		12			Bits
Sampling rate				6	MSPS
Full-scale transition error voltage at xINP (see Note 2)	Single-ended mode, $V_{I(xINN)}$ = 2.5 V, DAC code = 000H	–100		100	mV
Zero-scale transition error voltage at xINP (see Note 3)	Single-ended mode, $V_{I(xINN)}$ = 2.5 V, DAC code = 000H	–100		100	mV
Full-scale transition error voltage, $V_{I(xINP)} – V_{I(xINN)}$ (see Note 2)	Differential mode, DAC code = 000H	–25		25	mV
Zero-scale transition error voltage, $V_{I(xINP)} – V_{I(xINN)}$ (see Note 3)	Differential mode, DAC code = 000H	–25		25	mV
Differential nonlinearity (DNL) (see Note 4)				1.5	LSB
Maximum number of missing codes		0		8	CODES
Integral nonlinearity (INL) (see Note 5)			±2	±5	LSB

NOTES: 2. The full-scale transition at xINP is the difference between the signal input voltage that causes the 4094 to 4095 transition and the measured reference voltage $V_{ref(RT)}$.
3. The zero-scale transition at xINP is the difference between the signal input voltage that causes the 0 to 1 transition and the reference voltage $V_{ref(RB)}$.
4. Differential nonlinearity (DNL) is the difference between the measured value between any two adjacent codes and the ideal 1 LSB value.
5. Integral nonlinearity (INL) is the maximum deviation of the output from the ideal straight line between zero and the full-scale value.

switching characteristics

PARAMETER		MIN	TYP	MAX	UNIT
$t_{pd(D)}$	Propagation delay time, MCLK↓ to output valid		50	75	ns
$t_{en(PZE)}$	Enable time, output, OE↓ to data valid		70	75	ns
$t_{dis(PEZ)}$	Disable time, output, OE↑ to high impedance		70	25	ns

PARAMETER MEASUREMENT INFORMATION

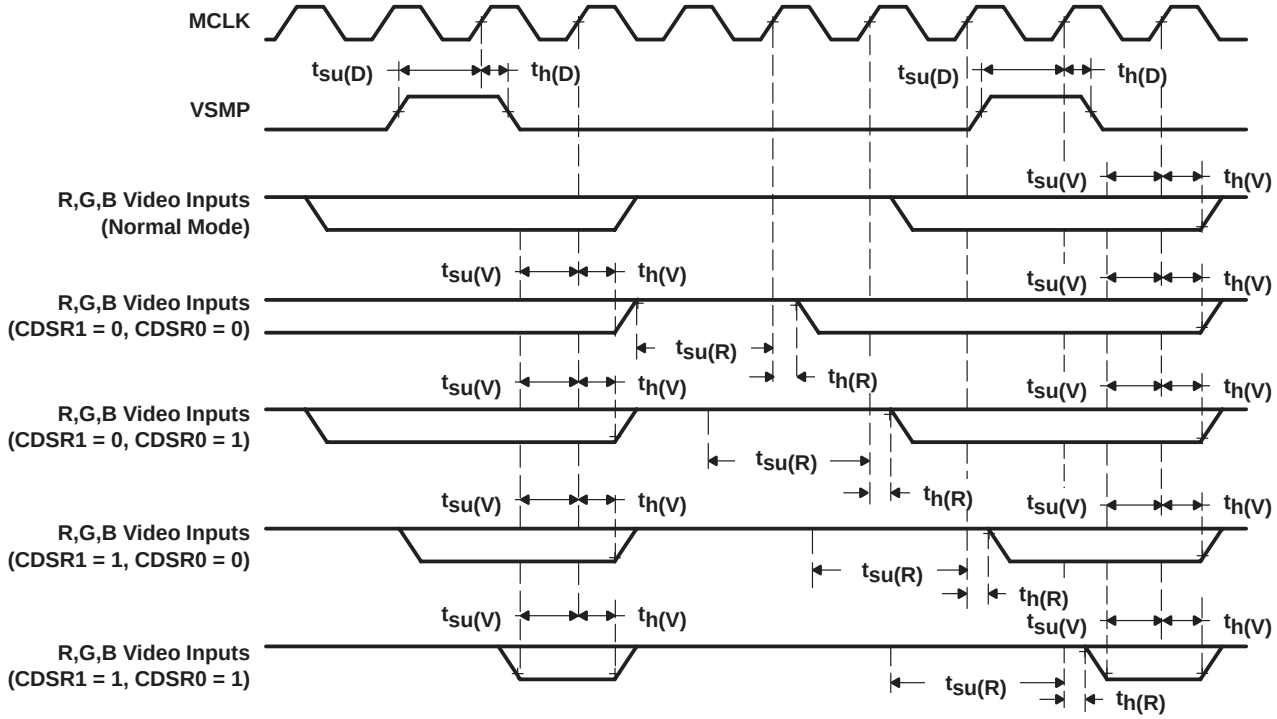


Figure 1. Detailed Video Input Timing – Color Mode

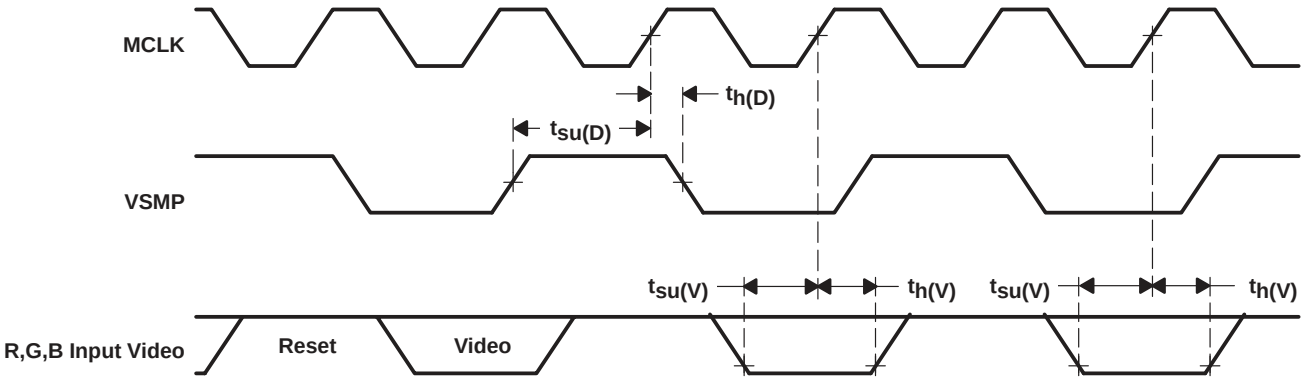


Figure 2. Detailed Video Input Timing – Monochrome Mode

PARAMETER MEASUREMENT INFORMATION

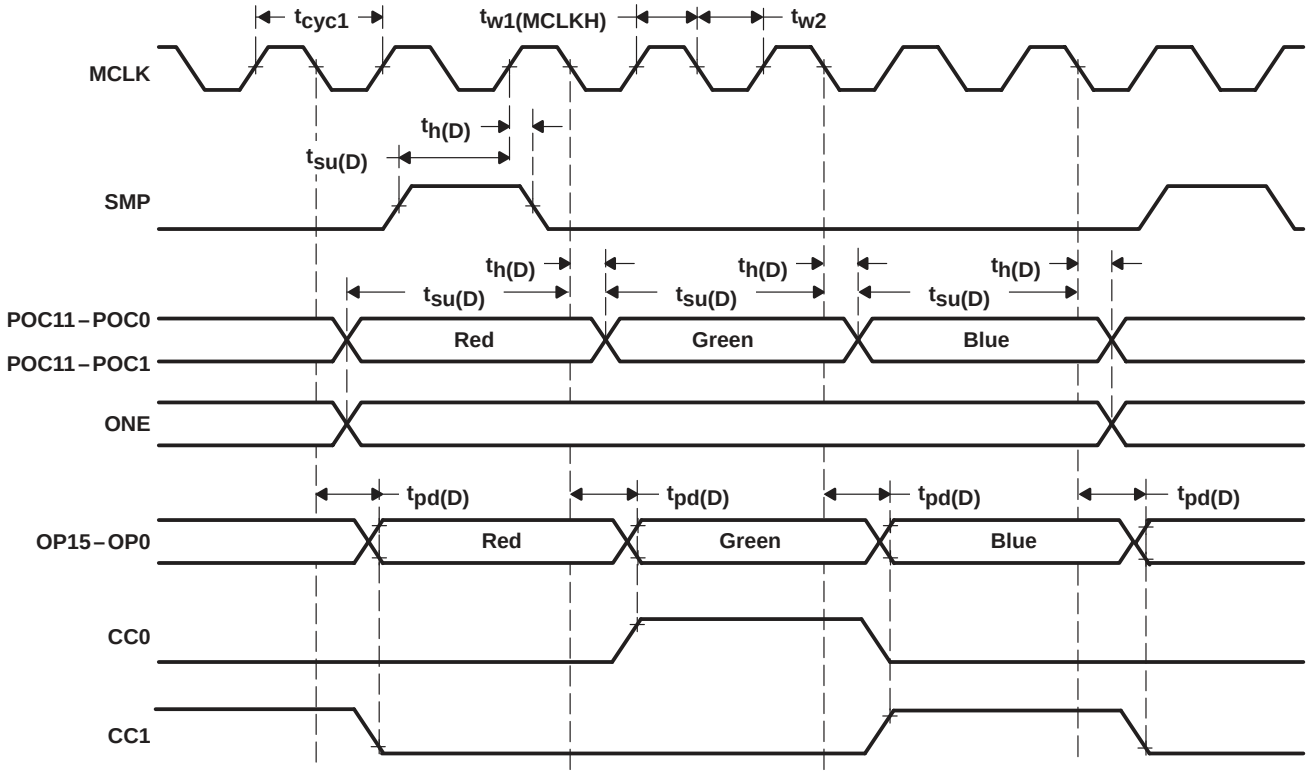


Figure 3. Detailed Digital Timing – Color Mode

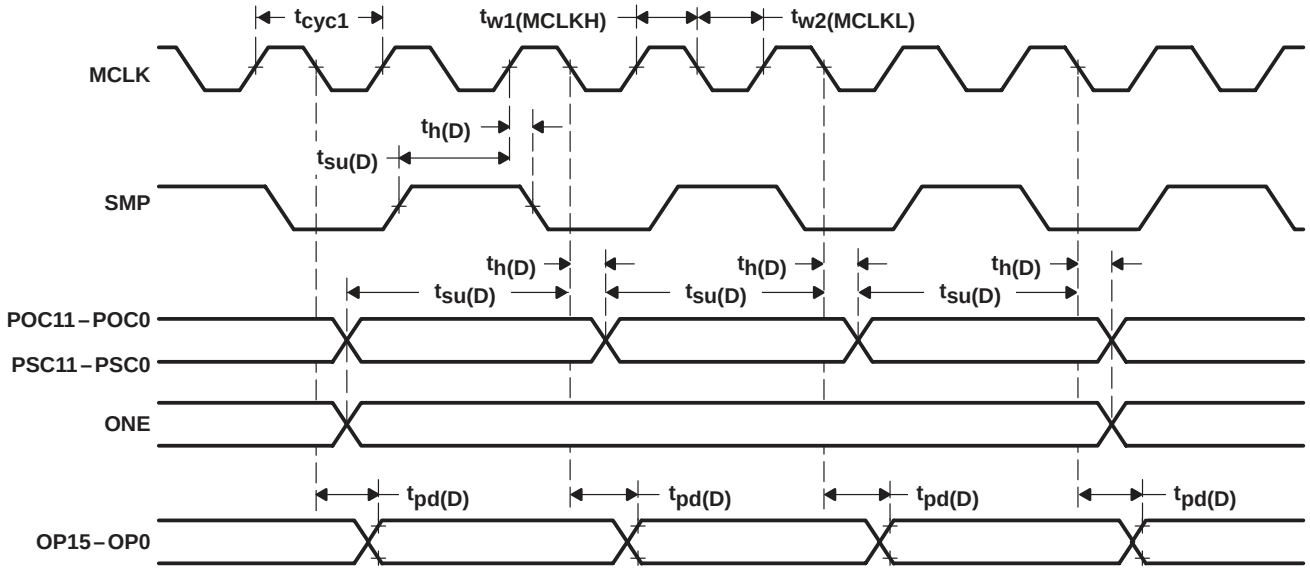


Figure 4. Detailed Digital Timing – Monochrome Mode

PARAMETER MEASUREMENT INFORMATION

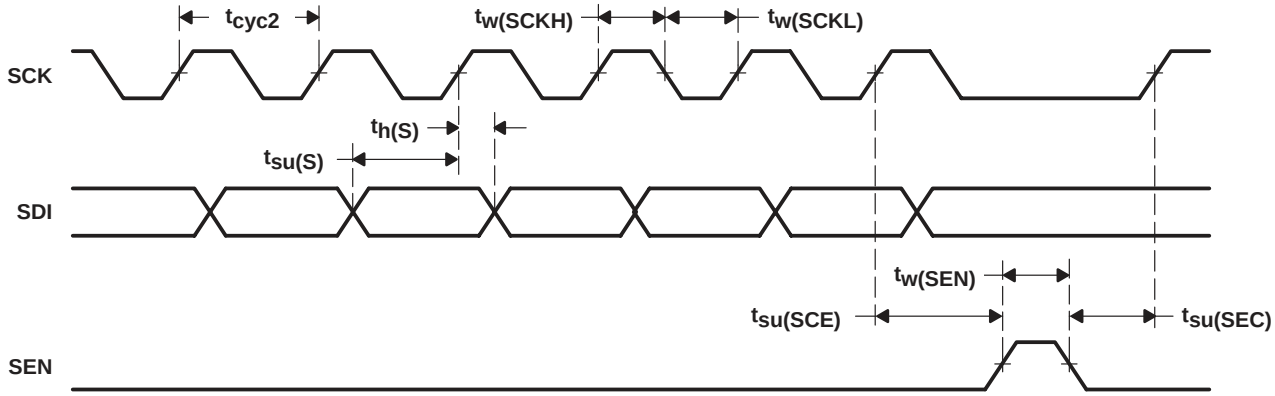


Figure 5. Detailed Digital Timing – Serial Interface

TYPICAL CHARACTERISTICS

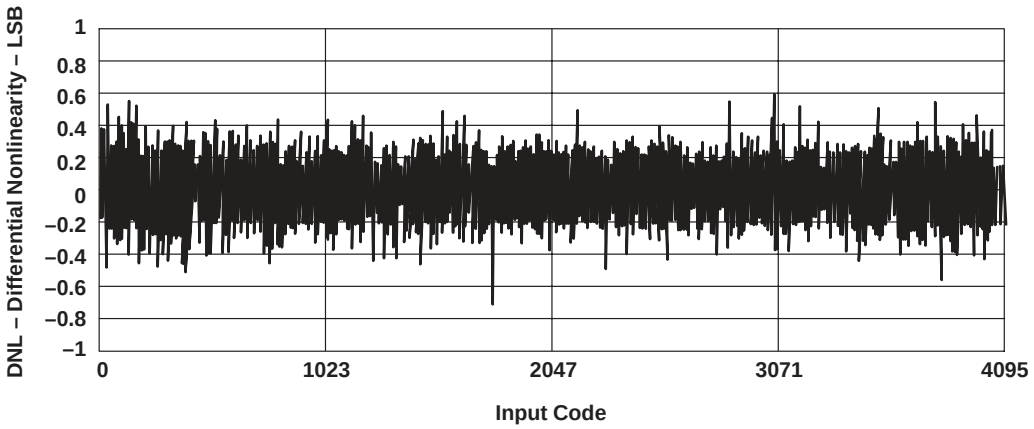


Figure 6. Differential Linearity With Code

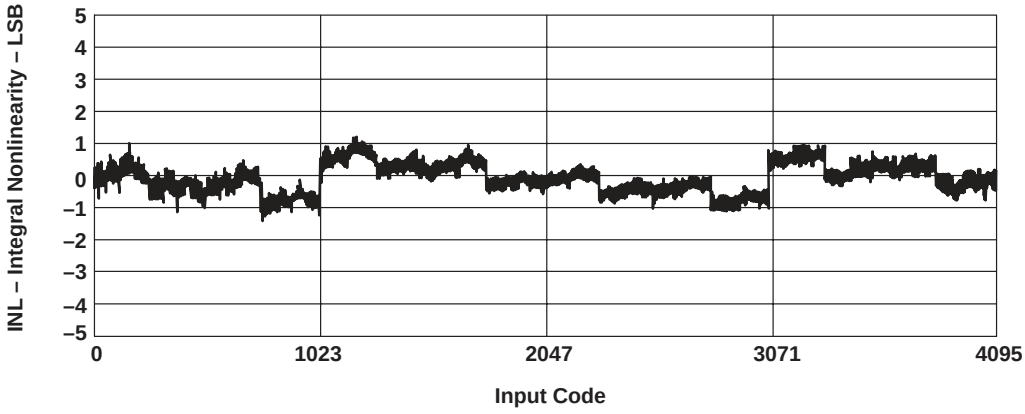


Figure 7. Integral Linearity With Code

PRINCIPLES OF OPERATION

general CCD system operation

CCD image sensor array output summary

Figure 8 shows a simplified CCD image sensor linear array system with typical CCD array inputs and outputs. The inputs for the shift gate (SH), reset, and two-phase clock drive the array. An electronic charge proportional to the light input is generated by a photo diode for each pixel of the array. The charge for each pixel is transferred in parallel into the analog CCD shift register using the shift gate input and then shifted out serially using a two-phase clock. At the CCD output (OS terminal), the array converts the charge for each pixel into a voltage using a capacitor and source follower MOS transistor. The charge on this capacitor is reset for each pixel by the reset pulse input. A typical output signal then includes a reset period, a dark period, and a period containing video output for each pixel, as shown in Figure 9. This signal sits on a varying dc offset of typically 5 V and is negative going for an increase in video output. An output (DOS terminal) also provides only the dc level from the CCD array.

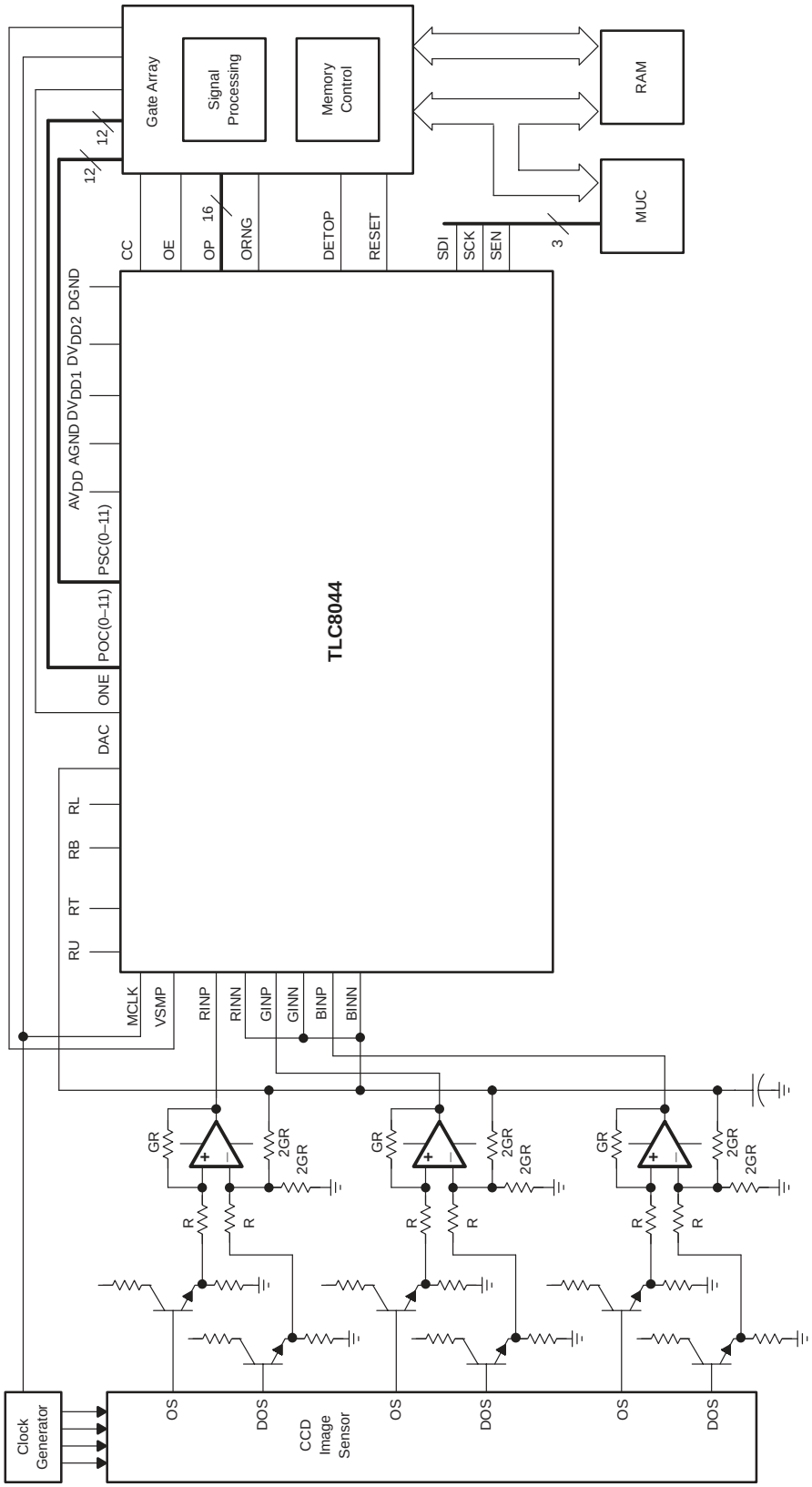


Figure 8. System Diagram

PRINCIPLES OF OPERATION

CCD image sensor array output summary (continued)

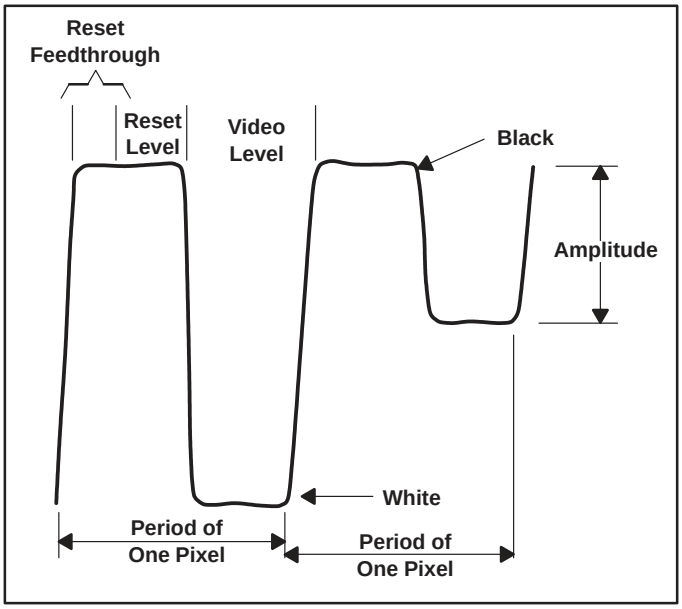


Figure 9. A Typical Charge-Coupled Display (CCD) Output Signal

CCD array analog-to-digital interface functions

The interface to the CCD array analog output and the conversion of the output into digital form involves the following functions:

1. The video output waveform first has to be removed from the varying dc level on which it sits and shifted in level to be compatible with an interface device running from a single 5-V supply rail.
2. Gain has to be applied to bring the signal up to the full-scale range of the analog-to-digital converter (ADC) and a means provided to adjust static gain to compensate for variations between devices or multiple outputs of color arrays. Once these static dc levels (offsets) and gain levels have been adjusted, dynamic corrections are needed on a pixel-by-pixel basis.
3. Dynamic gain adjustment is needed to compensate for the fall off in output from the center to the ends of the array when used in scanner applications (see Figure 10). Dynamic offset adjustments are required to compensate for the pixel-by-pixel variation in black dc levels obtained from different CCD array elements.
4. DC restoration may optionally be required. Global adjustments of gain and offset across a whole scan are respectively used to correct color balance and contrast and to change brightness.

PRINCIPLES OF OPERATION

CCD array analog-to-digital interface functions (continued)

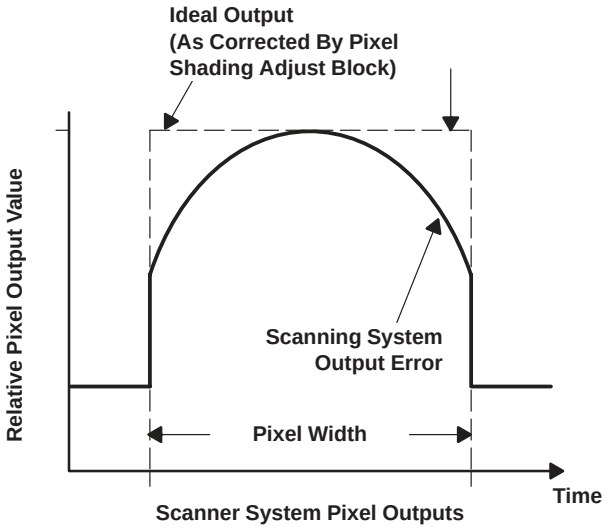


Figure 10. Scanner System Relative CCD Pixel Output

CCD scanner analog-to-digital interface subsystem

input dc level shift, output offset, and channel gain

The TLC8044 uses external operational amplifiers configured as differential amplifiers to remove the dc level present in the CCD outputs by using the common mode voltages from the OS and DOS outputs for each channel (see the functional block and system diagrams). DC bias is provided for the external differential amplifier from the TLC8044 DAC output as shown in the system diagram in Figure 8. Without any residual offset from the CCD, the differential amplifier minimum output is (DAC result)/2 and is uneffected by the external differential amplifier gain setting (G). The offset at the output of the external differential amplifiers, including residual offset from the CCD, should be low enough to ensure the CCD amplified signal is within the input common mode range of the TLC8044 and that the offset can be adjusted out by the TLC8044 internal DACs.

The external differential amplifiers also provide the system gain for each channel to ensure the output amplitude of each channel is greater than one half the ADC full-scale range. Variations between the RGB channels of the CCD can have a 10 to 1 ratio in output. To minimize the offset at the amplifier output with the highest gain, the external amplifiers should be configured for gains in the range 1/3 to 3 rather than 1 to 10 to compensate for this output variation. This is achieved by scaling the gain setting resistors shown in the system diagram by the gain factor (G) over this 1/3 to 3 range.

RGB channel multiplexer and sampler

For color CCD image sensor arrays, a combined three-input multiplexer and sampler is used enabling the use of a single fast 12-bit ADC and DSP channel.

The TLC8044 multiplexer has three differential inputs for each of the RGB channel outputs and a further internal input for each channel which is used to compensate for the residual offset in the input signal. This internal offset compensation is provided by the TLC8044 three 8-bit plus sign DACs, which provide bipolar offset correction with respect to the input reference levels. The DACs are updated through the serial interface.

PRINCIPLES OF OPERATION

RGB channel multiplexer and sampler (continued)

The input structure can be set up for use in single-ended or fully differential mode, under control of the serial interface data. The configuration shown in the system diagram is single ended, with the negative inputs tied to the DAC, which is the buffered midpoint of the ADC reference chain. Differential mode can be used when an amplifier with differential outputs is placed between the CCD image sensor and the TLC8044.

In color operation, the three-channel sampling system multiplexes the three channels to the ADC input in a sequence defined by the VSMP input synchronization pulse. In monochrome operation, channel synchronization between R, G, and B inputs is achieved through the serial interface.

analog-to-digital converter

The ADC is implemented using a 12-bit pipelined architecture which performs conversions at one half the MCLK clock rate. The ADC full-scale range is defined by the voltages applied to terminals RT and RB, which should be set to 3.75 V and 1.25 V respectively to give a full-scale range of 3.75 V -1.25 V = 2.5 V.

The ADC internal input is differential with an input signal of 2.5 V corresponding to full scale (output code FFF hex) and -2.5 V corresponding to zero scale (output code 000 hex).

The RU and RL terminals are connected to extensions of the internal reference chain, which allow the 3.75-V and 1.25-V levels to be derived from a 5-V reference applied between RU and RL. All reference terminals should be capacitively decoupled externally.

The combination of the input multiplexer structure with the internal offset correction DACs accomodates a wide range of input voltages. The relationships between input voltage levels (at the positive and negative inputs INP and INN) and ADC full-scale and zero-scale results are shown in Tables 1 and 2 for a range of input offset voltages for both single-ended and differential input modes. The tables also show the DAC correction voltage and code required in each case.

The basic difference between single-ended and differential input modes is that a gain of 2 is applied to the input signal between INP and INN in the single-ended case. Thus an input differential of 1.25 V is converted to a full-scale ADC differential input of 2.5 V. Any residual offset present on the input signal is also gained by 2 in the single-ended mode, resulting in the required DAC values shown in Table 1.

Table 1. Single-Ended Mode Input Voltage Ranges

INPUT OFFSET VOLTAGE	FULL-SCALE INPUT VOLTAGE		ZERO-SCALE INPUT VOLTAGE		DAC VOLTAGE	DAC CODE (HEX)
	$V_{I(INP)}$	$V_{I(INN)}$	$V_{I(INP)}$	$V_{I(INN)}$		
0.625	4.375	2.5	1.875	2.5	-1.25	17F
0	3.75	2.5	1.25	2.5	0	000
-0.625	3.125	2.5	0.625	2.5	1.25	07F

Table 2. Differential Mode Input Voltage Ranges

DIFFERENTIAL INPUT OFFSET VOLTAGE	FULL-SCALE INPUT VOLTAGE		ZERO-SCALE INPUT VOLTAGE		DAC VOLTAGE	DAC CODE (HEX)
	$V_{I(INP)}$	$V_{I(INN)}$	$V_{I(INP)}$	$V_{I(INN)}$		
1.25	4.375	0.625	1.875	3.125	-1.25	17F
0	3.75	1.25	1.25	3.75	0	000
-1.25	3.125	1.875	0.625	4.375	1.25	07F

PRINCIPLES OF OPERATION

analog-to-digital converter (continued)

The examples in Tables 1 and 2 assume that the ADC reference terminals RT and RB are set to 3.75 V and 1.25 V, respectively. The signals shown in the tables cover the full-scale range of the ADC. In practice, a reduced range is used to allow some headroom, accomodating a wider range of input offset voltages. The ADC output code can be inverted under control of the serial interface. When not in use, the ADC can also be put into standby mode through the serial interface to reduce system power consumption.

sample modes

Two input sampling modes are provided, normal and correlated double sampling (CDS). Sampling mode selection is made through the serial interface. All video input timing and sampling is performed relative to the rising edge of the MCLK clock input signal. MCLK is applied to twice the required ADC conversion rate. Synchronization of sampling and channel multiplexing to the incoming video signals is performed by the VSMP input synchronization pulse. Table 3 is a summary of the device operating modes.

normal sampling mode

Figure 11(a) and Figure 11(b) show the timing of signals in normal sampling mode for both color and monochrome operation.

In color operation, all three input channels are sampled at the same instant on the first rising edge of MCLK after the VSMP pulse. An internal timing circuit then controls the multiplexing of the three channels to the ADC input in the R,G,B sequence. In this mode, VSMP is applied at the input pixel rate, and ADC conversions are performed at three times the input pixel rate.

For monochrome (single channel) operation, VSMP is again applied at the input pixel rate, however, for monochrome, the ADC is supplied with a continuous stream of samples from a single input channel. Input channel selection in this mode is achieved through the serial interface.

In both color and monochrome operation, a simple external delay circuit can be used to align the video data with the sampling instant, provided that the CCD clocks are generated from MCLK. Detailed timings for both cases are shown in Figures 3 and 4.

Table 3. Mode Summary

MODE	DESCRIPTION	CDS AVAILABLE	MAX SAMPLE RATE	SENSOR INTERFACE DESCRIPTION	TIMING REQUIREMENTS	REGISTER CONTENTS WITH CDS†	REGISTER CONTENTS WITHOUT CDS†
1	Color	Yes	2 MSPS	The three input channels (R, G, B) are sampled in parallel at 2 MSPS maximum. The sampled data is multiplexed into a single data stream before the internal ADC, giving an internal serial data rate of maximum 6 MSPS.	MCLK max: 12 Mhz MCLK: VSMP ratio is 6:1	Setup register 1: Word 1: 00h Word 2: 81h	Setup register 1: Word 1: 00h Word 2: 80h
2	Monochrome	Yes	2 MSPS	One input channel is continuously sampled. The internal multiplexer is held in one position under control of the user.	Identical to mode 1	Setup register 1: Word 1: 00h Word 2: 91h Setup register 2: Word 2: bits b(1,0) define which channel to be sampled	Setup register 1: Word 1: 00h Word 2: 90h Setup register 2: Word 2: bits b(1,0) define which channel to be sampled
3	Fast monochrome	Yes	4 MSPS	Identical to mode 2	MCLK max: 12 MHz MCLK: VSMP ratio is 3:1	Identical to mode 2 plus Setup register 2: Word 1: bits b(1,0) must be set to 00h	Identical to mode 2
4	Max speed monochrome	No	6 MSPS	Identical to mode 2	MCLK max: 12 MHz MCLK: VSMP ratio is 2:1	Not supported	Setup register 1: 5Dh Setup register 2: Word 2: bits b(1,0) define which channel to be sampled

† Only indicates relevant register bits.

PRINCIPLES OF OPERATION

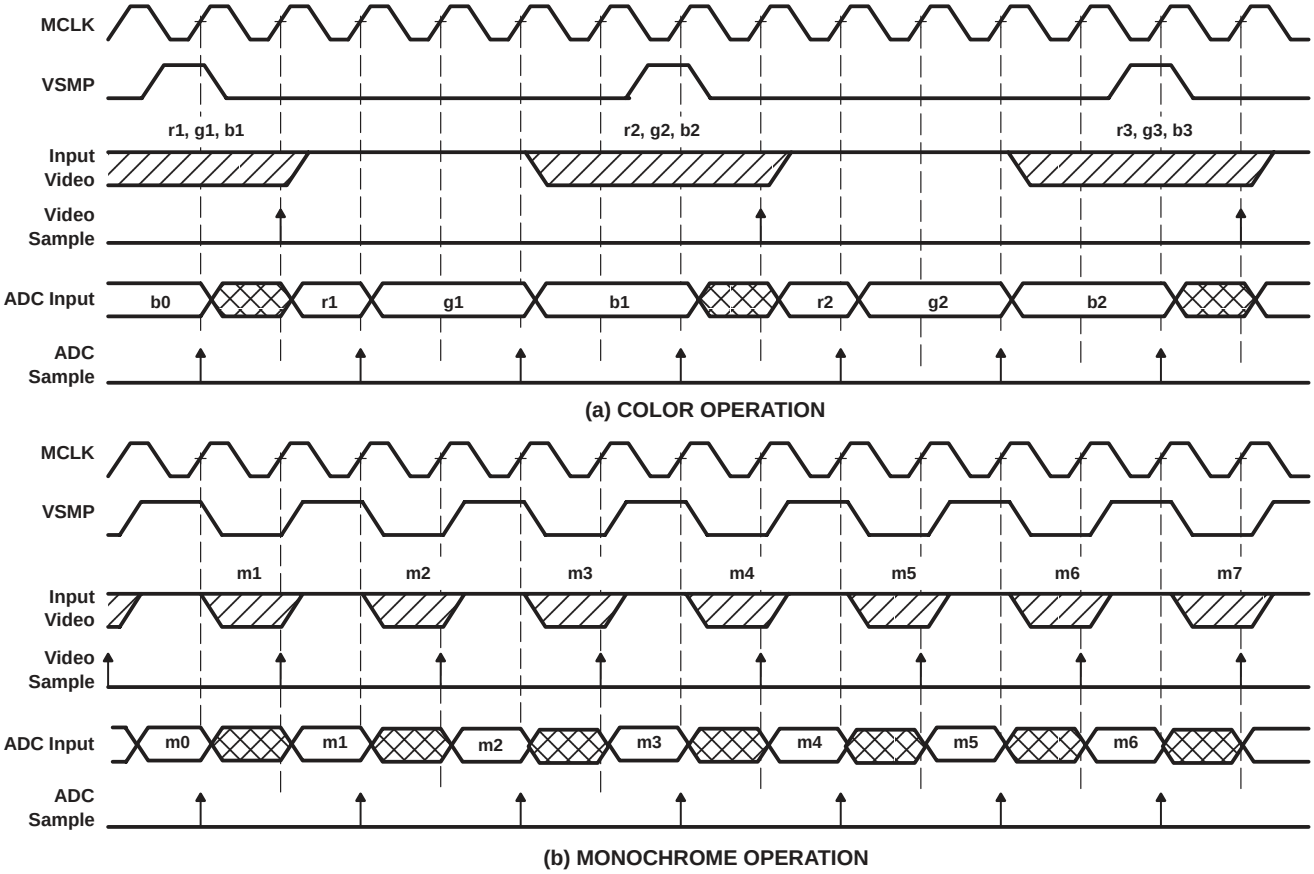


Figure 11. Normal Mode Input Timing

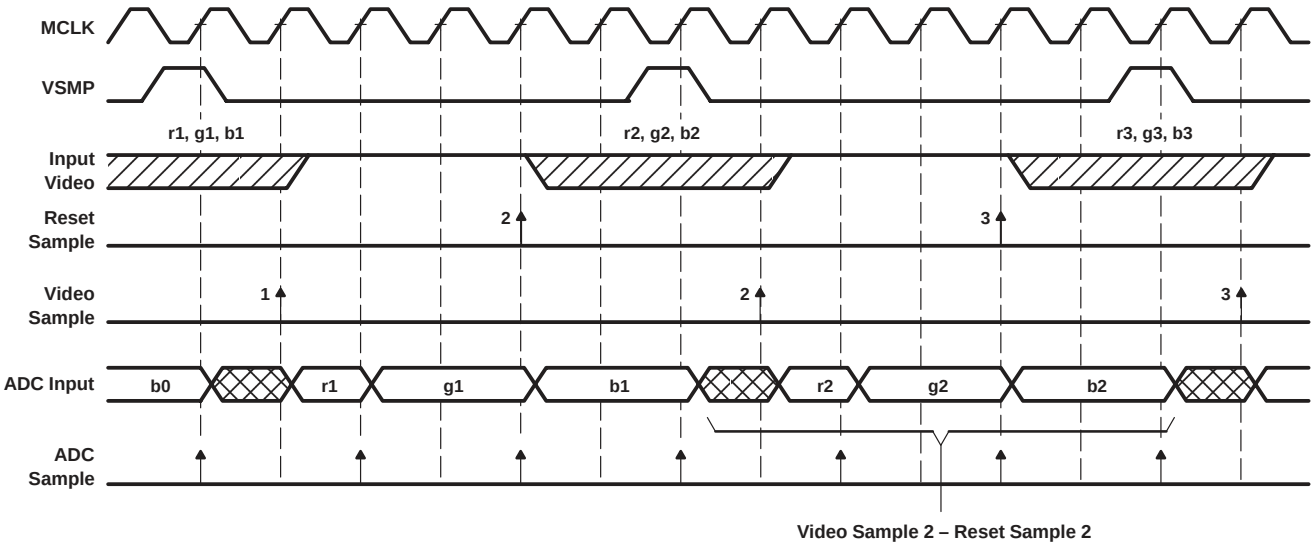


Figure 12. CDS Mode Input Timing

PRINCIPLES OF OPERATION

correlated double sampling

Correlated double sampling is a circuit technique for reducing any correlated noise between the reset (black) level and the video level of the CCD array. Referring to the block diagram shown in Figure 13(a), a sample of the CCD output is taken and held at the reset level and another sample is taken and held at the video level. These two levels are subtracted essentially nulling any common signal, and thereby minimizing the correlated noise that exists at both the reset level and the video level. Figure 13(b) shows relative timing.

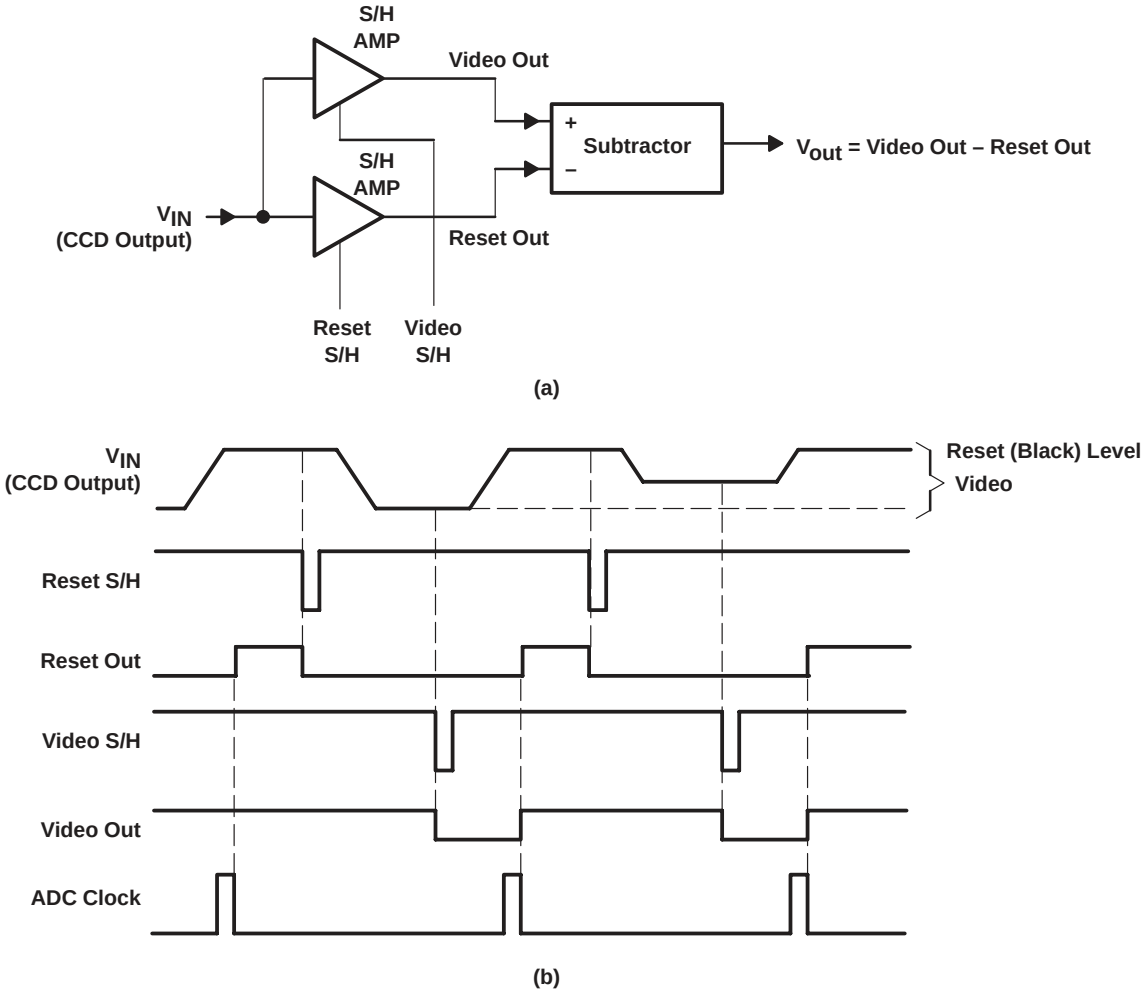


Figure 13. Samplified Correlated Double Sampling

correlated double sampling mode

In CDS mode, two samples are taken per channel within each pixel period. Figure 12 shows the timing diagram for this mode of operation. The video signal is sampled during the reset phase and during the video information with timing defined relative to the VSMP input. The difference between these two samples forms the input to the ADC. The relative timing of the reset and video samples shown in Figure 12 is the default (post-reset) condition. The timing of the reset sample relative to the video sample can be advanced by one or retarded by one or two MCLK periods under control of the serial interface. Figure 1 shows a detailed video input timing diagram with all four CDS timing options.

PRINCIPLES OF OPERATION

correlated double sampling mode (continued)

To perform CDS input sampling, the device should be set up in single-ended mode with the differential inputs of each channel (xINP, xINN) connected together to the video input signal.

For positive going input signals, i.e., white signal level greater than the reset level, the offset DACs should be set to the maximum negative value (DAC code 1FF hex). This configuration sets the zero signal level (video input equal to the reset level) at the ADC zero-scale code transition. Increasing the DAC code towards zero moves the zero signal level up from the ADC zero-scale code transition. For negative-going input signals, i.e., white signal level less than the reset level, the DACs should be set to the maximum positive value (DAC code 0FF hex). This configuration sets the zero signal level at the ADC full-scale code transition. The polarity of the ADC output signal can be inverted under control of the serial interface data.

The multiplexing shown in Figure 12 refers to color operation, however the same overall timing scheme applies to monochrome CDS operation, in that a single input sample is applied to the ADC per VSMP period. Thus the maximum sampling rate in monochrome CDS mode is limited to one third of the maximum rate achievable in normal monochrome sampling mode.

digital image processing

The digital image processing functions following the ADC as shown in the functional block diagram include the following:

- DC restore: This allows fine adjustment of the dc video level at the ADC output with adjustment values being programmed through the serial interface.
- Pixel-by-pixel offset compensation: This uses offset coefficients that are either externally supplied at the multiplexed channel rate or supplied from internal default registers whose values are programmed through the serial interface.
- Compensation for pixel-by-pixel shading curve nonuniformity and photo response nonuniformity within the sensor: Coefficients are externally supplied at the multiplexed channel rate. Default registers are provided for use during calibration.
- Global offset adjust: Offset adjust over the whole scan for each channel to give brightness control. Values are programmed through the serial interface.
- Global gain adjust: Independent gain adjust over the whole scan for each channel to give contrast and color balance control. Gain values are programmed through the serial interface.
- Programmable output word length selection: The output word length can be programmed to 8, 10, 12, or 16 bits through the serial interface.
- Programmable threshold detector with independent thresholds for each channel.

Global adjustments are implemented after the pixel-by-pixel compensations allowing calibrations and modifications in operational use without having to recalibrate the pixel-by-pixel factors.

DC restore

The dc restore block is used for fine adjustment of the dc signal level at the ADC output by adding a value stored in an internal register. Separate level adjust registers are provided for each channel (color) with multiplexing between channels controlled internally. The level adjust registers are programmed through the serial interface as 12-bit 2s complement numbers with a range of ±0.5 of the ADC full scale, allowing 1-bit resolution in adjustment of the ADC output. The dc adjustment registers are reset to zero.

PRINCIPLES OF OPERATION

pixel offset compensation

The output of the dc restore circuit is passed to an adder which performs pixel-by-pixel offset compensation. Compensation values can either be supplied externally at the multiplexed pixel rate, allowing different correction values for each pixel in the array, or supplied from internal default values programmed through the serial bus. Selection between the two sources is controlled through the serial bus. Two sets of internal default registers are provided to allow correction values to be stored internally for use on even and odd pixels with selection between the two sets under control of the ONE terminal (ONE low for even registers, ONE high for odd registers). This feature allows correction of differing dc offsets output on even and odd pixels, which occur in some CCD sensors, using internally stored data.

Pixel offset correction values are input or stored as 12-bit 2s complement numbers. Programmable internal scaling is provided which allows the offset correction factors to cover ±0.5, ±0.25, ±0.125, or ±0.0625 of the ADC full-scale range. The internal pixel correction registers are reset to zero.

pixel shading compensation

This stage is implemented as a digital multiplier which corrects for nonuniform shading using externally supplied 12-bit unsigned values. The external correction factors are supplied at the multiplexed pixel rate. The external correction range is from 0 to 4, which allows shading nonuniformity of up to 75% (i.e., the minimum input signal is 25% of the peak) to be corrected without loss of resolution in the high gain pixels at the center of the scan. Internal default registers are provided to set the gain through this block during calibration. The internal registers default to a value of 1 (equivalent to decimal 1024 in this range) on reset.

global offset adjust

Global offset adjust is provided by an adder using three independent bipolar offset coefficients set through the serial interface. A range of ±4 times the ADC full-scale range in steps of a half output LSB is provided. This range allows the output signal to be shifted across the entire range of the 16-bit output bus. The global offset coefficients are programmed as 16-bit 2s complement numbers, which default to zero on reset.

global gain adjust

Global gain adjust is provided by a multiplier using gain values set through the serial interface. Three independent 16-bit gain values with a range of 0 to 2 are stored (one for each channel). The default value of the global gain coefficients is 1 (equivalent to decimal 32768 in this range).

threshold detector

The threshold detector operates on the output signal from the global gain adjust stage, comparing the signal to individual threshold levels for each color channel, which are programmed through the serial interface. If the signal exceeds the threshold, the DETOP terminal is forced high. Two basic modes of operation can be programmed, either multiplexing between the three channels in sequence with the internal data, or operating continuously on one of the three channels. The input signals to the threshold detector are represented as 16-bit bipolar 2s complement numbers. Threshold values should be programmed as 15-bit unipolar numbers in the range 0 to 32767.

effect of image processing on ADC output

The combined effect of the image processing sections on the ADC output is summarized by the formula in the note following Table 4. All values are shown in decimal. Examples of the process are given in Table 4. Examples 1–8 show the results with no pixel offset scaling. Examples 9–11 show the added effect of pixel offset scaling. All examples use a half range ADC value (2048) for the ADC output (ADCOP).

If defaults are used throughout, then the output of the ADC is output directly on the OP0–OP11 bus as listed in Table 4, example 1.

PRINCIPLES OF OPERATION

effect of image processing on ADC output (continued)

In Table 4, example 2 shows how the half range ADCOP value (2048) is affected by adding dc restoration (value 128). This value is added directly to the ADCOP value. All other parameters are default, so this result passes directly to the OP0–OP11 output. Inserting the values in the formula gives:

$$OP0–OP11 = (((2048 + 128 + (0 \times 1)) \times 1) + (0.5 \times 0)) \times 1$$

In Table 4, example 9 shows the effect of internal scaling (POSCL) on the pixel offset compensation (POC). The value 01 on POSCL indicates a scaling factor of 0.5 (refer to Table 5, setup register 2). The POC value of 128 is multiplied by 0.5. The result is added to the ADC output. Defaults have been used on all other stages, so the resulting value of 2048 is directly output on OP0–OP11. Examples 10 and 11 show the effect of different scaling factors. Inserting the values in the formula gives:

$$OP0–OP11 = (((2048 + 0 + (128 \times 0.5)) \times 1) + (0.5 \times 0)) \times 1$$

Table 4. Examples of Image Processing on ADC Output

PARAMETER	ADCOP	DCREST	POC	POSCL	PCS	GLOBAL OFFSET	GLOBAL GAIN	OP0–OP11
Range	0 to 4095	–2048 to 2047	–2048 to 2047		0 to 4095	–32768 to 32767	0 to 65536	0 to 4095
Default		0	0	00	1024	0	32768	
Example 1	2048	0	0	00	1024	0	32768	2048
Example 2	2048	128	0	00	1024	0	32768	2176
Example 3	2048	0	–256	00	1024	0	32768	1792
Example 4	2048	0	0	00	512	0	32768	1024
Example 5	2048	–64	128	00	1536	0	32768	3168
Example 6	2048	0	0	00	1024	1024	32768	2560
Example 7	2048	0	0	00	1024	0	16384	1024
Example 8	2048	–64	128	00	512	1024	16384	784
Example 9	2048	0	128	01	1024	0	32768	2112
Example 10	2048	0	128	10	1024	0	32768	2080
Example 11	2048	0	128	11	1024	0	32768	2064

NOTE:

$$OP0–OP11 = (((ADCOP + DCREST + (POC \times POSCL)) \times PSC) + (0.5 \times Global\ Offset)) \times Global\ Gain$$

where:

ADCOP	12-bit output of the ADC
DCREST	2s complement 12-bit number source directly from the DC restore registers
POC	2s complement 12-bit number source directly from the POC bus or registers
POSCL	scaling factor as defined in Table 5 setup register 2
PSC	12-bit unsigned number sourced from the PSC bus or register and divided by 1024
Global Offset	16-bit 2s complement number sourced directly form the global offset adjust registers
Global Gain	16-bit unsigned number sourced from the global gain register and divided by 32768
OP0–OP11	12-bit result of the image processing that is output from the device on the bus OP0–OP15

PRINCIPLES OF OPERATION

output word length select

This block is used to define the output word length, which can be programmed to 8, 10, 12, or 16 bits through the serial interface. An internal clip function is provided that can be used in unipolar or bipolar fashion. For example, if an 8-bit output word length is selected, the output data on OP0 – OP15 is limited to the range 0 to 255 for unipolar clipping or – 128 to 127 for bipolar clipping. If the signal to this block exceeds the positive clip level, the ORNG signal is forced high. In 8-, 10-, and 12-bit output modes, the output data bit OP15 functions as an under range flag; i.e., it is driven high if the input signal is less than the negative clip level. OP15 also functions as an under range signal in 16-bit unipolar clipping mode.

serial interface

The serial interface data is used to configure the device operation and to program internal data registers. Figure 14 shows a timing diagram of a serial write operation. A serial data stream applied to the SDI terminal is clocked into the device on the rising edge of SCK. The data stream comprises 6 address bits and two 8-bit data words. When this data has is shifted into the device, a pulse applied to SEN transfers the data to the appropriate internal register.

Tables 5 and 6 define the internal register map for the device and control bit functionality, respectively. The first 4 addresses in Table 5 (address bit a5 = 0) are used to program setup registers and to provide a software reset feature. The remaining eight entries in Table 5 define the address locations of internal data registers, and three additional subaddresses are defined for the red, green, or blue registers. Address bits a1 and a0 select between the red, green, and blue registers, as defined in Table 5. When a1 and a0 are set to 1, all three registers are updated to the same date value, as specified in data words 1 and 2. Blank entries in Table 5 are taken as don't care values.

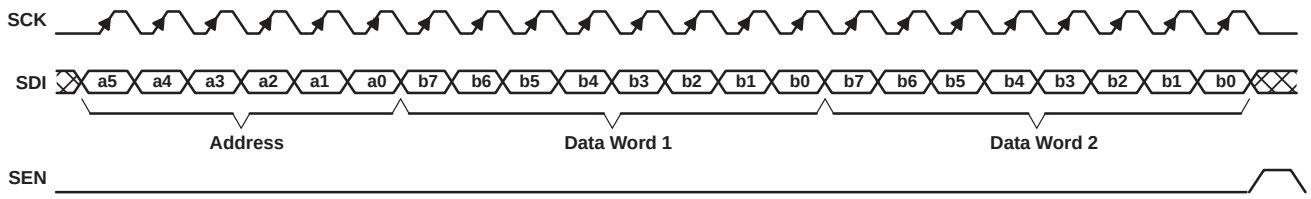


Figure 14. Serial Interface Timing

system timing

System timing diagrams that relate the timing between taking an input sample, applying the related pixel offset and shading coefficients, and the output of the digital video data are shown in Figures 1 and 2. These diagrams show the overall latency of the device in both color and monochrome operating modes. Detailed digital timing diagrams are shown in Figure 15, 16, and 17.

PRINCIPLES OF OPERATION

Table 5. Serial Interface Register Map

ADDRESS <a5...a0>	DESCRIPTION	DATA WORD	BIT							
			b7	b6	b5	b4	b3	b2	b1	b0
000000	Setup register 1	1 2	ENADC	BICLIP	ADCMX	MONO	DEFPG	DEFPO	DNS	INVADC CDS
000001	Setup register 2	1 2	POSCL1	POSCL0	WLSEL1	WLSEL0	THSEL1	THSEL0	CDSREF1 CHAN1	CDSREF0 CHAN0
000010	Reserved	1 2								
000011	Software reset	1 2								
1000xx	DAC values	1 2	D7	D6	D5	D4	D3	D2	D1	POL D0(LSB)
1001xx	DC restore values	1 2	D7	D6	D5	D4	D11(MSB) D3	D10 D2	D9 D1	D8 D0(LSB)
1010xx	Default even pixel offsets	1 2	D7	D6	D5	D4	D11(MSB) D3	D10 D2	D9 D1	D8 D0(LSB)
1011xx	Default odd pixel offsets	1 2	D7	D6	D5	D4	D11(MSB) D3	D10 D2	D9 D1	D8 D0(LSB)
1100xx	Default pixel gains	1 2	D7	D6	D5	D4	D11(MSB) D3	D10 D2	D9 D1	D8 D0(LSB)
1101xx	Global offsets	1 2	D15(MSB) D7	D14 D6	D13 D5	D12 D4	D11 D3	D10 D2	D9 D1	D8 D0(LSB)
1110xx	Global gains	1 2	D15(MSB) D7	D14 D6	D13 D5	D12 D4	D11 D3	D10 D2	D9 D1	D8 D0(LSB)
1111xx	Threshold values	1 2	D7	D14(MSB) D6	D13 D5	D12 D4	D11 D3	D10 D2	D9 D1	D8 D0(LSB)

xx		ADDRESS LSB DECODE†	DEFAULT PIXEL DECODE‡
a1	a0		
0	0	Red register	Blue register
0	1	Green register	Red register
1	0	Blue register	Green register
1	1	Red, green, and blue	Red, green, and blue

† Default address
‡ The address decoding is applicable for default pixel gain in monochrome mode.

PRINCIPLES OF OPERATION

Table 6. Control Bit Descriptions

REGISTER	BITS	DEFAULT	DESCRIPTION
Setup Register 1	ENADC	1	ADC standby control: 0 = standby 1 = active
	BICLIP	0	Bipolar clip enable: 0 = unipolar clip 1 = bipolar clip
	ADCMX	0	ADC MUX control: 0 = normal operation 1 = ADC output multiplexed to OP
	MONO	0	Mono/color select: 0 = color operation 1 = monochrome operation
	DEFPG	0	Select default pixel gain: 0 = external pixel gain 1 = default (internal)
	DEFPO	0	Select default pixel offsets: 0 = external pixel offsets 1 = default (internal)
	DNS	0	Select differential/single-ended mode: 0 = single ended 1 = differential
	INVADC	0	ADC output polarity: 0 = noninverted 1 = inverted
	CDS	0	Select correlated double sampling mode: 0 = normal sampling 1 = CDS mode
Setup Register 2	POSCL1, 0	00	Pixel offset scaling: 00 = $\pm 0.5\ f_S$ 01 = $\pm 0.25\ f_S$ 10 = $\pm 0.125\ f_S$ 11 = $\pm 0.0625\ f_S$
	WLSEL1, 0	10	Output word length select: 00 = 8 bits (OP0 - OP7 contains output word) 01 = 10 bits (OP0 - OP9 contains output word) 10 = 12 bits (OP0 - OP11 contains output word) 11 = 16 bits (OP0 - OP15 contains output word)
	THSEL1, 0	11	Threshold detector operating mode: 00 = Operating on red channel only 01 = Operating on green channel only 10 = Operating on blue channel only 11 = Three channel
	CDSREF1, 0	01	CDS mode reset timing adjust: 00 = Advance 1 MCLK period 01 = Normal 10 = Retard 1 MCLK period 11 = Retard 2 MCLK periods
	CHAN1, 0	00	Monochrome mode channel select: 00 = Red channel 01 = Green channel 10 = Blue channel 11 = Not used

PRINCIPLES OF OPERATION

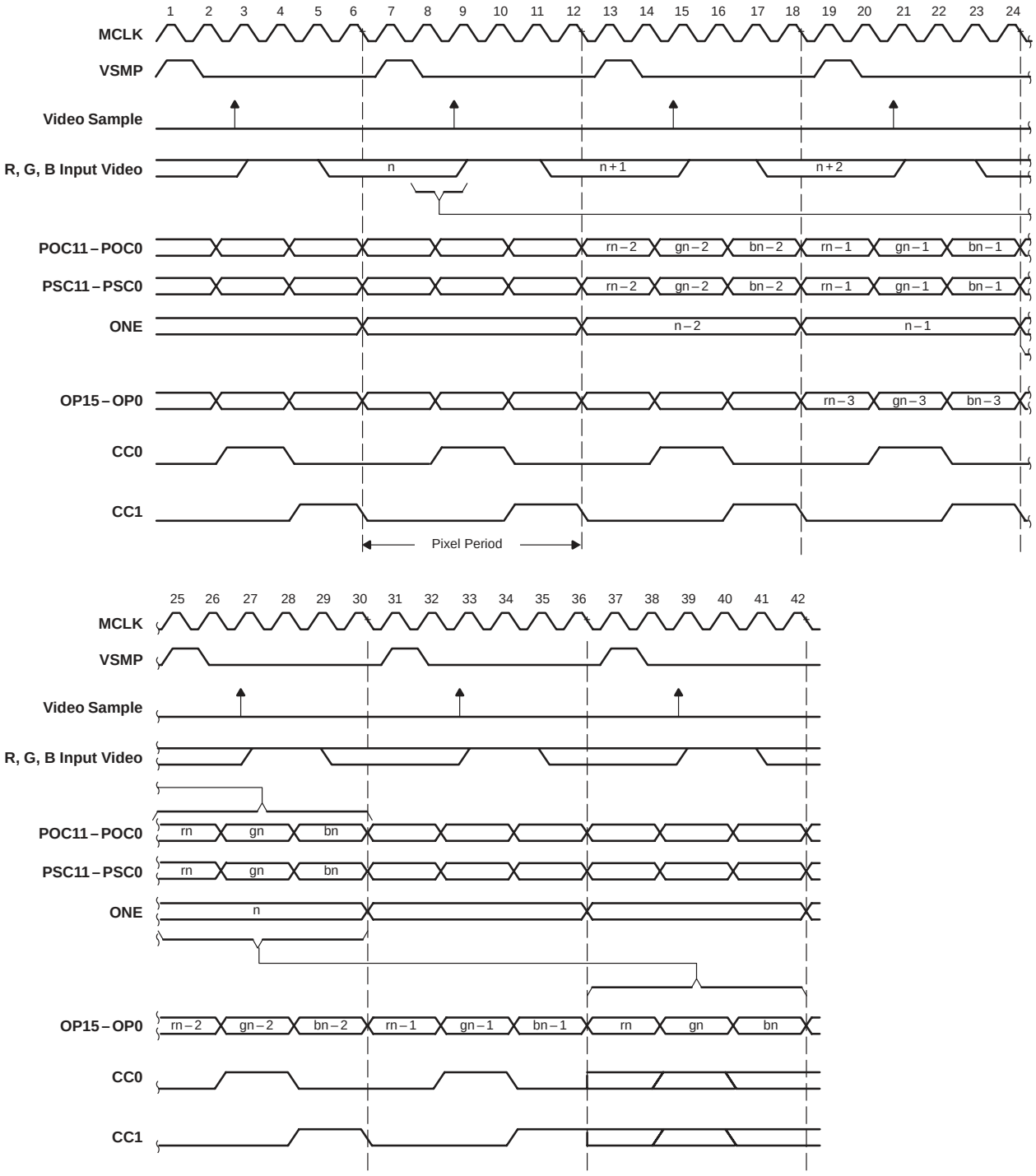
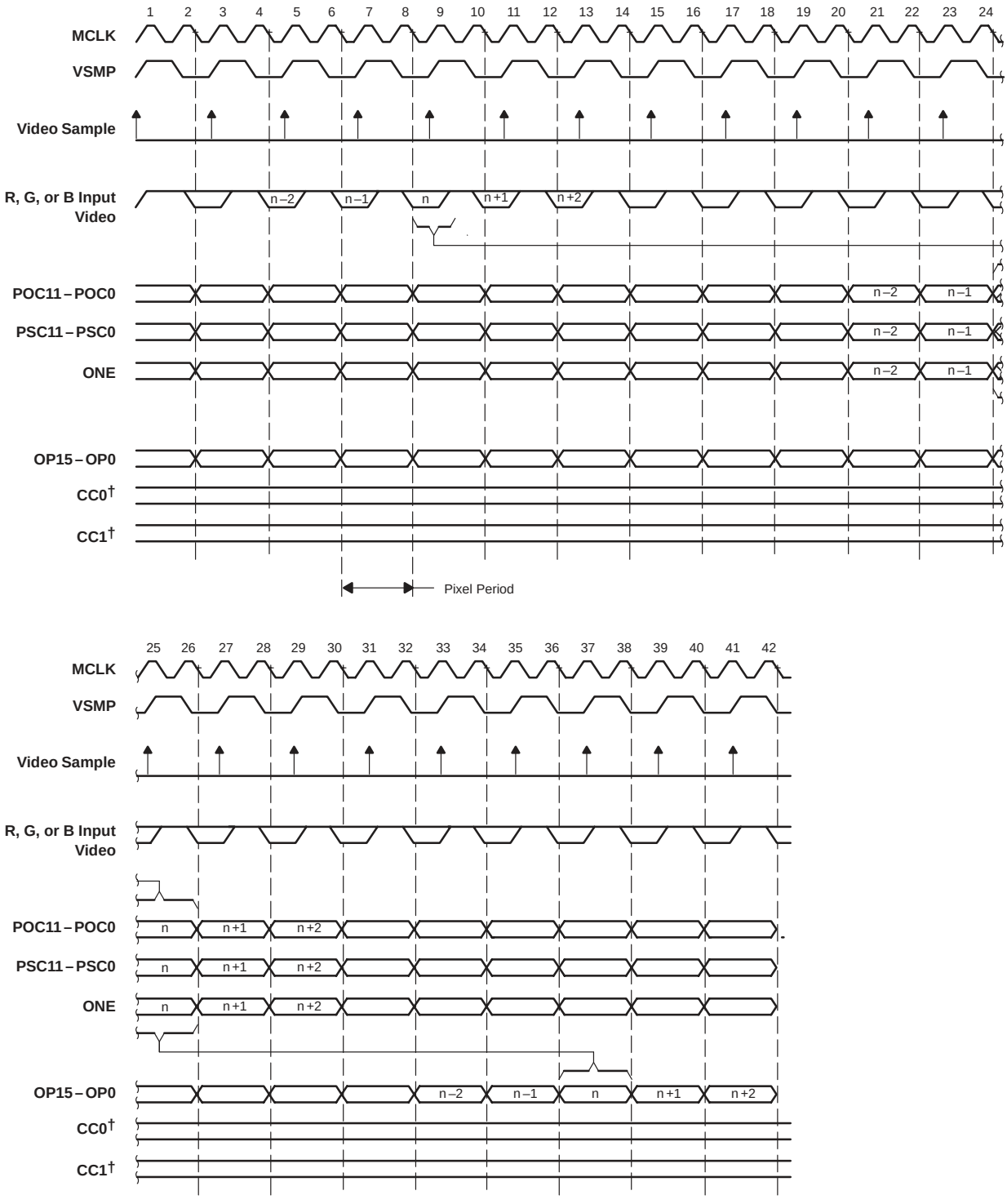


Figure 15. System Timing – Color Mode

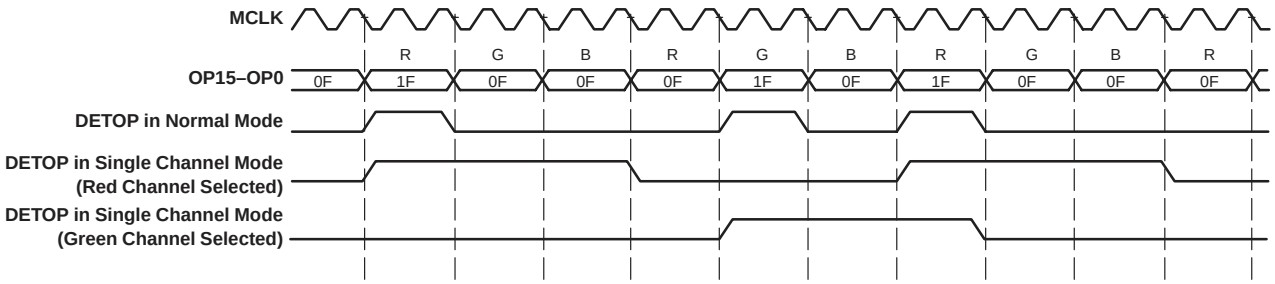
PRINCIPLES OF OPERATION



† The CC(10) output state is defined via the serial bus in monochrome mode.

Figure 16. System Timing – Monochrome Mode

PRINCIPLES OF OPERATION



NOTE A: All thresholds are set to 10 hex.

Figure 17. Timing of Threshold Detector Output DETOP

APPLICATION INFORMATION

running the TLC8044 at 4-megasamples/sec in CDS monochrome mode

The TLC8044 can be set up to provide a 4-megasample/sec throughput when in CDS monochrome mode; however, the VSMP input must run continuously at 4 MHz.

The following paragraphs describe operation of the TLC8044 in monochrome mode (sampling one channel only). The maximum sample rate in color CDS mode is 2-megasamples/channel/sec.

In CDS mode, the video signal is sampled both during the reset phase and when video information is present with timing defined to a VSMP input. The difference between these two samples forms the input to the ADC. In monochrome mode, all samples are taken from one input video channel. The device is set up as listed in Table 6. See Tables 4 and 5 for offset DAC values in CDS mode.

System timing is shown in Figure 18. MCLK clocks the device at 12 MHz (as normal). VSMP, which controls the sample rate, is run at 4 MHz. A reset sample is taken on the rising edge of MCLK after VSMP is asserted. The corresponding video sample is taken on the next MCLK rising edge. Compensation coefficients (pixel offset and pixel shading) are sampled on the falling edge of MCLK 26.5 periods after the initial reset sample. The processed digital outputs appear on OP0–OP15 41.5 MCLK periods after the initial reset sample.

In Figure 18 the system timing diagram shows a negative-going video sample. The polarity of the ADC output signal can be inverted under control of the serial interface. Setup and hold times are specified in the recommended operating conditions table.

Table 7. Relevant Register Settings

REGISTER	BITS	VALUE†	DESCRIPTION
Setup register 1	ENADC	U	ADC standby control
	BICLIP	U	Select unipolar clip
	ADCMX	0	ADC MUX control
	MONO	1	Monochrome operation
	DEFPG	U	Select default pixel gain
	DEFPO	U	Select default pixel offsets
	DNS	0	Select single-ended mode
	INVADC	U	ADC output polarity
	CDS	1	Select correlated double sampling mode
Setup register 2	POSCL1,0	UU	Pixel offset scaling
	WLSEL1,0	UU	Select 12-bit output word
	THSEL1,0	UU	Three channel
	CDSREF1,0	00	Advance one MCLK period
	CHAN1,0	UU	Select channel to be sampled

† U = User defined

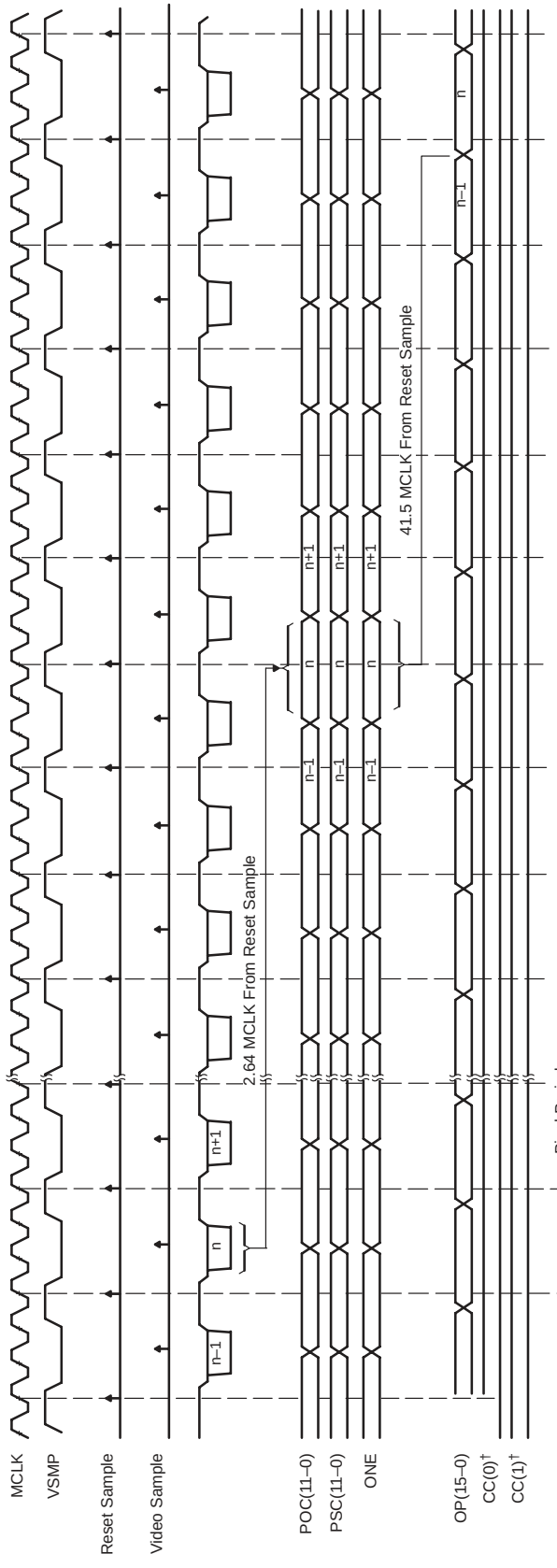


Figure 18. System Timing – CDS Mode at 4-Megasamples/Sec

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TLC8044CFN	OBSOLETE	PLCC	FN	68		TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
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